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Enterprise

# **DDR4 server memory population rules for HPE Intel Xeon Gen10 servers**

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## Introduction

This paper provides an overview of HPE DDR4 SmartMemory and its use in the HPE ProLiant Gen10 servers using the Intel® Xeon® Processor Scalable family. HPE ProLiant Gen10 will introduce HPE DDR4-2666 memory that has faster data rates, lower latencies, and greater power efficiency than the memory used in previous generations of HPE ProLiant servers. HPE SmartMemory also provides superior performance over third-party memory when used in HPE ProLiant servers.

The HPE ProLiant Gen10 servers feature a somewhat different memory architecture to that introduced with Gen9 servers. HPE ProLiant Gen10 servers using the Intel Xeon Processor Scalable family include six separate memory channels per CPU and up to 24 DIMM slots in two-socket servers and 48 DIMM slots in four-socket servers—allowing large memory configurations and delivering improved memory performance. They also incorporate HPE Advanced Memory Protection technology, which improves the prediction of critical memory error conditions.

In addition to describing these improvements, this white paper reviews the rules, best practices, and optimization strategies that should be used when installing HPE DDR4 memory on HPE ProLiant Gen10 servers.

## Populating HPE DDR4 memory in HPE ProLiant Gen10 servers

The high-level memory system architecture for HPE ProLiant Gen10 servers with the Intel Xeon Processor Scalable family is in many ways different from that of HPE Gen9 servers. One characteristic that HPE Gen10 and HPE Gen9 servers share in common is that they both have either 12- or eight-memory slot (per CPU) configurations.

### Population rules for HPE ProLiant Gen10 servers

HPE ProLiant Gen10 systems support a variety of flexible memory configurations, enabling the system to be configured and run in any valid memory controller configuration. For optimal performance and functionality, you should follow the rules when populating HPE ProLiant Gen10 servers with HPE DDR4 memory. Violating these rules may result in reduced memory capacity, performance, or error messages during boot. Table 1 summarizes the overall DIMM population rules for HPE ProLiant Gen10 servers.

**Table 1.** DIMM population rules for HPE ProLiant Gen10 servers

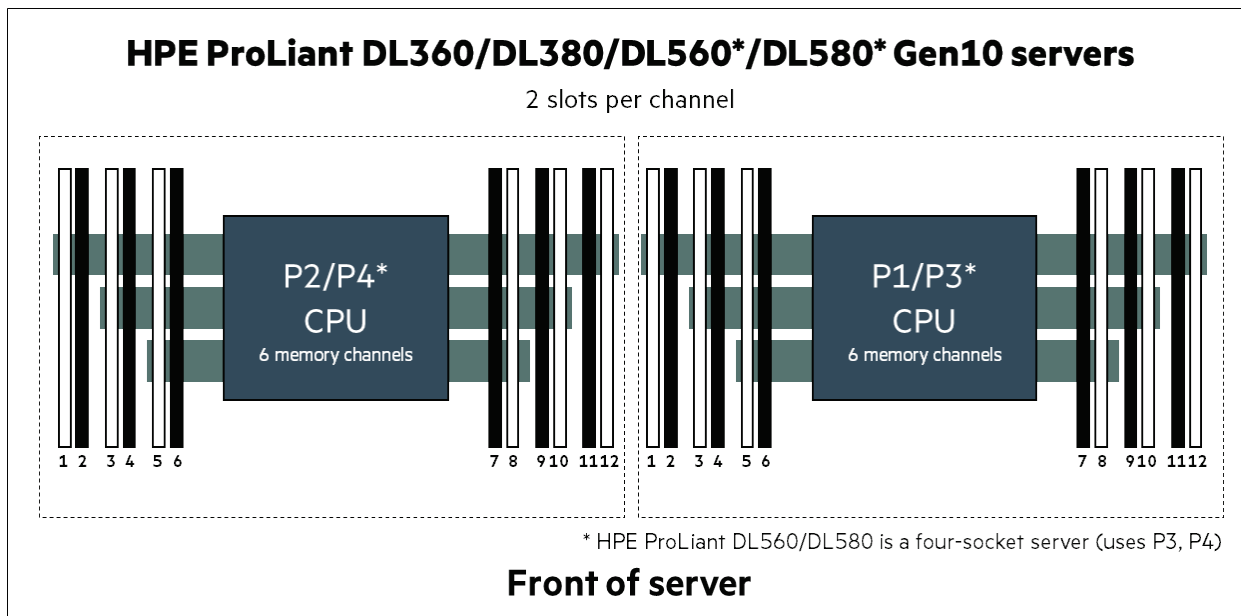
Category	Population guidelines
Processors and DIMM slots	<p>Install DIMMs only if the corresponding processor is installed. If only one processor is installed in a two-processor system, only half of the DIMM slots are available.</p> <p>If a memory channel consists of more than one DIMM slot, the white memory slot will be located furthest from the CPU. White DIMM slots denote the first slot to be populated in a channel. For 1 DPC (DIMM per channel) populate white memory slots only.</p> <p>When mixing DIMMs of different ranks on the same channel, place the DIMMs with the heaviest electrical load (highest number of ranks) in the white memory slot. Within a given channel, populate DIMMs from the heaviest electrical load (dual rank) to the lightest load (single rank).</p> <p>If multiple CPUs are populated, split the DIMMs evenly across the CPUs and follow the corresponding CPU rule when populating DIMMs.</p>
Performance	<p>To maximize performance, it is recommended to balance the total memory capacity across all installed processors and load the channels similarly whenever possible (see <a href="#">Appendix B</a>).</p> <p>If the number of DIMMs does not spread evenly across the CPUs, populate as close to evenly as possible.</p>
DIMM types and capacities	<p>The maximum memory capacity is a function of the number of DIMM connectors on the platform: the largest DIMM capacity qualified on the platform and the number and model of qualified processors installed on the platform.</p> <p>Do not mix RDIMMs and LRDIMMs in the same system. Do not mix 128 GB LRDIMMs with other capacity DIMMs.</p> <p>Unbuffered DIMMs (UDIMMs) are not supported.</p> <p>x4 and x8 DIMMs can be mixed in the same channel. RAS features affected when mixing x4 and x8 DIMMs are Online Spare, Mirrored Memory, and HPE Fast Fault Tolerance.</p>
DIMM speed	<p>The maximum memory speed is a function of the memory type, memory configuration, and processor model.</p> <p>DIMMs of different speeds may be mixed in any order; however, the server will select the highest common speed among all of the DIMMs/CPU.</p> <p>HPE memory from previous generation servers is not compatible with the current generation. Certain HPE SmartMemory features such as Memory Authentication and Enhanced Performance may not be supported.</p>
Heterogeneous mix	<p>There are no performance implications for mixing sets of different capacity DIMMs at the same operating speed. For example, latency and throughput will not be negatively impacted by installing an equal number of 16 GB dual-rank DDR4-2666 DIMMs (one per channel) and 32 GB dual-rank DDR4-2666 DIMMs (one per channel).</p> <p>Take each DIMM type and create a configuration as if it were a homogeneous configuration.</p> <p>Depending on the per-channel rules, populate the DIMMs with highest rank count in white memory slots in each channel. Populate the other DIMMs in the black memory slots in each channel (see mixed DIMM configuration example in <a href="#">Appendix B</a>).</p>



**DIMM connector location**

In general, memory population order follows the same logic for all HPE ProLiant servers—although physical arrangement may vary from server to server. To populate server memory in the correct order and location, refer to illustrations found in [Appendix B](#). Each illustration reflects in which memory slots to populate memory for a given number of memory DIMMs around a single processor, given a common DIMM type. If multiple processors are installed, split the DIMMs evenly across the processors and follow the corresponding rule when populating DIMMs for each processor (see Figure 7 for an example). For optimal throughput and reduced latency, populate all six channels of each installed CPU identically.

Figure 1 shows the memory slot configuration for the 24-slot HPE ProLiant DL380 Gen10 two-socket server. In this figure, the first memory slots for each channel on each processor are the white memory slots.



**Figure 1.** DIMM slot locations for 24-slot HPE ProLiant DL380 Gen10 two-socket servers



Figure 2 shows the memory slot configuration for 16-slot HPE ProLiant Gen10 two-socket servers. The configuration is similar to the 24-slot servers with the main difference being the number of slots on each memory channel. In these servers, one channel on each side of the CPU has two slots attached, while the remaining channels on each side of the CPU have only one slot attached. In the rest of this white paper, this will be referenced as a **2+1+1** configuration. Again, the first memory slots for each channel on each processor are the white memory slots. You should populate the memory for these servers following the illustrations found in [Appendix B](#).

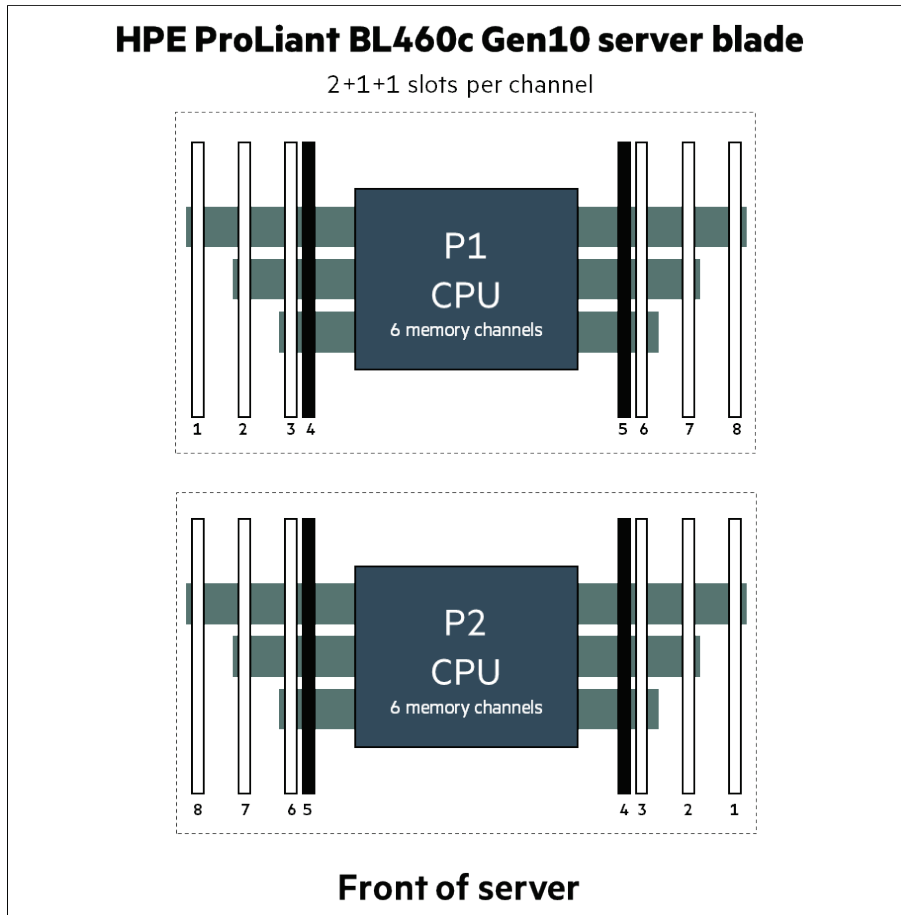


Figure 2. DIMM slot locations for 16-slot HPE ProLiant BL460c Gen10 two-socket servers



### DIMM population order

Figure 3 and Figure 4 show the DIMM population order for HPE ProLiant Gen10 servers (both 12 memory slots per CPU and eight memory slots per CPU). For a given number of DIMMs per CPU, populate those DIMMs in the corresponding numbered memory slot(s) on that row within the chart.

HPE ProLiant Gen10 12 slot per CPU DIMM population order											
1 DIMM								8			
2 DIMMs							8		10		
3 DIMMs							8		10		12
4 DIMMs			3		5		8		10		
5 DIMMs*			3		5		8		10		12
6 DIMMs	1		3		5		8		10		12
7 DIMMs*	1		3		5		7	8		10	12
8 DIMMs			3	4	5	6	7	8	9	10	
9 DIMMs*	1		3		5		7	8	9	10	11 12
10 DIMMs*	1		3	4	5	6	7	8	9	10	12
11 DIMMs*	1		3	4	5	6	7	8	9	10	11 12
12 DIMMs	1	2	3	4	5	6	7	8	9	10	11 12
* Unbalanced, not recommended											

Figure 3. DIMM population order for HPE ProLiant Gen10 12 slot per CPU servers

As shown in Figure 3, memory should be installed as indicated based upon the total number of DIMMs being installed per CPU. For example, if two DIMMs are being installed per CPU, they should be located in white memory slots numbered 8 and 10. If six DIMMs are being used per CPU, they should be installed in memory slots 1, 3, 5, 8, 10, and 12. Unbalanced configurations are noted with an asterisk and are not recommended because memory performance will be inconsistent or degraded compared to a balanced configuration.

HPE ProLiant Gen10 8 slot per CPU DIMM population order							
1 DIMM			3				
2 DIMMs		2	3				
3 DIMMs	1	2	3				
4 DIMMs		2	3			6	7
5 DIMMs*	1	2	3			6	7
6 DIMMs	1	2	3			6	7 8
7 DIMMs*	1	2	3	4		6	7 8
8 DIMMs*	1	2	3	4	5	6	7 8
* Unbalanced, not recommended							

Figure 4. DIMM population order for HPE ProLiant Gen10 eight slot per CPU servers

As shown in Figure 4, memory should be installed as indicated based upon the total number of DIMMs being installed per CPU. For example, if two DIMMs are being installed, they should be located in white memory slots numbered 2 and 3. If six DIMMs are being used, they should be installed in memory slots 1, 2, 3, 6, 7, and 8. Unbalanced configurations are noted with an asterisk and are not recommended because memory performance will be inconsistent or degraded compared to a balanced configuration.



HPE ProLiant Gen10 6 slot per CPU DIMM population order						
1 DIMM				4		
2 DIMMs				4	5	
3 DIMMs				4	5	6
4 DIMMs		2	3	4	5	
5 DIMMs*		2	3	4	5	6
6 DIMMs	1	2	3	4	5	6
* Unbalanced, not recommended						

Figure 5. DIMM population order for HPE ProLiant Gen10 six slot per CPU servers

As shown in Figure 5, memory should be installed as indicated based upon the total number of DIMMs being installed per CPU. For example, if two DIMMs are being installed, they should be located in white memory slots numbered 4 and 5. If four DIMMs are being used, they should be installed in memory slots 2, 3, 4, and 5. Unbalanced configurations are noted with an asterisk and are not recommended because memory performance will be inconsistent or degraded compared to a balanced configuration.

## Memory interleaving

Memory interleaving is a technique used to maximize memory performance by spreading memory addresses evenly across memory devices. Interleaved memory results a contiguous memory region across multiple devices with sequential accesses using each memory device in turn, instead of using the same one repeatedly. The result is higher memory throughput due to the reduced wait times for memory banks to become available for desired operations between reads and writes.

Memory interleaving techniques include:

### Channel interleaving

When configured correctly, sequential reads will be interleaved across memory channels. Channel bandwidth will be accumulated across the interleaved channels.

### Rank interleaving

When configured correctly, sequential reads within the channel will be interleaved across ranks. This enhances channel throughput by increasing utilization on the channel. Rank interleaving is a low priority than channel interleaving when creating an interleave region and a 1-DPC region across three channels will be higher priority than a two-DIMM region within a channel.

### Memory controller interleaving

This technique is used where multiple memory controllers exist in each physical CPU using high-bandwidth, low-latency interconnect. When configured correctly, sequential reads will also be interleaved across these memory controllers. Memory controller bandwidth will be accumulated across interleaved memory controllers.

### Node interleaving

This option is available from the ROM-Based Setup Utility (RBSU) Advanced Options menu and controls how the server maps the system memory across the processors. When node interleaving is disabled (default and recommended setting), BIOS maps the system memory such that the memory addresses for the DIMMs attached to a given processor are together, or contiguous. In typical applications, this arrangement is more efficient, allowing the processors to directly access the memory addresses containing the code and data for the programs they are executing.

When node interleaving is enabled, system memory addresses are alternated, or interleaved, across the DIMMs installed on both processors. In this case, each successive page in the system memory map is mapped to a different processor. There may be some workloads—in particular, those using shared data sets—that will see improved performance with node interleaving enabled.



### Disabling memory interleaving

This option is available from the Advanced Power Management menu in the RBSU Advanced Options menu. Disabling memory interleaving not only saves some power per DIMM but also decreases overall memory system performance.

### Understanding balanced memory configurations

Optimal memory performance is achieved when the system is configured with a fully homogeneous and balanced memory configuration. Unbalanced memory configurations are those in which the installed memory is not distributed evenly across the memory channels and/or the processors. Hewlett Packard Enterprise discourages unbalanced configurations because they will always have lower performance than similar balanced configurations. There are two types of unbalanced configurations, each with its own performance implications.

- Unbalanced across channels: A memory configuration is unbalanced across channels if the memory installed on each populated channel is not identical.
- Unbalanced across processors: A memory configuration is unbalanced across processors if a different amount of memory is installed on each of the processors.

### Memory configurations that are unbalanced across channels

In unbalanced memory configurations across channels, the memory controller will split memory into regions, as shown in Figure 6. In a balanced configuration, there will be one region that includes all installed DIMMs. If the memory configuration is unbalanced, it will attempt to create multiple balanced regions. First, it will create the largest possible balanced region with the installed memory. The next largest region comes next, and so on. In this manner, the memory controller will create regions until all installed memory has been assigned to a region.

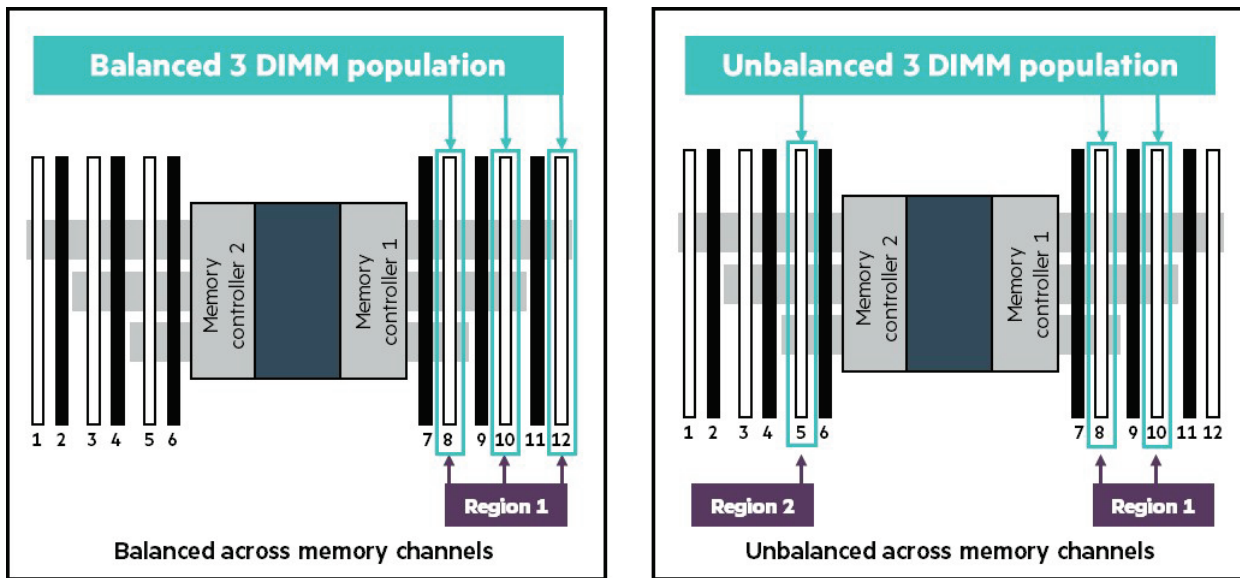


Figure 6. Examples of a balanced and an unbalanced configuration

In Figure 6, the illustration on the left depicts a balanced configuration, since each of the populated memory channel contains the same number of DIMMs (one each). Conversely, the image on the right is unbalanced because the DIMM in memory slot 5 creates a second memory region.

The primary effect of memory configurations that are unbalanced across channels is a decrease in memory throughput in those regions that span fewer memory channels. In the unbalanced example in Figure 6, worst case measured memory throughput in Region 2 would be 33% or less than the throughput in the balanced example. Even in Region 1 in the unbalanced picture, throughput would be limited to no more than 66% of what the single region in the balanced example could provide.





### Memory configurations that are unbalanced across processors

Figure 7 shows a memory configuration that is unbalanced across processors. The CPU 1 threads operating on the larger memory capacity of CPU 1 may have adequate local memory with relatively low latencies and high throughput. The CPU 2 threads operating on the smaller memory capacity of CPU 2 may consume all available memory on CPU 2 and request remote memory from CPU 1. The longer latencies and limited throughput of cross-CPU communications associated with the remote memory will result in reduced performance of those threads. In practice, this may result in nonuniform performance characteristics for software program threads, depending on which processor executes them.

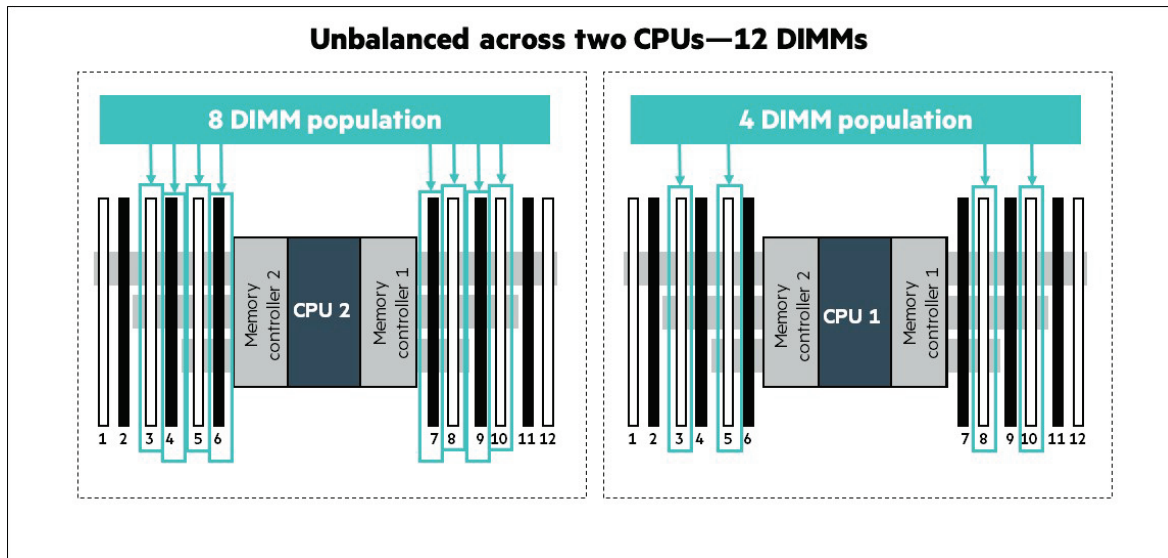


Figure 7. Example of memory that is unbalanced across processors

Figure 7 shows an example of unbalanced memory configurations across processors. In this example, the first processor contains four DIMMs while the second CPU has eight DIMMs installed.

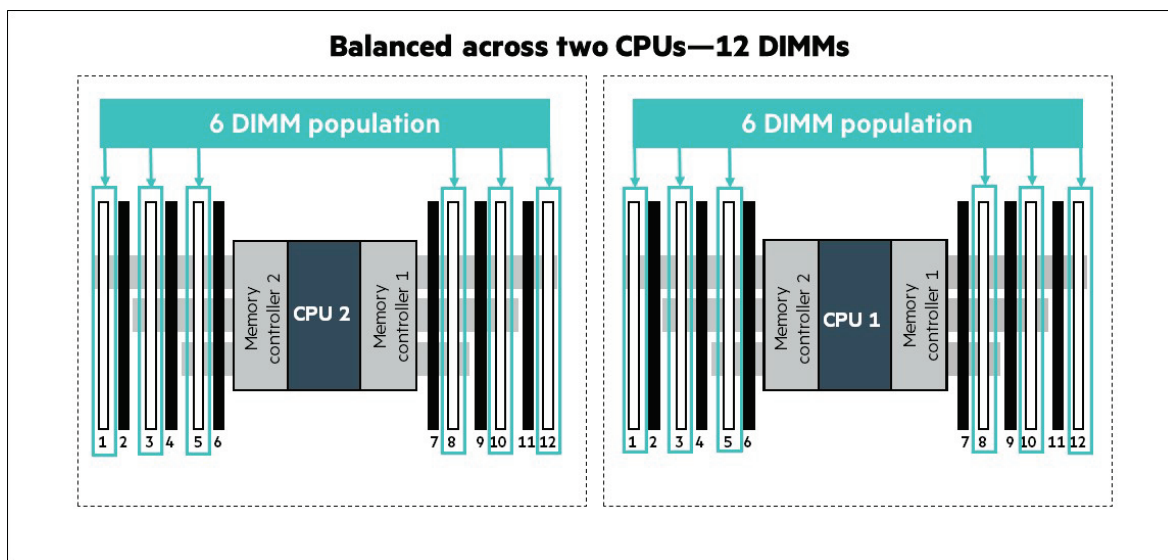


Figure 8. Example of a memory configuration that is balanced across processors

Figure 8 shows an example of a configuration that is balanced across processors. In this example, both processors have six DIMMs installed.



## Memory RAS mode and population requirements

HPE ProLiant Gen10 servers using the Intel Xeon Processor Scalable family support four different memory RAS modes. If you plan to enable any of these advanced RAS modes, please see the [HPE Server Memory RAS white paper](#) for more specific information regarding memory configuration and population rules.

- Advanced Error Correction Code
- Online Spare
- Mirrored Memory
- HPE Fast Fault Tolerance

The rules on channel DIMM population and channel DIMM matching vary by the RAS mode used. However, regardless of RAS mode, the requirements for DIMM population within a system and a channel must be met at all times.

For RAS modes that require matching DIMM populations, the same memory slot positions across channels must hold the same DIMM type with regard to size and organization. DIMM timings do not have to match, but timings will be set to support all DIMMs populated (that is, DIMMs with slower timings will force faster DIMMs to the slower common timing modes).

## Conclusion

HPE SmartMemory for HPE ProLiant Gen10 servers offers greater memory performance than ever before. The HPE DDR4-2666 SmartMemory for HPE ProLiant Gen10 servers that use the Intel Xeon Processor Scalable family delivers increased memory throughput and lower latencies. HPE SmartMemory also provides extended performance in many configurations by operating at higher speeds compared to third-party memory.

## Appendix A—HPE Gen10 server memory connector locations

This section illustrates the physical location of the memory slots for the HPE ProLiant Gen10 servers using the Intel Xeon Processor Scalable family.

### HPE ProLiant DL360/DL380/DL560/DL580 Gen10 memory connector locations

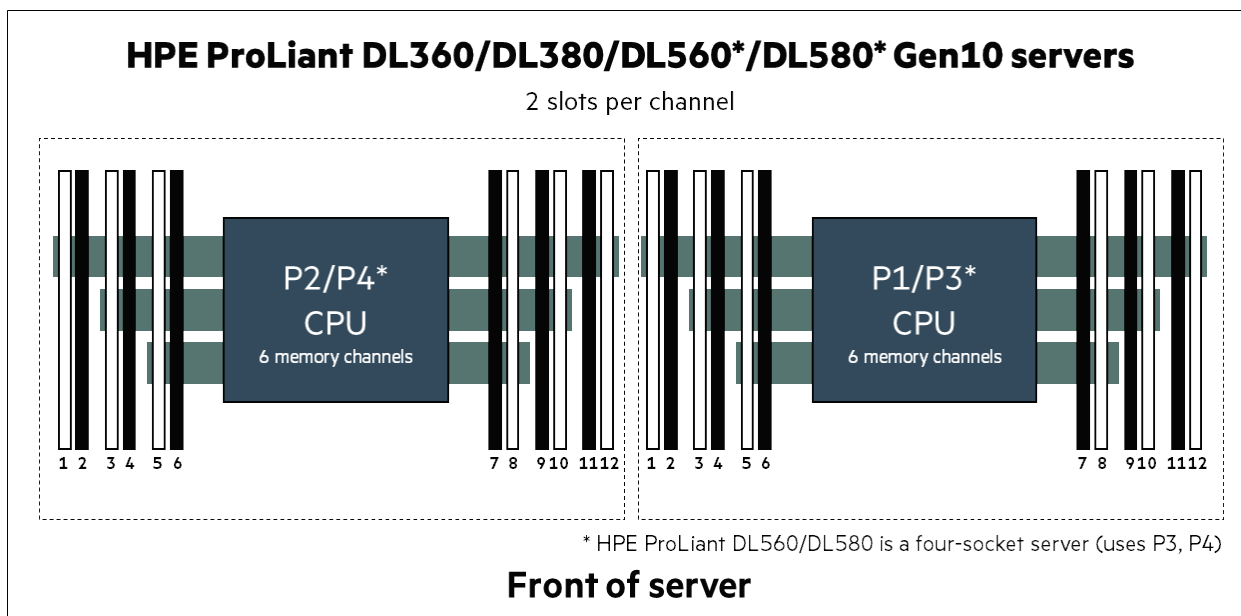


Figure 9. HPE ProLiant DL360/DL380/DL560 Gen10 server DIMM socket positions



### HPE Synergy 480 Gen10 memory connector locations

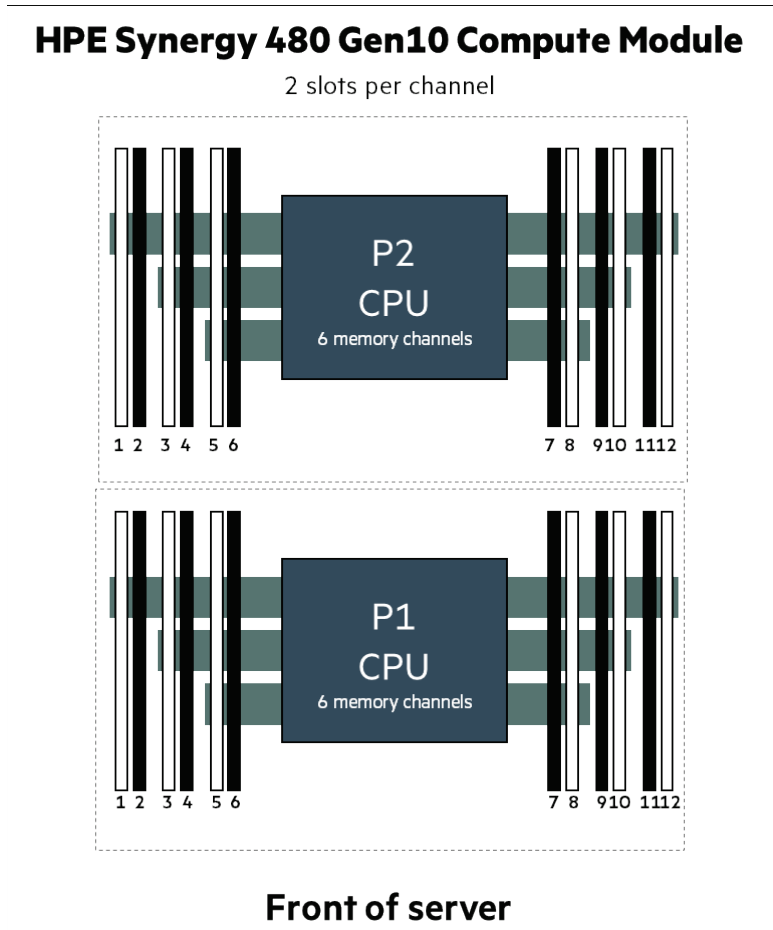


Figure 10. HPE Synergy 480 Gen10 DIMM socket positions



### HPE ProLiant ML350 Gen10 memory connector locations

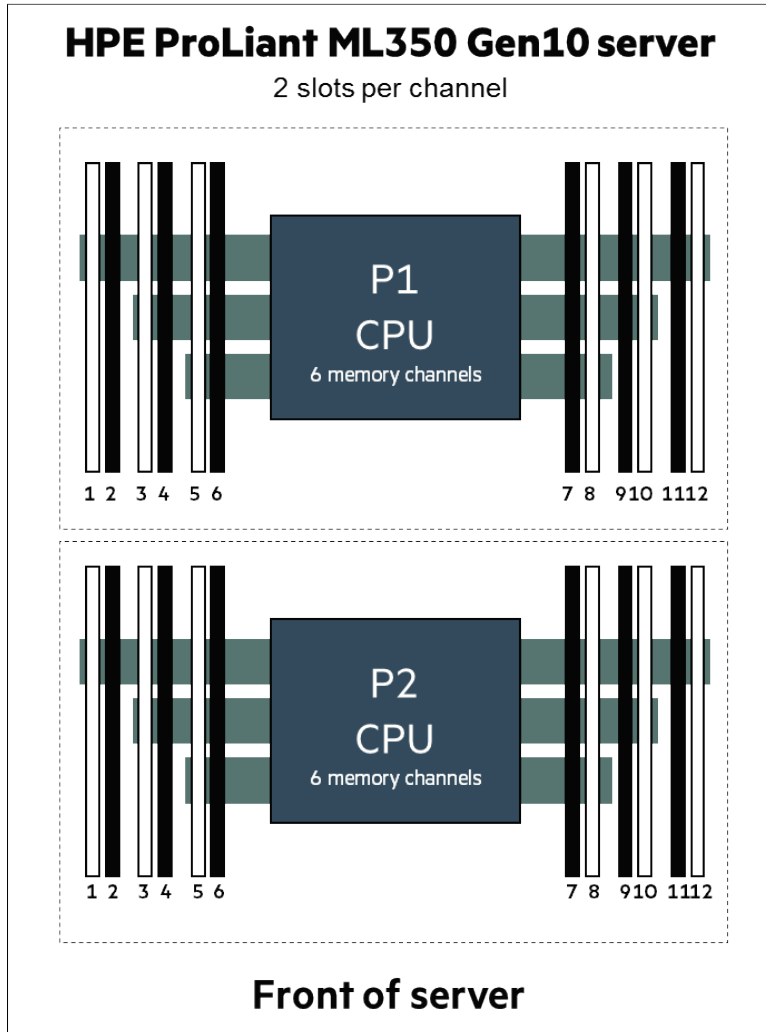
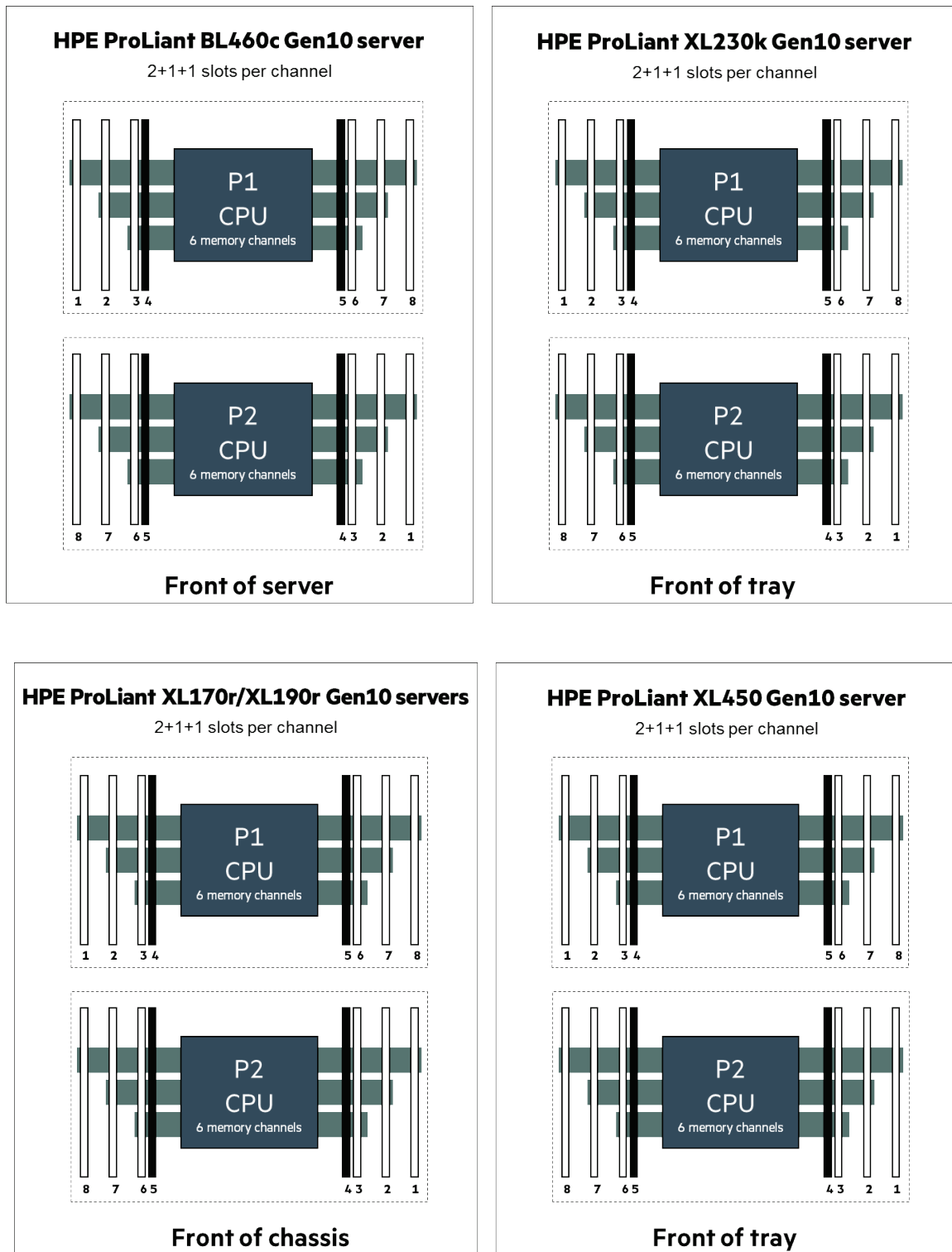


Figure 11. HPE ProLiant ML350 Gen10 Server DIMM socket positions



**HPE ProLiant BL460c Gen10 server blade/HPE ProLiant XL450/XL170r/XL190r/XL230k Gen10 memory connector locations**



**Figure 12.** HPE ProLiant BL460c Gen10 server blade/HPE ProLiant XL230k/HPE ProLiant XL170r/XL190r/HPE ProLiant XL450 Gen10 DIMM socket positions



### HPE ProLiant ML110 Gen10 server

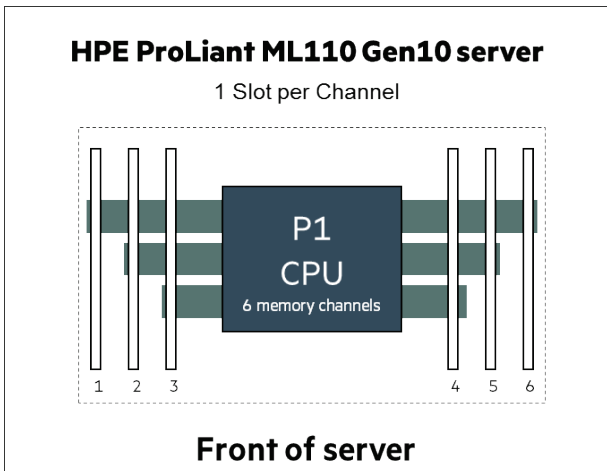


Figure 13. HPE ProLiant ML110 Gen10 DIMM socket positions

### HPE Synergy 660 Gen10 compute module memory connector locations

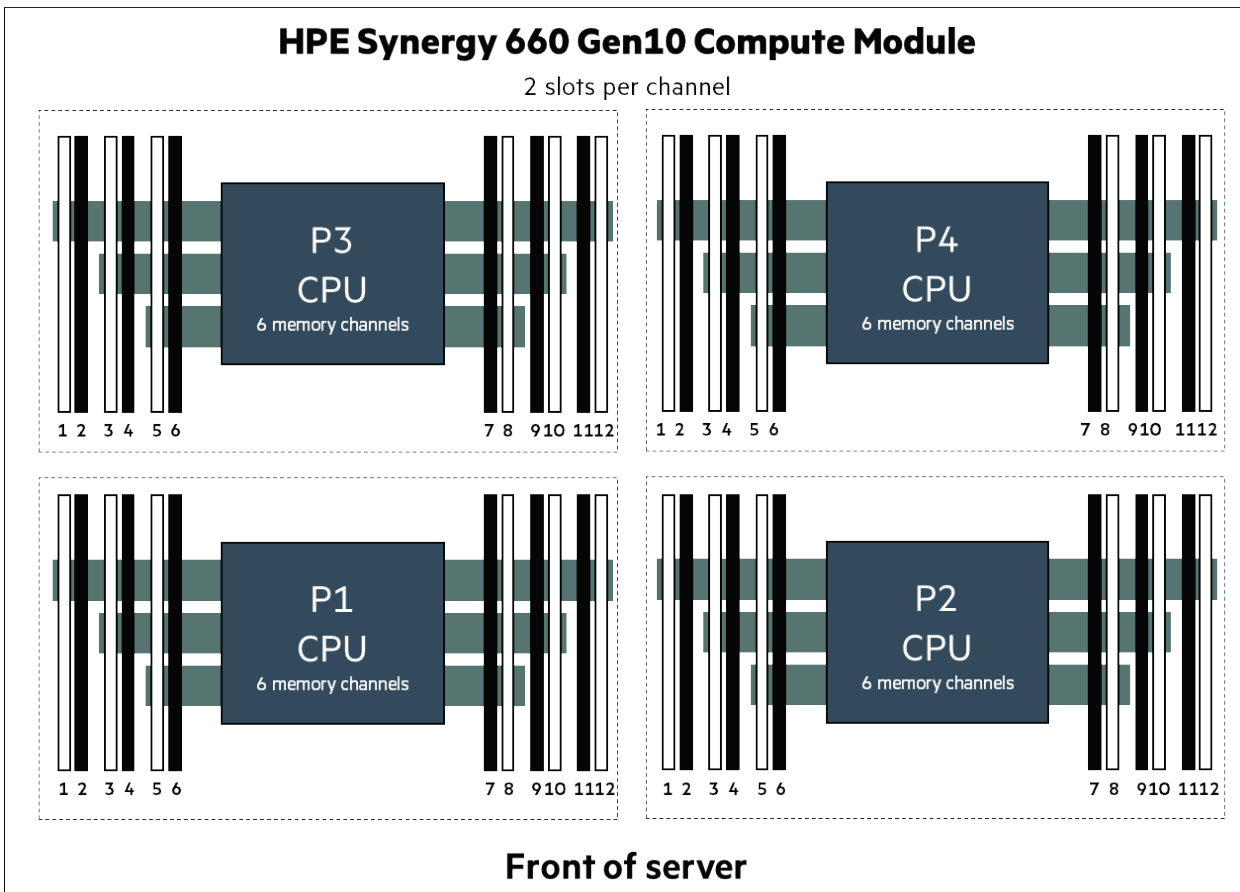


Figure 14. HPE Synergy 660 Gen10 DIMM socket positions



## Appendix B—HPE Gen10 DIMM population locations

This section illustrates which memory slots to use when populating memory in HPE ProLiant Gen10 servers using the Intel Xeon Processor Scalable family. Each illustration reflects in which memory slots to populate memory for a given number of memory DIMMs around a single processor, given a common DIMM type. If multiple processors are installed, split the DIMMs evenly across the processors and follow the corresponding rule when populating DIMMs for each processor. Figures 15 to 22 represent the bootstrap processor and the population shown will ensure that the first DIMM populated is in the right place. Unbalanced configurations are noted with an asterisk and are not recommended because memory performance will be inconsistent or degraded compared to a balanced configuration.

In cases of a heterogeneous mix, take each DIMM type and create a configuration as if it were a homogeneous configuration. Depending on the per-channel rules, populate the DIMMs with highest rank count in white memory slots in each channel, then populate the other DIMMs in the black memory slots in each channel. See the last illustration for an example of a popular mix.

### HPE ProLiant DL360/DL380/ML350/DL560/DL580/Synergy 480/Synergy 660 Gen10 servers

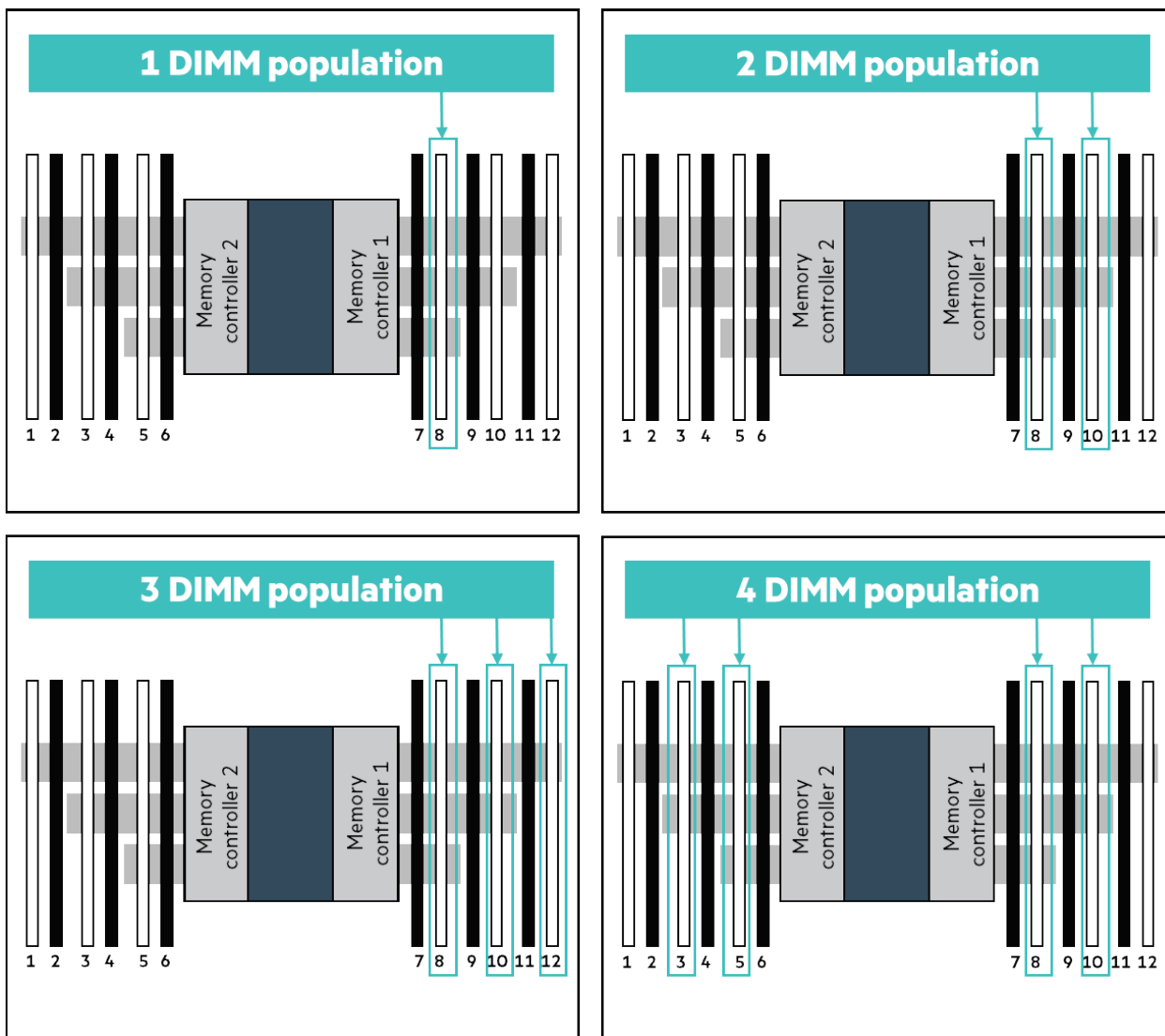


Figure 15. Per-CPU DIMM population diagrams for servers with 12 DIMM sockets per CPU (examples for one to four DIMMs)



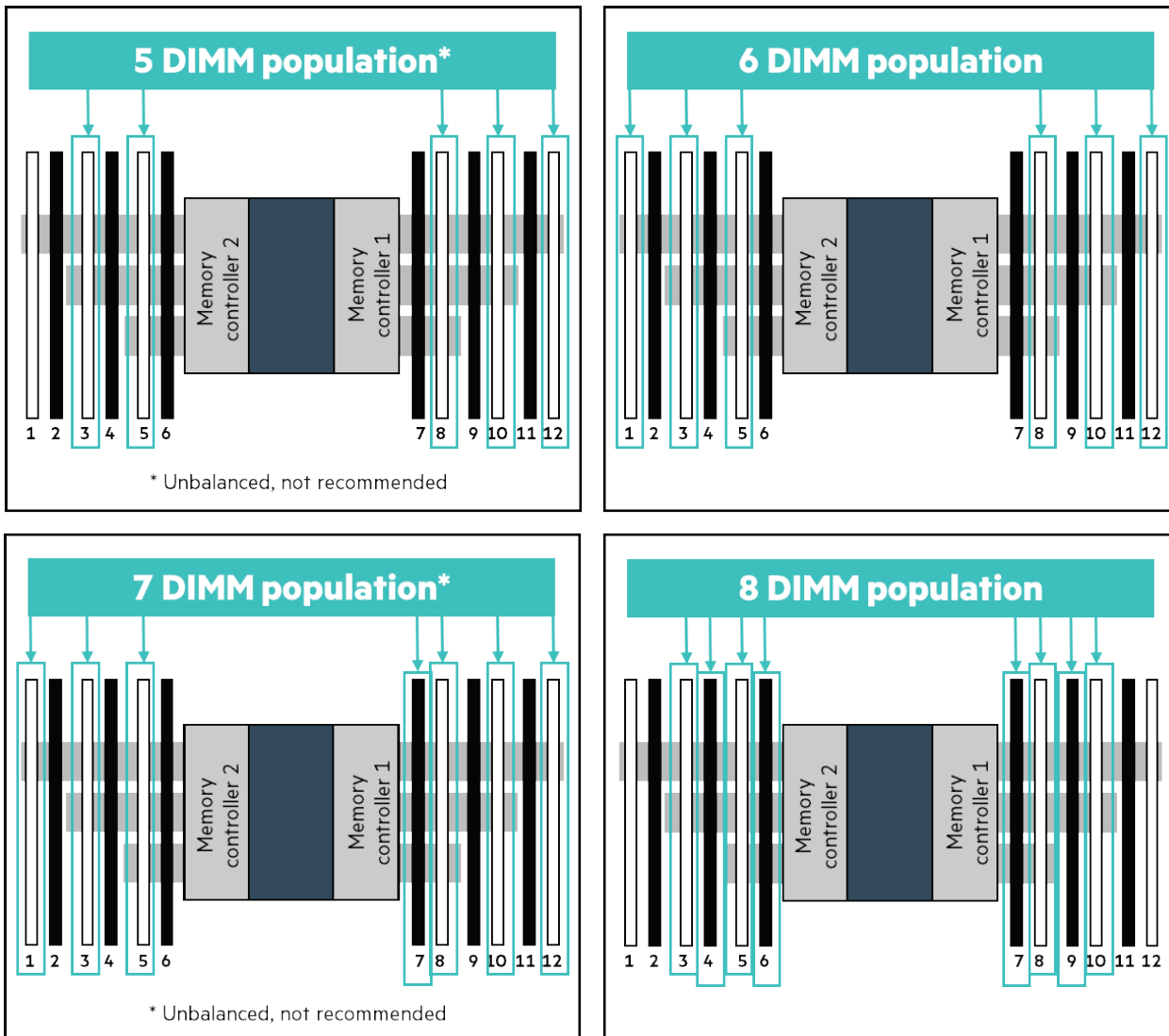


Figure 16. Per-CPU DIMM population diagrams for servers with 12 DIMM sockets per CPU (examples for five to eight DIMMs)





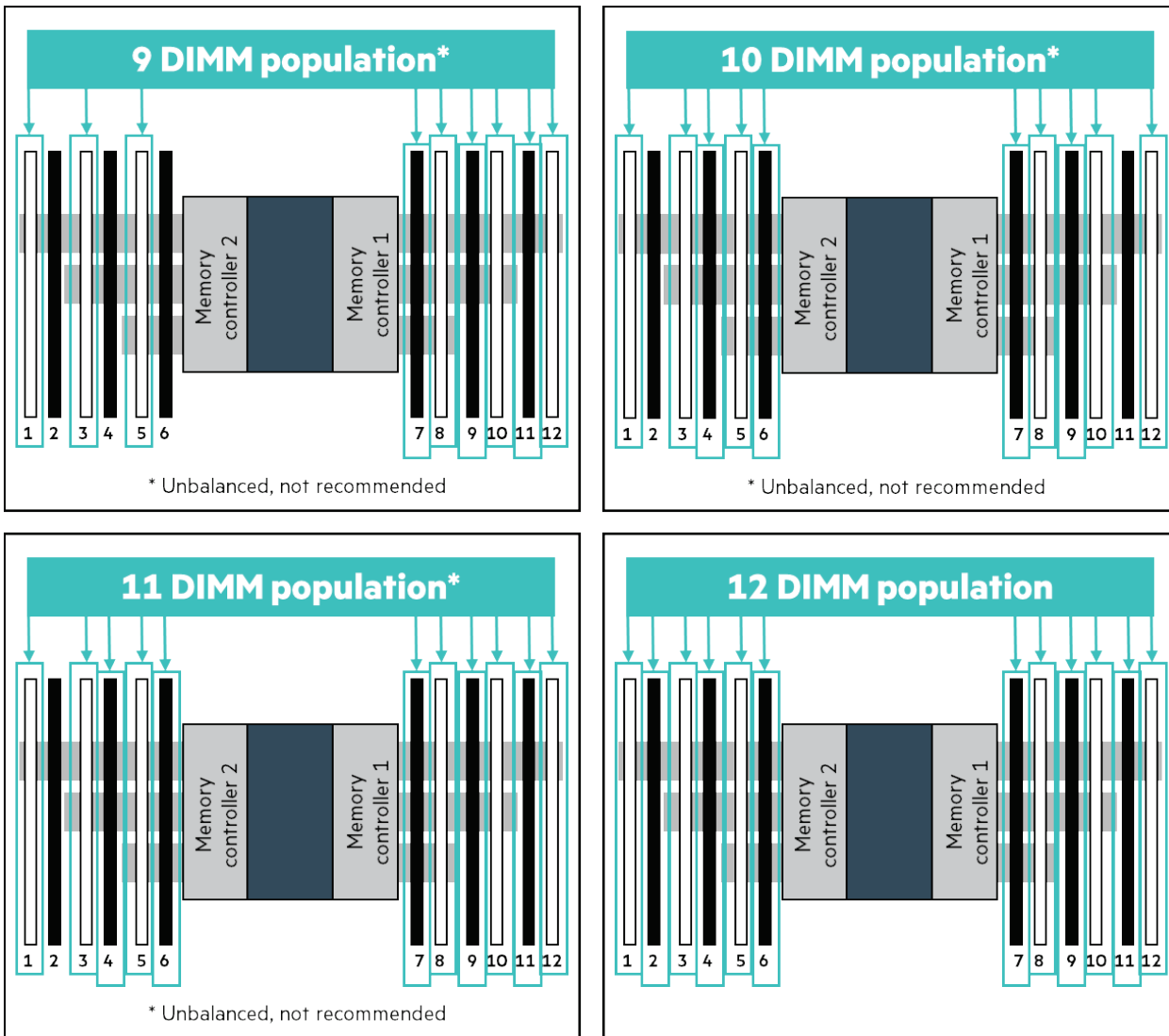


Figure 17. Per-CPU DIMM population diagrams for servers with 12 DIMM sockets per CPU (examples for nine to 12 DIMMs)



**HPE ProLiant BL460c Gen10 server blade/HPE ProLiant XL170r/XL190r/XL230k/XL450 Gen10 server**

On these platforms, for maximum throughput, the recommended configuration is six DIMMs per CPU. Eight DIMMs per CPU while maximizing memory capacity results in an unbalanced configuration, which will reduce performance.

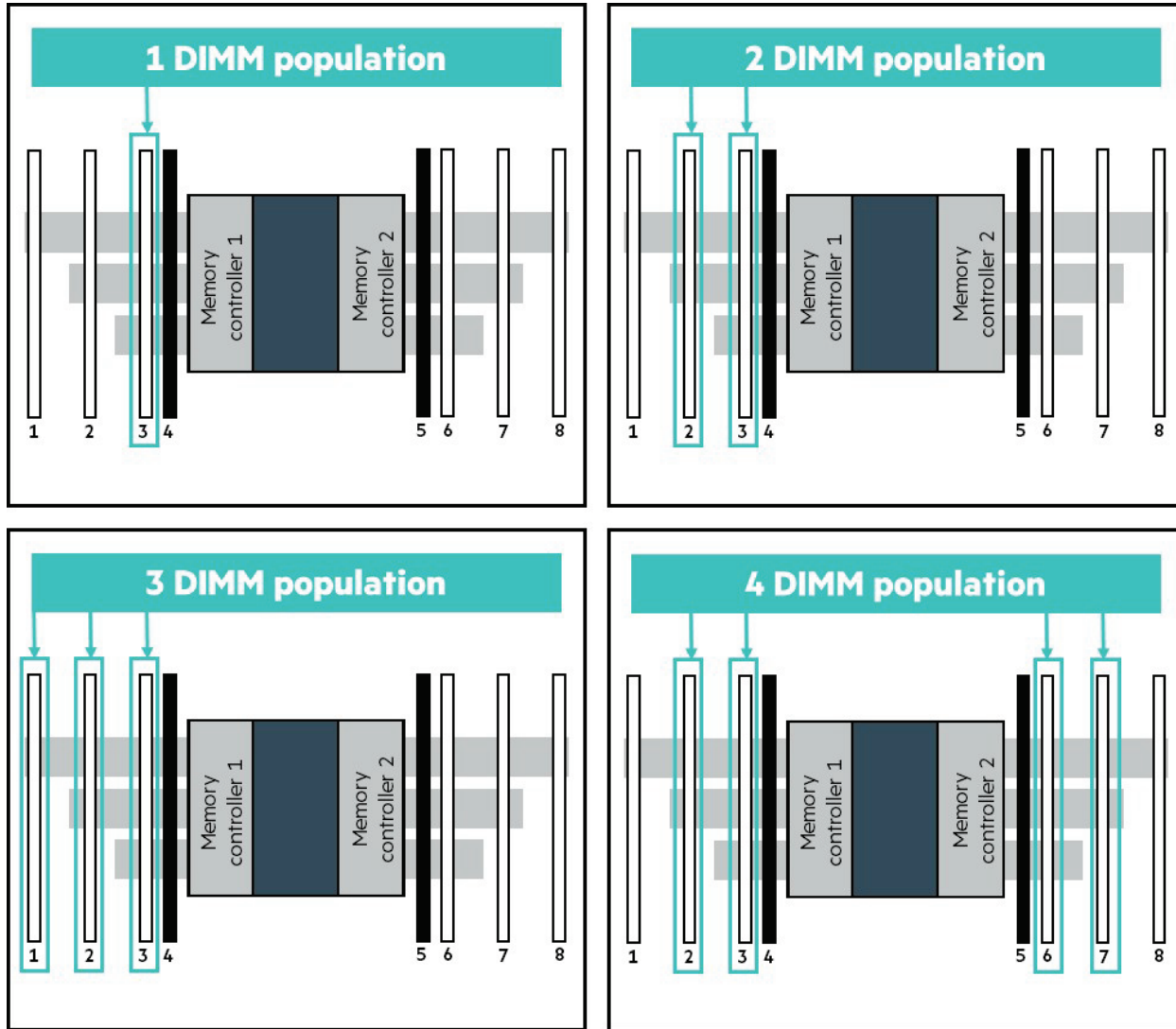


Figure 18. Per-CPU DIMM population diagrams for servers with eight DIMM sockets per CPU (examples for one to four DIMMs)



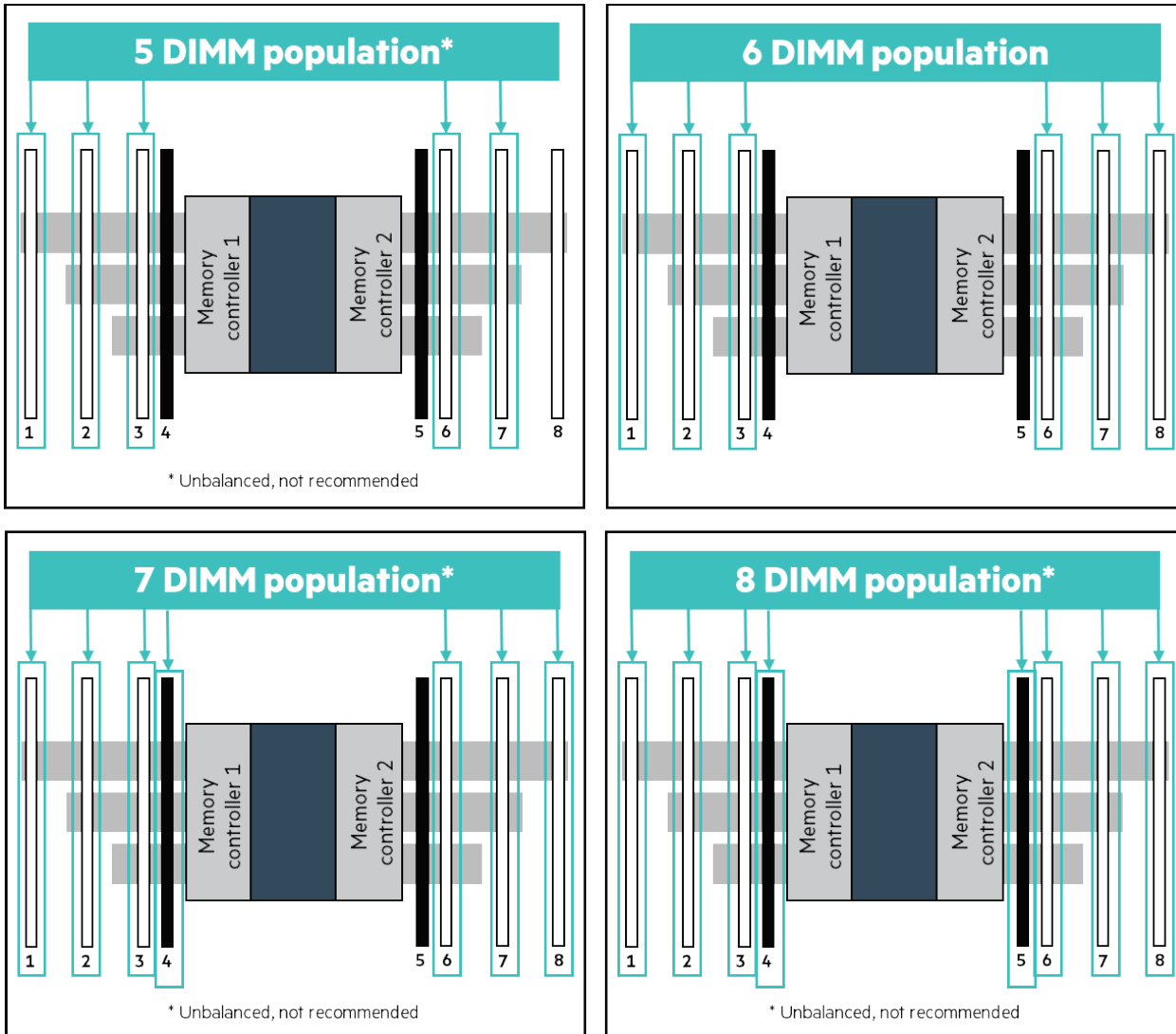


Figure 19. Per-CPU DIMM population diagrams for servers with 8 DIMM sockets per CPU (examples for five to eight DIMMs)



### HPE ProLiant ML110 Gen10 server

On these platforms, for maximum throughput, the recommended configuration is six DIMMs per CPU. Eight DIMMs per CPU while maximizing memory capacity results in an unbalanced configuration, which will reduce performance.

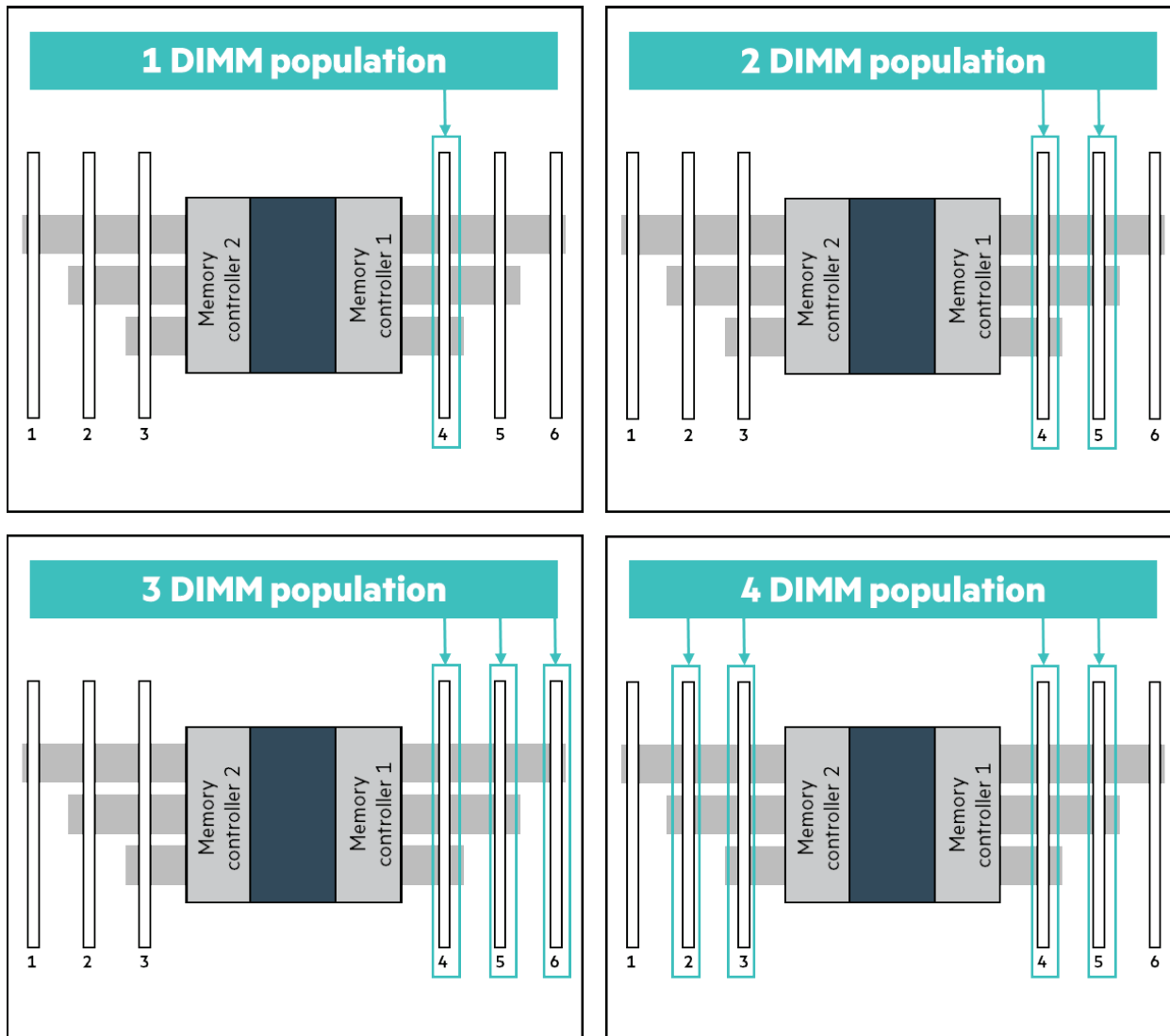


Figure 20. Per-CPU DIMM population diagrams for servers with six DIMM sockets per CPU (examples for one to four DIMMs)



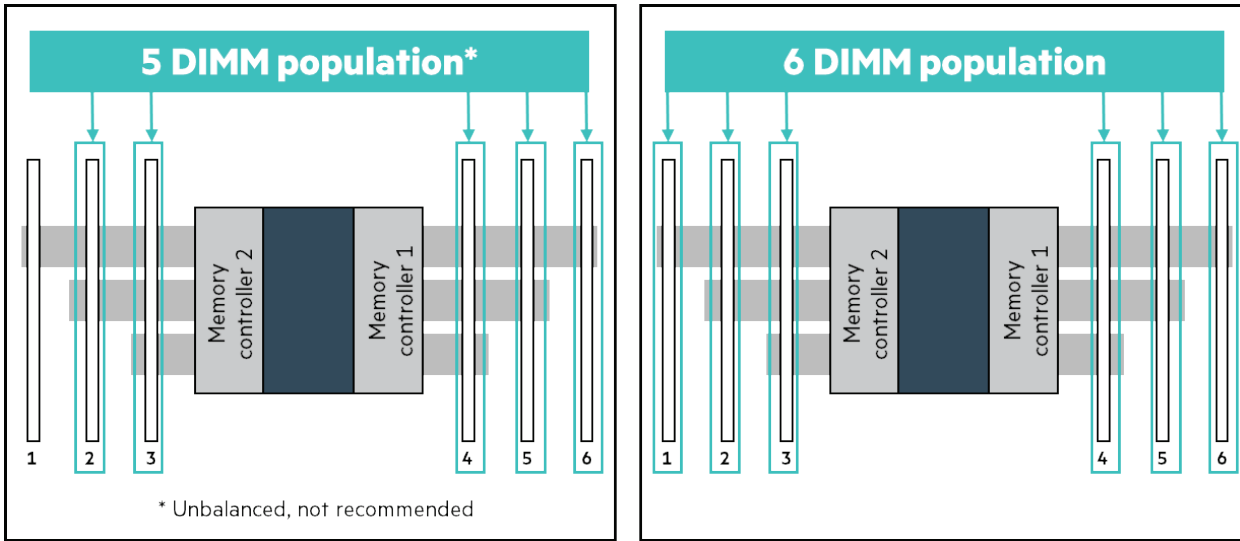


Figure 21. Per-CPU DIMM population diagrams for servers with six DIMM sockets per CPU (examples for five to six DIMMs)

### Mixed DIMM configurations

In cases of a heterogeneous mix, take each DIMM type and create a configuration as if it were a homogeneous configuration. Depending on the per-channel rules, populate the DIMMs with highest rank count in white memory slots in each channel, then populate the other DIMMs in the black memory slots in each channel as shown in the following illustration.

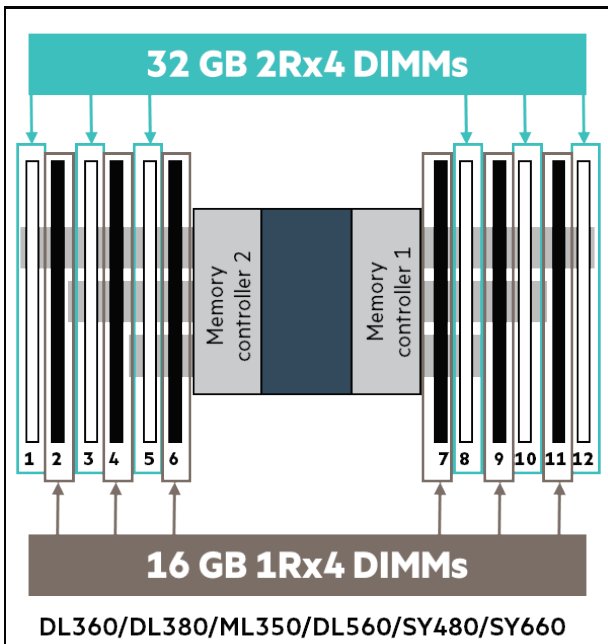


Figure 22. Mixing 32 GB and 16 GB DIMMs



## Technical white paper

### Resources

HPE servers technical white papers library

[hpe.com/docs/servertechnology](http://hpe.com/docs/servertechnology)

HPE Server Memory

[hpe.com/info/memory](http://hpe.com/info/memory)

HPE Memory Configurator

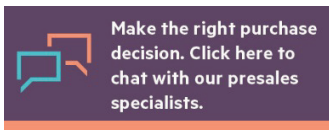
[hpe.com/servers/servermemoryconfigurator](http://hpe.com/servers/servermemoryconfigurator)

HPE Server Memory whiteboard video

[hpe.com/h22228/video-gallery/us/en/products/EB2D5B6E-B6CB-435E-AB08-B42DA06A9962/r/video](http://hpe.com/h22228/video-gallery/us/en/products/EB2D5B6E-B6CB-435E-AB08-B42DA06A9962/r/video)

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