Signal/Power Integrity for Flipchip BGA Package

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- System Level Model
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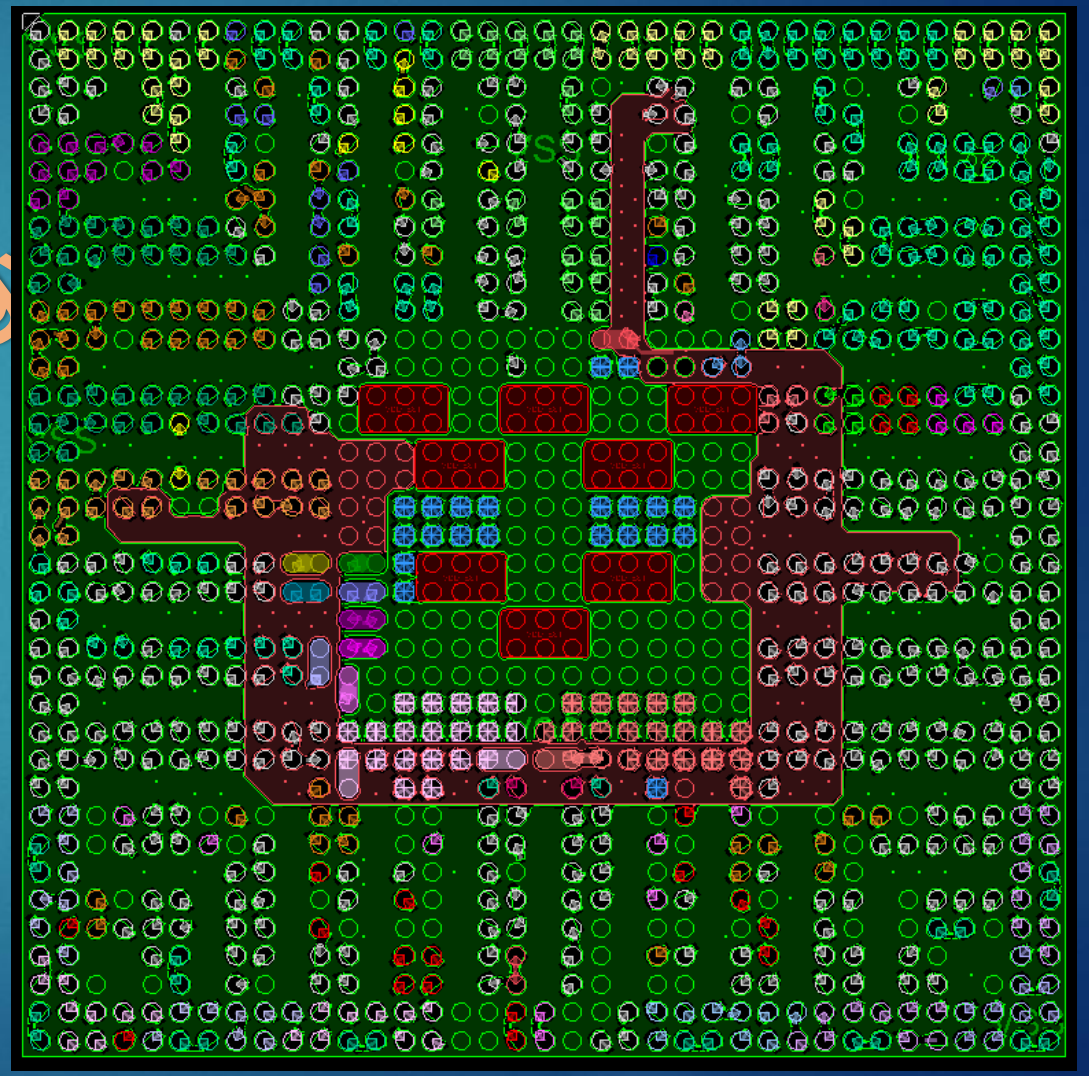
PKG Overview:

- Die size: 13.071x10994 (post shrink incl. seal ring/scribe lines)
- Die Bumps: 5231
- Bump pitch: 162.95x162.00um
- Package type: 8-layers flip chip BGA
- Package size: 25x25mm
- Ball count: 1086 with 0.65mm pitch
- Channelled ball pattern for ease of routability
- Decaps: 24 (core:14, DDR:4, VDDIO: 6, HDMI:3)

Ballout with Chnnels

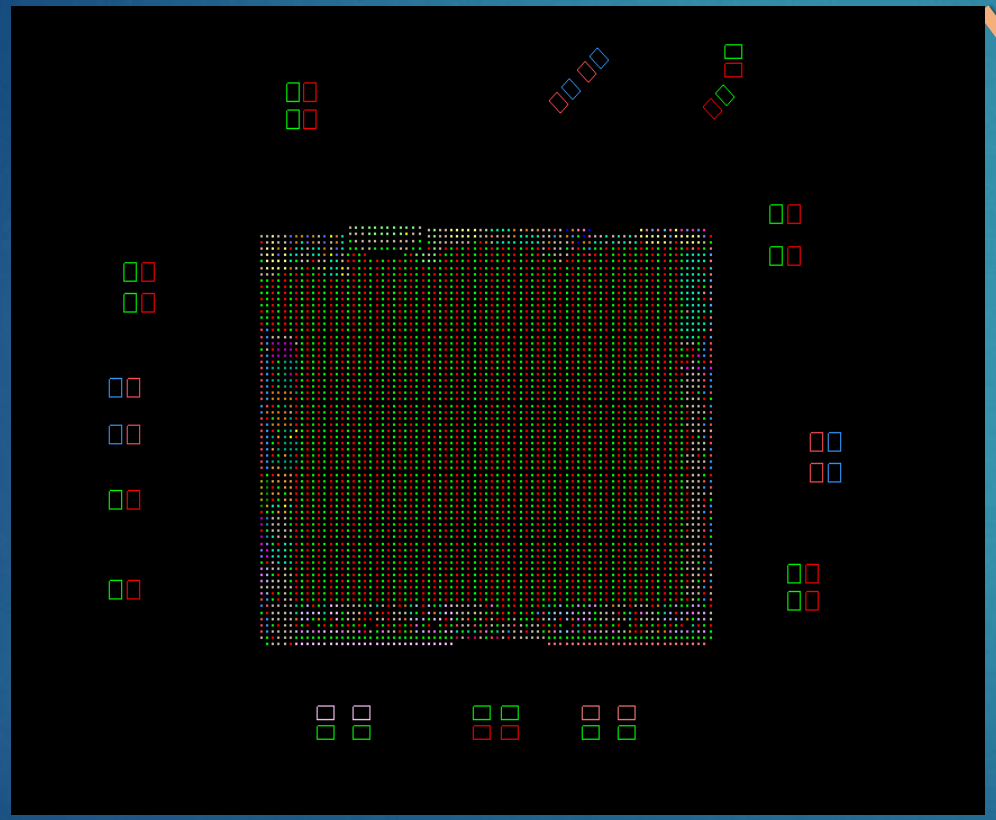
25x25mm FC BGA
1086 Balls
0.65mm Pitch

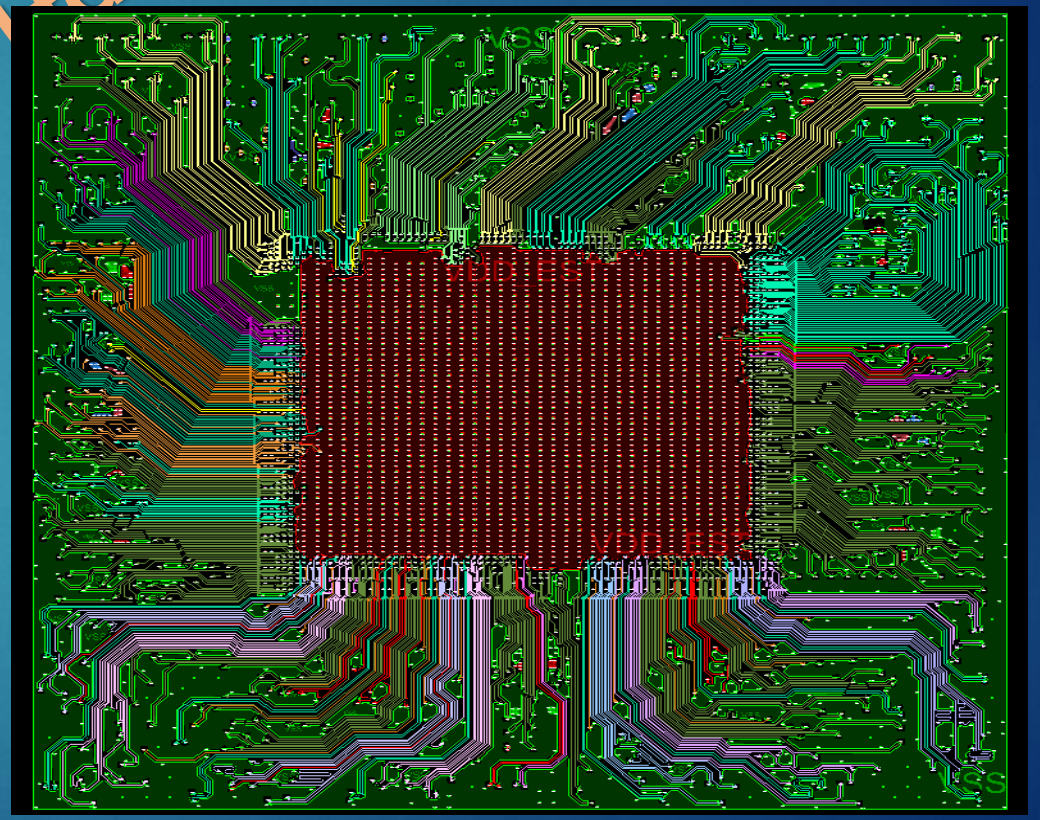


Substrate Stackup

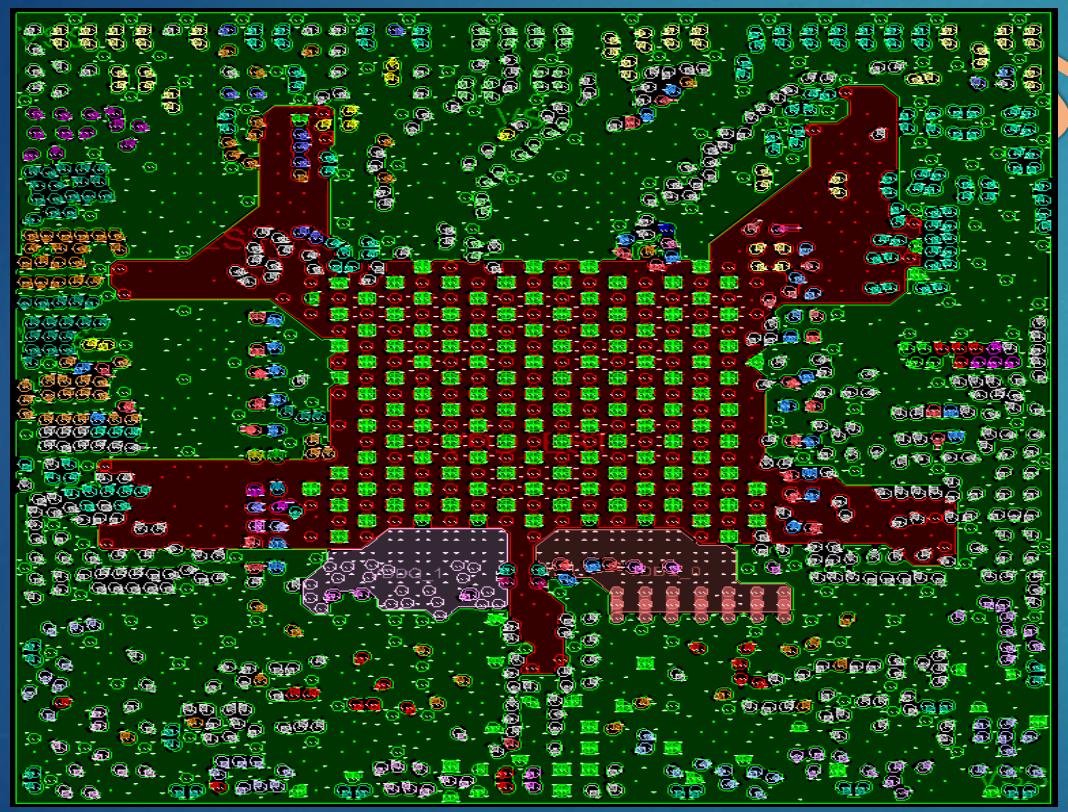
Subclass Name	Type	Material	Thickness (UM)	Conductivity (mho/cm)	Dielectric Constant	Loss Tangent	Freq Dep File	Negative Artwork	Shield	Width (UM)	Etch Factor (Degrees)	Unused Pin Pad Suppression	Unused Via Pad Suppression
	SURFACE	AIR		0	1	0							
	DIELECTRIC												
CU-1	CONDUCTOR	COPPER	15.000000	595900	4.5	0				14	90.00		
DRILL1-2	DIELECTRIC	ABF-GX13	35.000000	0	3.35	0.012							
CU-2	CONDUCTOR	COPPER	15.000000	595900	3.35	0.012				75	90.00		
DRILL2-3	DIELECTRIC	ABF-GX13	35.000000	0	3.35	0.012							
CU-3	CONDUCTOR	COPPER	15.000000	595900	3.35	0.012				75	90.00		
DRILL3-4	DIELECTRIC	ABF-GX13	35.000000	0	3.35	0.012							
CU-4	CONDUCTOR	COPPER	18.000000	595900	3.35	0.012				75	90.00		
DRILL4-5	DIELECTRIC	E679FGR	800.000000	0	4.7	0.018							
CU-5	CONDUCTOR	COPPER	18.000000	595900	3.35	0.012				75	90.00		
DRILL5-6	DIELECTRIC	ABF-GX13	35.000000	0	3.35	0.012							
CU-6	CONDUCTOR	COPPER	15.000000	595900	3.35	0.012				75	90.00		
DRILL6-7	DIELECTRIC	ABF-GX13	35.000000	0	3.35	0.012							
CU-7	CONDUCTOR	COPPER	15.000000	595900	3.35	0.012				14	90.00		
DRILL7-8	DIELECTRIC	ABF-GX13	35.000000	0	3.35	0.012							
CU-8	CONDUCTOR	COPPER	15.000000	595900	4.5	0				14	90.00		
	DIELECTRIC												
	SURFACE	AIR		0	1	0							

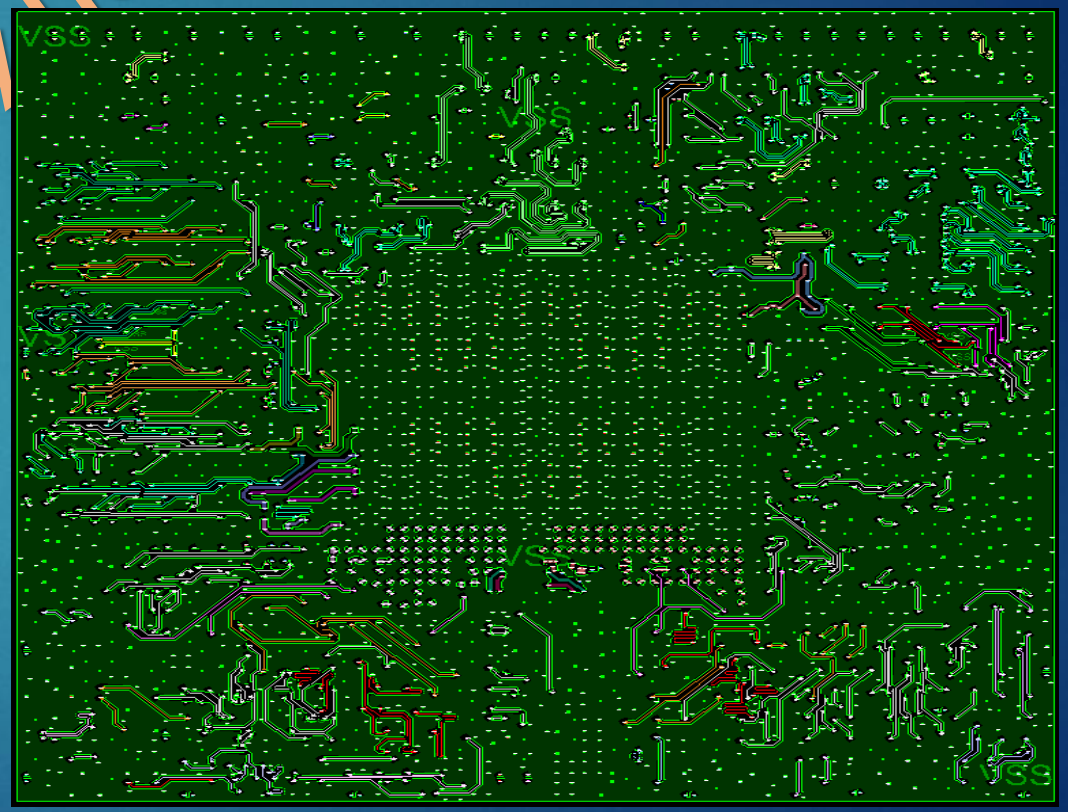
Substrate Layers





Substrate Layers (Cont.)





High Speed Nets Balancing

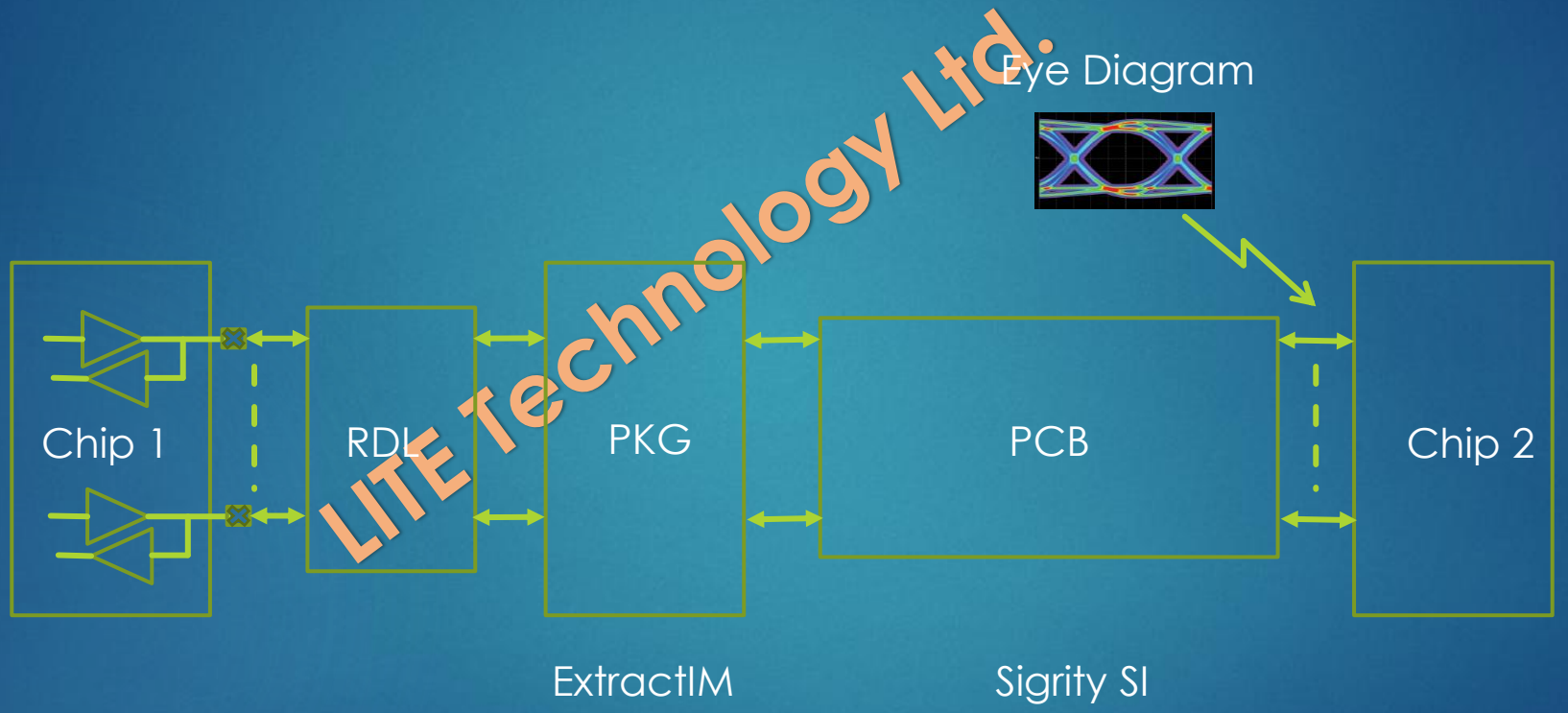
Skew Budget

Package Design Requirement: Please specify by group															
Interface/Net	DDR	MIPI CSI	MIPI DSI	HiSPi	NAND	SDHOST	LVDS	ETHERNET	HDMI-RX	HDMI-TX	USB	RF	AFE	SENSOR	LR ADC
Single End Impedance	50 Ω	50 Ω	50 Ω	50 Ω	50 Ω	50 Ω	50 Ω	50 Ω	-	-					
Differential Impedance	100 Ω	100 Ω	100 Ω	100 Ω	100 Ω	100 Ω	100 Ω	100 Ω	100 Ω	100 Ω	100 Ω	100 Ω	100 Ω	100 Ω	100 Ω
Time Skew in Pair	3ps	10ps	10ps	50ps	-	-	7ps	-	25ps	5ps	3ps		3ps	5ps	3ps
Time Skew in Group (Lane to Lane) - CMD/ADDR/CTRL lines	25ps	50ps	50ps	-	100ps	1.92ns	10ps	100ps	100ps	30ps	50ps			50ps	
Time Skew in Group (Lane to Lane) - data lines	10ps	-	-	100ps				-	-						
Return Loss @ Frequency															
Insertion Loss @ Frequency															
Resistance/Inductance/Capacitance															
Cross Talk noise Coefficient to Adjacent Signal															

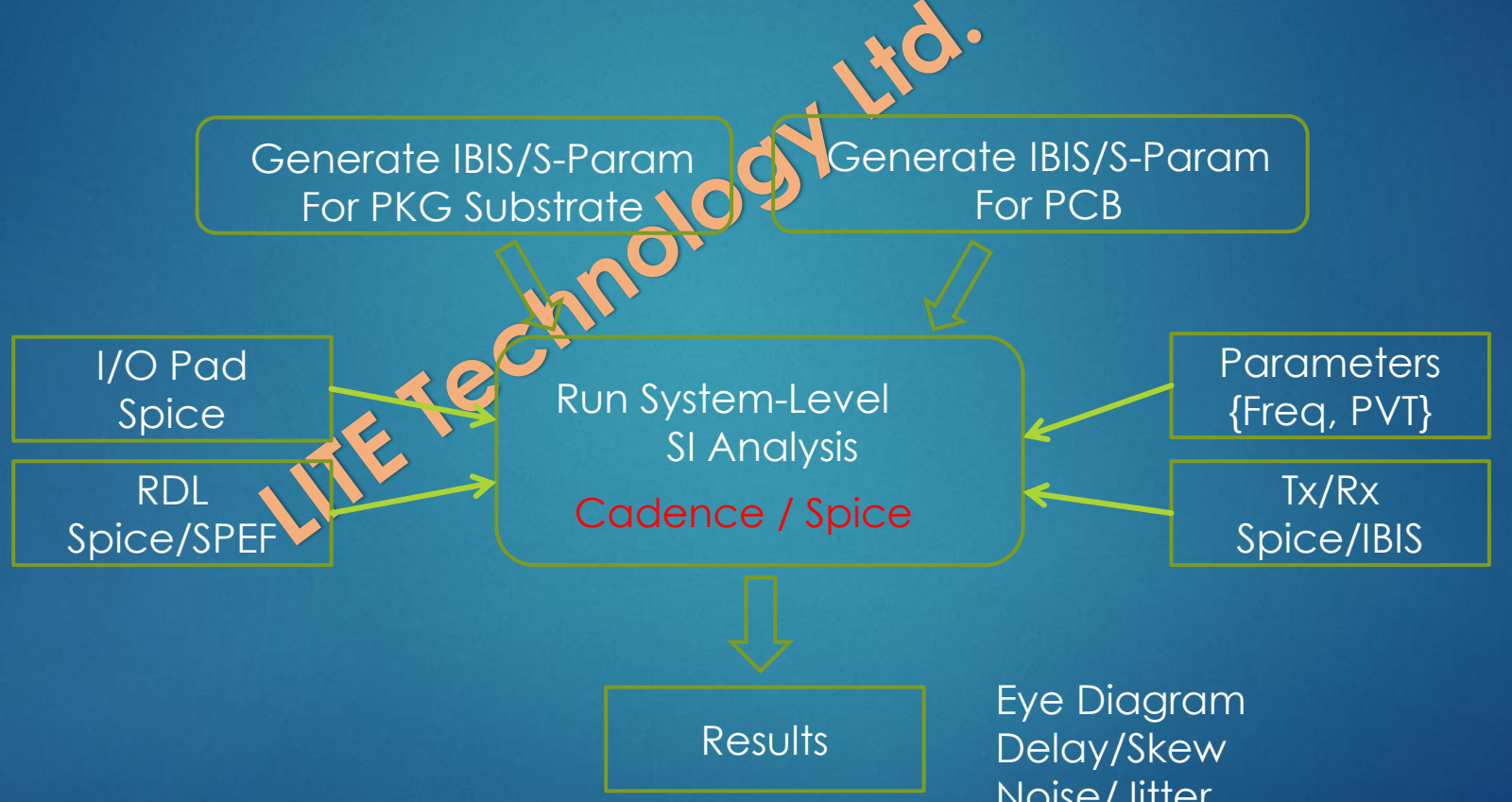
System Level SI Analysis

- High Speed Interfaces
  - DDR, HDMI, USB, etc.
- End-to-End Model
  - I/O pads: Spice, IBIS
  - RDL: RLC, SPEF, Spice
  - Package: IBIS, S-Parameters, Spice
  - PCB: IBIS, S-Parameters, Spice
  - DDR (3rd Party): Spice, IBIS
- Tools
  - Star-RC / RedHawk for RDL extraction
  - XtractIM for PKG extraction
  - Sigrity SI for PCB extraction and analysis

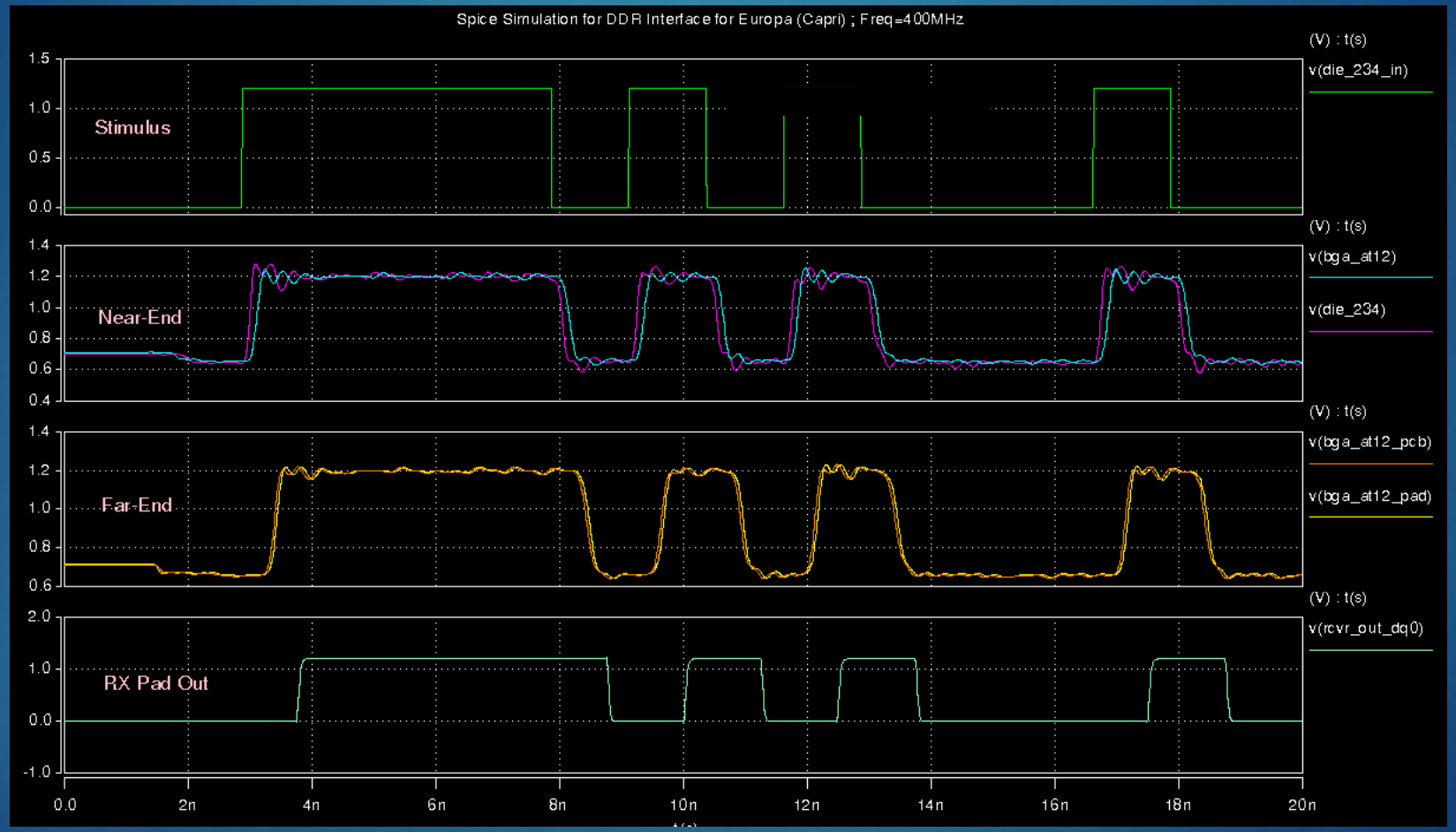
System Model



Signal Integrity Analysis Flow



DDR Spice Simulation @400MHz



Power Integrity Analysis

- Analyses:
  - IR-Drop (DIE, PKG, PCB)
  - Electro migration
  - Decoupling capacitors selection/ optimisation
- PKG Supplies
  - Core Power Plane
  - I/O Power Plane
  - DDR Power Plane
  - Special Power Nets
    - PLL, USB, HDMI, MIPI, NAND
- Tools
  - Voltus / RedHawk for IC power integrity (IR-Drop, EM and decap optimisation)
  - RDL: Voltus / RedHawk / Star RC?
  - PowerDC for PKG IR-Drop, impedance measurement, decaps
  - Sigrity SI/PI for PCB power analysis

IR Drop

- Calculated IR drop for all supplies against a 2.5% voltage drop target

$$V_{drop} = \frac{\rho . L . I}{A} = \frac{\rho . L . I}{T . W}$$

ρ - Resistivity of Cu, 1.68e-8 Ωm
L - Length of Trace (um)
T - Trace thickness (15um)
W - Trace width (um)
I - Current (A)

Non violating supplies

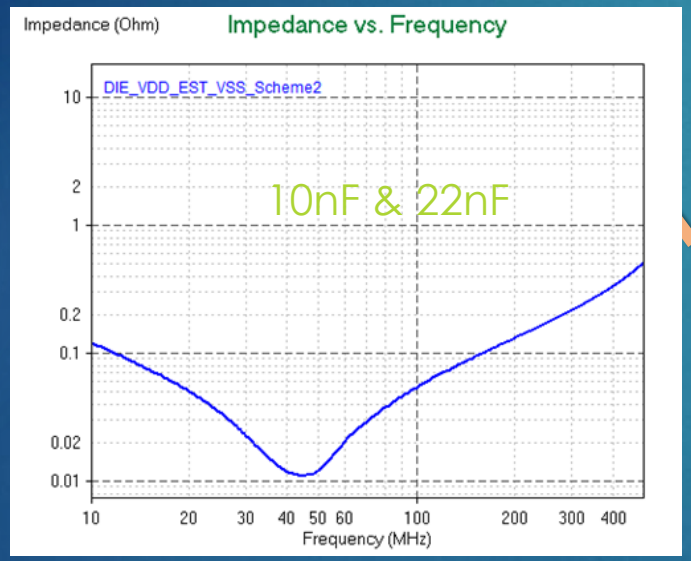
NET-NAMES	No of Pads	No of Bumps	Trace width (um)	Length (um)	Supply (V)	Current drawn per interface (mA)	IR drop (mV)	% IR drop
HDMI_RX_VPH	1	1	20	817.164	1.8	60	2.74567104	-
HDMI_RX_VPH	1	1	50	7971.627	1.8	60	10.71386669	-
HDMI_RX_VPH	1	1	50	125	1.8	60	0.168	-
HDMI_RX_VPH	1	1	100	235.85	1.8	60	0.1584912	-
HDMI_RX_VPH	1	1	100	235.85	1.8	60	0.1584912	-
HDMI_RX_VPH	1	1	26	2220.721	1.8	60	5.739709662	-
HDMI_RX_VPH	1	1	100	285.044	1.8	60	0.[illegible]1549568	-
HDMI_RX_VPH	TOTAL - IR drop						**19.87577936**	1.10421

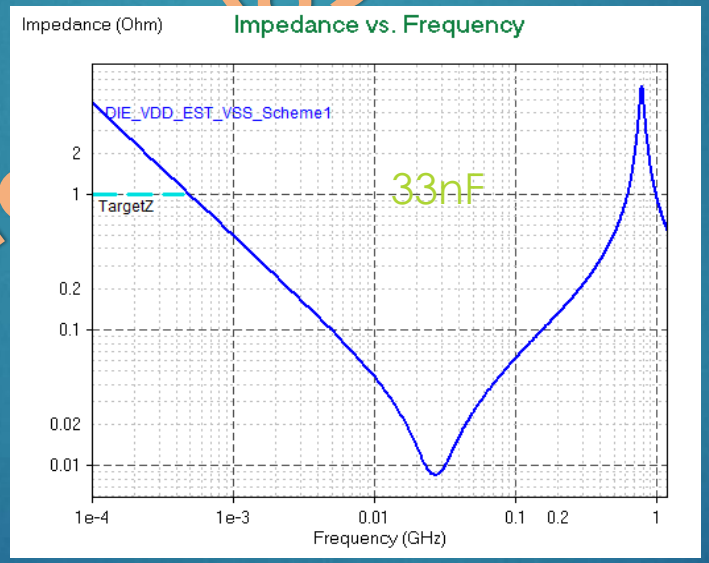
Violating supplies

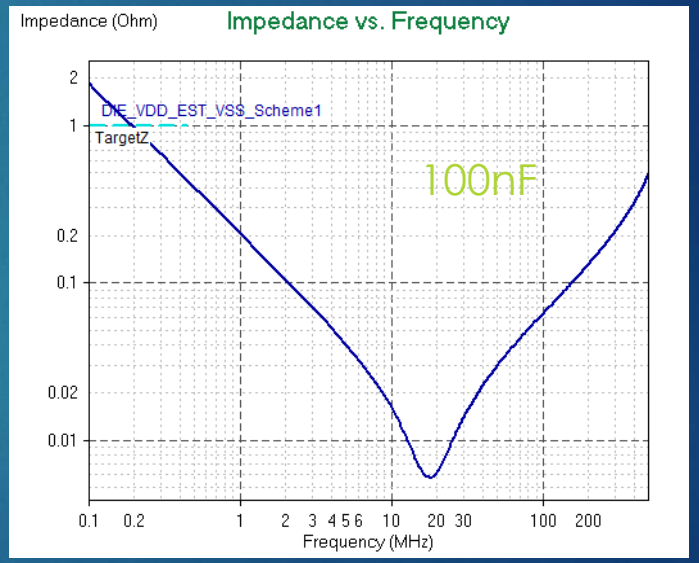
NET-NAMES	No of Pads	No of Bumps	Trace width (um)	Length (um)	Supply (V)	Current drawn per interface (mA)	IR drop (mV)	% IR drop	Layer
DDR_IF_0_PLL_DX_0	3	3	100	235.85	1.8	498	[illegible].31547696	-	CU-5
DDR_IF_0_PLL_DX_0	3	3	26	4880.635	1.8	498	1[illegible].7008838	-	CU-6
DDR_IF_0_PLL_DX_0	3	3	100	285.044	1.8	498	1.589861414	-	CU-8
DDR_IF_0_PLL_DX_0	TOTAL - IR drop						**139.8456816**	7.769205	-
DDR_IF_0_PLL_AC	3	3	20	1745.079	1.8	498	48.66676315	-	CU-1
DDR_IF_0_PLL_AC	3	3	100	233.24	1.8	498	1.300919424	-	CU-4
DDR_IF_0_PLL_AC	3	3	100	235.85	1.8	498	1.31547696	-	CU-5
DDR_IF_0_PLL_AC	3	3	26	1703.858	1.8	498	36.[illegible]5168608	-	CU-6
DDR_IF_0_PLL_AC	3	3	100	285.044	1.8	498	1.58[illegible]61414	-	CU-8
DDR_IF_0_PLL_AC	TOTAL - IR drop						**89.42470703**	4.968039	-

Decoupling Capacitors

Sweeping frequency with various combinations of decaps 10nF ~ 220nF
Generate loop inductance for each decap

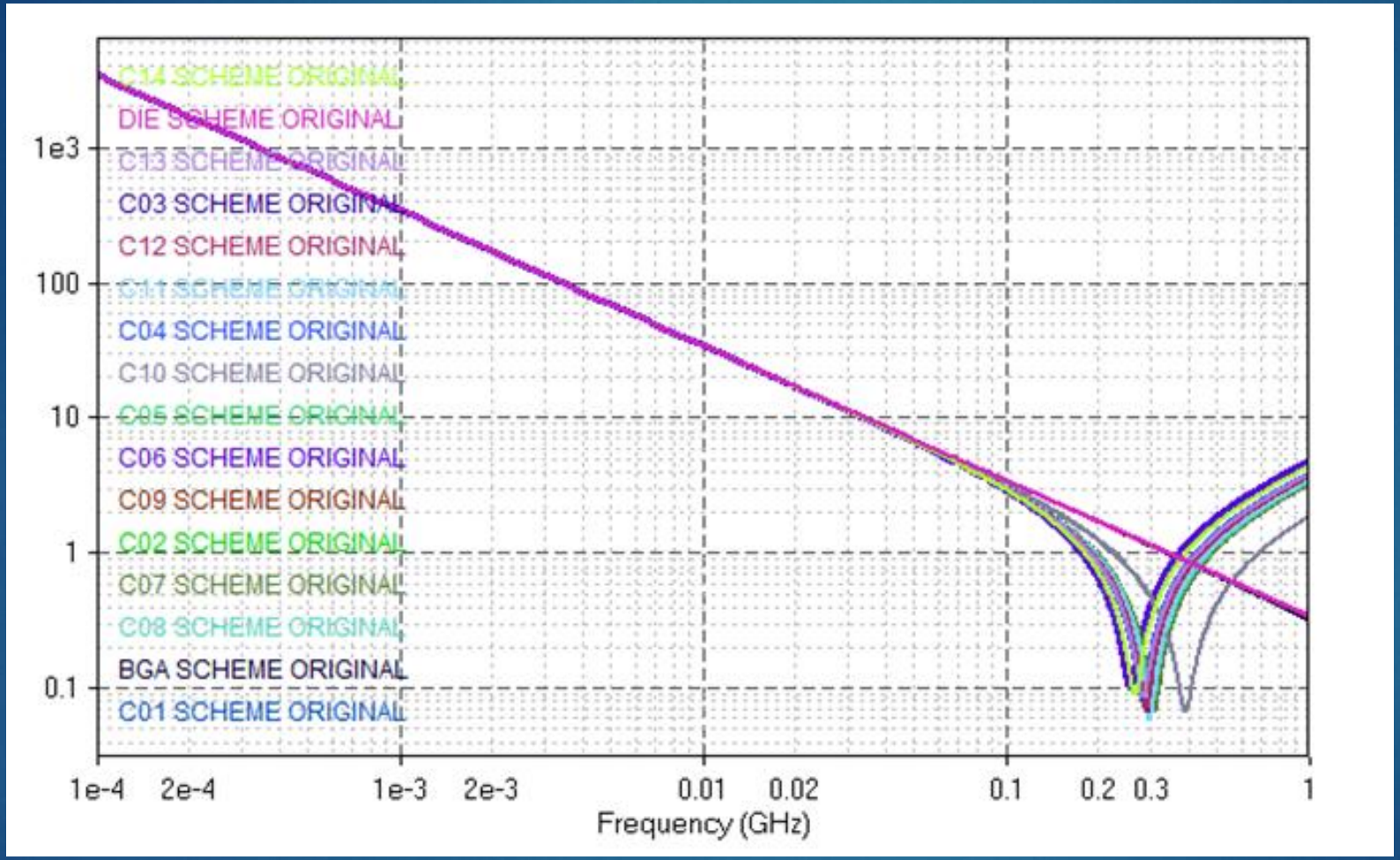






Decoupling Capacitors (Cont.)

Core VDD/VSS (13 decaps)

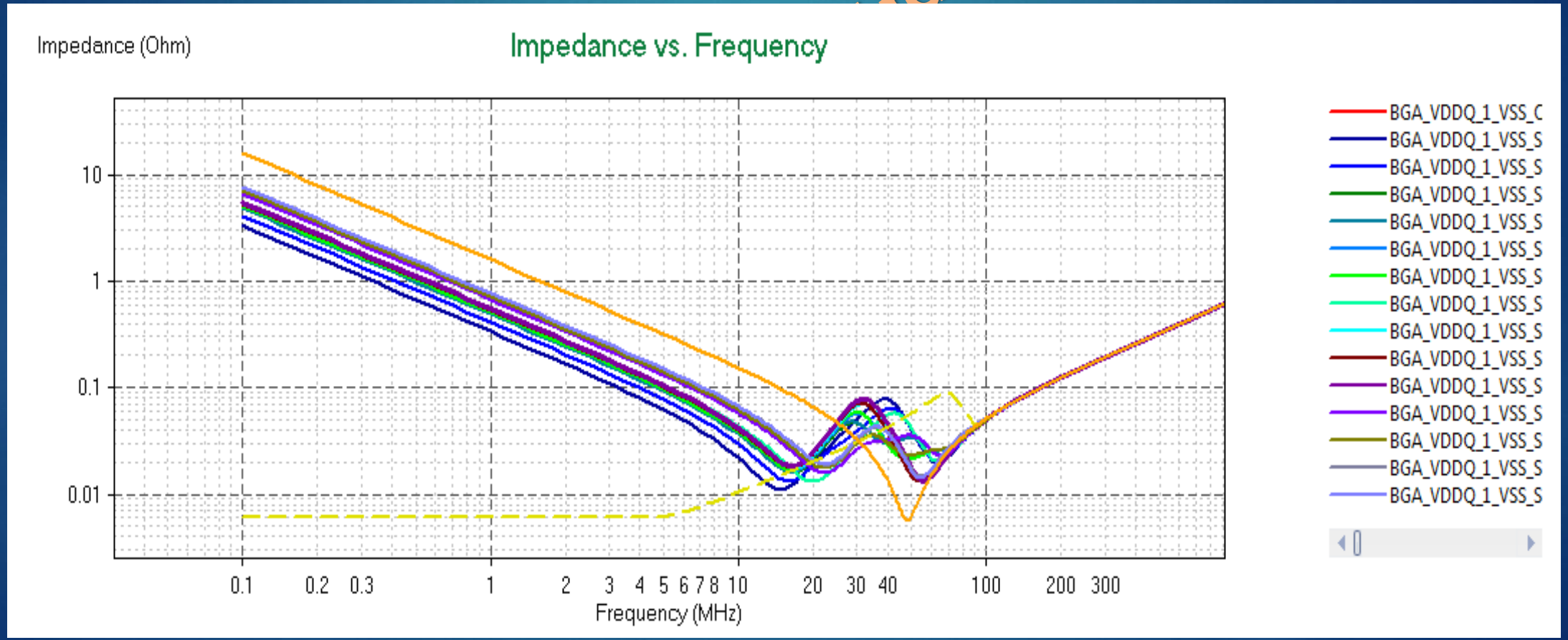


Various schemes have different min impedance but show similar results at low and high frequencies

Decoupling Capacitors (Cont.)

- DDR1 VDDQ/VSS

Decaps values: 10nF~220nF



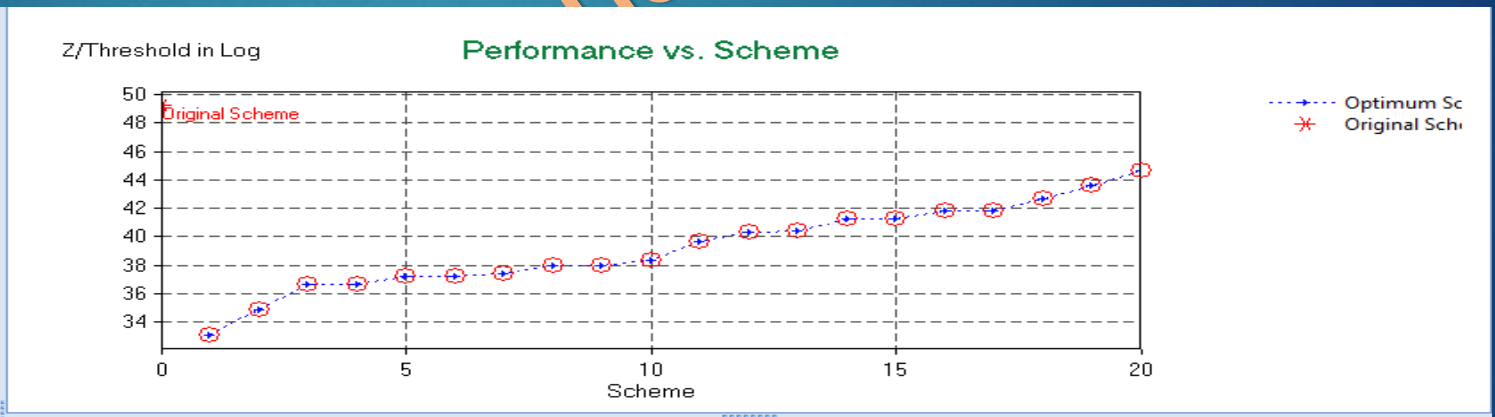
Decoupling Capacitors

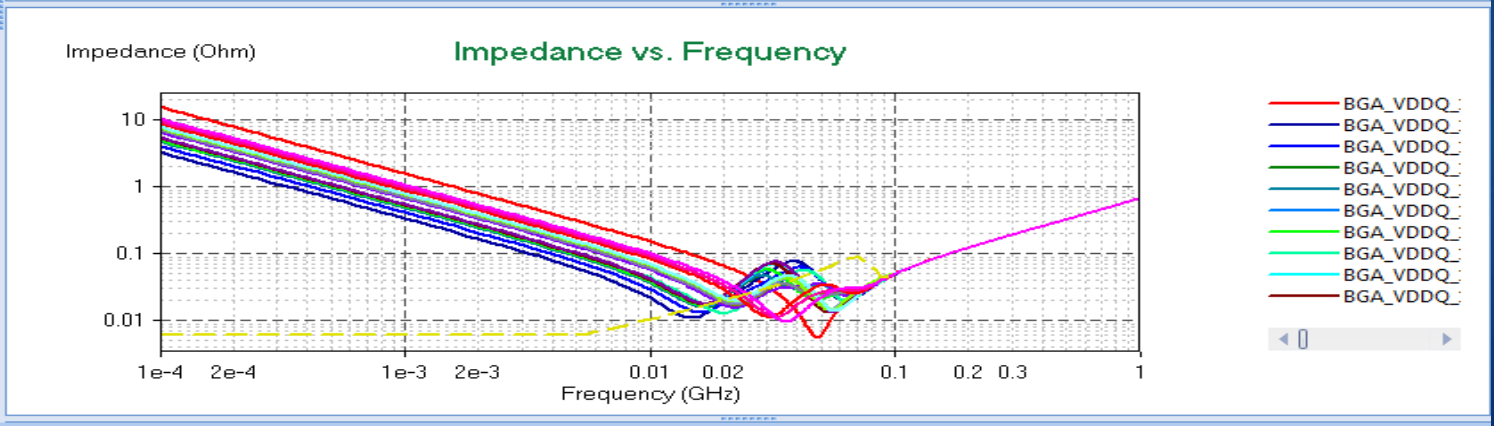
- DDR0 VDDQ/VSS

Decaps values: 10nF~220nF

Show Impedance with Capacitors Opened
Show Impedance with All Capacitors Shorted
Show Impedance with Original Capacitors
Show Relative Values to Original Scheme
Total Cost
Component Cost
Mounting Cost
BOM penalty Cost

Scheme ID	Cost	Number	Number of Capacitor Types	Area	Impedance Measure
Original ...	0	0	0	0	49.2646
Scheme 1	2	2	1	400	33.0678
Scheme 2	2	2	2	400	34.8968
Scheme 3	2	2	2	400	36.6132
Scheme 4	2	2	2	400	36.6442
Scheme 5	2	2	2	400	37.1949
Scheme 6	2	2	2	400	37.2352
Scheme 7	2	2	1	400	37.3981
Scheme 8	2	2	2	400	37.9243
Scheme 9	2	2	2	400	37.9697
Scheme 10	2	2	2	400	38.3442
Scheme 11	2	2	2	400	39.6548
Scheme 12	2	2	2	400	40.3549
Scheme 13	2	2	2	400	40.3722
Scheme 14	2	2	2	400	41.2521
Scheme 15	2	2	2	400	41.2745
Scheme 16	2	2	2	400	41.799
Scheme 17	2	2	2	400	41.8233
Scheme 18	2	2	1	400	42.6417
Scheme 19	2	2	2	400	43.5923
Scheme 20	2	2	1	400	44.6324





Summary

- Ballout and substrate stackup for flipchip BGA presented
- Delay/skew of DDR interface based on trace length and simulation compared
- System level SI analyses are required for high-speed interfaces
- IR Drop simulation is mandatory to ensure system power integrity
- Decoupling capacitors analysis have been done in OptimizePI tool
- Assign different decaps to each supply to avoid anti-resonance peaks

Thank You!

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