Flipchip BGA Package Design

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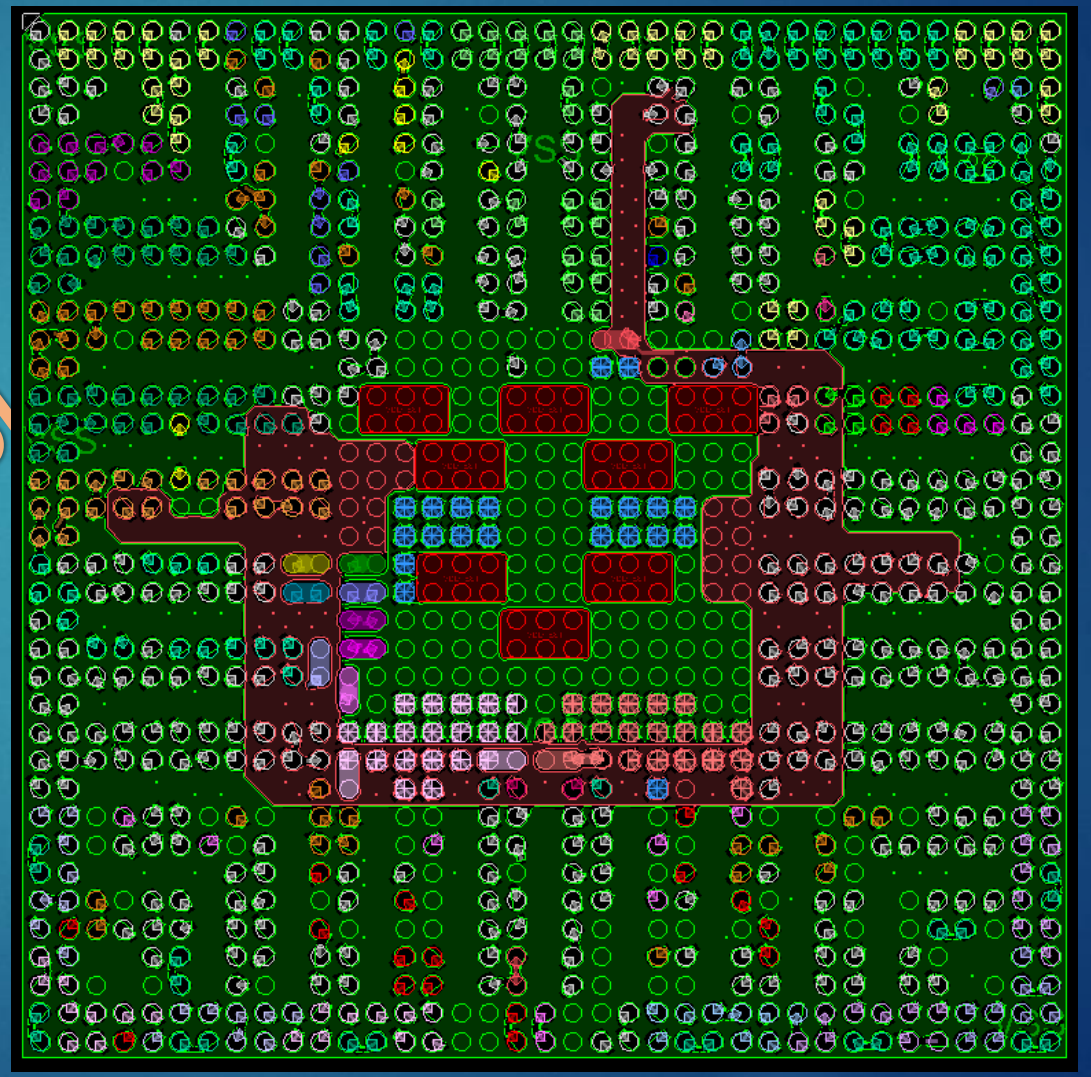
PKG Overview:

- Die size: 13.071x10994 (post shrink incl. seal ring/scribe lines)
- Die Bumps: 5231
- Bump pitch: 162x162um
- Package type: 8-layers flip chip BGA
- Package size: 25x25mm
- Ball count: 1086 with 0.65mm pitch
- Channelled ball pattern for ease of routability
- Decaps: 24 (core:14, DDR:4, VDDIO: 6, HDMI:3)

Ballout with Channels

25x25mm FC BGA
1086 Balls
0.65mm Pitch

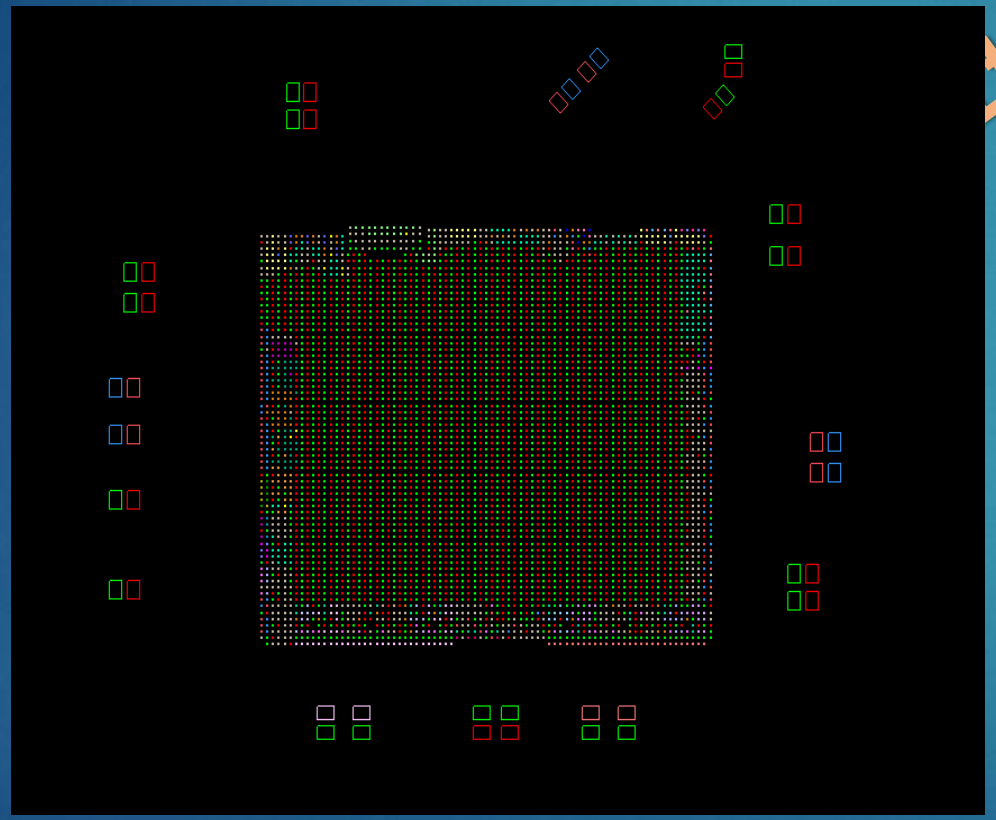


Substrate Stackup

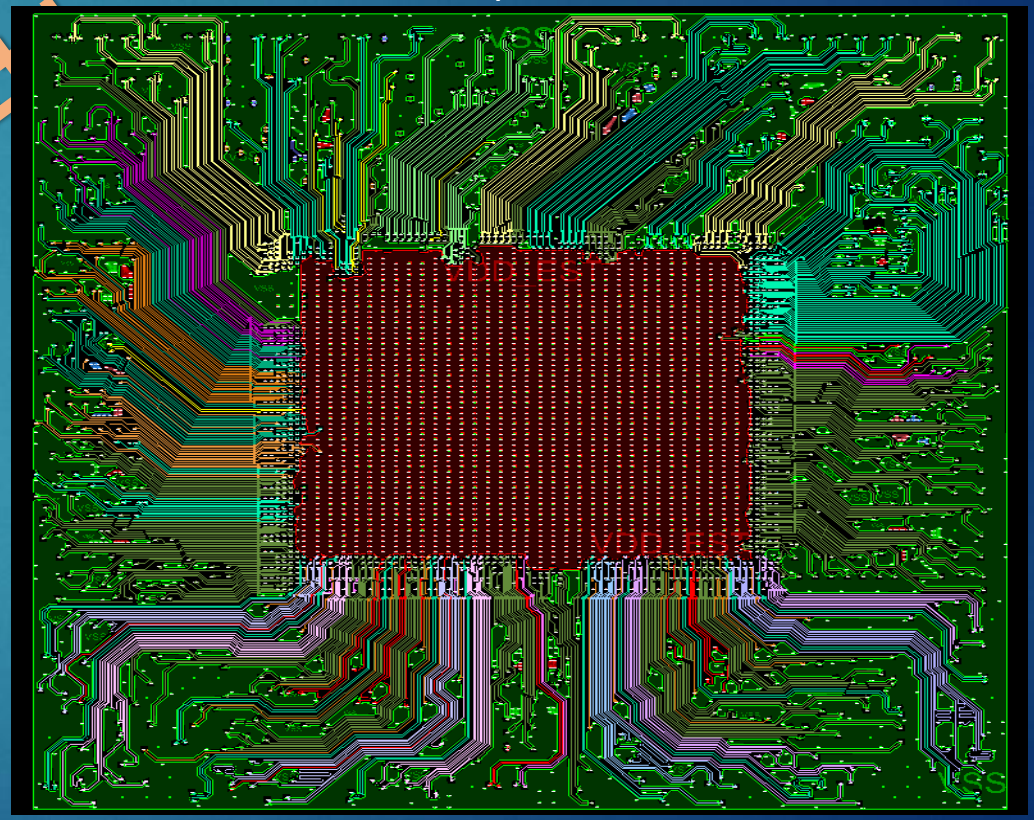
Subclass Name	Type	Material	Thickness (UM)	Conductivity (mho/cm)	Dielectric Constant	Loss Tangent	Freq Dep File	Negative Artwork	Shield	Width (UM)	Etch Factor (Degrees)	Unused Pin Pad Suppression	Unused Via Pad Suppression
	SURFACE	AIR		0	1	0							
	DIELECTRIC												
CU-1	CONDUCTOR	COPPER	15.000000	595900	4.5	0				14	90.00		
DRILL1-2	DIELECTRIC	ABF-GX13	35.000000	0	3.35	0.012							
CU-2	CONDUCTOR	COPPER	15.000000	595900	3.35	0.012				75	90.00		
DRILL2-3	DIELECTRIC	ABF-GX13	35.000000	0	3.35	0.012							
CU-3	CONDUCTOR	COPPER	15.000000	595900	3.35	0.012				75	90.00		
DRILL3-4	DIELECTRIC	ABF-GX13	35.000000	0	3.35	0.012							
CU-4	CONDUCTOR	COPPER	18.000000	595900	3.35	0.012				75	90.00		
DRILL4-5	DIELECTRIC	E679FGR	800.000000	0	4.7	0.018							
CU-5	CONDUCTOR	COPPER	18.000000	595900	3.35	0.012				75	90.00		
DRILL5-6	DIELECTRIC	ABF-GX13	35.000000	0	3.35	0.012							
CU-6	CONDUCTOR	COPPER	15.000000	595900	3.35	0.012				75	90.00		
DRILL6-7	DIELECTRIC	ABF-GX13	35.000000	0	3.35	0.012							
CU-7	CONDUCTOR	COPPER	15.000000	595900	3.35	0.012				14	90.00		
DRILL7-8	DIELECTRIC	ABF-GX13	35.000000	0	3.35	0.012							
CU-8	CONDUCTOR	COPPER	15.000000	595900	4.5	0				14	90.00		
	DIELECTRIC												
	SURFACE	AIR		0	1	0							

Substrate Layers

Layer 1

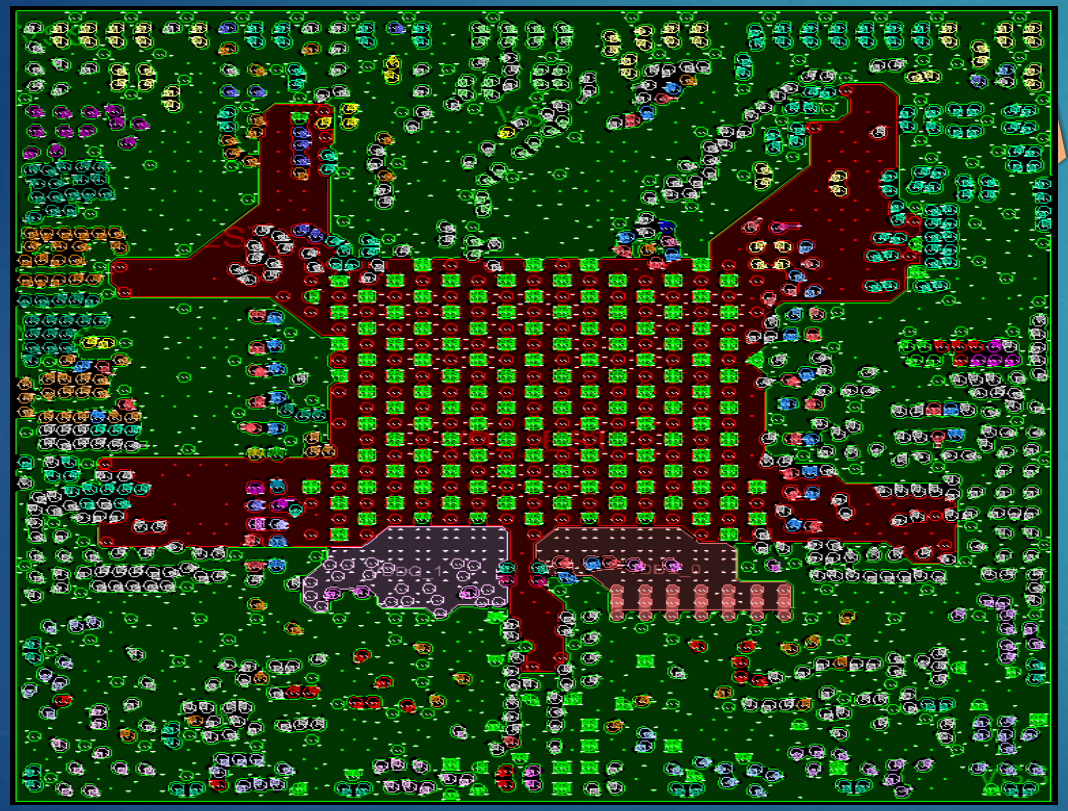


Layer 3

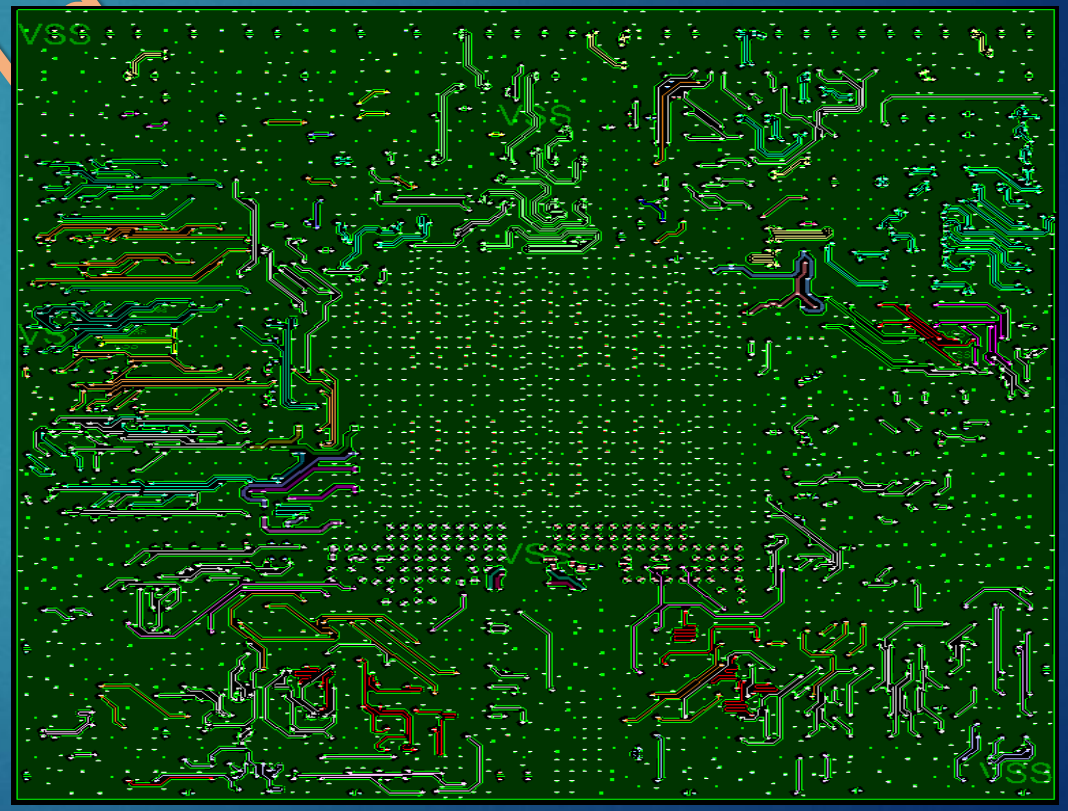


Substrate Layers (Cont.)

Layer 5



Layer 6



High Speed Nets Balancing

Skew Budget

Package Design Requirement: Please specify by group															
Interface/Net	DDR	MIPI CSI	MIPI DSI	HiSPi	NAND	SDHOST	LVDS	ETHERNET	HDMI-RX	HDMI-TX	USB	RF	AFE	SENSOR	LR ADC
Single End Impedance	50 Ω	50 Ω	50 Ω	50 Ω	50 Ω	50 Ω	50 Ω	50 Ω	-	-					
Differential Impedance	100 Ω	100 Ω	100 Ω	100 Ω	100 Ω	100 Ω	100 Ω	100 Ω	100 Ω	100 Ω	100 Ω	100 Ω	100 Ω	100 Ω	100 Ω
Time Skew in Pair	3ps	10ps	10ps	50ps	-	-	7ps	-	25ps	5ps	3ps		3ps	5ps	3ps
Time Skew in Group (Lane to Lane) - CMD/ADDR/CTRL lines	25ps	50ps	50ps	-	100ps	1.92ns	10ps	100ps	100ps	30ps	50ps			50ps	
Time Skew in Group (Lane to Lane) - data lines	10ps	-	-	100ps				-	-						
Return Loss @ Frequency															
Insertion Loss @ Frequency															
Resistance/Inductance/Capacitance															
Cross Talk noise Coefficient to Adjacent Signal															

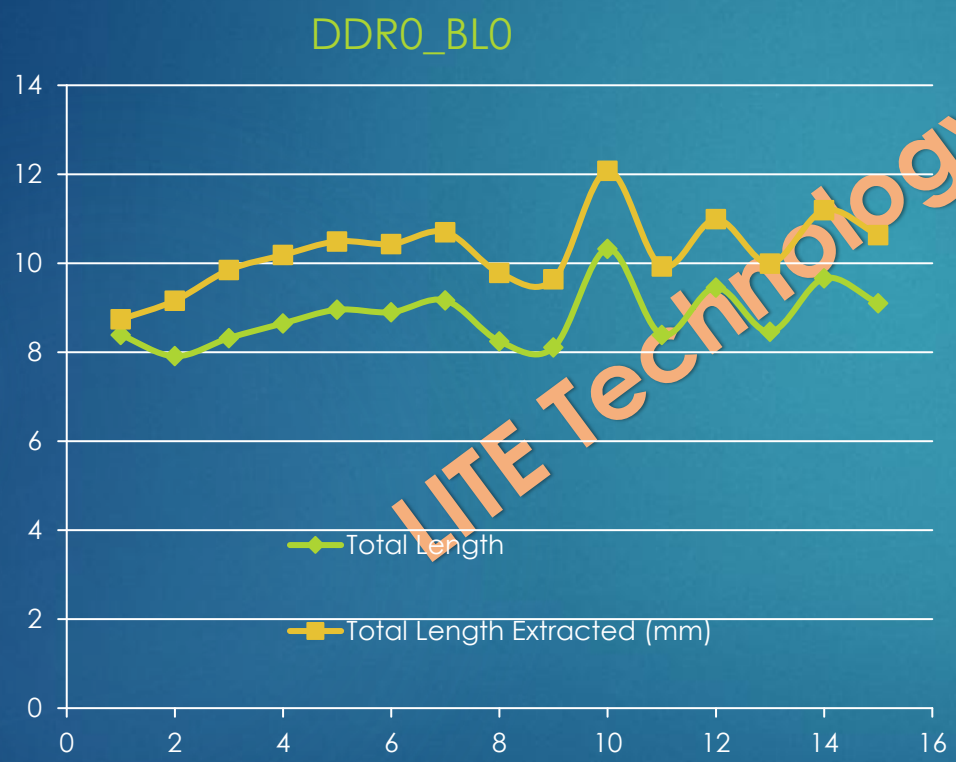
Delay/Skew Results

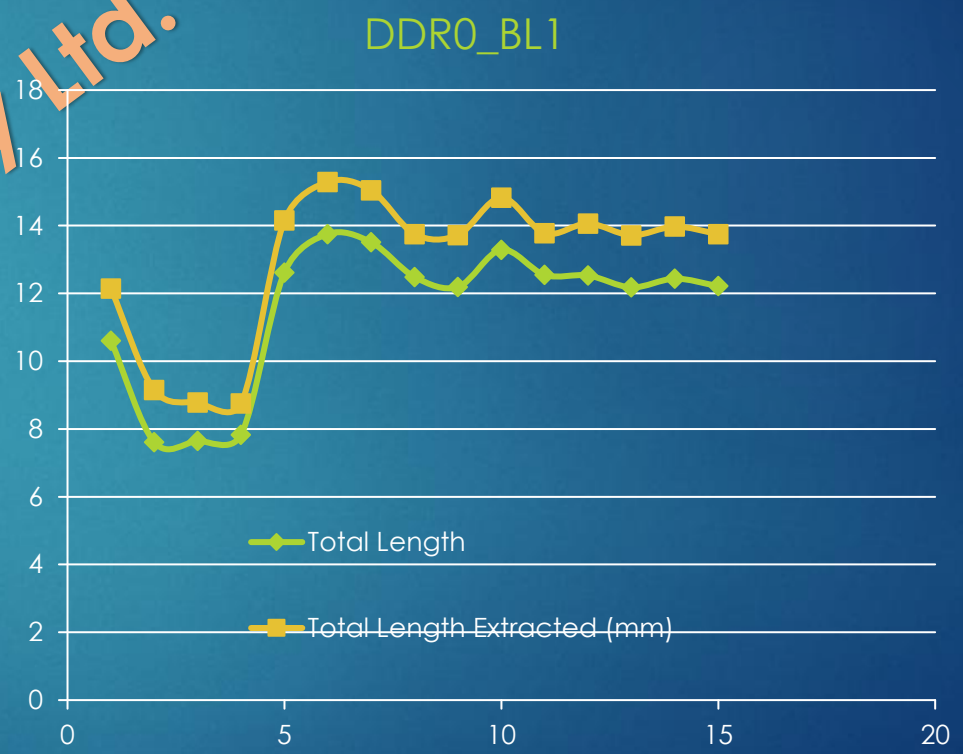
- Generated net delay based on RDL + Substrate trace lengths
  - Inaccurate due to Z-direction and coupling
- Extracted delay using Cadence XtractIM tool
  - Includes Z-direction (vias) and coupling effect
- Simulation: Used extracted ibis & Spice models
  - Suitable for small circuits; doesn't include RDL
  - Used for cross checking to validate extracted data

Delay/Skew Results (Cont.)

	A	B	C	D	E	F	G	H	I	J	K	L	M	N	O	P	Q	R	S	T
1																				
2	Net Name	Skew -/+ ps	Cond Length_09032016 (mm)	Sub Trace length 160526a	Extracted Length (mm)	RDL Length (mm)	Total Length SiP (mm)	Total Length	Total Length Extracted (mm)	Tolerance	Tolerance Extracted (mm)	Total Delay (ps)	Xtracted Delay (ps)	Total Delay Extracted (ps)	Skew based on Xtraction (ps)	Judge (length)	net length improvement	diff (skew)	CLK-Data Skew	data-strobe Differential Addresses/Ctrl
3	DDR_0_ACT_N		12.447694	12.447694	13.983	0.259652	12.707346	12.707346	14.242252	1.728756	1.727136	80.06	106.41	108.04			0			
4	DDR_0_ATO		12.379426	12.379426	13.910	0.615067	12.994493	12.994493	14.524967	2.015903	2.009851	81.87	105.92	109.80			0			
5	DDR_0_A[0]	25	6.409426	7.596303	7.946	0.793017	7.202443	8.38932	8.738947	3.776147	3.776169	52.85	59.55	64.55	31.78	OK	16		ERROR	ADDR/CTRL signals -ddr0
6	DDR_0_A[1]	25	7.360917	7.645101	8.896	0.264656	7.625573	7.909757	9.160246	3.353017	3.35487	49.83	69.50	71.17	25.16	OK	4		ERROR	ADDR/CTRL signals -ddr0
7	DDR_0_A[2]	25	7.707614	7.707614	9.239	0.611733	8.319347	8.319347	9.850323	2.659243	2.664793	52.41	70.84	74.69	21.64	OK	0		OK	ADDR/CTRL signals -ddr0
8	DDR_0_A[3]	25	7.656859	7.656859	9.193	0.991532	8.648391	8.648391	10.184922	2.330199	2.330194	54.48	66.72	72.96	23.36	OK	0		OK	ADDR/CTRL signals -ddr0
9	DDR_0_A[4]	25	9.614462	9.614462	11.151	0.992464	10.606926	10.606926	12.143364	0.371664	0.371752	66.82	86.64	92.89	3.43	OK	0		OK	ADDR/CTRL signals -ddr0
10	DDR_0_A[5]	25	6.803301	6.803301	8.340	0.809461	7.612762	7.612762	9.149211	3.365828	3.365905	47.96	67.61	72.71	23.61	OK	0		OK	ADDR/CTRL signals -ddr0
11	DDR_0_A[6]	25	6.980873	7.38694	8.517	0.261827	7.2427	7.648767	8.779257	3.73589	3.735859	48.19	69.01	70.66	25.67	OK	6		ERROR	ADDR/CTRL signals -ddr0
12	DDR_0_A[7]	25	6.603911	7.217632	8.139	0.612729	7.21664	7.830361	8.751269	3.76195	3.763847	49.33	66.32	70.18	26.14	OK	9		ERROR	ADDR/CTRL signals -ddr0
13	DDR_0_A[8]	25	8.244123	8.244123	9.781	0.611733	8.855856	8.855856	10.392373	2.122734	2.122743	55.79	77.62	81.47	14.85	OK	0		OK	ADDR/CTRL signals -ddr0
14	DDR_0_A[9]	25	6.847743	7.359872	8.383	0.263704	7.111447	7.623576	8.646334	3.867143	3.868782	48.03	67.79	69.45	26.87	OK	7		ERROR	ADDR/CTRL signals -ddr0
15	DDR_0_A[10]	25	9.969958	9.969958	11.503	0.975129	10.945087	10.945087	12.478229	0.033503	0.036887	68.95	89.14	95.29	1.04	OK	0		OK	ADDR/CTRL signals -ddr0
16	DDR_0_A[11]	25	9.077543	9.077543	10.611	0.983142	10.060685	10.060685	11.594042	0.917905	0.921074	63.38	81.46	87.65	8.68	OK	0		OK	ADDR/CTRL signals -ddr0
17	DDR_0_A[12]	25	8.424149	8.424149	9.961	0.790842	9.214991	9.214991	10.751462	1.763599	1.763654	58.05	76.06	81.04	15.29	OK	0		OK	ADDR/CTRL signals -ddr0
18	DDR_0_A[13]	25	6.876038	7.514067	8.411	0.258989	7.135027	7.773056	8.669959	3.843563	3.845157	48.97	67.02	68.65	27.68	OK	9		ERROR	ADDR/CTRL signals -ddr0
19	DDR_0_A[14]	25	7.977397	7.977397	9.514	0.626976	8.604373	8.604373	10.140946	2.374217	2.37417	54.21	73.93	77.88	18.44	OK	0		OK	ADDR/CTRL signals -ddr0
20	DDR_0_A[15]	25	8.676195	8.676195	10.213	0.796051	9.472246	9.472246	11.008851	1.506344	1.506265	59.68	80.32	85.34	10.99	OK	0		OK	ADDR/CTRL signals -ddr0
21	DDR_0_A[16]	25	9.201461	9.201461	10.738	0.614404	9.815865	9.815865	11.352404	1.162725	1.162712	61.84	84.51	88.38	7.94	OK	0		OK	ADDR/CTRL signals -ddr0
22	DDR_0_A[17]	25	9.412962	9.412962	10.948	0.266831	9.679793	9.679793	11.214731	1.298797	1.300385	60.98	86.15	87.83	8.50	OK	0		OK	ADDR/CTRL signals -ddr0
23	DDR_0_BA[0]	25	9.863657	9.863657	11.400	0.794937	10.658594	10.658594	12.195037	0.319996	0.320079	67.15	88.44	93.45	2.88	OK	0		OK	ADDR/CTRL signals -ddr0
24	DDR_0_BA[1]	25	9.666925	9.666925	11.201	0.996544	10.663469	10.663469	12.197244	0.315121	0.317872	67.18	88.27	94.55	1.78	OK	0		OK	ADDR/CTRL signals -ddr0
25	DDR_0_BG[0]	25	11.174381	11.174381	12.711	0.805878	11.980259	11.980259	13.516778	1.001669	1.001662	75.48	97.91	102.99	6.66	OK	0		OK	ADDR/CTRL signals -ddr0
26	DDR_0_BG[1]	25	13.269942	13.269942	14.798	0.636938	13.90688	13.90688	15.434538	2.92829	2.919422	87.61	112.34	116.36	20.03	OK	0		OK	ADDR/CTRL signals -ddr0
27	DDR_0_CK	3	10.349874	10.349874	11.886	0.628716	10.97859	10.97859	12.515116	0	0	69.17	92.37	96.33	1.04	OK	0	OK		Reference Clock - ADDR/CTRL s
28	DDR_0_CKE	25	11.44387	11.44387	12.980	0.618671	12.062541	12.062541	13.599071	1.083951	1.083955	75.99	98.99	102.89	6.56	OK	0		OK	ADDR/CTRL signals -ddr0
29	DDR_0_CK_N	3	10.368261	10.368261	11.905	0.796289	11.16455	11.16455	12.700989	0.18596	0.185873	70.34	90.27	95.29	1.04	OK	0	OK		
30	DDR_0_CS_N	25	10.763678	10.763678	12.300	0.256815	11.020493	11.020493	12.557015	0.041903	0.041899	69.43	93.34	94.96	1.37	OK	0		OK	ADDR/CTRL signals -ddr0
31	DDR_0_DM[0]	10	8.15192	8.15192	9.688	0.802834	8.954754	8.954754	10.491204	0.054544	0.058336	56.41	77.83	82.88	0.42	OK	0		OK	Bytelane 0
32	DDR_0_DM[1]	10	12.008362	12.008362	13.539	0.611733	12.620095	12.620095	14.150833	1.132691	1.138373	79.51	103.74	107.59	8.43	OK	0		OK	Bytelane 1
33	DDR_0_DM[2]	10	12.778207	12.638272	14.309	0.799603	13.57781	13.437875	15.108403	1.443435	1.439378	84.66	112.87	117.91	11.09	OK	-1		ERROR	Bytelane 2
34	DDR_0_DM[3]	10	10.363551	10.363551	11.893	0.620183	10.983734	10.983734	12.513283	0.567276	0.560379	69.20	95.16	99.06	6.69	OK	0		OK	Bytelane 3
35	DDR_0_DQS[0]	3	8.638342	8.638342	10.171	0.261868	8.90021	8.90021	10.432868	0.263598	0.267458	56.07	81.66	83.31	1.99	OK	0	OK		Reference signal to bytelane 0
36	DDR_0_DQS[1]	3	12.73988	12.73988	14.276	1.012906	13.752786	13.752786	15.289206	0.243951	0.243911	86.64	109.64	116.02	1.72	OK	0	OK		Reference signal to bytelane 1
37	DDR_0_DQS[2]	3	11.86655	12.310487	13.401	0.267825	12.134375	12.578312	13.669025	0.319878	0.319723	79.24	105.13	106.81	2.78	OK	4	OK		Reference signal to bytelane 2
38	DDR_0_DQS[3]	3	9.394854	9.394854	10.931	1.021604	10.416458	10.416458	11.952904	0.429519	0.429511	65.62	85.94	92.37	1.94	OK	0	OK		Reference signal to bytelane 3
39	DDR_0_DQS_N[0]	3	8.731582	8.731582	10.268	0.432226	9.163808	9.163808	10.700326	0.263598	0.267458	57.73	82.58	85.30	1.99	OK	0	OK		

Delay/Skew Results (Cont.)





Extraction Vs. Simulation

ExtractIM Simulation results			SpiceSimulation results - Separate Interface (DATA & ADDR)			
SignalNetName	NetLength(mm)	Delay(pS)	SignalNetName	NetLength(mm)	Delay(pS)	Delta (pS)
DDR_0_A[0]	7.94593	59.5357	DDR_0_A[0]	7.94593	59.13	0.4057
DDR_0_A[1]	8.89559	69.6253	DDR_0_A[1]	8.89559	77.9	8.2747
DDR_0_A[2]	9.23859	70.8286	DDR_0_A[2]	9.23859	72.8	1.9714
DDR_0_A[3]	9.19339	66.6323	DDR_0_A[3]	9.19339	73.83	7.1977
DDR_0_A[4]	11.1509	86.5493	DDR_0_A[4]	11.1509	100.8	14.2507
DDR_0_A[5]	8.33975	67.7612	DDR_0_A[5]	8.33975	67.72	0.0412
DDR_0_A[6]	8.51743	69.1471	DDR_0_A[6]	8.51743	69.15	0.0029
DDR_0_A[7]	8.13854	66.3938	DDR_0_A[7]	8.13854	58.15	8.2438
DDR_0_A[8]	9.78064	77.6018	DDR_0_A[8]	9.78064	81.78	4.1782
DDR_0_A[9]	8.38263	67.7613	DDR_0_A[9]	8.38263	67.81	0.0487
DDR_0_A[10]	11.5031	89.1093	DDR_0_A[10]	11.5031	94.51	5.4007
DDR_0_A[11]	10.6109	81.501	DDR_0_A[11]	10.6109	83.8	2.299
DDR_0_A[12]	9.96062	76.0402	DDR_0_A[12]	9.96062	77.28	1.2398
DDR_0_A[13]	8.41097	66.8931	DDR_0_A[13]	8.41097	70.52	3.6269
DDR_0_A[14]	9.51397	73.9172	DDR_0_A[14]	9.51397	77.82	3.9028
DDR_0_A[15]	10.2128	80.3645	DDR_0_A[15]	10.2128	81.6	1.2355
DDR_0_A[16]	10.738	84.6467	DDR_0_A[16]	10.738	88.59	3.9433
DDR_0_A[17]	10.9479	86.1217	DDR_0_A[17]	10.9479	95.01	8.8883
DDR_0_BA[0]	11.4001	88.3166	DDR_0_BA[0]	11.4001	92.76	4.4434
DDR_0_BA[1]	11.2007	88.3575	DDR_0_BA[1]	11.2007	90.86	2.5025
DDR_0_BG[0]	12.7109	97.9009	DDR_0_BG[0]	12.7109	102.5	4.5991
DDR_0_BG[1]	14.7976	112.401	DDR_0_BG[1]	14.7976	122.1	9.699
DDR_0_CK	11.8864	92.4043	DDR_0_CK	11.8864	113.3	20.8957
DDR_0_CKE	12.9804	99.1017	DDR_0_CKE	12.9804	104.6	5.4983
DDR_0_CK_N	11.9047	90.1875	DDR_0_CK_N	11.9047	100.2	10.0125
DDR_0_CS_N	12.3002	93.3203	DDR_0_CS_N	12.3002	104.6	11.2797
DDR_0_DM[0]	9.68837	78.0277	DDR_0_DM[0]	9.68837	89.54	11.5123
DDR_0_DM[1]	13.5391	103.784	DDR_0_DM[1]	13.5391	115.2	11.416
DDR_0_DM[2]	14.3088	112.978	DDR_0_DM[2]	14.3088	127.5	14.522
DDR_0_DM[3]	11.8931	95.1765	DDR_0_DM[3]	11.8931	107.2	12.0235
DDR_0_DQS[0]	10.171	81.6469	DDR_0_DQS[0]	10.171	89.11	7.4631
DDR_0_DQS[1]	14.2763	109.595	DDR_0_DQS[1]	14.2763	119.7	10.105
DDR_0_DQS[2]	13.4012	105.098	DDR_0_DQS[2]	13.4012	115.8	10.702
DDR_0_DQS[3]	10.9313	85.9996	DDR_0_DQS[3]	10.9313	93.56	7.5604

gy Ltd.

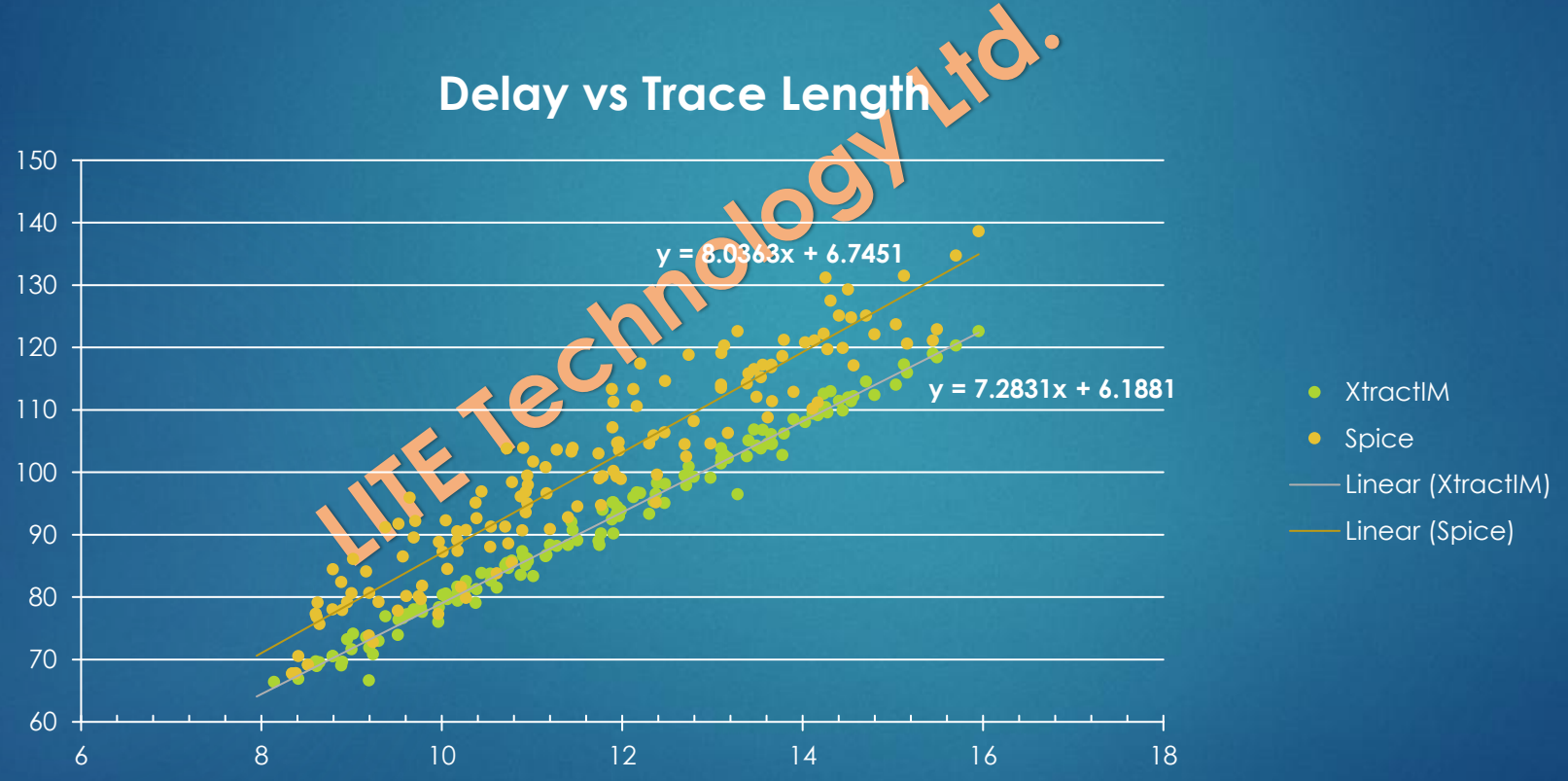
Table represents part of the nets in DDR interface

For the same trace length, the propagation delay shows some discrepancy between extraction and Spice simulation setups

Hspice simulation delay is consistently greater than that calculated by XtractIM

Final skew could not be determined because the RDL delay is missing in the flow

Extraction Vs. Simulation (Cont.)



Summary

- Ballout and substrate stackup for flipchip BGA presented
- Delay/skew of DDR interface based on trace length and simulation compared
- Net balancing based on trace length matching is inaccurate
- Accurate delay/skew (Xtract IM tool) reasonably match Spice simulation
- IBIS/Spice/S-Param models are available for the i/o pad, pkg, pcb and memory; RDL model is missing.

Thank You!

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