Emerging Memory Product Lifecycle

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NEW MEMORY PRODUCT LIFECYCLE

- Memory Technologies all go through certain steps from concept to mass production. Historical data tells us:
  - There are certain timeline expectations … how long does it take
  - There are certain milestones and technical achievements in a certain order
  - Most technologies fails or are indefinitely delayed before mass production
- This model for development allows us to put ideas and concepts into perspective
  - What are the next steps we need to achieve?
  - What timeframe seems logical
  - Where do different technologies stand on the lifecycle
- We have models on how to accelerate this or save money on this lifecycle

Uses for Model

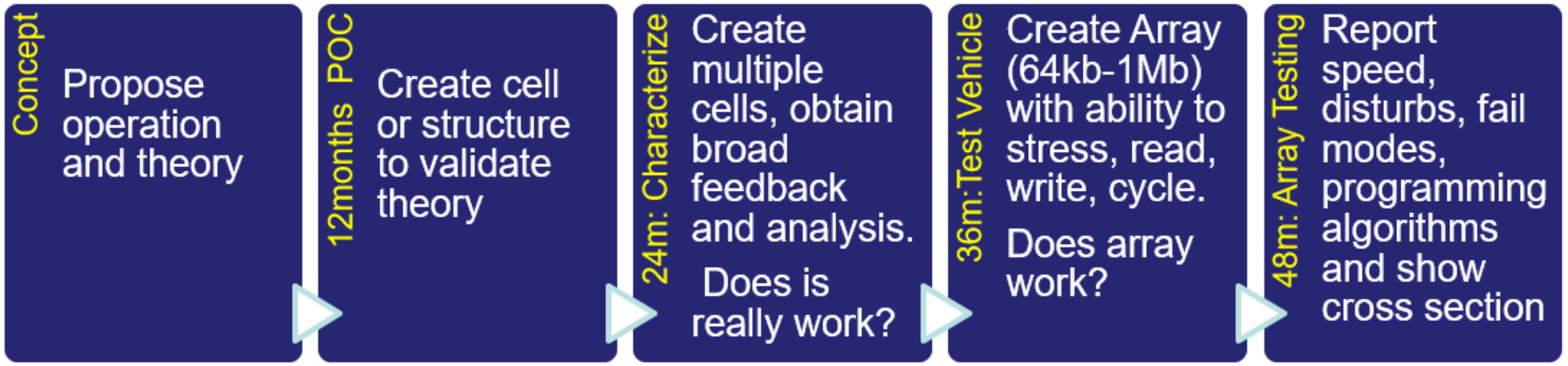
- I have a new technology proposal
  - What are next steps
  - When do I need to look for partners
  - What do I need to do and show to get support from equipment companies, memory companies and application companies
- When can we expect other technologies to mature
  - “Why ramp 3D Xpoint when Nanotubes are just around corner”
  - “Micron will be out a business when MRAM replaces DRAM”
  - Each technology has a logical timeline to maturity

Parts of the Model

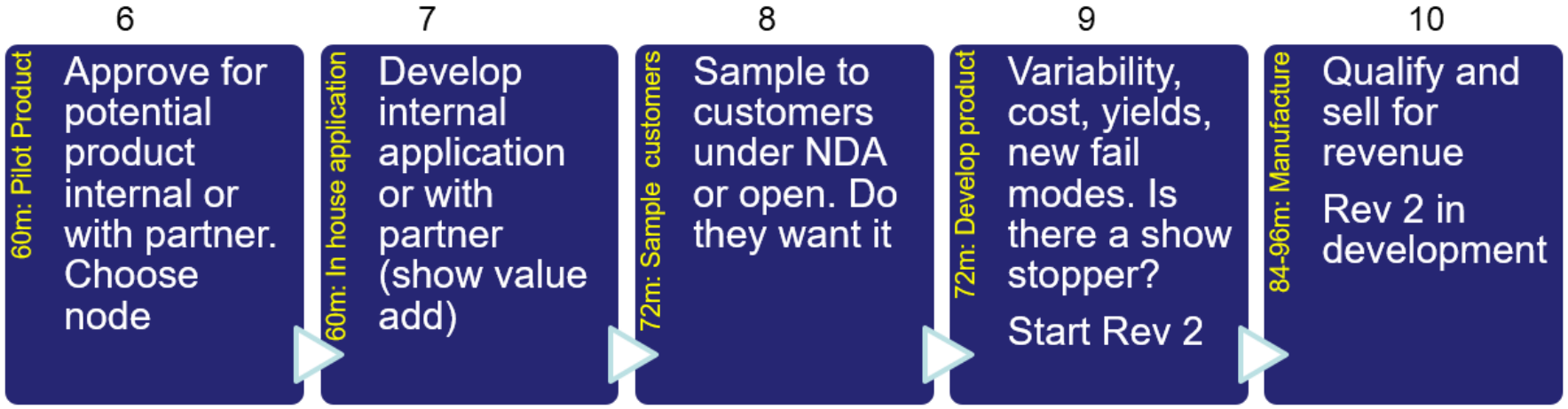
- Two Parts and each part has 5 stages
  - Part 1 is Technical development and demonstration
    - Often open data sharing, lots of publications, learning environment
    - Physical model, test cells, basic operation, first mini-array, and full checkout of Array
    - 4+ years
    - Stage 1-5 1.1 to 1.5
  - Part 2 is Product development
    - Only 10% of technologies make it to this area
    - Often stealth or closed environment. IP protected
    - Business model, partnerships, ROI, Product and application design and development
    - Ends with full product selling to public
    - Stage 6-10, 2.1 to 2.5

Memory Product Lifecycle

Part 1
(Stage 1-5)



Part 2
(Stage 6-10)



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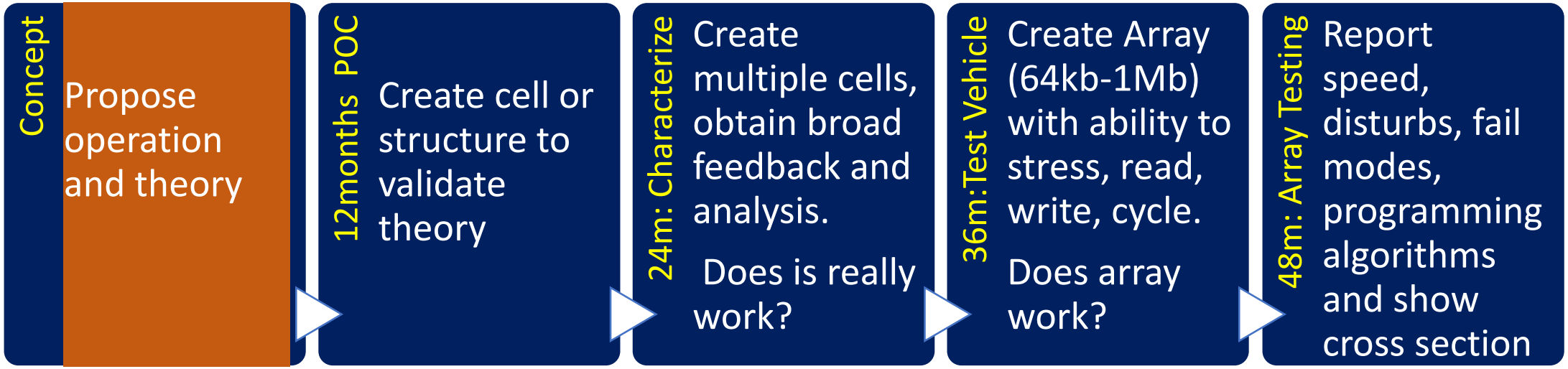
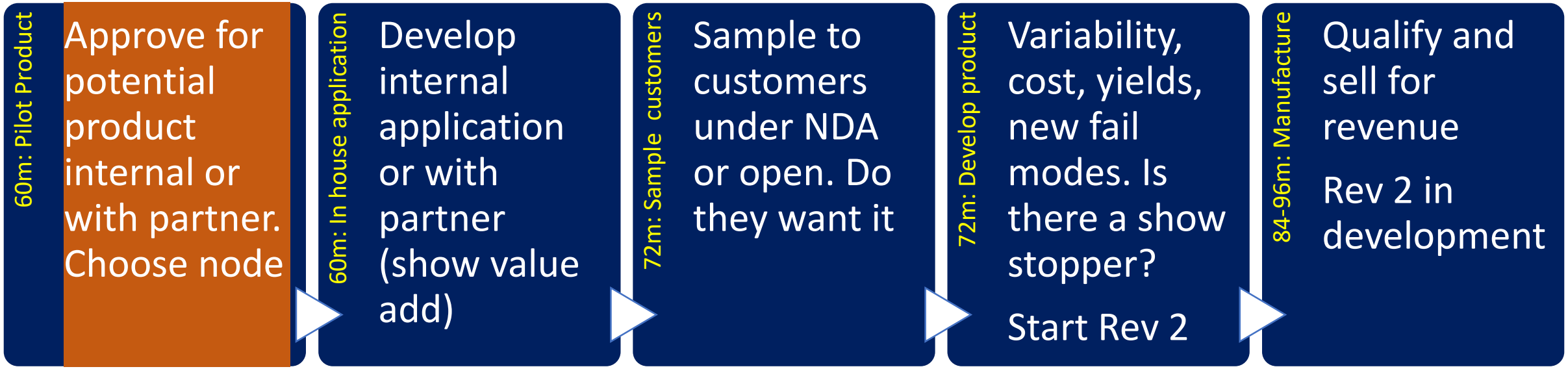
Product Lifecycle for Memory
Part 1: Technical Proof/Open Communication



End Result: a working technology fully demonstrated and checked out

- Documented Summary: " A Novel xRAM technology built in 90nm Lithography "
- Doesn't need to be on leading edge lithography, but should be capable
- With pictures/TEMs/SEMs (4-5 years after concept)

Product Lifecycle for Memory Part 2: "We are going to build a product"



- 7-8 Years from concept assuming no restarts or resource limitations from concept to revenue
- Usually performed in a stealth mode. Presentations disappear (3DXP example)
- Next announcement is samples or early production (MRAM/Xpoint)

Problem with Hype/New tech

- People want to jump to page two before completing page one. Fine to speed flow, but we know that 90% of technology concepts don't make it to products
- It rarely makes sense to be stealth in part one
  - You want to show research, You need funding
  - The work is either patented or is not novel
  - You need to get feedback and advice and investors
- Open and closed companies follow this (FinFet, 3D NAND, PCM, MRAM, ReRAM, NRAM, etc)

- RECOMMENDATION: Complete all stages of part 1 in detail to be efficient in development
- RECOMMENDATION: Evaluate all technologies and chance for success based on where they are on lifecycle.

Some Examples of Technologies

Notes: Stealth work could cause error in judgement

- MRAM: 2.5 (S10)
- Optane/3D Xpoint: Intel 2.5(S10). Micron 2.3 (S8)
  - Other company crosspoint PCM is 1.5 (IBM, Hynix, ST)
- DNA/Molecular based storage: 1.2 (S2)
- ReRAM
  - Adesto/Panasonic: 2.5 (S10)
  - Crossbar: 2.2 (S7) on 1T1R. 1.4 (S4) on 1TnR
  - 4DS: 1.3 (S3)
  - Weebit Nano 1.3 (S3)
- NRAM: Seems like 1.4 (S4)… but reportedly at 2.3+ (S8)
  - Marketing and partnership can diverge from technology. But that doesn't always speed things up
- New FRAMs: 1.3 (S3) (Old FeRAMs are at 2.5 (S10))

How to use “divergence” from the model

- Mini array not demonstrated. But full Product being discussed
  - This is a great idea to save years of development IF no issues are found
  - …. This has never happened.
  - Product development is VERY high risk with large amount of investment at risk. Backup plans needed.
- Example: Apple says universal memory allows breakthrough performance of phone. Commit new design to one memory
  - The invest $1B in development. If it doesn’t work, they use back up plan and added money to deal with issues
  - Apple has backup phone is parallel. Ramp this if universal memory doesn’t work
  - This is a rare, but not unheard of situation (Intel processors)
- MRAM, PCM, ReRAM all have examples of divergence and results

Each Phase requirement

- We can give overview (shown on next slides)
- Then there is a longer lists of details and examples of what causes delays (one page per phase)
- Then there are “PLC Milestone reports” where a full report exists for each phase (~10 pages)
- The Key to make this effective and speed development is
  - Don’t skip steps, validate first step in full, then move to next. Prevents repeats and allows fault correction
  - Each phase will highlight a brand new challenge. Old ones must have be controlled
  - If you know there is a disturb mechanism in phase 2, you can test out controls in phase 3 so phase 4 is ready to deal with it.

Each Stage Requirements/Milestones

- Stage 1: Propose Operations and Theory
  - Why should this work. What is the physical mechanism
  - What are the competitive advantages (in Theory)
  - How is it novel?
  - What are the potential Risks/Showstoppers
  - How would it be made
    - Research
    - Development
    - high volume
  - Inputs from equipment/materials people

Each Stage Requirements/Milestones

- Stage 2: Create Cell or structure to validate theory
  - Can I create one cell or structure (could be 1mm in size) to validate the theory of memory operation. Program, erase, retention
  - Run simulations and skews
  - Determine voltages, timing, that might go into an array
  - Determine disturbs in voltage and timing and thermal effects
  - Basic validation of materials properties
  - In parallel think about process tools and requirements

Each Stage Requirements/Milestones

- Stage 3: Create multiple cells in some array pattern
  - 4x4 array or one row of 10 cells
  - WL and BL are external connections. Test pads everywhere
  - Determine array layout options (5-10+ options are typical with ability to control all nodes)
  - Can you program a pattern, read it, erase or re-write, store charge. Are there disturb mechanisms? Temperature effects?
  - Publish results with idea to get feedback and quantitative analysis. Review with technical advisors
  - Propose cell size and options (next step can have multiple cell sizes)
  - We have list of items to look for based on previous technologies
  - Repeat step if needed….
- A Lot of technologies get stuck at beginning or end of this phase!

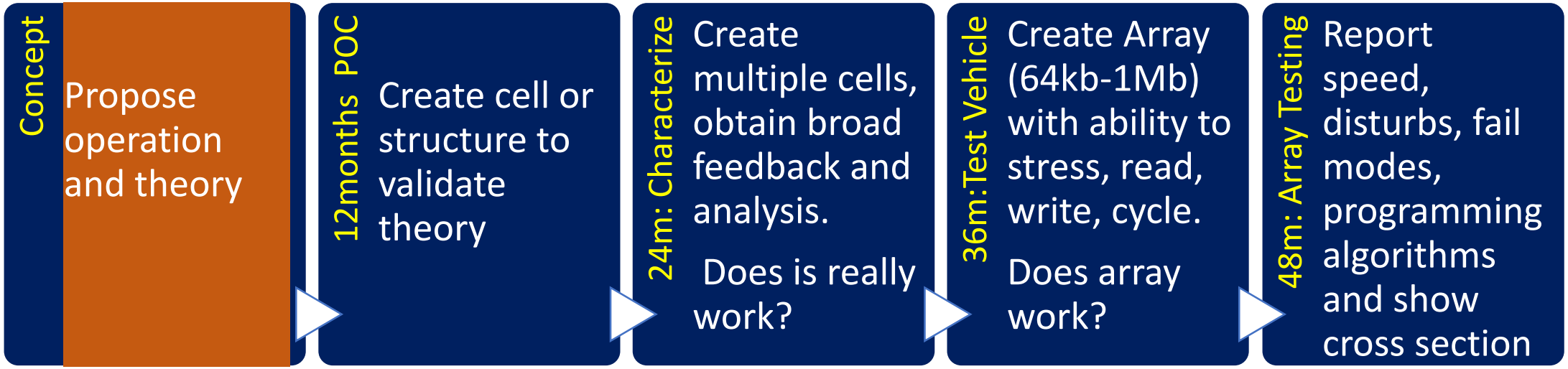
Each Stage Requirements/Milestones

- Stage 4: Create full “array” with decoders, latches
  - 64Kbits to 1Mbit. There could be intermediate arrays (4K-64K)
  - We assume technology works (Many do not). We want to create a chip/array to demonstrate production capability.
  - Determine process flow and array architecture. Think about fault detection and correction. Difference spacing/cell sizes
  - Blocks, planes, redundancy should be tested on this array
  - Ability to isolate all WLs and BLs if needed. Ability to change voltages
  - Multiple design rule and architecture options
  - This should be a potentially mass producible process flow and array.

Each Stage Requirements/Milestones

- Stage 5: Test and validate array and all aspects for products
  - Phase 4/5 are often longest phase. Design and process changes are needed to get manufacturable results.
  - Yield, fail modes, disturb modes, speed, VARIABILITY, testability, etc
  - Publish results “A Novel xRAM technology built in 90nm Lithography”
  - Some people expect production chip immediately after publication
  - Peer feedback and investor feedback should be significant.
  - A fully functioning array is something any semiconductor company will want to buy or fund
  - IF there is a second stage 5… it should be to change design

REPEAT: Product Lifecycle for Memory
Part 1: Technical Proof/Open Communication



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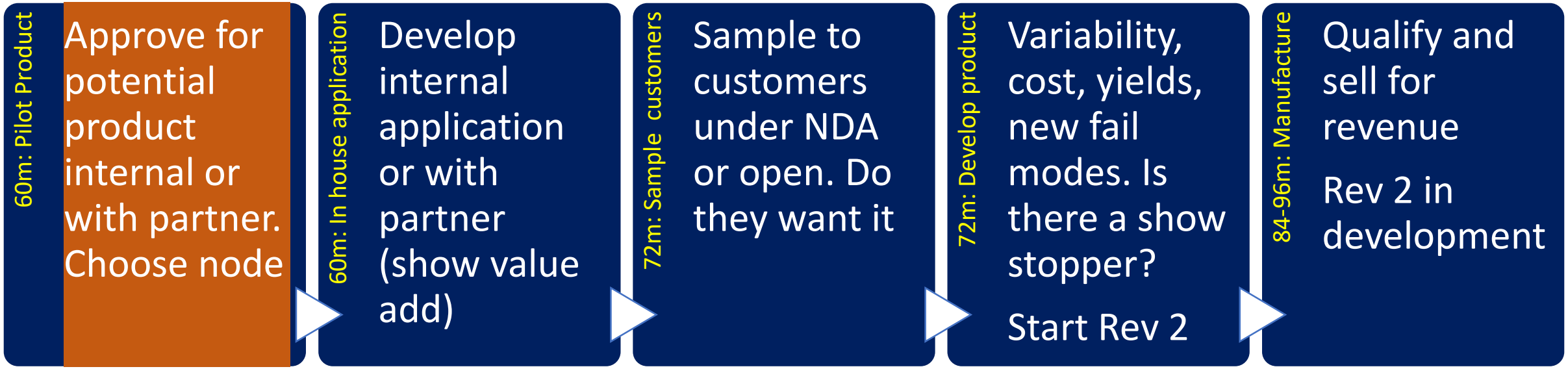

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Stealth Projects

- Most technologies (nearly all) follow the PLC. There might be a lot of public data or little. But we can track progress easily
- It is possible that some could skip parts to stay stealth.
  - Requires private funding, with a large return on risk taken
  - Requires return for keeping it quiet (2+year lead on competition)
- Examples:
  - An Apple universal memory (Allows smaller faster A15 chip)
  - A national security item (say AI/Neural network)
  - A breakthrough architecture in a large market (DRAM or NAND replacement)
    - Micron/Samsung rumors
  - Note: 3D NAND, 3D Xpoint, MRAM all followed normal PLC with stealth “part 2”

How to Speed Adoption and Increase Awareness (hype) of Technology

New Memory should be used, but it can have significant “helpers”

- Make a real product that wont ramp but can be used as Demo
  - Test arrays used as cache or bulk storage
  - Use massive over provisioning, ECC, only lasts 10-100 cycles
- Simulate effects of Memory…. Even when not using it
  - Make a USB drive with controller/FPGA and any memory that simulates the effects of the proposed memory
  - DRAM+SLC NAND byte addressable. Make specs match what would be seen from new memory
- Small cache on larger product.
  - A 256Mbit cache attached to the front of a 16Gbyte SSD
- Use in “reclaim” memory applications with no reliability requirements
  - One song music player sold in China
  - Allows someone to test it out, don’t hype it until ready
- Make a <64bit array and embed in an existing process product
- Design flexible arrays with lots of ECC/backup
- Find System or memory partner looking for hype.
  - A up and coming SSD company would love to try out a new technology

Investment and Venture Capital

- Companies/investors will support all phases depending on their goals
  - “place bets” based on Phase 1. They just want to see data
  - Invest to support phase 2, 3. Often many parallel companies invest.
  - Phase 4 is where companies look to control investment and IP.
  - After Phase 5, companies are planning what the mass market revenue is.
- Manage Internal, investor, and external communication differently
  - Mark’s saying: “I strongly support your goal to get additional funding based on optimistic presentations!”
  - Make sure you know real risks and probabilities and that the IP/ownership is controlled with respect to that.
  - Do you want to license, sell operation, grow operations, control technology …. Every technology and person is different.
- I have advised companies on how to invest (iCAP, WDC) and what to look for. Often they have competing or different motives than advisors
  - “we want to control it, even if we don’t think it will work”
  - “we have IP/patent issues that we need to manage”

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Summary

- Assess where we are in the lifecycle
- Assess where we are in time and where we will be in next year or two
- Keep investors posted on where we are, learnings and help needed
- Don’t skip steps. It tends to cause delay and wasted resources on a good technology

Questions/Comments?