



New Wave Design

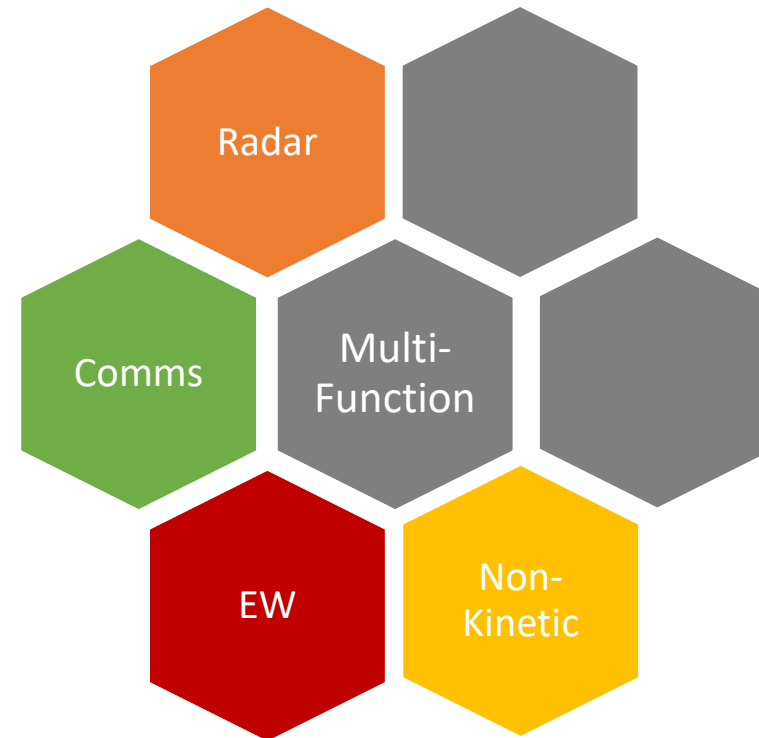
**Unlocking Multi-Function Aperture Sensors for Next-
Generation Defense Systems**

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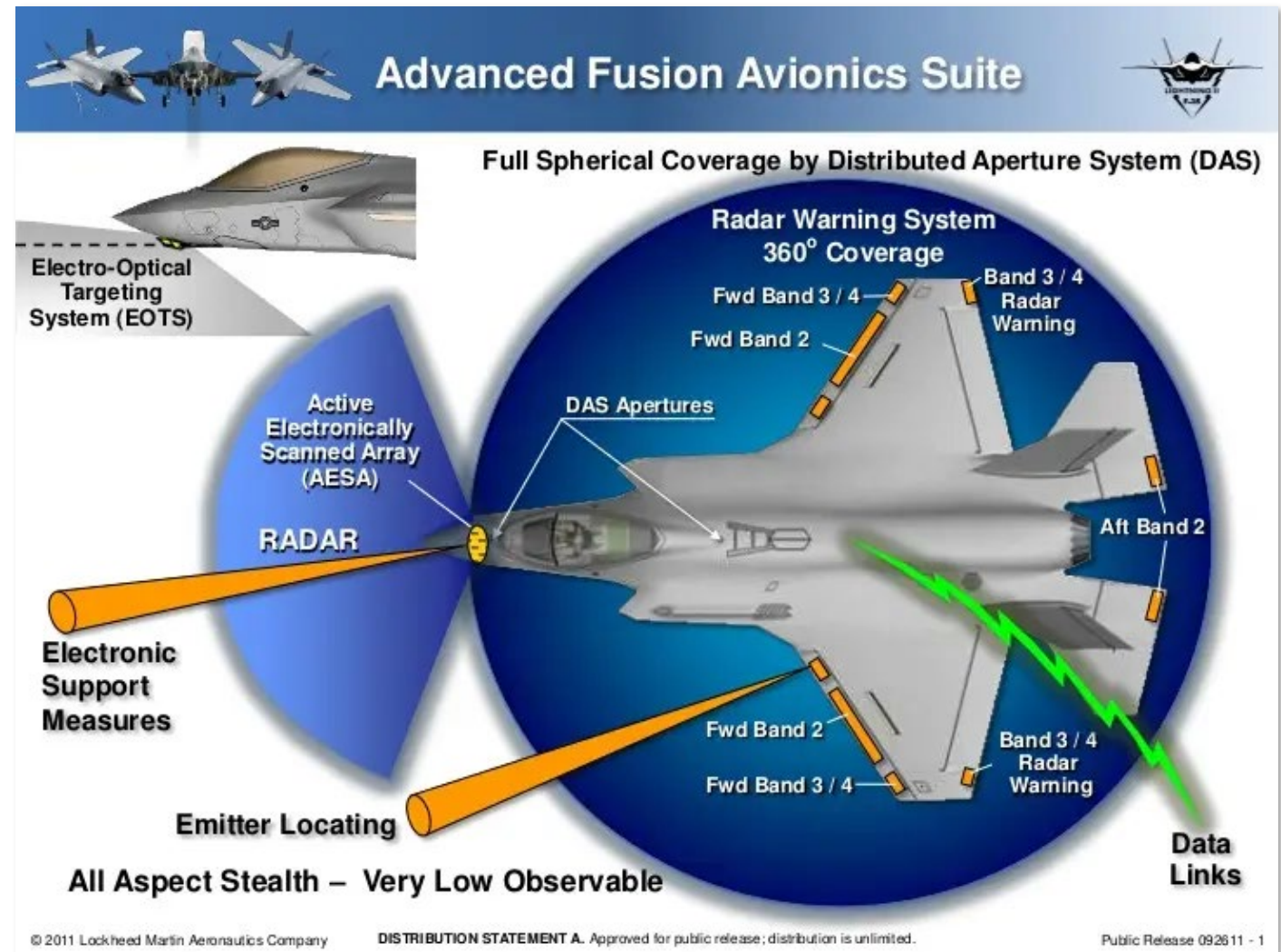
What is a Multi -Function Aperture (MFA) Sensor

- Consolidates multiple capabilities into a single sensor
- Multiple functions can be deployed simultaneously
- Software -defined, allowing resources to be dynamically allocated based on mission and threats
- Increased capabilities with improved SWaP



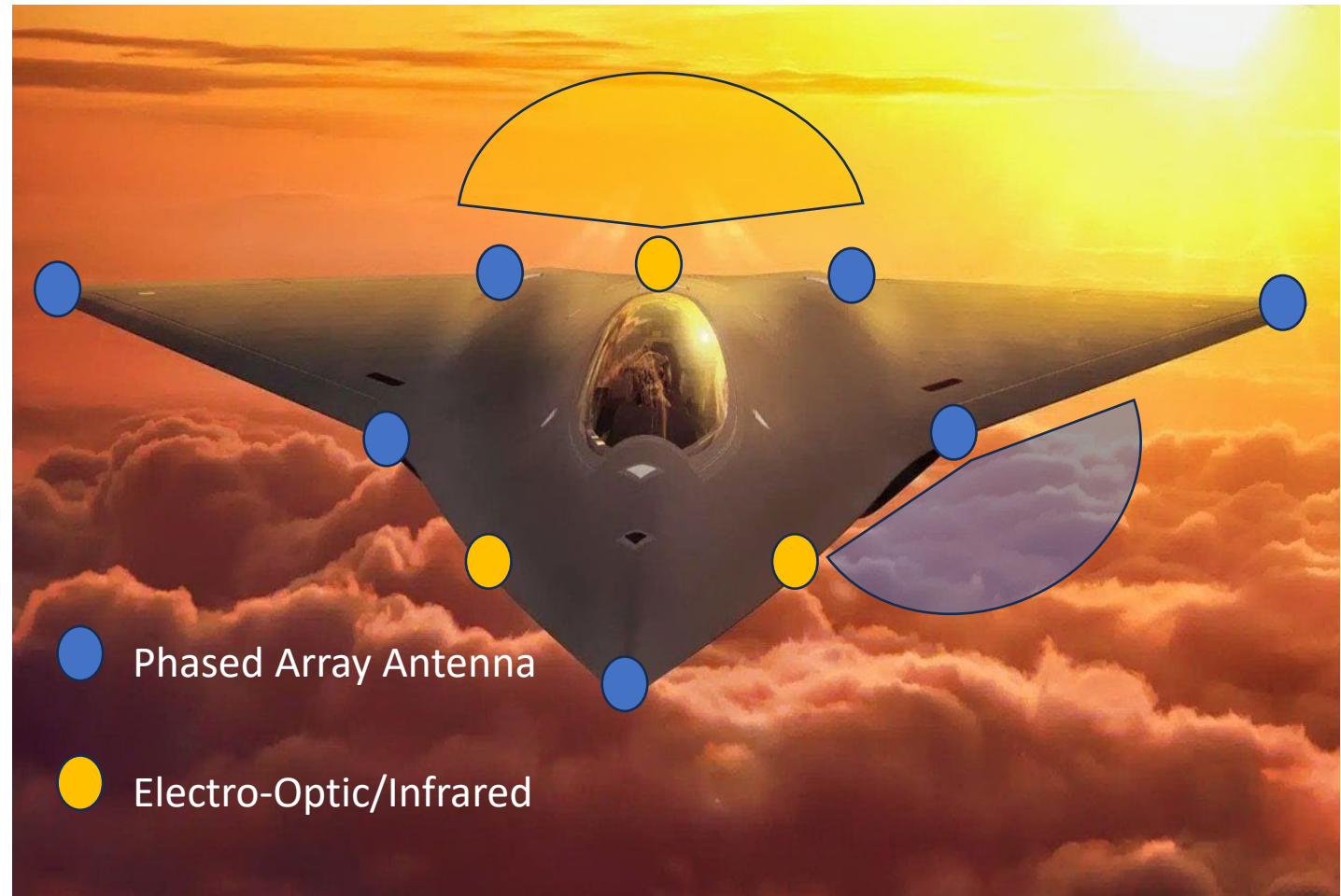
5th Gen Sensor Architecture

- Each sensor system has a dedicated set of apertures that are tuned for their specific domain
- Sensor processors from other domains do not have access to all available sensor data
- Sensor processing hardware is idle when a given domain is not in use



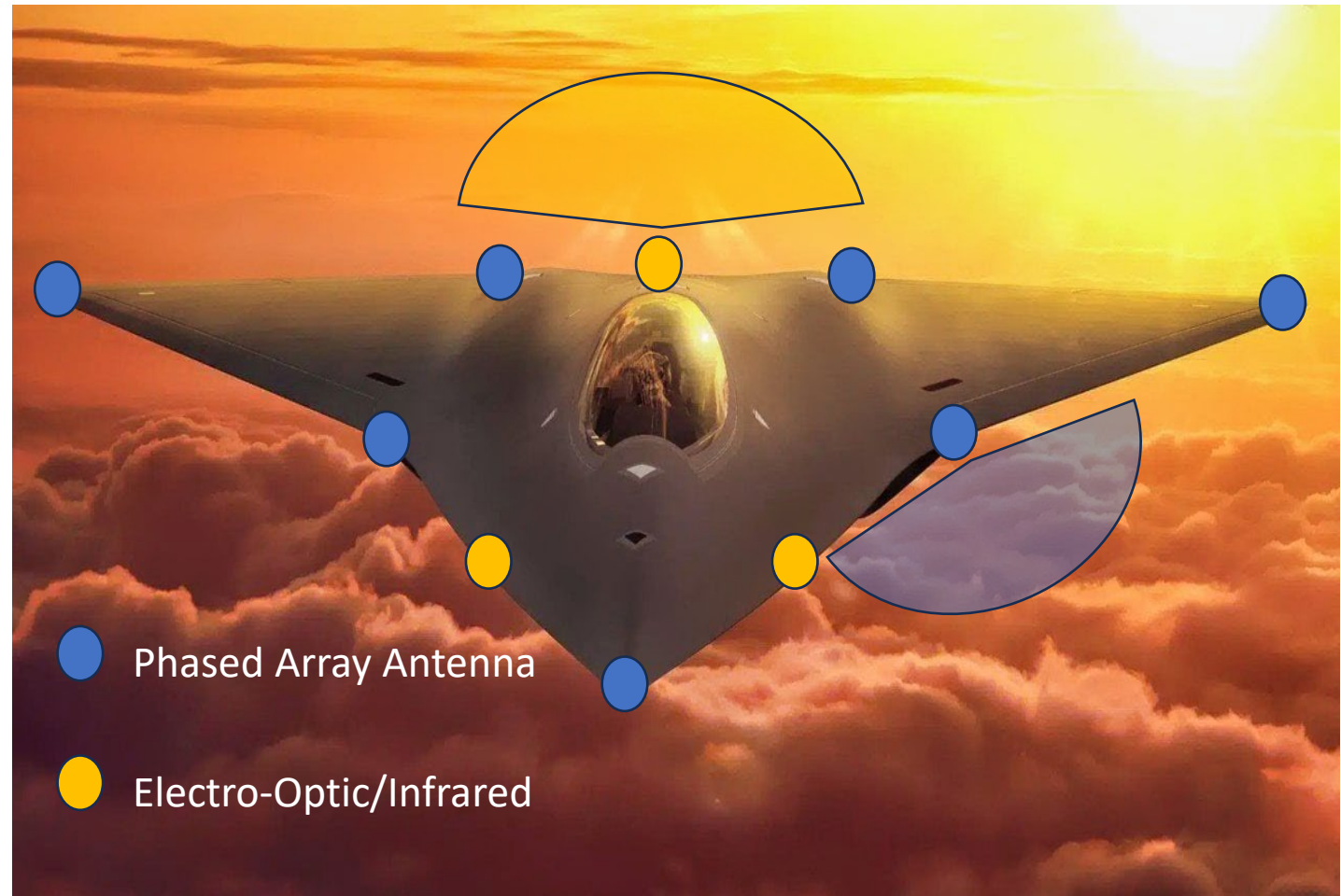
Next Gen MFA Architecture

- High-performance RF and EOIR sensors are shared across multiple mission threads (EW, EOIR, Radar, Comms, etc.)
- Sensor processing systems have access to data from any aperture
- Requires significant amounts of data movement in platform



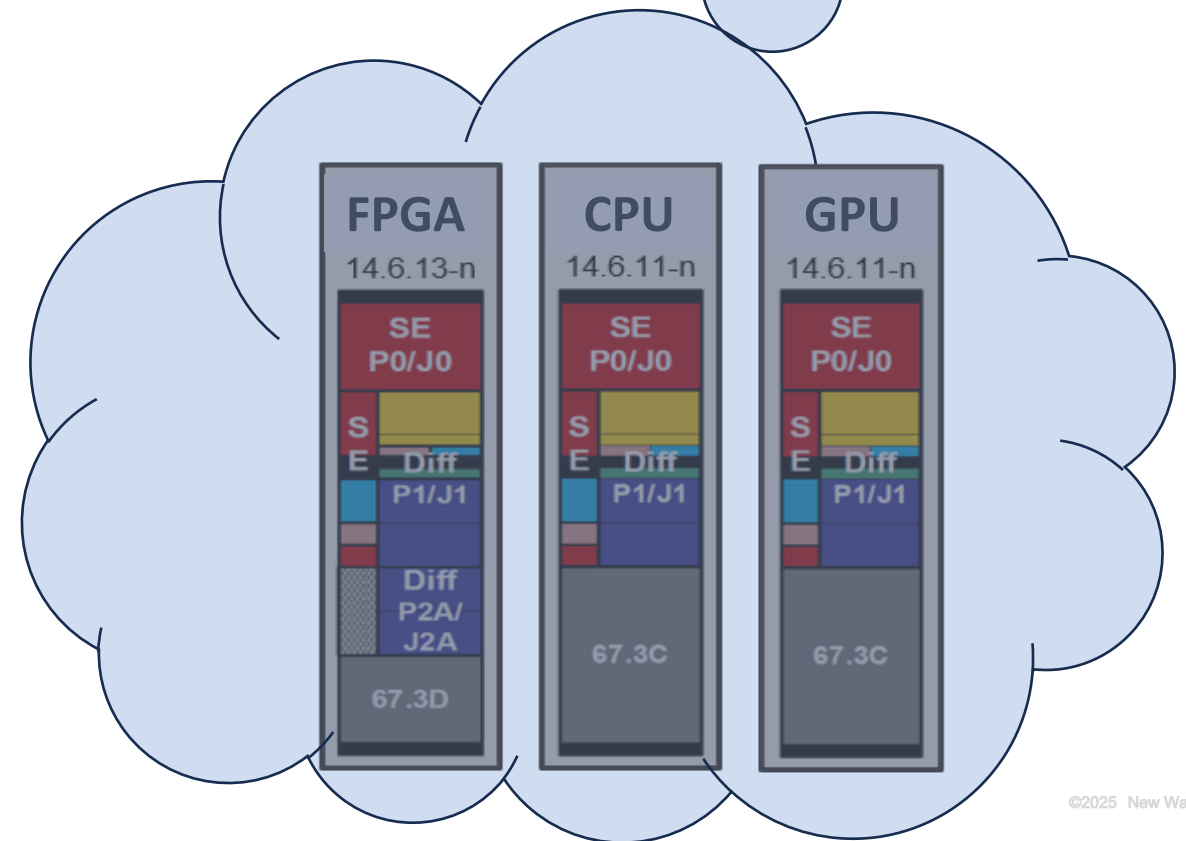
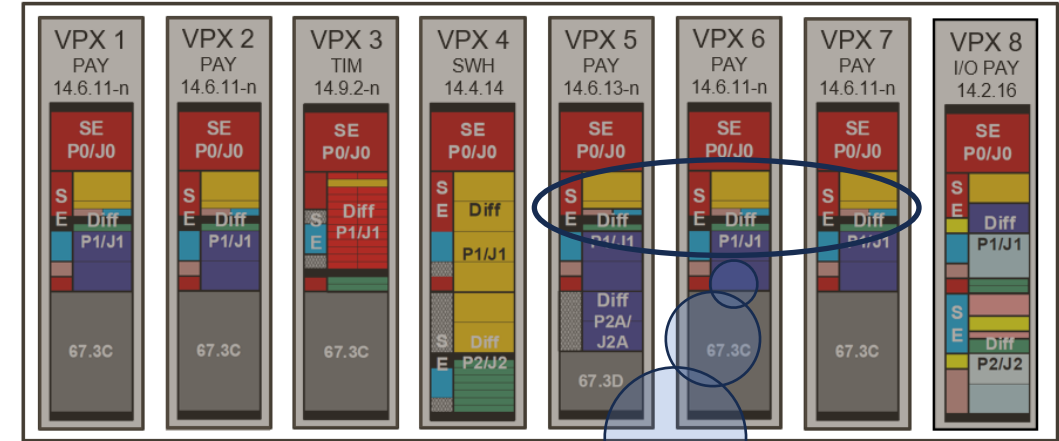
Next Gen MFA Architecture

- Phased arrays with increasing element counts that push farther into the EM spectrum can generate data rates near 1 Tb/s per sensor
- The ability to digitize, perform minimal compute and convert to optical data becomes paramount
- Efficient and smart data transfer protocols like RoCEv2 are necessary



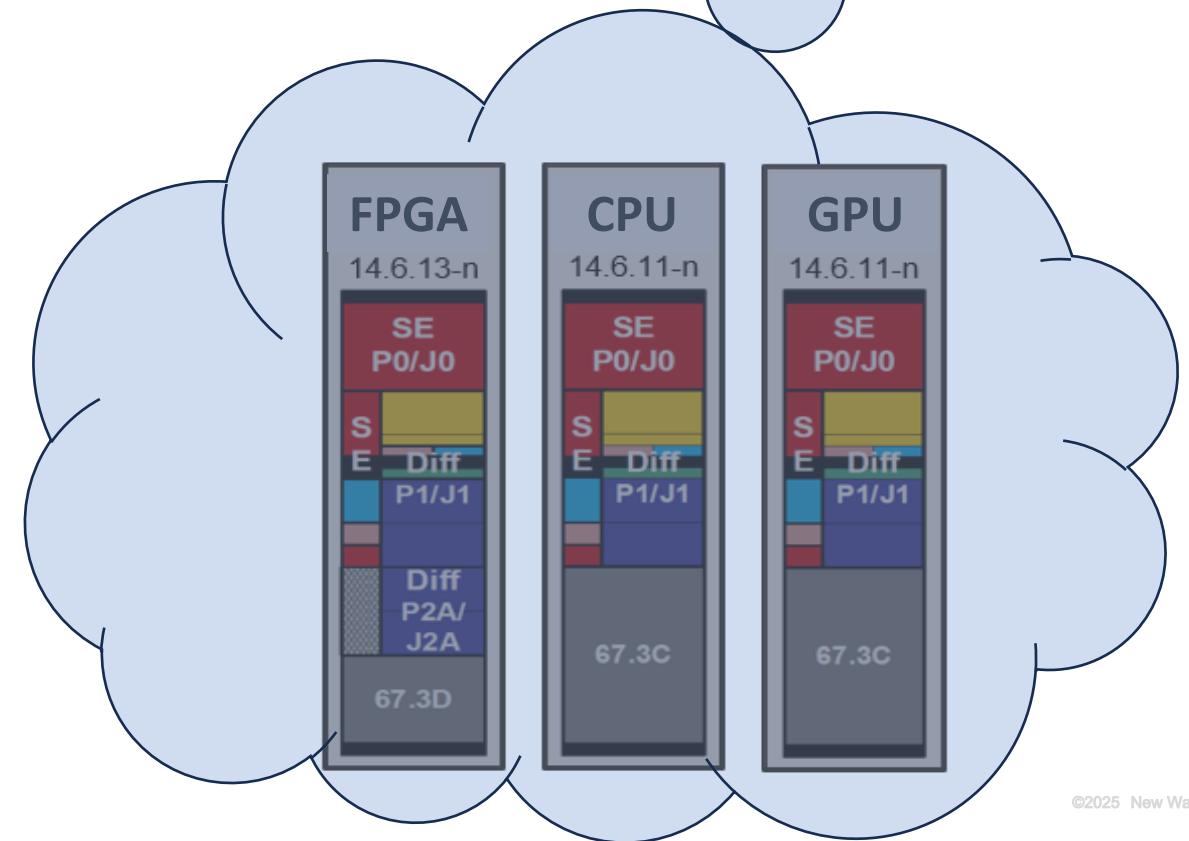
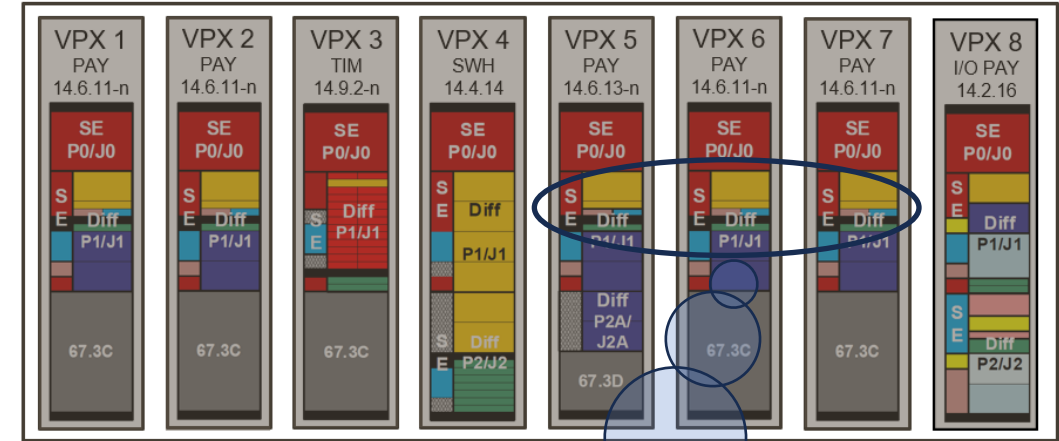
Next Gen MFA Architecture

- Rugged heterogenous sensor fusion processor with industry -best processing elements are essential
- High-density optical and RF connector options are needed
- Flexible hardware configuration that can be allocated for the mission at hand must be adopted



Next Gen MFA Architecture

- Ability for processing algorithms and techniques to access all sensor data available
- Ability to upgrade hardware to keep pace with advancing technology
- Enable new businesses to participate in rapid innovation





Challenges on the Road Ahead

- System qualification strategies are needed to accommodate shrinking upgrade cycles for processing algorithms and hardware
- Efficient allocation of hardware resources for multiple mission threads
- Cutting -edge silicon chips are large, power hungry, and have increased pin counts
- Similar capabilities and architectures are needed in ever -increasing SWaP-constrained environments

THANK YOU

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