VITA 100 Slot Profiles – Evolution from VITA 65

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9 January 2025

This work is sponsored by the Department of the Air Force under Air Force Contract #FA8702-15-D-0001. Opinions, interpretations, conclusions and recommendations are those of the author and are not necessarily endorsed by the United States Government.

Abstract and Bio

- **Abstract**

  This presentations goes over the Slot Profiles planned for VITA 100.0. It contrasts what is planned for VITA 100.0 with how VITA 65.0 evolved. This presentation also summarizes the contributors to a factor 8 increase in available bandwidth between PIMs (Plug-In Modules) and the backplane.

- **Bio**

  Greg Rocco is a member of Technical Staff at MIT Lincoln Laboratory.

  He is the editor of: VITA 65.0 (OpenVPX System Standard), VITA 65.1 (OpenVPX System Standard -- Profile Tables), VITA 100.0 and 100.1. He was editor of VITA 46.0 (VPX Baseline Standard) up through the recent release of ANSI/VITA 46.0-2023. He is a key contributor to other VITA, SOSA, and HOST standards.

Outline

- Communities getting input from
- Terminology
- Increase in available bandwidth between PIM (Plug-In Modules) and backplane
- Counts of ANSI/VITA 65.0 Slot Profiles over time
- VITA 100 3U, 4U, and 6U Slot Profiles
- Counts of VITA 65.0 Slot Profiles over time compared to proposed VITA 100.0 Slot Profiles
- Summary

Getting Input From a Community Of Other Standards

- **For what goes into VITA 100, getting input from:**
  - VITA Member companies
  - SOSA (Sensor Open Systems Architecture) Hardware Working Group (https://www.opengroup.org/sosa)
  - HOST (Hardware Open Systems Technologies) community of both those working on it and those using it (https://host-oa.com/)
  - Army C5ISR Center's CMOSS (C4ISR/EW Modular Open Suite of Standards) Community thru their influence of SOSA
- **Several of us participate in both VITA and SOSA**
- **In SOSA we have discussions, which are Export controlled, to come up with best solutions in relation to target applications**
  - The VITA Standards Organization (https://www.vita.com/) is international, so we cannot have discussions involving export controlled and other sensitive information
- **A SOSA Working Group passed on requirements to VITA**

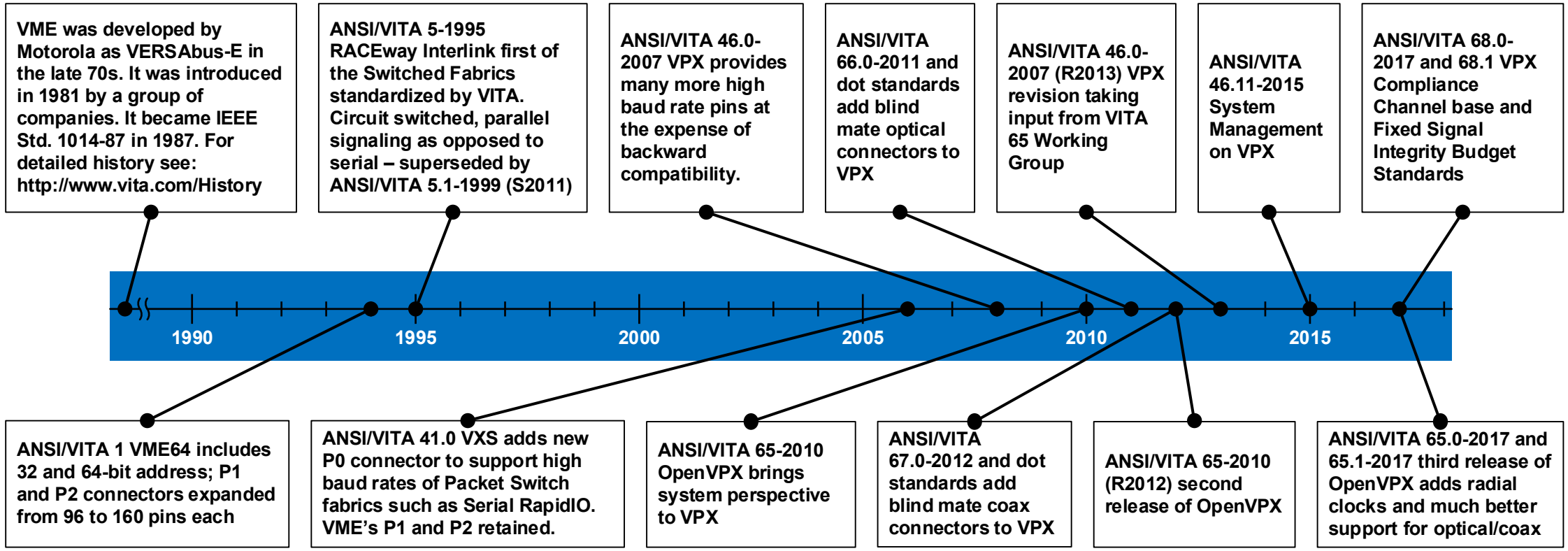
Terminology

- **Baud:** The number of symbols (data signaling events) per second sent across a single transmission path. Depending on the encoding method used, a data signaling event (symbol) can contain less than 1 bit, exactly 1 bit, or more than 1 bit.
  - For example: PCI Express 2.0 over a single path (x1) has a bit rate of 4.0 Gbit/sec. The data is transmitted using 8B/10B encoding, which encodes 8 bits of data into 10 symbols. One way to look at the encoding is that each transmitted symbol represents 0.8 of a bit. Thus, the baud rate to achieve a 4.0 Gbit/second data rate is the bit rate divided by the symbols per bit which is 4 Gbit/sec / 0.8 bits/baud = 5 Gbaud.
  - For example: 1000BASE-T over 4 paths has a bit rate of 1 Gbit/sec in one direction. The data is transmitted using PAM5 encoding (Pulse Amplitude Modulation with 5 levels). PAM5 encoding has five levels – +2, +1, 0, -1, -2; 4 levels are used for data encoding two bits per symbol (00, 01, 10, 11) and the 5th level is used to support forward error correction. Baud rate = bit rate / number of paths / bits per symbol = (1 Gbit/sec) / 4 / 2 = 125 Mbaud.
  - Note: The term symbol is sometimes used differently from above. For example, the PCIe uses the term GT/s (GigaTransfers/sec) to mean the same as what Gbaud means above. With PCIe a symbol refers to 10 of the symbols above. Using the PCIe terminology a symbol is decoded into an 8-bit byte.
- **Pipes:** A physical aggregation of differential pairs or optical fibers used for a common function that is characterized in terms of the total number of differential pairs or optical fibers. A Pipe is not characterized by the protocol used on it. The following Pipes used in these slides:
  - **Ultra-Thin Pipe (UTP):** A Pipe comprised of two differential pairs or two optical fibers. Example: 1000BASE-KX Ethernet, 1x Serial RapidIO, x1 PCIe, and 10GBASE-SR interfaces.
  - **Thin Pipe (TP):** A Pipe composed of four differential pairs or four optical fibers. Example: 1000BASE-T interfaces.
  - **Fat Pipe (FP):** A Pipe composed of eight differential pairs or eight optical fibers. Example: 4x Serial RapidIO, x4 PCIe, 10GBASE-KX4, 40GBASE-SR4 (40 Gbit Ethernet over fiber) interfaces.

Increasing Available Bandwidth between PIMs (Plug-In Modules) and Backplane by Factor of 8

- **Approximately 2X number of pins/pairs**
- **Approximately 2X the baud rate**
  - From 25.78125 Gbaud with ANSI/VITA 46.30-2020 and VITA 46.31-2020-VDSTU to 53.125 Gbaud
- **Approximately 2X by enabling PAM4 (Pulse Amplitude Modulation with 4 levels)**
  - Enabling 2 bits/baud as opposed to just 1 bit/baud
- **Some Ethernet Protocols being targeted for VITA 100:**
  - 100GBASE-KR1 – (53.125 Gbaud, PAM4 Signaling) – [IEEE 802.3ck] Clause 163 over a UTP
  - 200GBASE-KR2 – (53.125 Gbaud, PAM4 Signaling) – [IEEE 802.3ck] Clause 163 over a TP
  - 400GBASE-KR4 – (53.125 Gbaud, PAM4 Signaling) – [IEEE 802.3ck] Clause 163 over a FP

Timeline VME, VXS, VPX, and OpenVPX Thru 2017



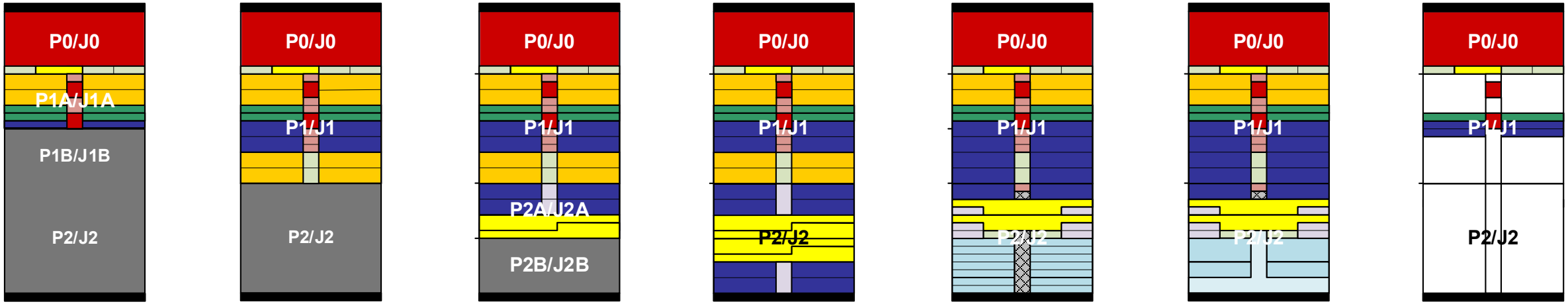
- **OpenVPX builds on VPX to add system thinking**
  - VPX (VITA 46) has dot standards for each protocol and some others: VME, RapidIO, PCIe, Ethernet
  - OpenVPX has profiles which spell out how multiple protocols are to be used together
- **Not shown is the timeline for VITA 48 standards for cooling and packaging**
- **Note with timeline: Products have frequently been available before the associated standards are all the way through the ANSI standardization process**

ANSI/VITA 65.0 Slot Profiles Over Time

	3U							6U						
	Copper connectors only				Mix of copper and blind-mate optical/coax			Copper connectors only				Mix of copper & optical/coax		
	14.2	14.3	14.4	14.5	14.6	14.8	14.9	10.2	10.3	10.4	10.5	10.6	10.8	
VITA 65.0 Section	Payload	Per-ipheral	Switch	Misc	Payload	Switch	Misc	Payload	Per-ipheral	Switch	Misc	Payload	Switch	Overall Total
ANSI/VITA 65.0-2010	10	3	8	1				4	4	4	2			36
ANSI/VITA 65.0-2012	3		1		2			3	1	1				11
ANSI/VITA 65.0-2017	2	1	5	1	10	9	1		1		2	2		34
ANSI/VITA 65.0-2019	2		1		2		1	1				3	1	11
ANSI/VITA 65.0-2021												1		1
ANSI/VITA 65.0-2023														0
65.0-2025 in process														0
Totals for sections	17	4	15	2	14	9	2	8	6	5	4	6	1	93
Totals for 3U and 6U	63							30						93

- **Slot Profile counts in 2010 and 2012 versions reflect COTS supplier's desire to have standard align with product plans**
  - When OpenVPX first started VPX (ANSI/VITA 46.0-2007) had been out for a few years and COTS suppliers already had product roadmaps
- **2017 was first to have good coverage of optical/coax blind-mate connectors**
- **2019 added Slot Profiles driven by SOSA – after that only 1 new Slot Profile with 2021 and none after that**

Proposed VITA 100 3U Payload Slot Profiles

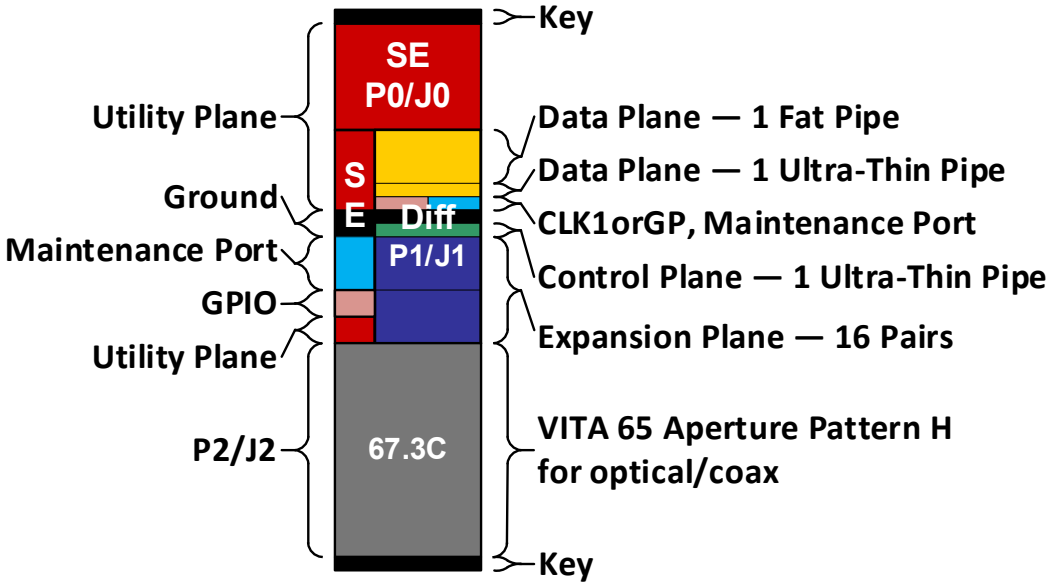


SLT300-PAY-10.2.1-n | SLT300-PAY-10.2.2-n | SLT300-PAY-10.2.3-n | SLT300-PAY-10.2.4-n | SLT300-PAY-10.2.5-n | SLT300-PAY-10.2.6-n | SLT300-PAY-10.2.7-n

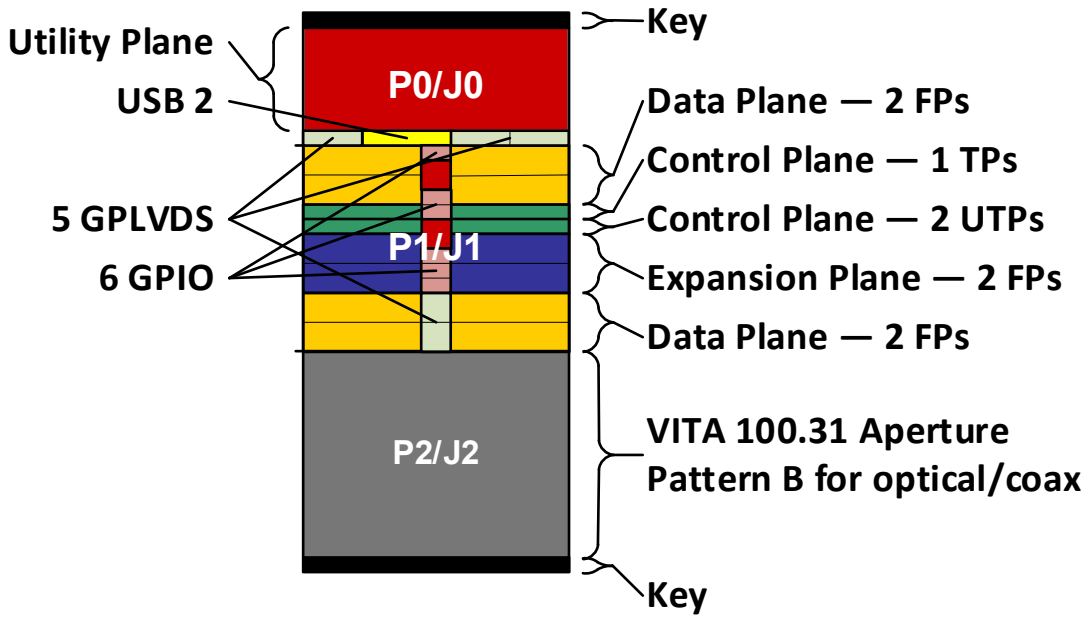
- **As go from Slot Profile 10.2.1 to 10.2.4 the I/O via connector wafers that is there stays and additional I/O is added as the size of the Aperture for blind-mate optical and coax decreases**
  - 10.2.2 adds more Data Plane, Expansion Plane, GPLVDS, and GPIO
  - 10.2.3 adds more Expansion Plane, USB 4 ports, and a GPLDutp (intended for TIA-422)
  - 10.2.4 adds more Expansion Plane, more USB 4 ports and another GPLDutp
- **10.2.4 and 10.2.6 start with 10.2.1 and add Expansion Plane, GPLDutp, GPLVDS, GPIO, and a mezzanine site**
  - 10.2.5 has a QMC site mapping – VITA 93 is a new mezzanine standard being develop and is about ¼ size of an XMC
  - 10.2.6 has an XMC site mapping
- **10.2.7 is primarily User Defined – intent is to get all the system specialized on these and/or mezzanines**

Proposed 3U Slot Profiles – Payload with VITA 100.31 Aperture B – SLT300-PAY-10.2.2-n

VITA 65.0 Slot Profile SLT3-PAY-1F1U1S1S1U1U2F1H-14.6.11-n



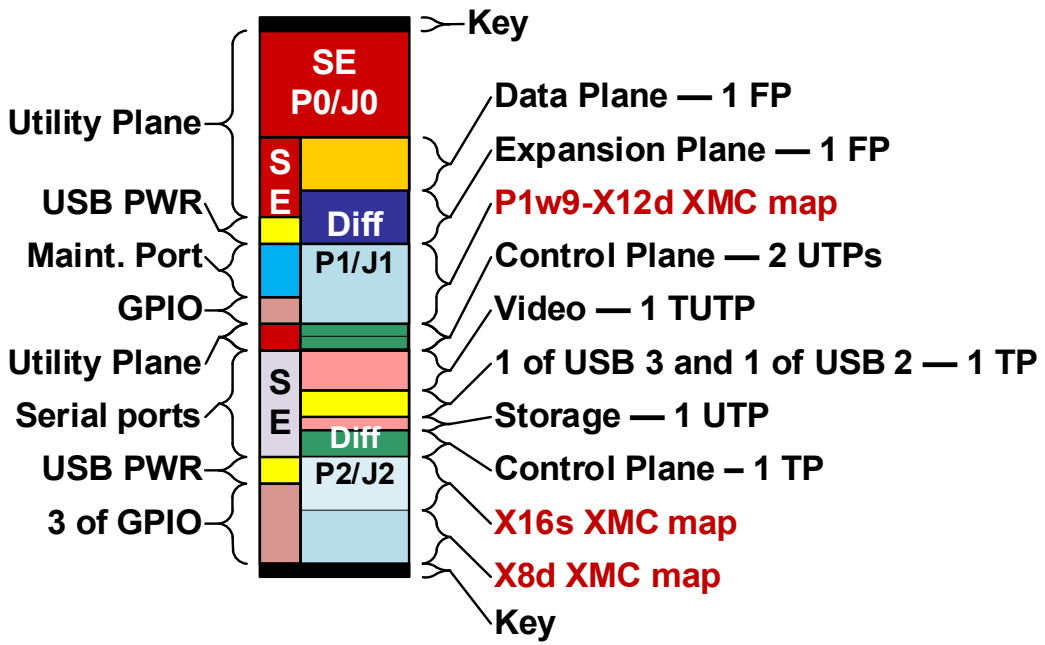
VITA 100.0 Slot Profile SLT300-TIM-10.4.1-n



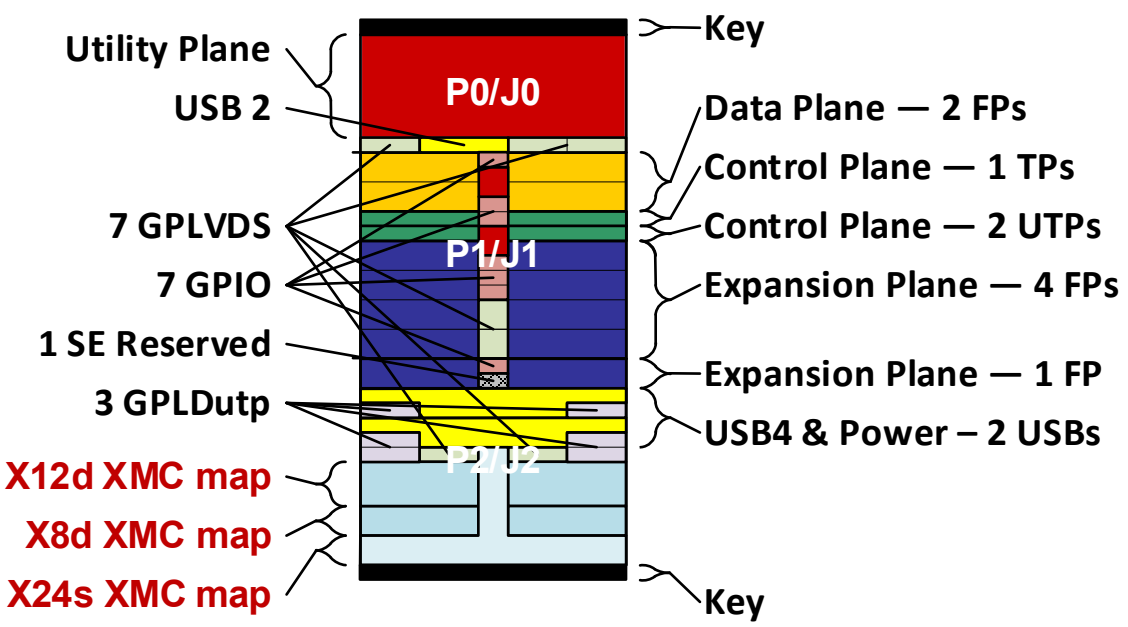
- **Intended for processing with coax/fiber I/O; Notice that VITA 100 Slot Profile adds:**
  - 1 Data Pane FP in place of a UTP, 2 Data Plane FPs, a Control Plane UTP and TP
  - Expansion Plane is the same with both
  - 5 GPLVDS (one of which replaces CLK1orGP), 5 GPIO
  - A USB 2

Proposed 3U Slot Profiles – Payload with Mapping of XMC – SLT300-PAY-10.2.6

VITA 65.0 Slot Profile SLT3-PAY-1F1F2U1TU1T1U1T-14.2.16



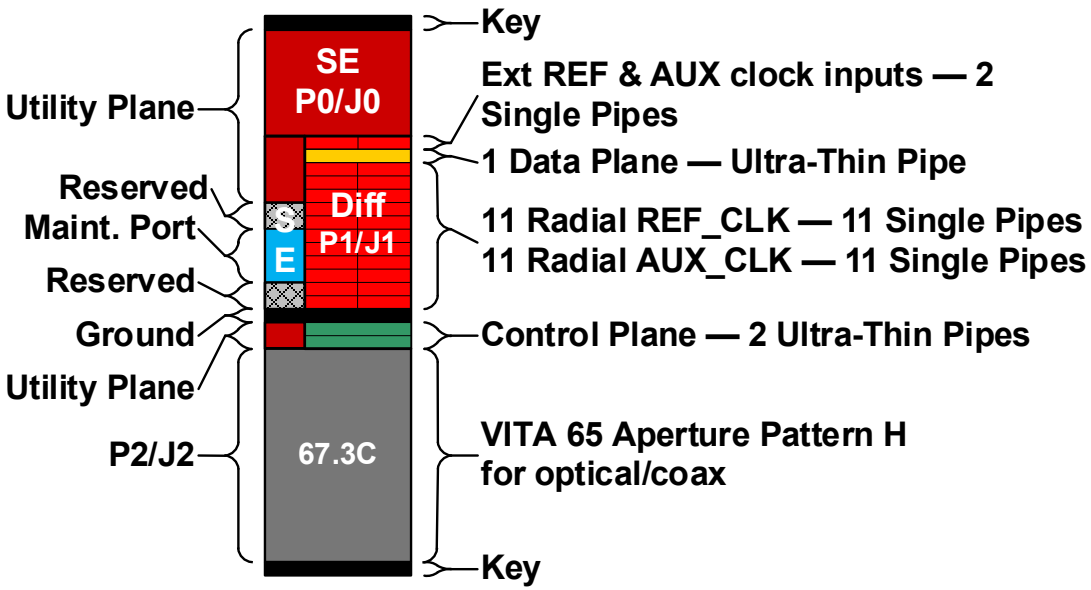
VITA 100.0 Slot Profile SLT300-TIM-10.4.1-n



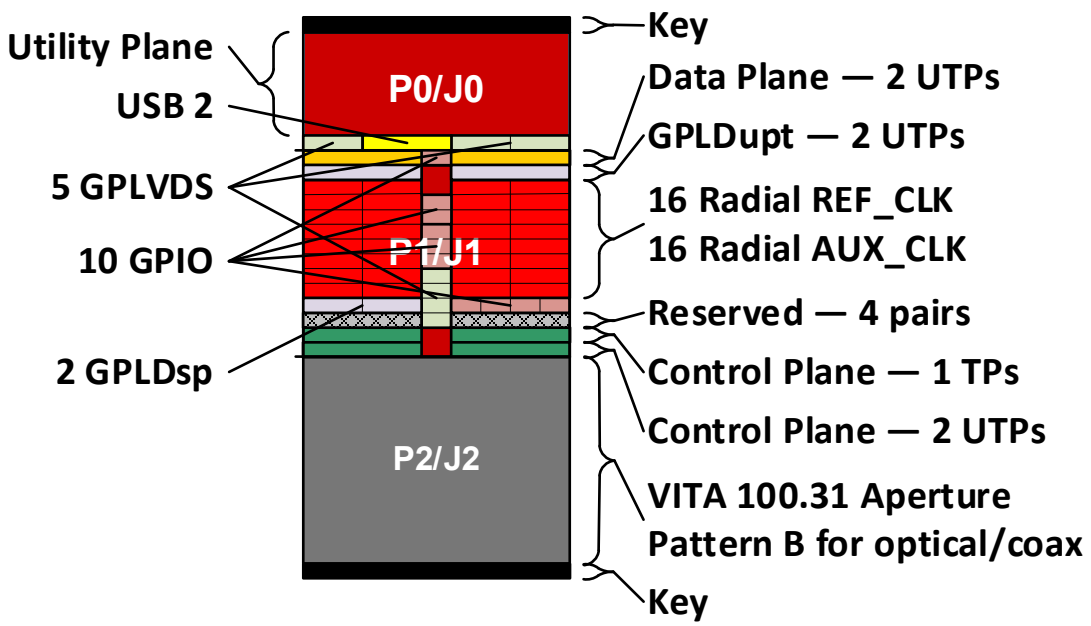
- **Intended for SBC with lots of I/O; Notice that VITA 100 Slot Profile adds:**
  - 1 Data Pane FP, a Control Plane TP
  - 3 Expansion Planes FPs
  - 7 GPLVDS, 4 GPIO, 3 GPLDutp (intended for TIA-422), 1 reserved Single-Ended
  - A USB 2, 2 USB 4, with power in place of 1 USB 3, a USB2, a video TUTP, and a storage UTP
  - 8 additional single-ended in XMC mapping (X16s to X24s)

Proposed 3U Slot Profiles – Radial Clock Driver – SLT300-TIM-10.4.1-n

VITA 65.0 Slot Profile SLT3x-TIM-2S1U22S1U2U1H-14.9.2-n



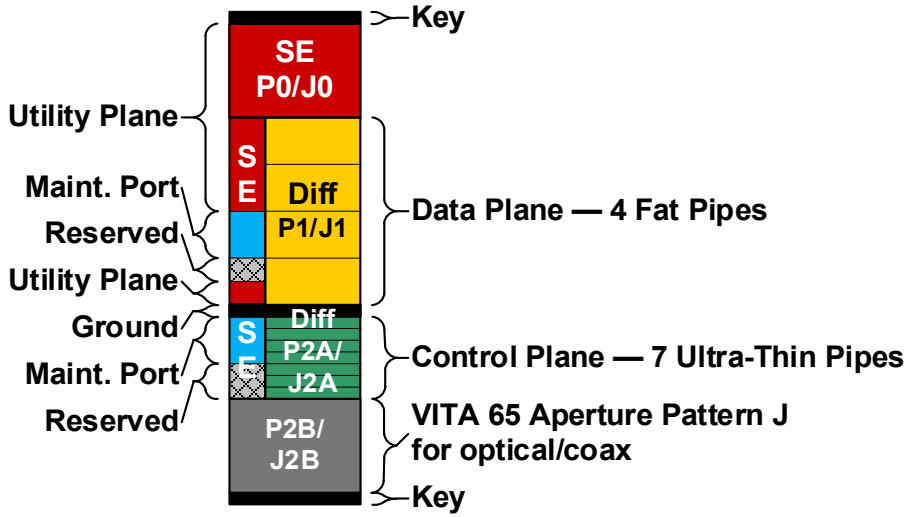
VITA 100.0 Slot Profile SLT300-TIM-10.4.1-n



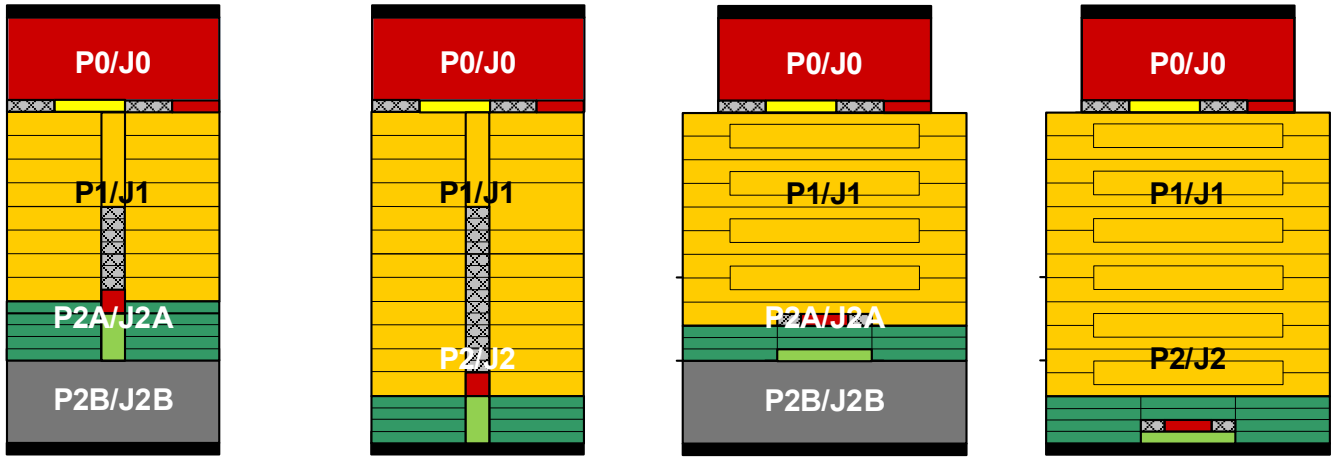
- **Notice that VITA 100 Slot Profile adds:**
  - 5 additional REF_CLK and 5 AUX_CLK radial clock outputs
  - Data Plane UTP and Control Plane TP
  - 5 GPLVDS, 10 GPIO, 2 GPLDutp (intended for TIA-422, and 2 GPLDsp (intended for TIA-485), 4 reserved pairs
  - A USB 2

Proposed 3U Switch Slot Profiles

VITA 65.0 Slot Profile SLT3-SWH-4F1U7U1J-14.8.7-n



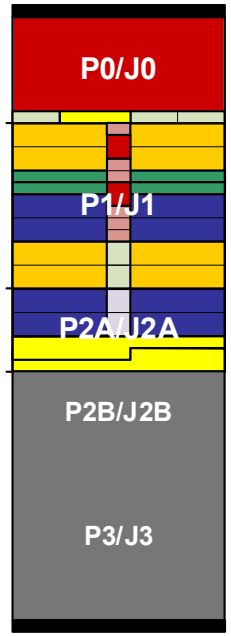
Proposed family of VITA 100 3U Switch Slot Profiles



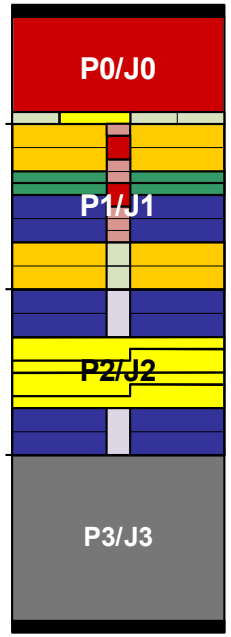
SLT400-SWH-11.3.1-n | SLT300-SWH-10.3.2-n | SLT300-SWH-10.3.3-n | SLT300-SWH-10.3.4-n

- **VITA 100 Switch Slot Profiles (lower-left) P1/J1, P2/J2 with 4-Pair + 1 Single-Ended 1.0-inch slot pitch**
  - **SLT300-SWH-10.3.1-n**
    - Data Plane: 8 FPs + 1 TP
    - Control Plane: 8 UTPs + 1 TP
    - Aperture C for optical/coax – 1.0-inch pitch
  - **SLT300-SWH-10.3.2**
    - Data Plane: 12 FPs + 1 TP
    - Control Plane: 8 UTPs
- **VITA 100 Switch Slot Profiles (lower-right) P1/J1, P2/J2 with 6-Pair 1.2-inch slot pitch**
  - **SLT300-SWH-10.3.3-n**
    - Data Plane: 13 FPs
    - Control Plane: 8 UTPs
    - Aperture D for optical/coax – 1.2-inch pitch
      - Room for 4 MTs instead of 3
  - **SLT300-SWH-10.3.4**
    - Data Plane: 18 FPs
    - Control Plane: 10 UTPs

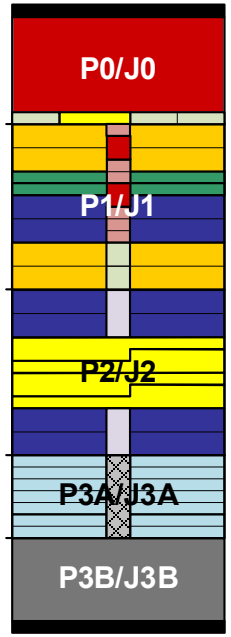
Proposed VITA 100 4U Payload Slot Profiles



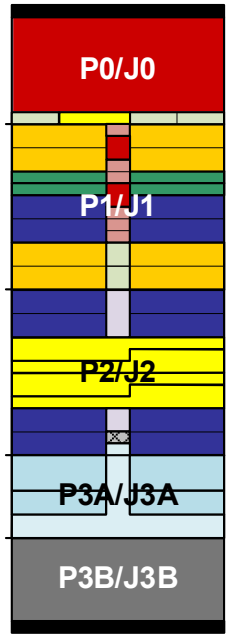
SLT400-PAY-11.2.1-n



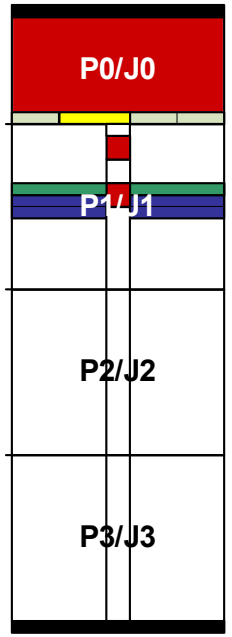
SLT400-PAY-11.2.2-n



SLT400-PAY-11.2.3-n



SLT400-PAY-11.2.4-n

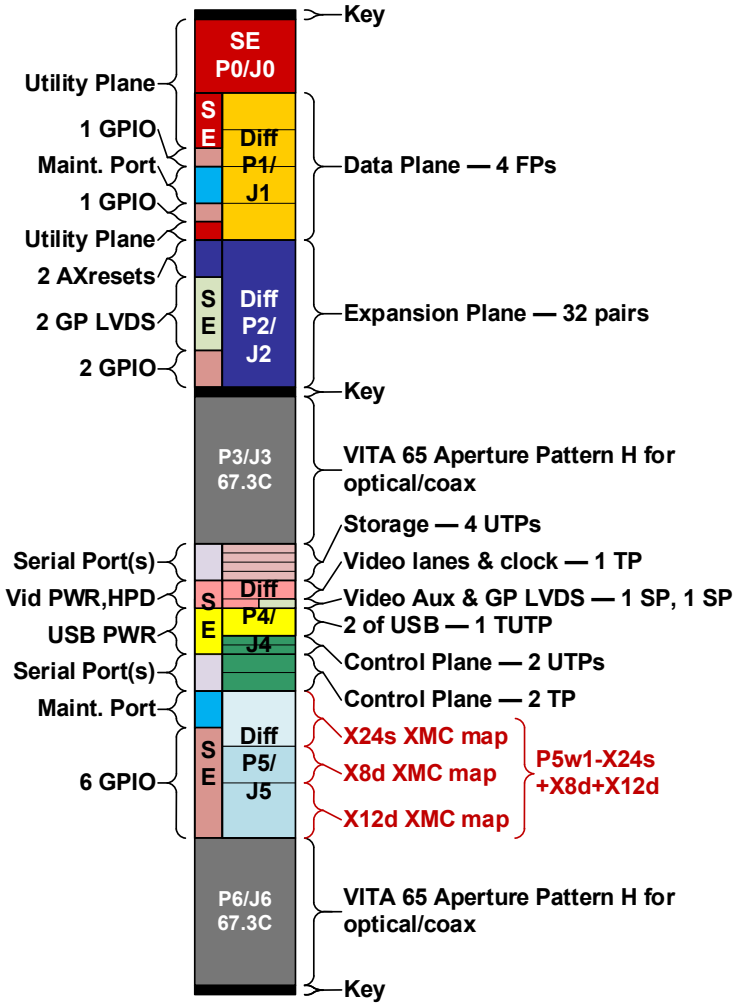


SLT400-PAY-11.2.5-n

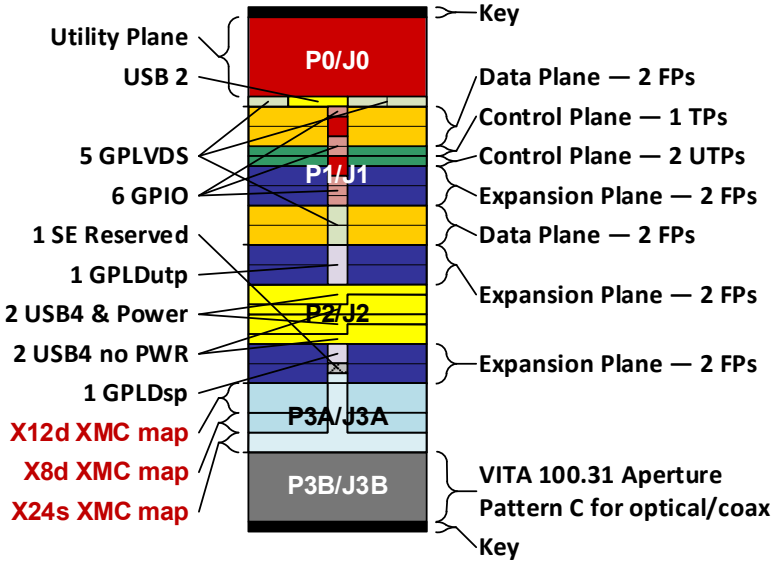
- **Like 3U as go from 11.2.1 to 11.2.3 the I/O via connector wafers that is there stays and additional I/O is added as the size of the Aperture for blind-mate optical and coax decreases**
  - 11.2.2 adds more USB 4 and Expansion Plane, and GPLDutp
  - 11.2.3 adds a QMC site mapping – VITA 93 is a new mezzanine standard being develop and is about ¼ size of an XMC
  - 11.2.4 is the same as 11.2.3 except has an XMC mapping instead of a QMC mapping
  - With 4U have enough I/O via connector wafers so do not see the need for Payload Slot Profiles with no Aperture, except 11.2.5
- **11.2.5 is primarily User Defined – intent is to get all the system specialized on these and/or mezzanines**

Proposed 4U Slot Profiles – Payload with Mapping of XMC – SLT400-PAY-11.2.4-n

VITA 65.0 Slot Profile SLT6-PAY-4F1Q1H4U1T1S1S1TU2U2T1H-10.6.3-n



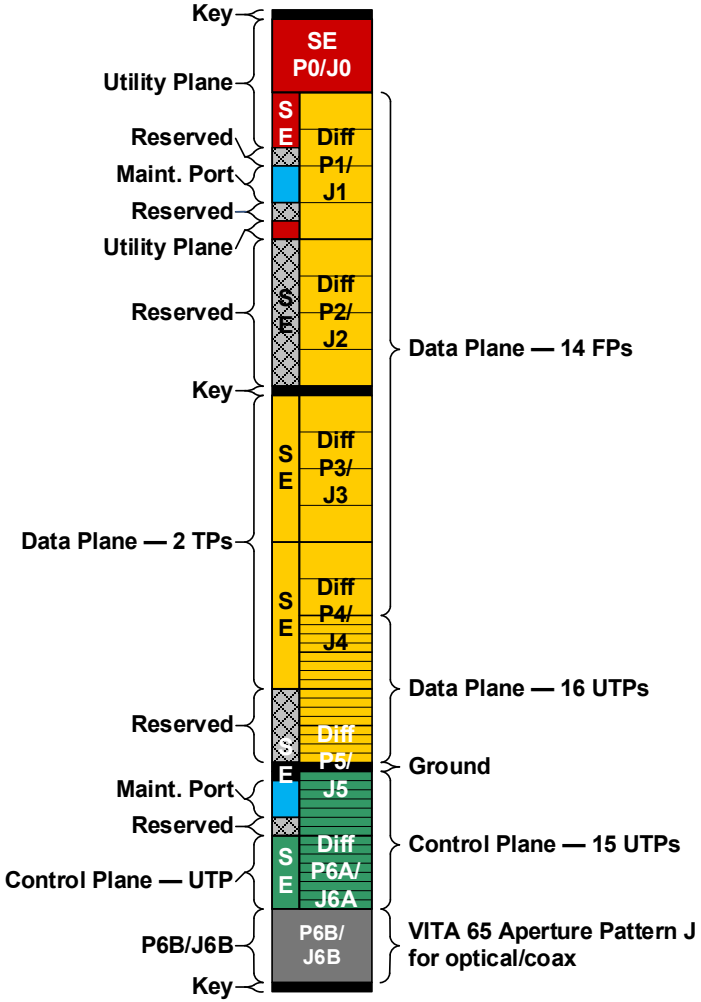
VITA 100.0 Slot Profile SLT400-PAY-11.2.4-n



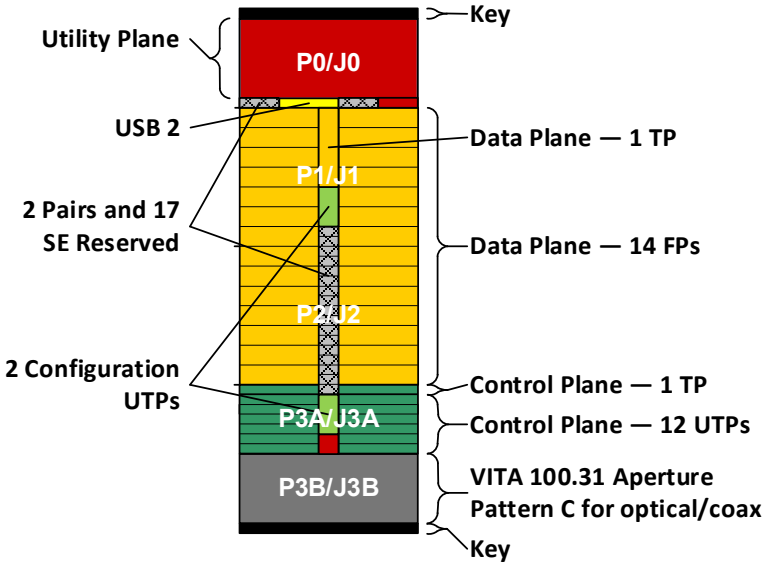
- **Other than less Aperture, VITA 100.0 4U 11.2.4 similar to VITA 65.0 6U 10.6.3:**
  - Both have 4 FPs of Data Plane and 2 UTPs or Control Plane
    - VITA 100 has 1 less Control Plane TP
  - VITA 100 has 6 FPs of Expansion Plane (24 lanes) vs 16 lanes with VITA 65.0
  - A USB 2, 4 USB 4 in place of 1 USB 3, a USB 2, a video port, and 4 storage UTP
    - Expansion Plane can also be used for storage
  - Both have XMC site mapping of 20 pairs and 24 single-ended

Proposed 4U Slot Profiles – Switch Slot Profiles

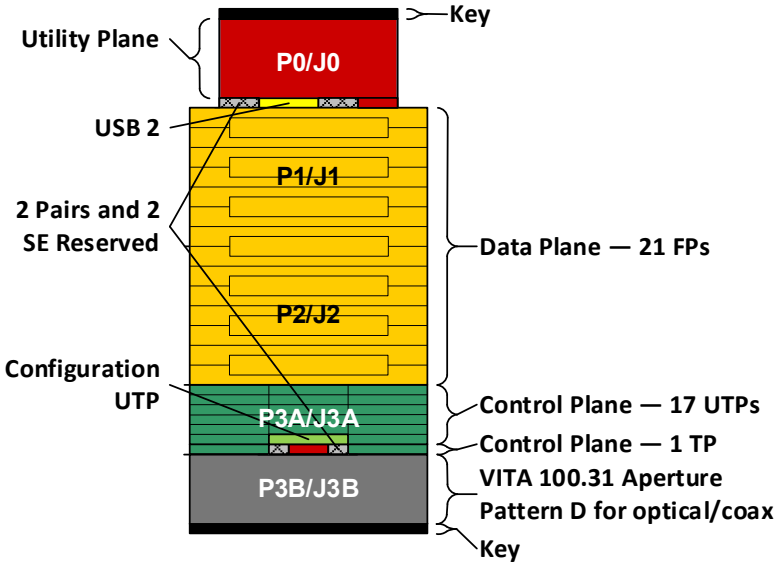
VITA 65.0 Slot Profile SLT6-SWH-14F16U1U15U1J-10.8.1-n



VITA 100.0 Slot Profile SLT400-SWH-11.3.1-n

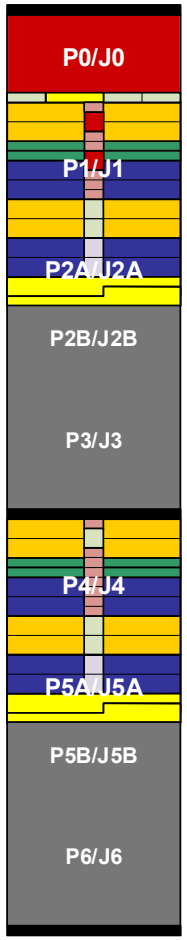


VITA 100.0 Slot Profile SLT400-SWH-11.3.2-n

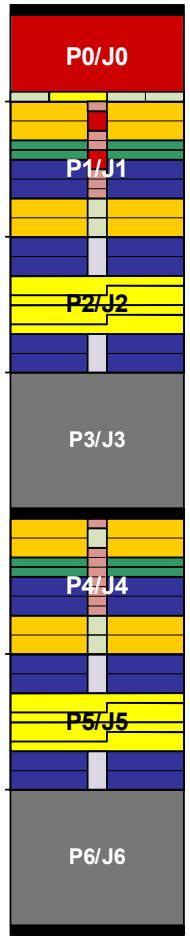


- **VITA 65.0 Slot Profile SLT6-SWH-14F16U1U15U1J-10.8.1-n**
  - Data Plane: 14 FPs + 16 UTPs + 2 TPs
  - Control Plane: 15 UTPs + 1 UTP on Single-Ended pins
- **VITA 100.0 Slot Profile SLT400-SWH-11.3.1-n – 4-Pair + 1 Single-Ended, 1.0-inch slot pitch**
  - Data Plane: 14 FPs + 1 TP + 1 UTP intended for configuration
  - Control Plane: 12 UTPs + 1 TP + 1 UTP intended for configuration
- **VITA 100.0 Slot Profile SLT400-SWH-11.3.2-n – 6-Pair, 1.2-inch slot pitch**
  - Data Plane: 21 FPs + 17 UTPs
  - Control Plane: 17 UTPs + 1 TP + 1 UTP intended for configuration

Proposed VITA 100 6U Slot Profiles – Each is 2 copies of a 4U Slot Profile Except Only One Copy of Stuff on P0/J0



SLT600-PAY-12.2.1-n – 2 of SLT400-PAY-11.2.1-n



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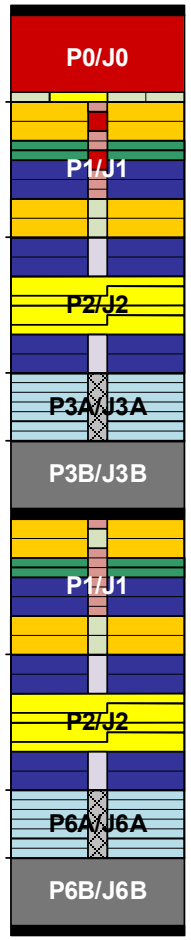

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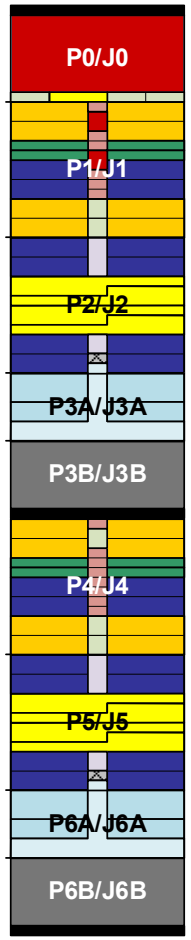
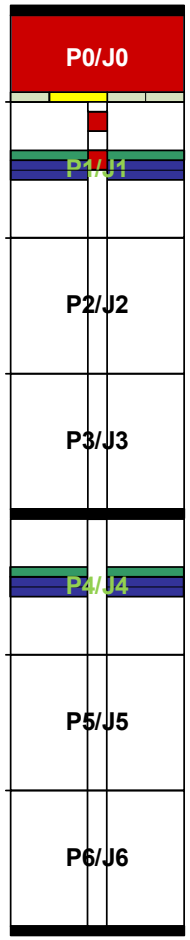
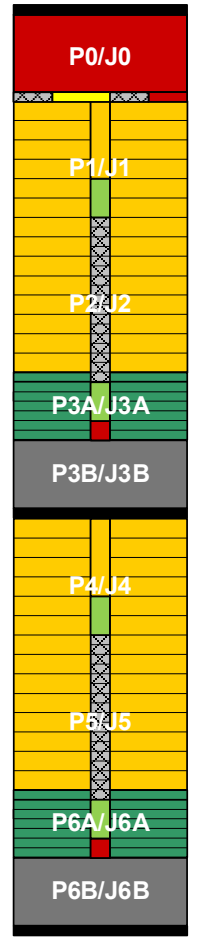


SLT600-PAY-12.2.4-n – 2 of SLT400-PAY-11.2.4-n



SLT600-PAY-12.2.5-n – 2 of SLT400-PAY-11.2.5-n



SLT600-SWH-12.3.1-n – 2 of SLT400-SWH-11.3.1-n

ANSI/VITA 65 Slot Profiles Over Time Compared to Proposed VITA-100

	3U							6U						
	Copper connectors only				Mix of copper and blind-mate optical/coax			Copper connectors only				Mix of copper & optical/coax		
	14.2	14.3	14.4	14.5	14.6	14.8	14.9	10.2	10.3	10.4	10.5	10.6	10.8	
VITA 65.0 Section	Payload	Per-ipheral	Switch	Misc	Payload	Switch	Misc	Payload	Per-ipheral	Switch	Misc	Payload	Switch	Overall Total
ANSI/VITA 65.0-2010	10	3	8	1				4	4	4	2			36
ANSI/VITA 65.0-2012	3		1		2			3	1	1				11
ANSI/VITA 65.0-2017	2	1	5	1	10	9	1		1		2	2		34
ANSI/VITA 65.0-2019	2		1		2		1	1				3	1	11
ANSI/VITA 65.0-2021												1		1
ANSI/VITA 65.0-2023														0
65.0-2025 in process														0
Totals for sections	17	4	15	2	14	9	2	8	6	5	4	6	1	93
Totals for 3U and 6U	63							30						93

		3U				4U				6U				
		10.2	10.3	10.4		11.2	11.3	11.4		12.2	12.3	12.4		
VITA 100.0 Section		Payload	Switch	Misc		Payload	Switch	Misc		Payload	Switch	Misc		Total
Totals for sections		7	4	1		5	2	0		5	1	0		25

- **VITA 100.0 is starting with a fewer Slot Profiles than the initial version of VITA 65.0 (ANSI/VITA 65.0-2010)**
  - Given we are leveraging the experience of OpenVPX, CMOSS, HOST, and SOSA, with the chosen Slot Profiles, expect little growth over time
  - The growth in Slot Profiles with VITA 65 decreased to only one after ANSI/VITA 65.0-2019

Summary

- **Increasing Available Bandwidth between PIMs (Plug-In Modules) and Backplane by Factor of 8**
- **Slot Profiles in early versions of OpenVPX were driven to some extent by product plans of member**
- **ANSI/VITA 65.0-2019 was the last version to add more than one Slot Profile**
  - ANSI/VITA 65.0/2019 was driven by VITA, CMOSS, HOST, and SOSA Communities – SOSA was a strong influence
- **With VITA 100 we are proposing families of Slot Profiles that build on each other**
- **With 3U and 4U we are taking advantage of the 6-pair connectors going to 1.2-inch slot pitch to get higher density switches**
  - Also, proposing a new Aperture that will take advantage of 1.2-inch pitch for to 4 MTs instead of 3