
**OpenVPX™ Trends and Updates with
CMOSS, SOSA™, and HOST Update**

Greg Rocco, MIT Lincoln Laboratory

23 January 2024

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Abstract and Bio

- **Abstract**

The hardware standards ANSI/VITA 65.0-2023 (OpenVPX System Standard) and ANSI/VITA 65.1-2023 (OpenVPX System Standard -- Profile Tables) are widely used for deployed military systems. The OpenVPX standard uses Plug-In Module mechanical, connectors, thermal, communications protocols, utility, and power definitions, provided by specific VITA standards to define a series of Slot, Backplane, Module, and Standard Development Chassis Profiles.

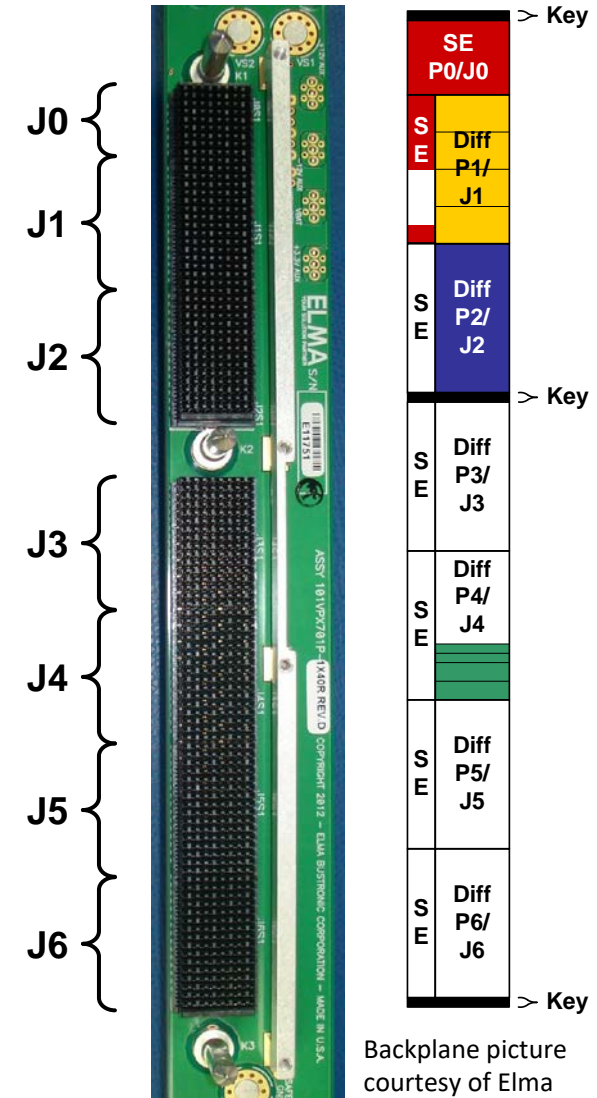
This session will give a high-level description of OpenVPX and go over some of the trends as the standards have evolved.

There is also an update on the CMOSS (C4ISR / Electronic Warfare (EW) Modular Open Suite of Standards), SOSA™ (Sensor Open Systems Architecture), and HOST (Hardware Open Systems Technology) standards.

- **Bio**

Greg Rocco is a member of Technical Staff at MIT Lincoln Laboratory.

He is the editor of: VITA 65.0 (OpenVPX System Standard) and VITA 65.1 (OpenVPX System Standard -- Profile Tables). He was editor of VITA 46.0 (VPX Baseline Standard) up through the recent release of ANSI/VITA 46.0-2023. He is a key contributor to other VITA standards, SOSA, and HOST.

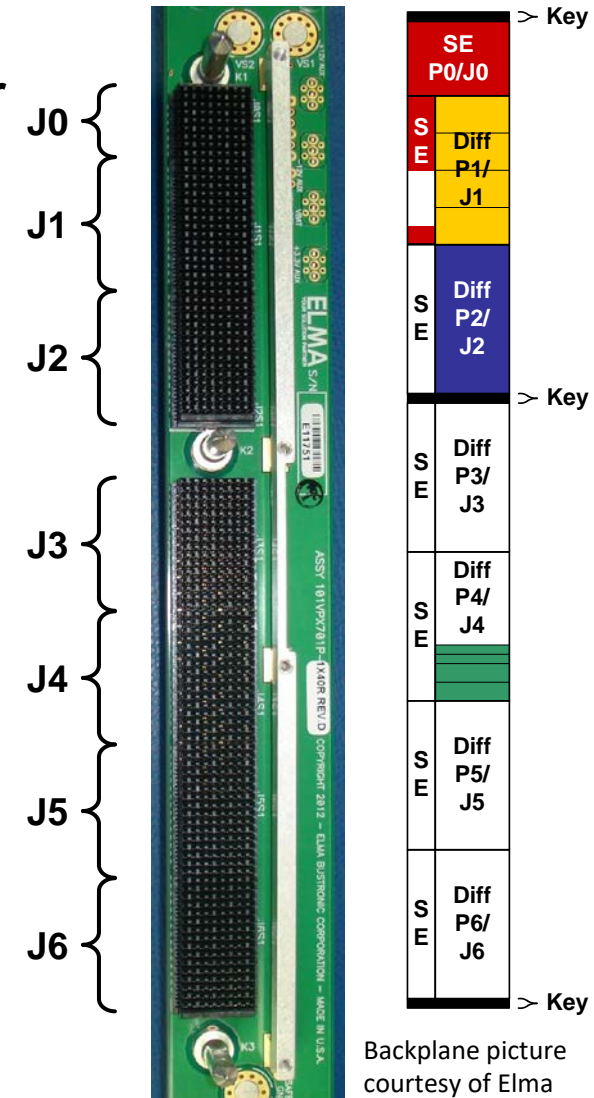




Outline

- **CMOSS, SOSA™, and HOST Update by Jason Dirner of U.S. Army C5ISR Center**
- **OpenVPX and associated standards**
 - Slot, Backplane and Module Profiles
 - VITA standards defining mechanical interface of optical/coax
- **Relationship of OpenVPX with other standardization efforts**
- **OpenVPX plans and trends**
 - Connector Modules in ANSI/VITA 65.1-2017, 2019, 2021, and 2023
 - Slot and Backplane Profiles added with 65.0-2019 and 2021 (none added with 2023)
 - Protocol sections added with ANSI/VITA 65.0-2019, 2021, and 2023
- **Summary**

Some of these slides were taken from the OpenVPX Tutorial. The full Tutorial as well as some others is available at: <http://www.vita.com/Tutorials>





U.S. ARMY COMBAT CAPABILITIES DEVELOPMENT COMMAND C5ISR CENTER

CMOSS, SOSA™, and HOST Update

12 DECEMBER 2023

JASON DIRNER

WHY MOSA?



ARMY CMOSS (from CMOSS Overview)

- Reduce size, weight, and power of C5ISR systems
- Share radio resources, processing, and data services
- Increase flexibility and adaptability
- Enable rapid insertion of new technology/capability
- Reduce lifecycle cost through increased competition
- Smaller logistics tails with common sparing

NAVY HOST (from HOST website)

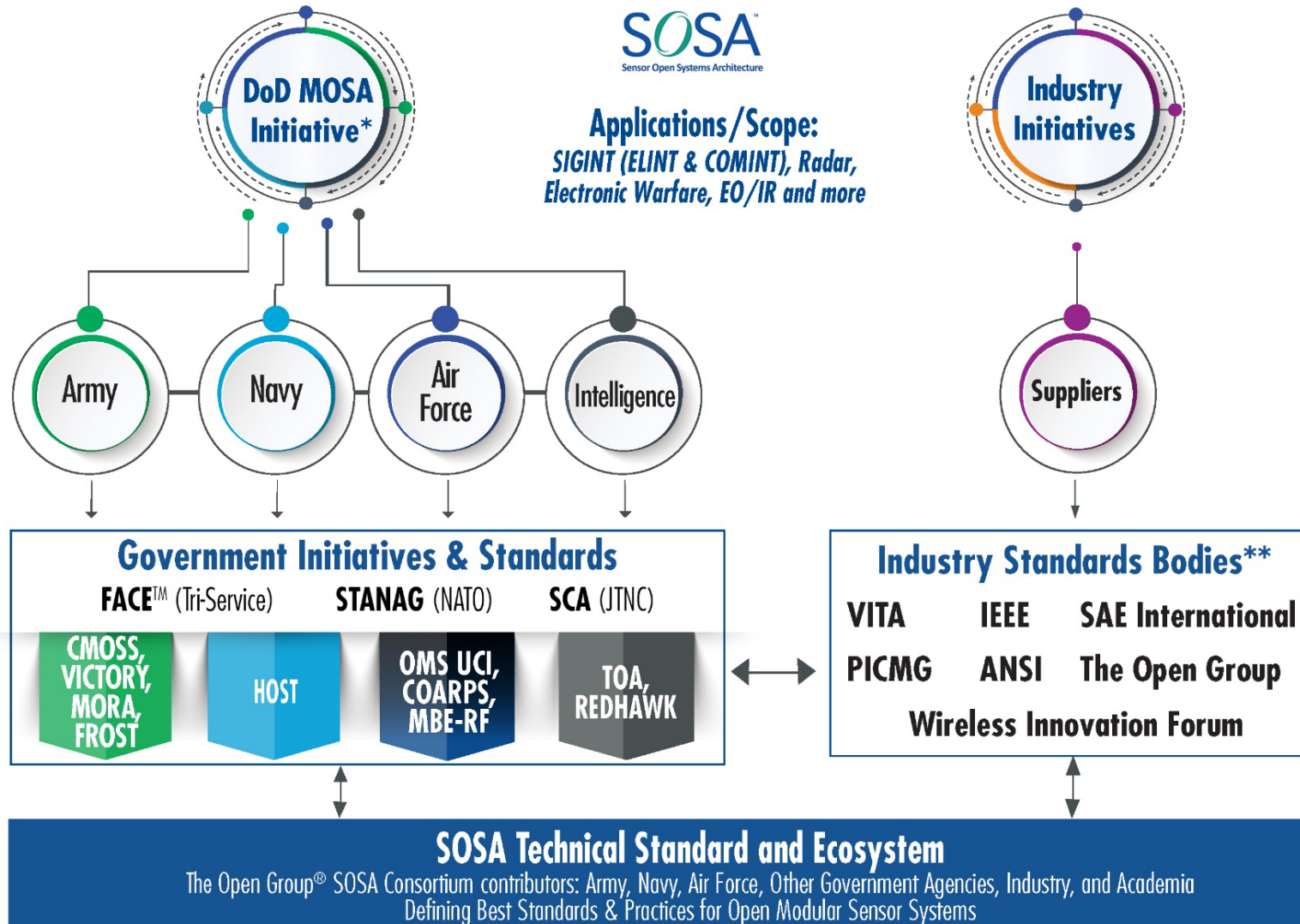
- Provide the hardware framework for developing open embedded systems for U.S. military defense systems
- Increase Interoperability and Interchangeability
- Incorporate Innovation
- Decrease Upgrade Time and Lifecycle Cost
- Improve Competition
- Promote Module Reuse

AIR FORCE SOSA™ (from SOSA Executive Overview)

- Develop a unified technical Open Systems Architecture standard for RADAR, EO/IR, SIGINT, EW, and Communications – and the supporting business models
- Improve sub-system, system, and platform affordability, re-configurability, upgradability, and hardware/software/firmware re-use – and to shorten cycle times to counter emerging threats
- “... an integrated business and technical strategy to achieve competitive and affordable acquisition and sustainment over the system life cycle”

We all have similar goals so why shouldn't we work together on a common standard? – WE ARE

SOSA™ - THE STANDARDS “MELTING POT”



The SOSA Consortium is adopting and aligning Government and Industry standards to create a common DoD-wide Open Systems Architecture standard

- Enables reuse across Services, Agencies, and Programs
- Maximizes Government investments
- Capitalizes on collective expertise of over 160 member organizations

Latest additions to the SOSA Consortium include:

- VICTORY and MORA Standards
- DEWS Reference Architecture
- New subcommittee responsible for SOSA sensors deployed in space

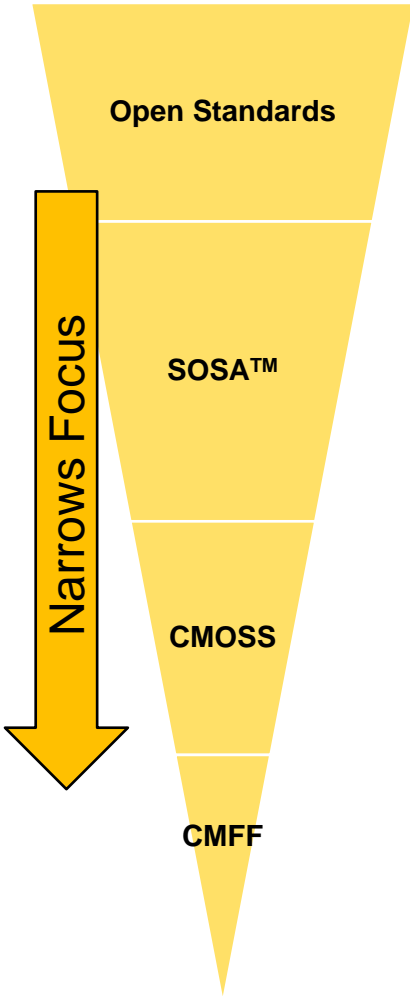
*In support of the US DoD MOSA Mandate memo.

** Representative group. Not all associated standards are listed.

LAYERED STANDARDS



Card Sizes	Slot Profile Options	Cooling	Software Run-Time Environments	System Management	C5ISR Functional Interfaces	Electrical Connector Standards	Mechanical Interface Standards	Environmental Standards
- Same as SOSA - VITA 46 - VITA 90	- 91 Profiles - VITA 65 - VITA 66.x - VITA 67.x	- SOSA+ - VITA 48.x	- FACE OSS - OCI Container - OVF VM	- VITA 46.11	- N/A	- SAE AS6129A	- SAE AS6169A - NATO	- Subset of MIL-STD-810 in VITA 47.1-3
- 3U VPX - 3U sVPX - 6U VPX - VNX+	- 33 Payload - 12 Switch - 4 PNT - 2 PS - AMPS	- 1.0" CC - 1.5" AFT - 1.0" LFT	- FACE OSS - OCI Container - OVF VM - SOSA Config Files	- VITA 46.11 Tier 3 IPMC and ChMC - SOSA In-Band System Mgmt	- SOSA EW, COMMS, SIGINT, Radar, EO/IR - VICTORY Position, Orientation, DOT - MORA	- SAE AS6129A - SOSA connectors - 40 identified	- SAE AS6169A - NATO - Leverages mounting of SAVE but not explicitly	- VITA + some ATPD-2404
- 3U VPX - 6U VPX	- 6 Payload - 4 Switch - 1 PNT - 2 PS - Reduced AMPS	- 1.0" CC - 1.5" AFT	- SCA - MMC* - FACE - Photon - Redhawk - SALVAGE - X-MIDAS	- VICTORY - MORA - VITA 46.11 Tier 3 IPMC and ChMC* - SOSA In-Band System Mgmt*	- VICTORY - MORA	- Same as SOSA	- Same as SOSA	- Same as SOSA*
- 3U VPX	- 2 Payload - 1 Switch - 1 PNT - 1 PS - Reduced AMPS	- 1.0" CC	- SCA - FACE - MMC	- VICTORY - MORA - VITA 46.11 Tier 3 IPMC and ChMC - SOSA In-Band System Mgmt	- VICTORY - MORA	- Subset of SOSA and SAVE TBD*	- SAVE	- SOSA + ATPD-2404 and AVN AQP



* = Future



WHAT'S NEXT FOR SOSA™?

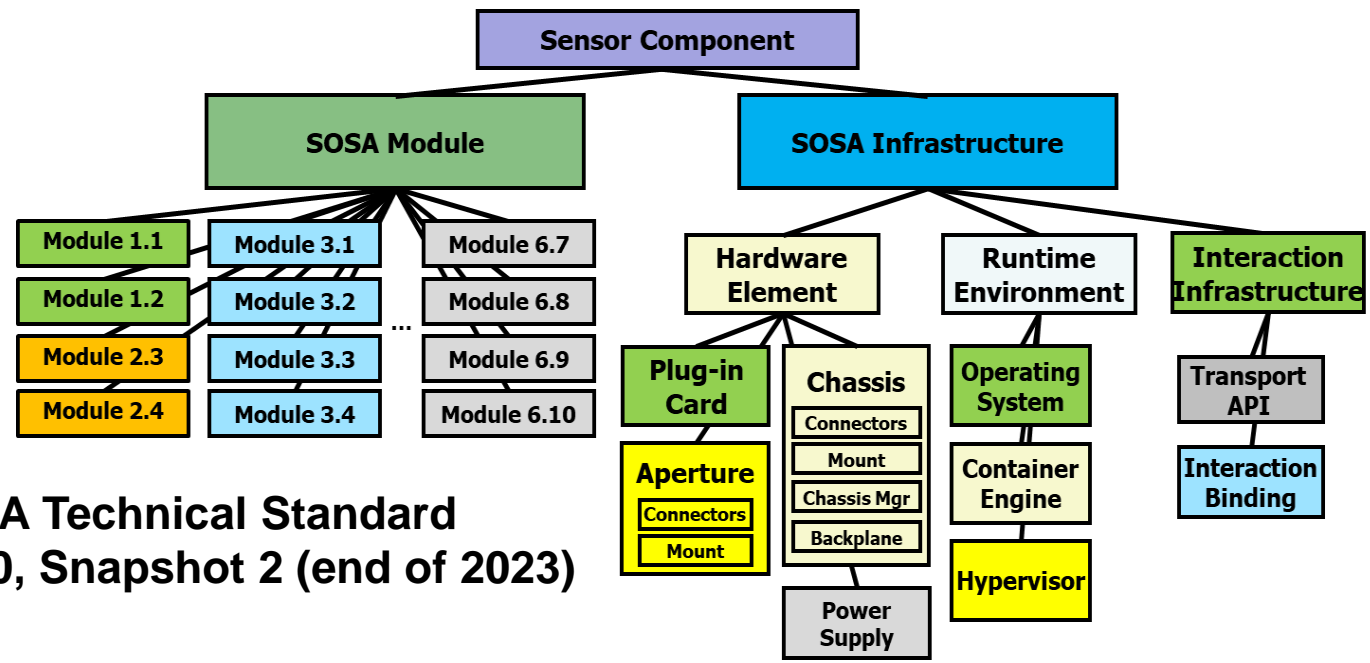
- EO/IR wide area search/surveillance
- Nav Data Service adoption of VICTORY
- Security Services definition
- Data model updates for EA, SIGINT, SAR, and EO/IR
- MORA V2.5 and VICTORY V1.10

- Additional Chassis Connectors
 - High-Speed Ethernet + Discrete Signals
 - High-Speed Ethernet
 - High-Density Fiber
 - Auxiliary
- Additional Mechanical Interfaces
 - Non-Turreted Sensor
 - Non-Turreted Antenna

- Tier 3 Intelligence Platform Management Interface (IPMI)
- Updated and Additional Plug-In Card Profiles (PICP)
 - Payload with Video
 - Timing with Signals of Opportunity (SOOP)
 - Security
 - High Density Switch
 - Enhanced environmental specifications
- Small Form Factor Additions
 - Alignment with SpaceVNX
 - Single Board Computer Slot Profile
 - Alternate Module Profile Scheme (AMPS)

- Run-Time Environment (RTE) System Management

- SOSA Data Messages (SDMs) definition



**SOSA Technical Standard
Edition 2.0, Snapshot 2 (end of 2023)**



WHAT'S NEXT FOR SOSA™?

- COMMS sensor thread
 - Encryptor/Decryptor definition
 - Digital Audio
- Extension of EO/IR sensor thread
- Nav Data Service
 - Updates for airborne community
 - Merger of Nav Data Service and Time & Frequency Service
- Tracker updates
- Security alignment with other standards

- Secure Startup updates for Zero Trust
- System Management
 - Discovery
 - Updates based on community feedback
- Data Model updates
 - EA, SIGINT, SAR, EO/IR, and COMMS sensor threads
 - System Management, Authentication, and Authorization

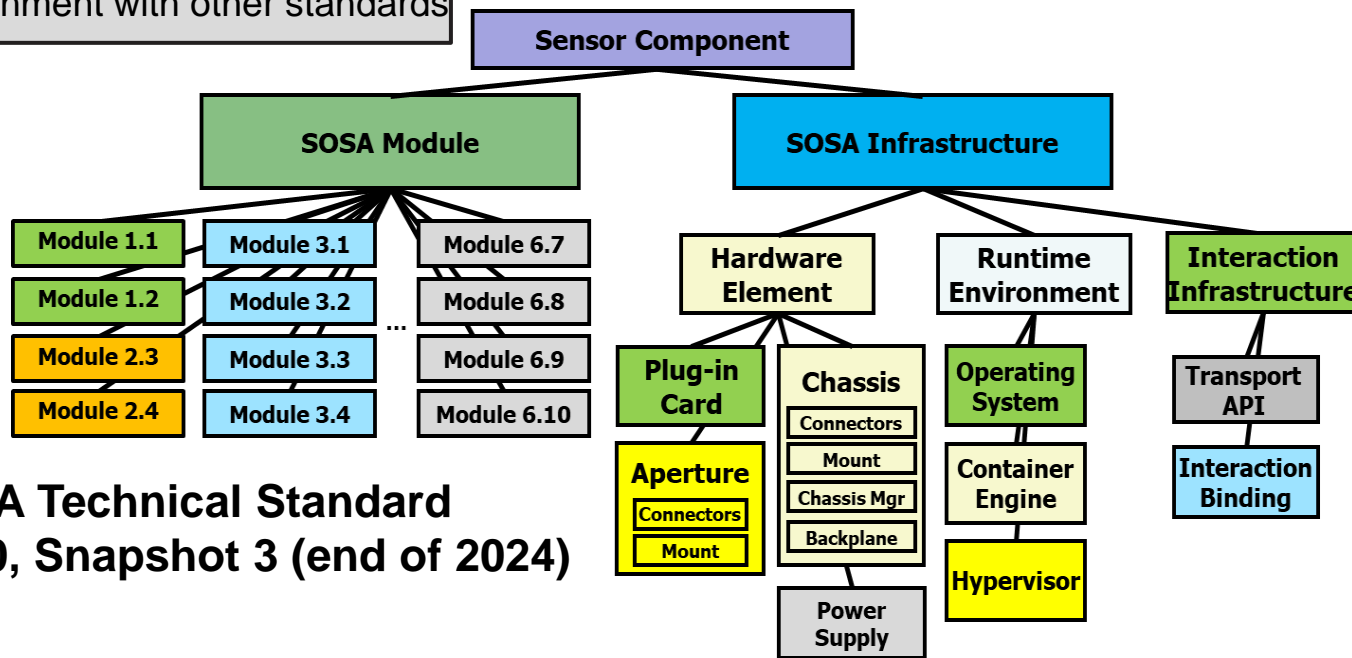
- Hardware Management Card (HMC) to contain chassis management functions
- Updated Plug-In Card Profiles (PICP)
 - Nuclear Event Detection (NED)
 - Security
 - Front-panel discrete signals
- Small Form Factor additions
 - Power Supply slots profiles
 - Video

- Signals of Opportunity (SOOP) chassis connector

- Run-Time Environments
 - Enhanced guidance for container portability
 - Initial FPGA Run-Time Environment

- Virtual Discretes
- Interaction Bindings nomenclature

- Document cleanup (SvcV-4 and Interaction tables, Security requirements, Chassis connector consolidation)



**SOSA Technical Standard
Edition 2.0, Snapshot 3 (end of 2024)**



WHAT'S NEXT FOR HOST?

- HOST 5.0/5.1 is released
- HOST 5.x model (CAMEO) based (document can be printed if desired)
 - Tier 1 and Tier 2 available (Distribution A (Public Release))
 - Tier 3 (Component Specific) Guide available
- HOST and SOSA differences paper completed and available
- Developing Verification Authority (Requirements Verification Metrics, Processes, Lab)
- Common Hardware Integration Layer (CHIL) Standard in development



ADDITIONAL INFORMATION

- **SOSA™**
 - SOSA Consortium (<https://www.opengroup.org/sosa>)
 - SOSA Technical Standard Edition 2.0, Snapshot 1
 - SOSA Reference Implementation Guide
 - SOSA Business Guide
 - SOSA Certification Program Certification Guide Version 1.0
 - SOSA Conformance Certification Program Conformance Certification Policy

- **CMOSS**
 - FY22-C5ISR-CMOSS on SAM.gov (<https://sam.gov/opp/1cc5def015a042c881e5ff7dcb35a87f/view>)
 - Joint Communications Marketplace (<https://jtnc.sites.crmforce.mil/>)
 - CMOSS Interoperability Requirements Specification (IRS) V1.1
 - VICTORY Standard Specifications V1.10
 - MORA Specification V2.5
 - MORA Training Material

- **HOST**
 - HOST (<https://host-oa.com/>)
 - Host Standard Tier 1
 - HOST Tier 2 OpenVPX Core Technology Standard
 - HOST Standard Tier 3 Specification Guide
 - HOST Tutorial

Disclaimer: Links to External Sites



SAM.gov



JCM



THANK YOU.

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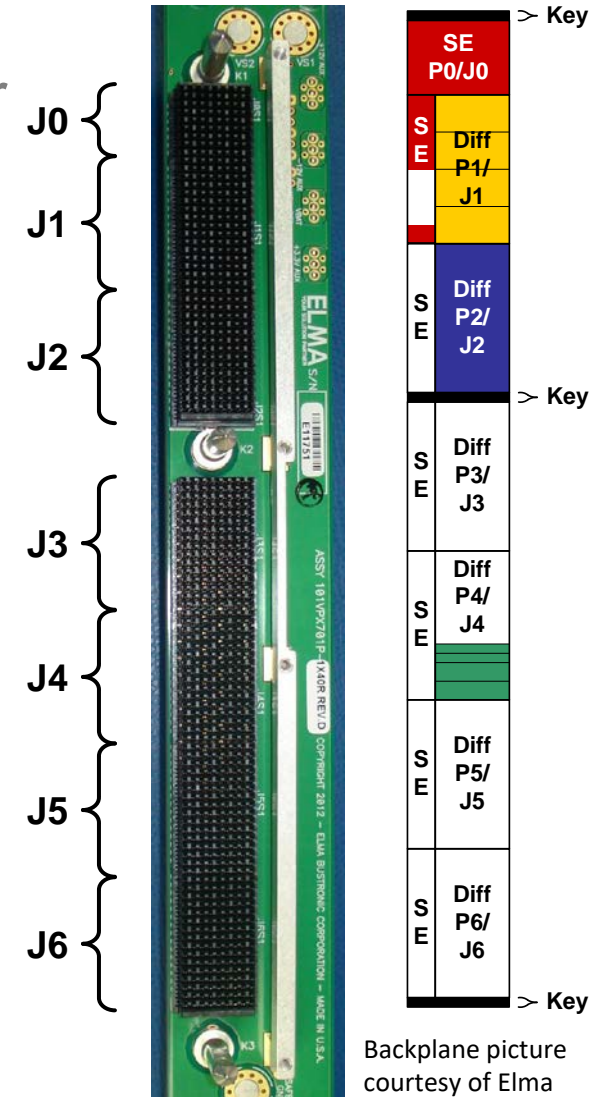




Outline

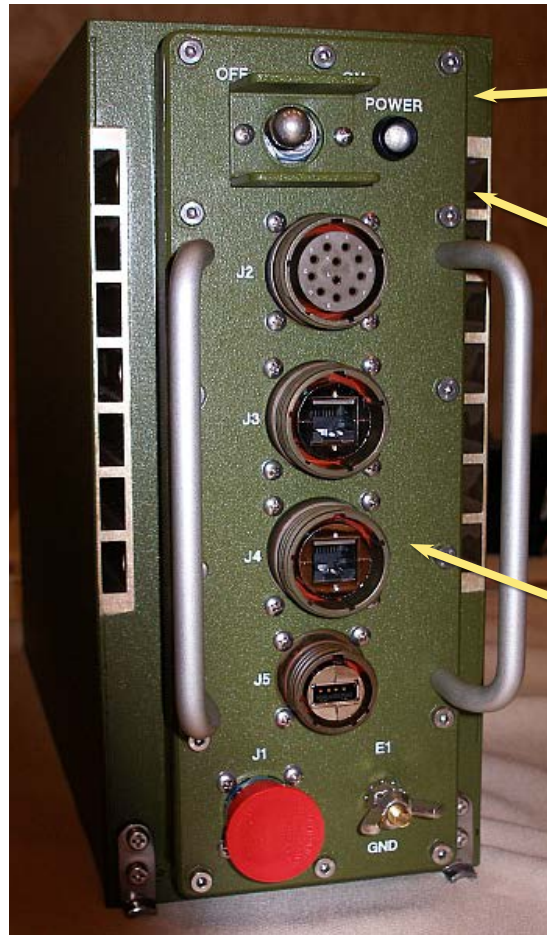
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OpenVPX and Associated Standards

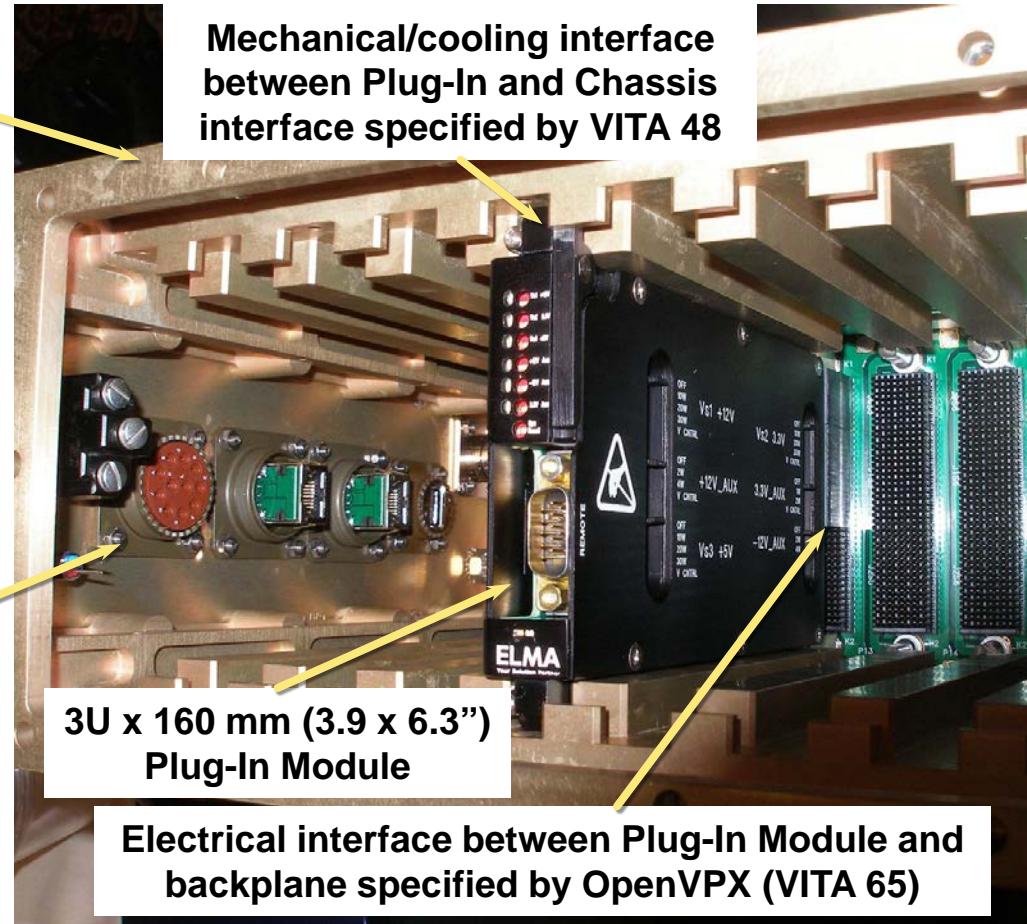


Conduction cooled chassis

Channels for cooling air

Chassis front panel

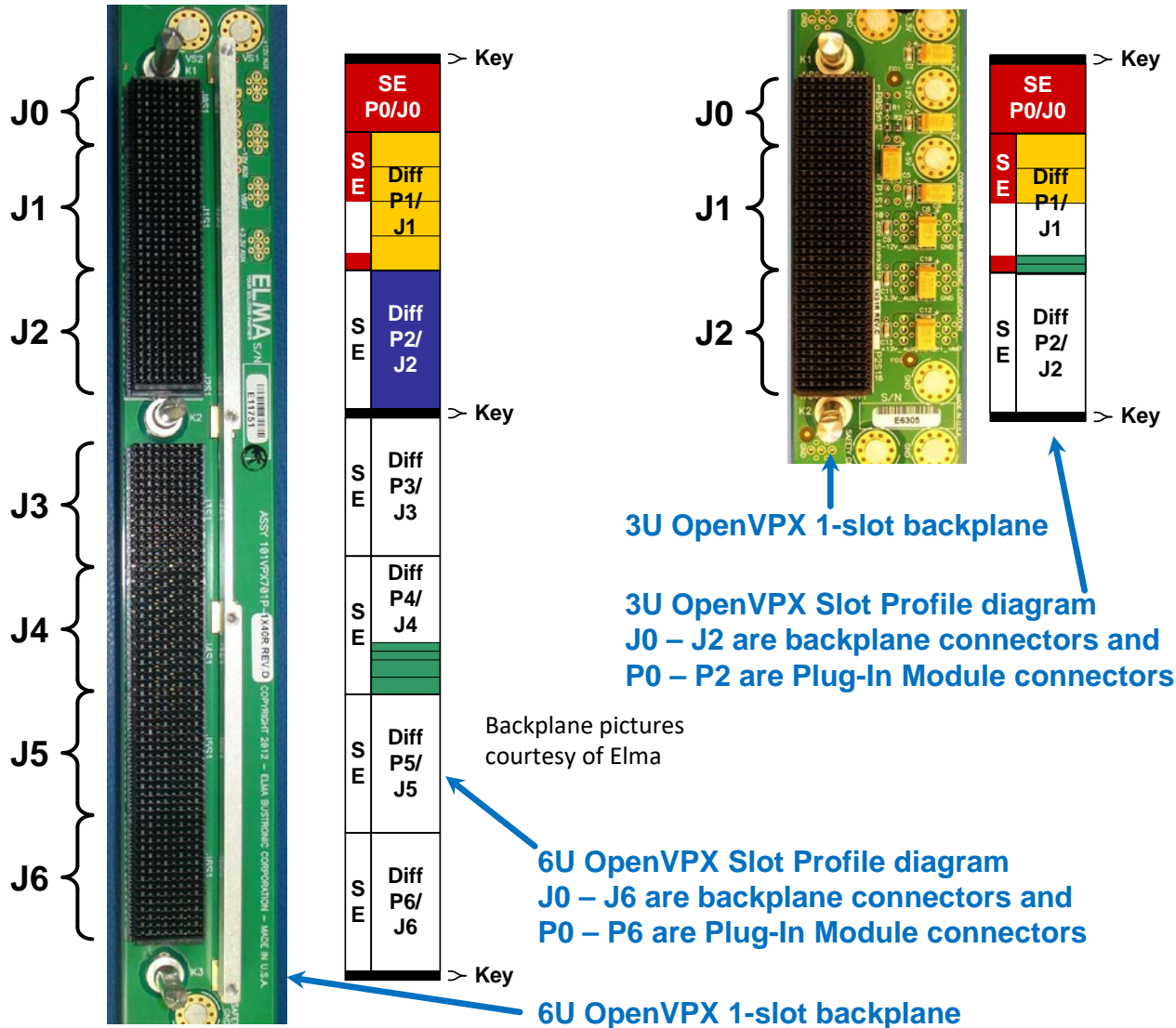
Pictures courtesy of Elma



- These standards define interfaces between Plug-In Modules and chassis for products intended to be deployed in harsh environments



OpenVPX Profiles



• Slot Profiles specify

- Pins associated with a backplane slot
- Pins associated with a Plug-In Module's backplane connector
- Pins assigned to particular ports
- Example Slot Profile name: SLT6-PAY-4F1Q2U2T-10.2.1

• Backplane Profiles specify

- Which Slot Profiles a particular backplane has
- How its Slot Profiles are interconnected
- Example Backplane Profile name: BKP6-CEN16-11.2.2-n

• Slot and Backplane Profiles are protocol agnostic

• Module Profiles specify

- The protocols to be mapped to the ports defined by the Slot Profile (e.g. 10GBASE-KR Ethernet)
- Example of Module Profile name using classic naming: MOD3p-PAY-1F1U1S1S1U1U2F1H-16.6.11-13
- Example of Module Profile name using AMPS (Alternative Module Profile Scheme) – an AMPS String: MODA3p-16.6.11-1-4-F2C-(E8-E7)(P3F-A2F)(E7)(N-G5)



VITA Standards Defining Mechanical Interface of Optical/Coax Connector Modules

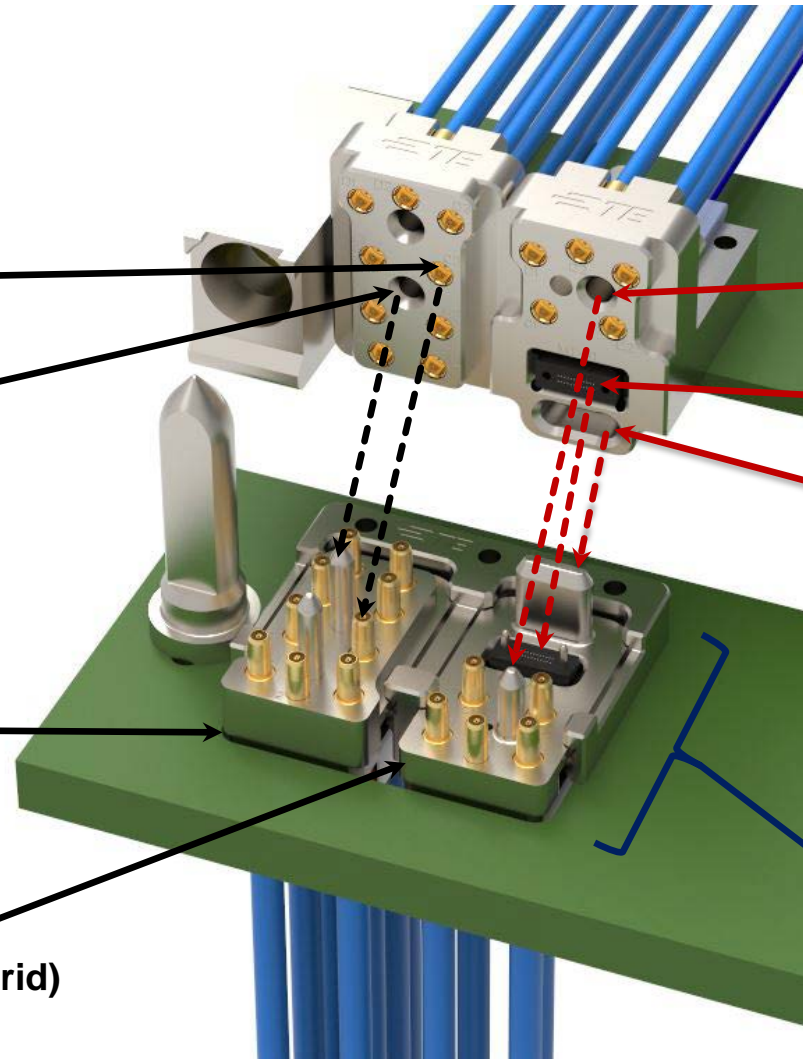
[VITA 67.3]

RF contact interface

RF Connector Module guide feature

Backplane Aperture – dimensions and location within a slot

Backplane Connector Module dimensions (RF, optical and hybrid)

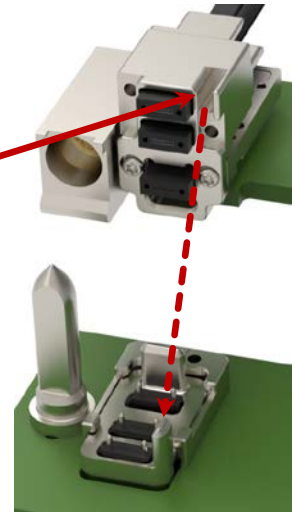


[VITA 66.5]

Secondary guide features for Optical and Hybrid Connector Modules

MT ferrule interface

Primary guide features (tab/slot) for Optical and Hybrid Connector Modules

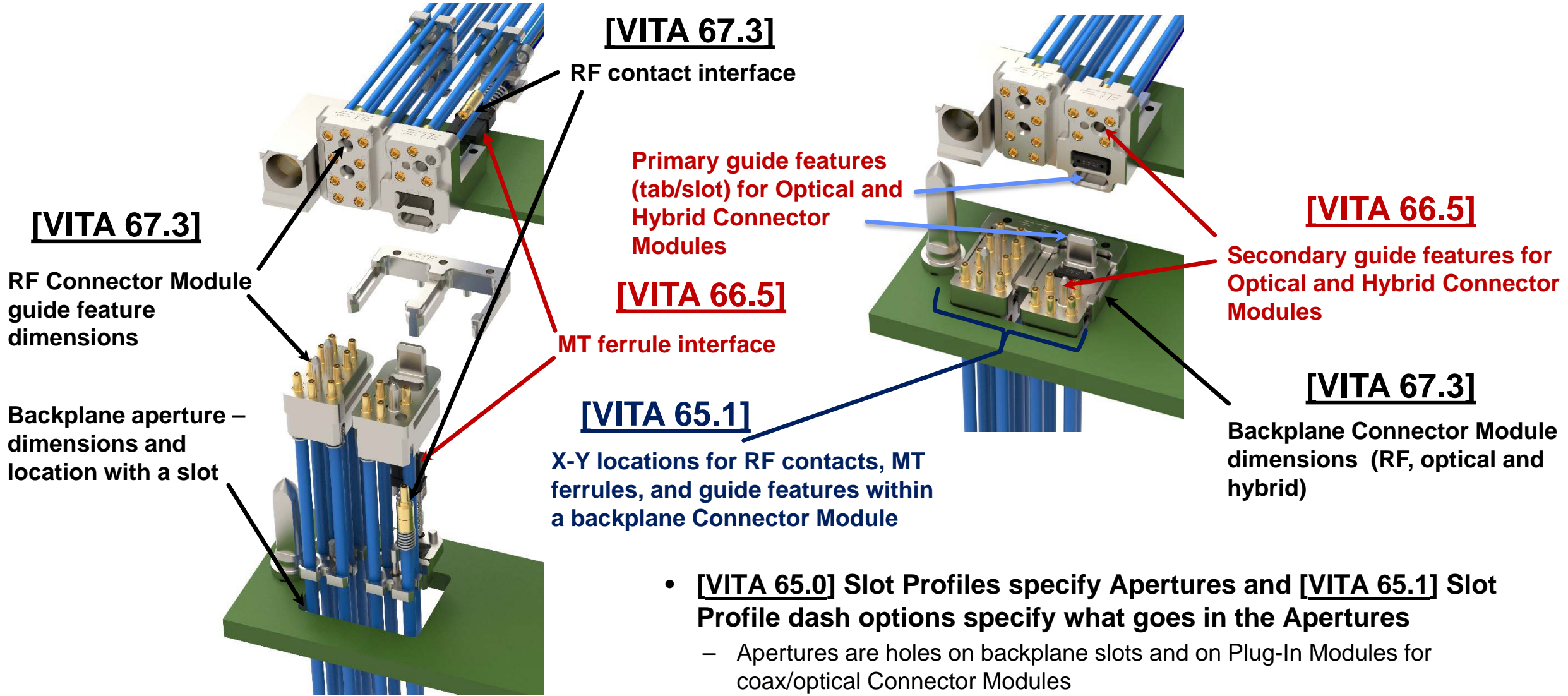


[VITA 65.1]

X-Y locations for RF contacts, MT ferrules, and guide features within a backplane Connector Module



VITA Standards Defining Mechanical Interface of Optical/Coax Connector Modules – More Detailed



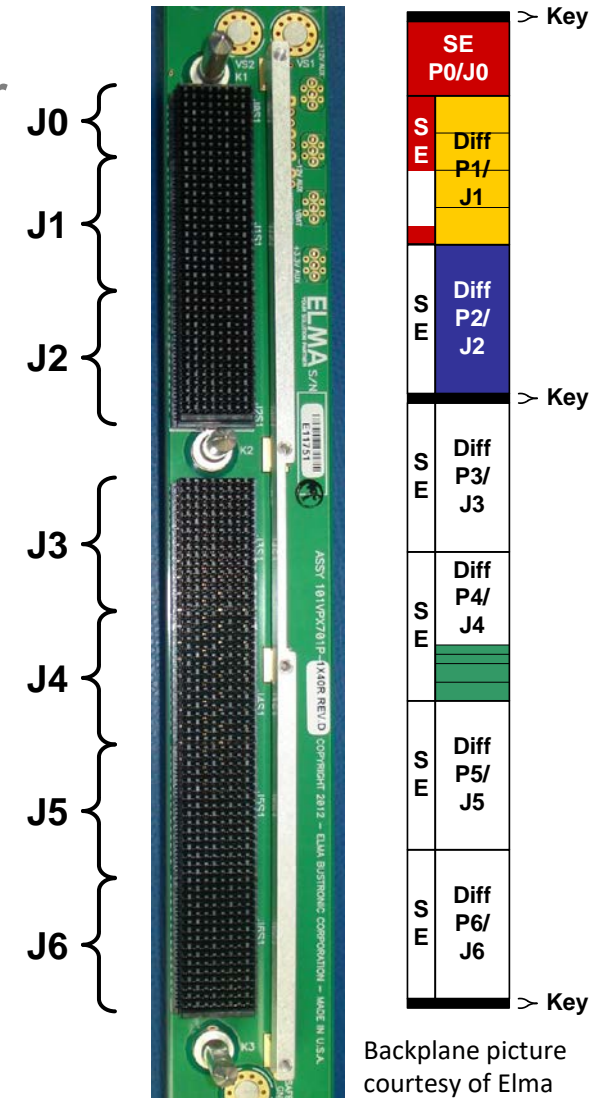
- **[VITA 65.0] Slot Profiles specify Apertures and [VITA 65.1] Slot Profile dash options specify what goes in the Apertures**
 - Apertures are holes on backplane slots and on Plug-In Modules for coax/optical Connector Modules



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Backplane picture courtesy of Elma



Relationship of OpenVPX to Other Standardization Efforts

- **For what goes into OpenVPX, continuing to get input from:**
 - VITA Member companies
 - SOSA (Sensor Open Systems Architecture) Hardware Working Group (<https://www.opengroup.org/sosa>)
 - HOST (Hardware Open Systems Technologies) community of both those working on it and those using it (<https://host-oa.com/>)
 - Army C5ISR Center's CMOSS (C4ISR/EW Modular Open Suite of Standards) Community thru their influence of SOSA
- **Also taking input from VITA 65 Working Group back to SOSA**
 - Several of us participate in both VITA and SOSA
- **In SOSA we have discussions, which are ITAR controlled, to come up with best solutions in relation to target applications**
 - The VITA Standards Organization (<https://www.vita.com/>) is international, so we cannot have discussions involving ITAR controlled and other sensitive information
- **Working to align SOSA, HOST, CMOSS and OpenVPX**
 - In terms of Slot and Module Profiles, expect SOSA, HOST, and CMOSS to continue to point at a subset of OpenVPX

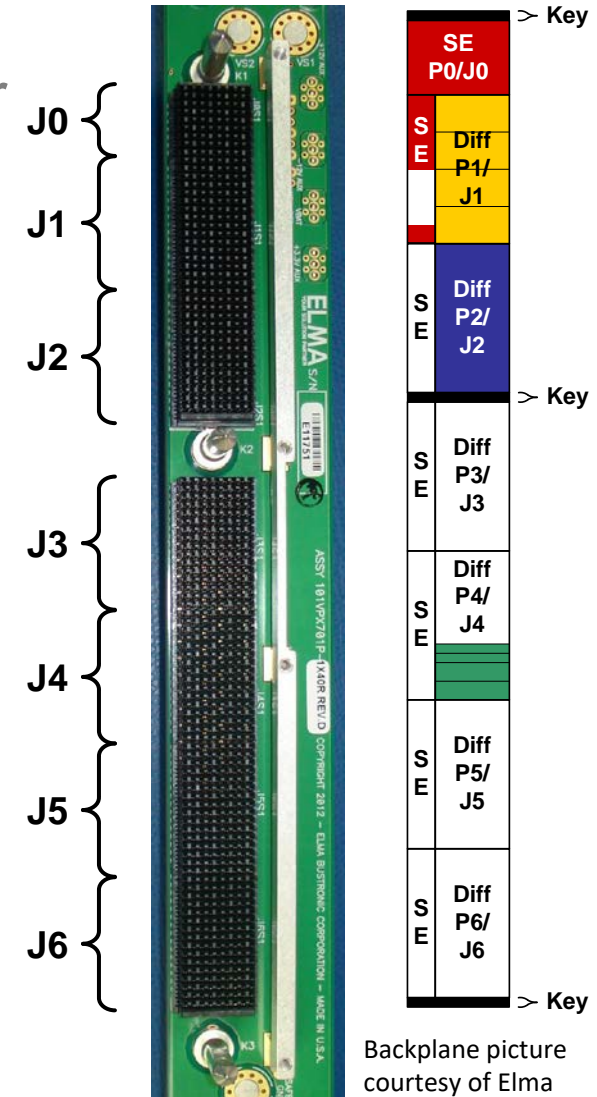




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OpenVPX Plans and Trends – Published Standards

- **Latest versions of OpenVPX™ Published June of 2023**
 - **ANSI/VITA 65.0-2023, OpenVPX™ System Standard; June 2023**
 - **ANSI/VITA 65.1-2023, OpenVPX™ System Standard – Profile Tables; May 2023**
- **ANSI/VITA 65.0-2023 and ANSI/VITA 65.1-2023 added:**
 - **2 Connector Modules to VITA 65.1, in addition to the 26 that are in ANSI/VITA 65.1-2021**
 - **Ethernet, General Purpose Electrical, Analog Video, and Digital Video protocol sections**
 - **No Slot or Backplane Profiles added with ANSI/VITA 65.0-2023, compared to:**
 - 5 new 6U and 6 new 3U Slot Profiles added with ANSI/VITA 65.0-2019
 - 1 new 6U and no new 3U Slot Profiles along with 2 new Backplane Profiles added with ANSI/VITA 65.0-2021
 - **Support for video:**
 - The 2 Connector Module added to ANSI/VITA 65.1-2023 have 75 ohm contacts
 - Added some Slot Profile dash options using the Connector Modules with 75 ohm contacts
 - Added several video protocol sections

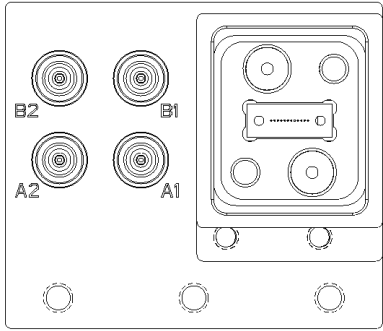


OpenVPX Plans and Trends – Work In Progress

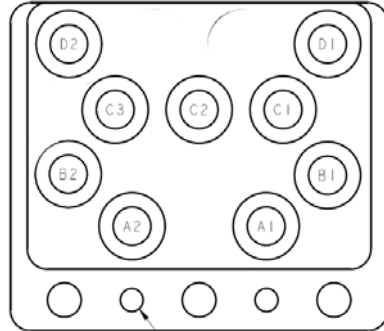
- **Working on next versions of VITA 65.0 & 65.1, expect out late 2024 or sometime in 2025, expected to add:**
 - **Protocol sections – Additional of DisplayPort 1.4**
 - **No new Slot or Backplane Profiles other than Slot Profile dash options**
 - Slot Profiles dash options (are in VITA 65.1) specify what Connector Modules go in apertures for optical/coax
 - Slot Profile dash options also specify Optical Profiles – how pipes for protocols are mapped to MTs
 - Regardless of the Slot Profile dash option, the aperture (hole) in the backplane stays the same
 - **Optical Profiles to support Single-Mode optical-fiber**
 - Slot Profile dash options that use these Optical Profiles
- **Working out what next generation VPX connectors are and how to standardize them**



Connector Modules In ANSI/VITA 65.1-2017

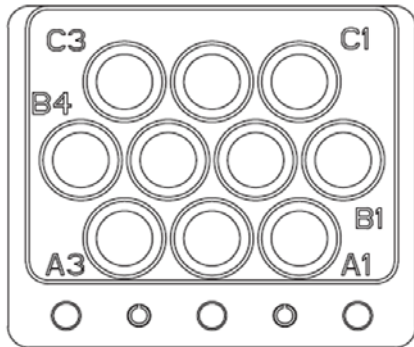


Hybrid_66.4+67.1-6.4.5.6.1

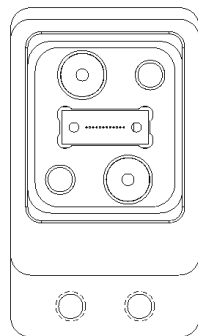


9_SMPM_contacts-6.4.5.6.2

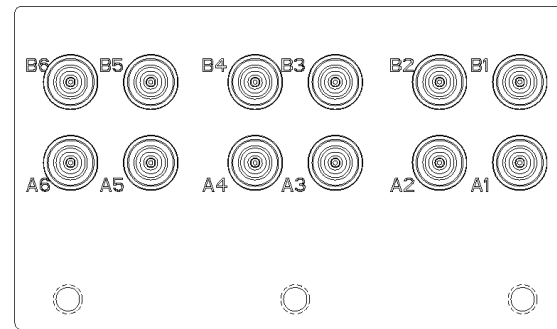
- **ANSI/VITA 65-2010 (R2012) has only two Slot Profiles with optical/coax**
 - These Slot Profiles have ANSI/VITA 67.1 Connector Modules – 4 RF contacts
 - No optical
- **ANSI/VITA 65.1-2017 was the initial version of 65.1**
 - ANSI/VITA 65-2010 and 65-2010 (R2012) have tables of Module and Backplane Profile dash options included – these moved to VITA 65.1
 - ANSI/VITA 65-2010 and 65-2010 (R2012) do not have Slot Profile dash options – added with VITA 65.1
 - OpenVPX Connector Module definitions are in VITA 65.1



10_SMPM_contacts-6.4.5.6.3



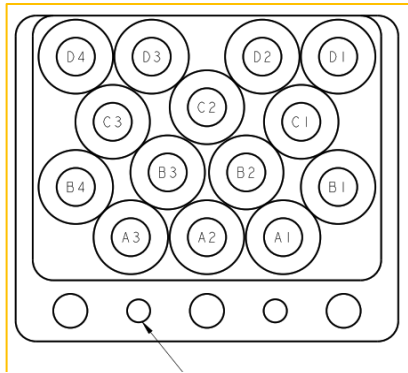
66.4_in_67.3D-6.4.5.7.1



3_of_67.1_in_67.3E-6.4.5.8.1

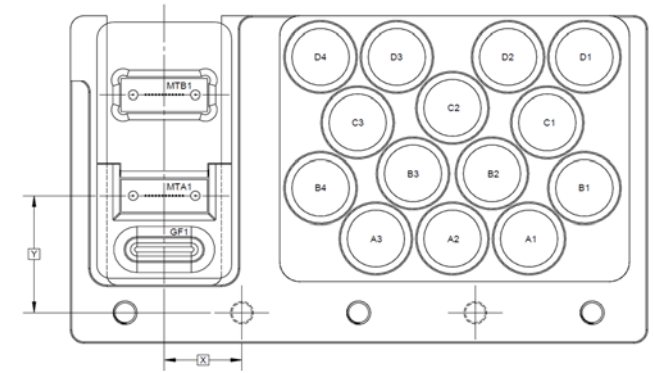


Connector Modules Added by ANSI/VITA 65.1-2019

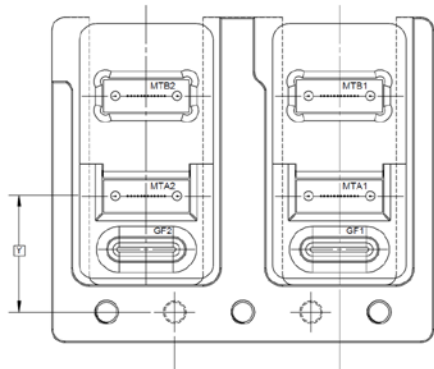


14_SMPM_contacts-6.4.5.6.4

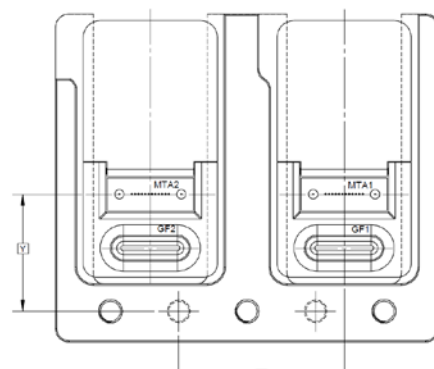
- With what is expected to be 2023 version of 65.1 all Connector Modules using ANSI/VITA 66.5-2022 Style B are not recommended for new designs
 - Style B has been superseded by Style D
 - Style B is included in ANSI/VITA 66.5-2022 to document existing designs
 - ANSI/VITA 65.1-2019 and 65.1-2021 do not include Recommendation to not use Style B in new designs



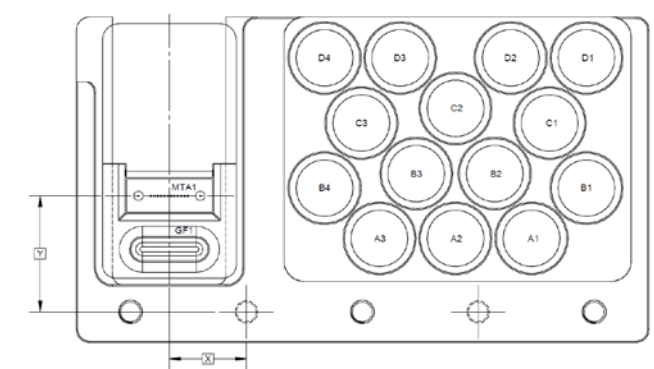
1_Style_B_66.5_insert_and_14_SMPM_contact-6.4.5.8.2
(not recommended for new designs)



2_Style_B_66.5_inserts-6.4.5.6.5
(not recommended for new designs)



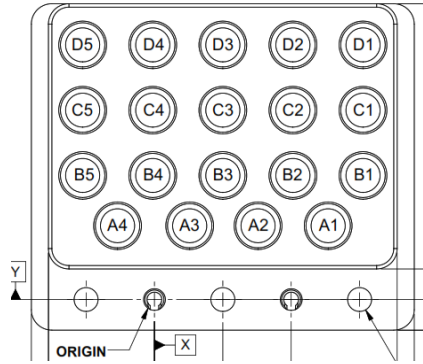
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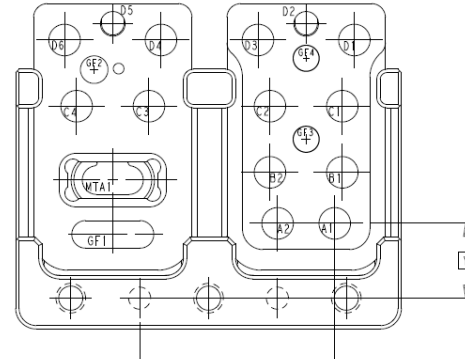
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Connector Modules Added by ANSI/VITA 65.1-2021 (1 of 3)

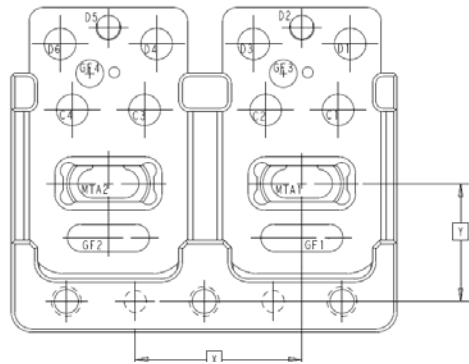


19_SMPS_contacts-6.4.5.6.7

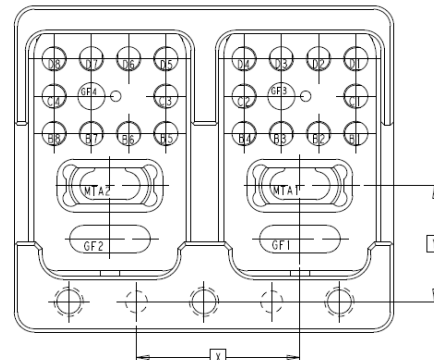


1_Style_C_insert_and_14_NanoRF_contacts-6.4.5.6.9

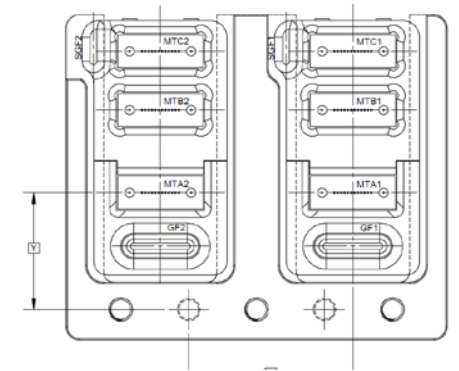
- **Addition of Connector Modules peaked with ANSI/VITA 65.1-2021**
 - 5 are in ANSI/VITA 65.1-2017
 - 5 added with ANSI/VITA 65.1-2019
 - 16 added with ANSI/VITA 65.1-2021
 - 2 added with ANSI/VITA 65.1-2023



2_Style_C_inserts_and_10_NanoRF_contacts-6.4.5.6.8



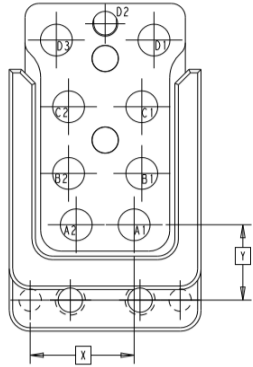
2_Style_C_inserts_and_20_NanoRF_contacts-6.4.5.6.10



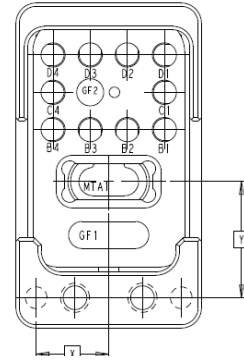
2_Style_D_inserts-6.4.5.6.11



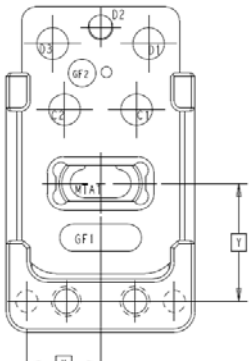
Connector Modules Added by ANSI/VITA 65.1-2021 (2 of 3)



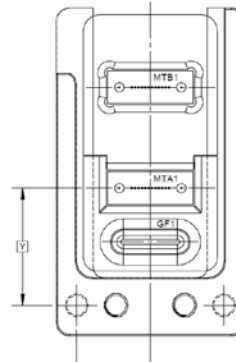
9_NanoRF_contacts-6.4.5.7.2



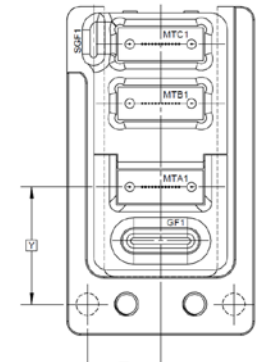
1_Style_C_insert_and_10_NanoRF_contacts-6.4.5.7.4



1_Style_C_insert_and_5_NanoRF_contacts-6.4.5.7.3



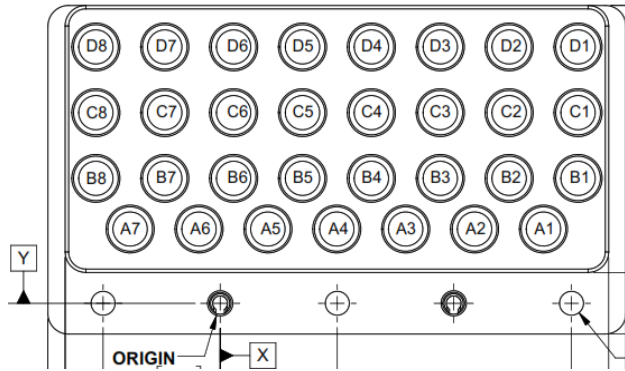
1_Style_B_insert-6.4.5.7.5
(not recommended for new designs)



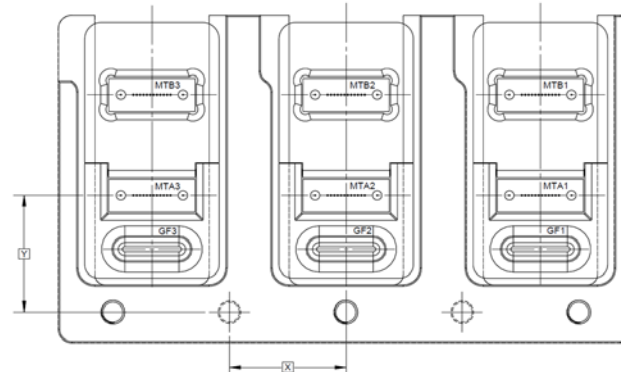
1_Style_D_insert-6.4.5.7.6



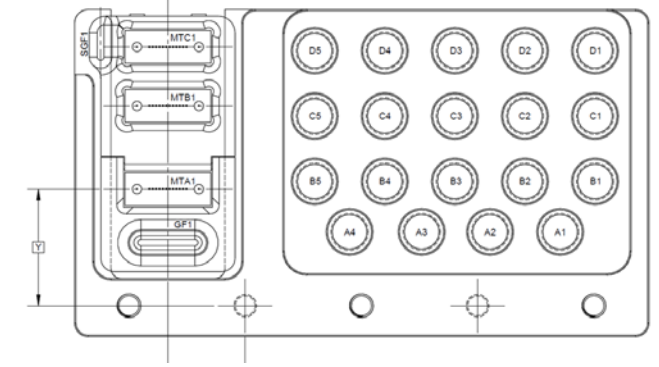
Connector Modules Added by ANSI/VITA 65.1-2021 (3 of 3)



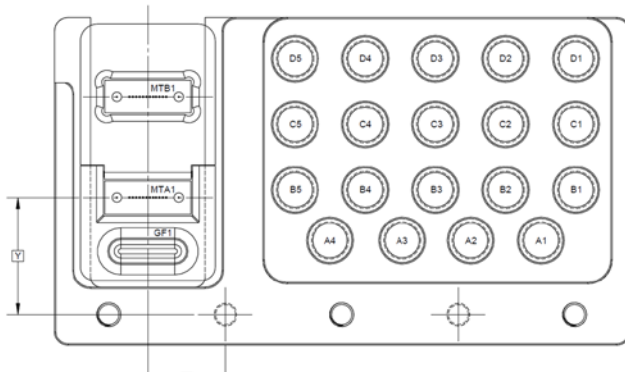
31_SMPS_contacts-6.4.5.8.4



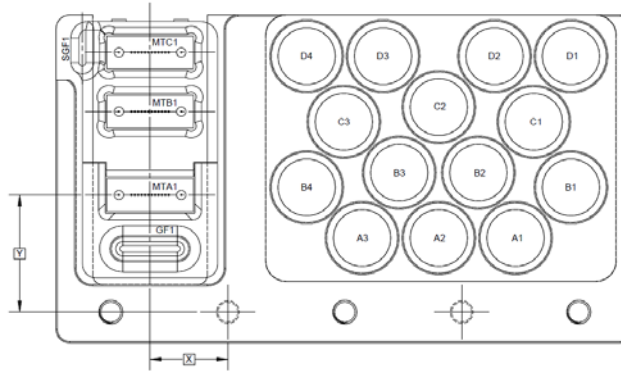
3_Style_B_inserts-6.4.5.8.6
(not recommended for new designs)



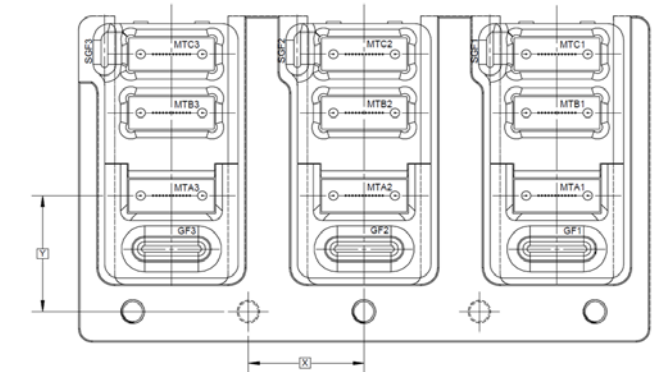
1_Style_D_insert_and_19_SMPS_contacts-6.4.5.8.8



1_Style_B_insert_and_19_SMPS_contacts-6.4.5.8.5
(not recommended for new designs)



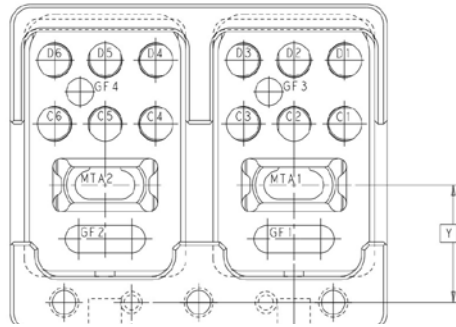
1_Style_D_insert_and_14_SMPM_contacts-6.4.5.8.7



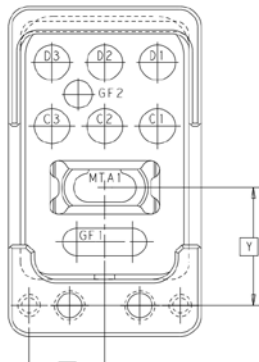
3_Style_D_inserts-6.4.5.8.9



Connector Modules Added by ANSI/VITA 65.1-2023



2_Style_C_inserts_and_12_75-OhmNanoRF_contacts-6.4.5.6.12

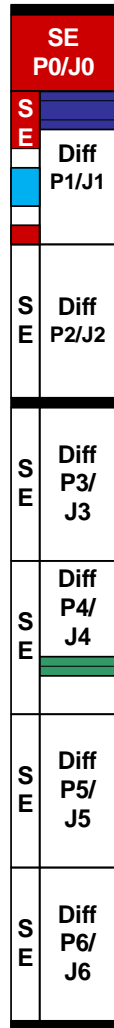


1_Style_C_insert_and_6_75-OhmNanoRF_contacts-6.4.5.7.7

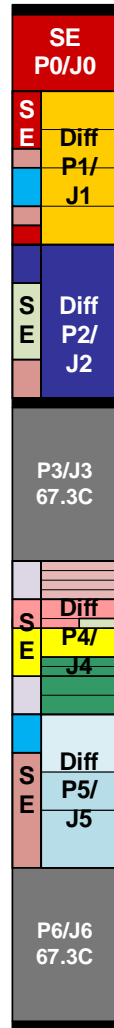
- **Adds Connector Modules with 75 ohm contacts**
 - Intended to be used with video protocols
- **Addition of Connector Modules peaked with ANSI/VITA 65.1-2021**
 - 5 are in ANSI/VITA 65.1-2017
 - 5 added with ANSI/VITA 65.1-2019
 - 16 added with ANSI/VITA 65.1-2021
 - 2 added with ANSI/VITA 65.1-2023



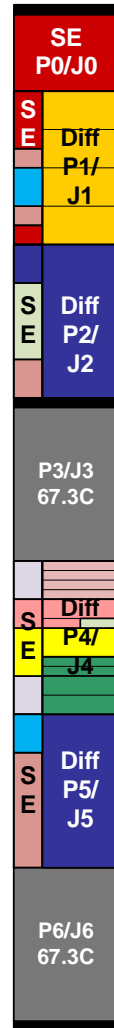
6U Slot Profiles Added by ANSI/VITA 65.0-2019



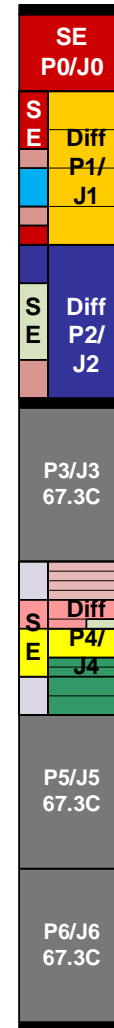
SLT6-PAY-4U2U-10.2.8



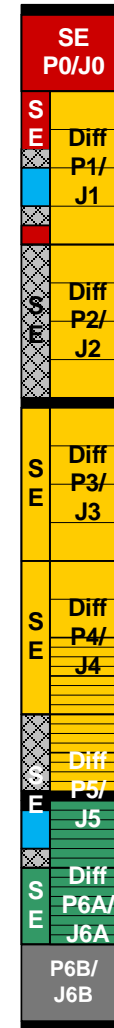
SLT6-PAY-...-10.6.3-n



SLT6-PAY-...-10.6.4-n



SLT6-PAY-...-10.6.5-n



SLT6-SWH-...-10.8.1

- Module Profiles for these Slot Profiles only use the following for power from the backplane:
 - 12 VDC (VS1 and VS2)
 - 3.3V_AUX
 - VBAT
- SLT6-PAY-4U2U-10.2.8 is the only one of these with UD (User Defined) pins
- No new Backplane Profiles added with ANSI/VITA 65.0-2019



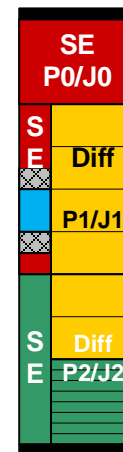
3U Slot Profiles Added by ANSI/VITA 65.0-2019



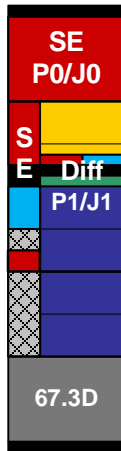
SLT3-PAY-14.2.16



SLT3-PAY-2U2U-14.2.17



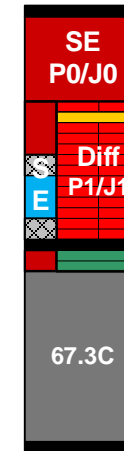
SLT3-SWH-6F8U-14.4.15



SLT3-PAY-14.6.13



SLT3-PAY-14.6.14

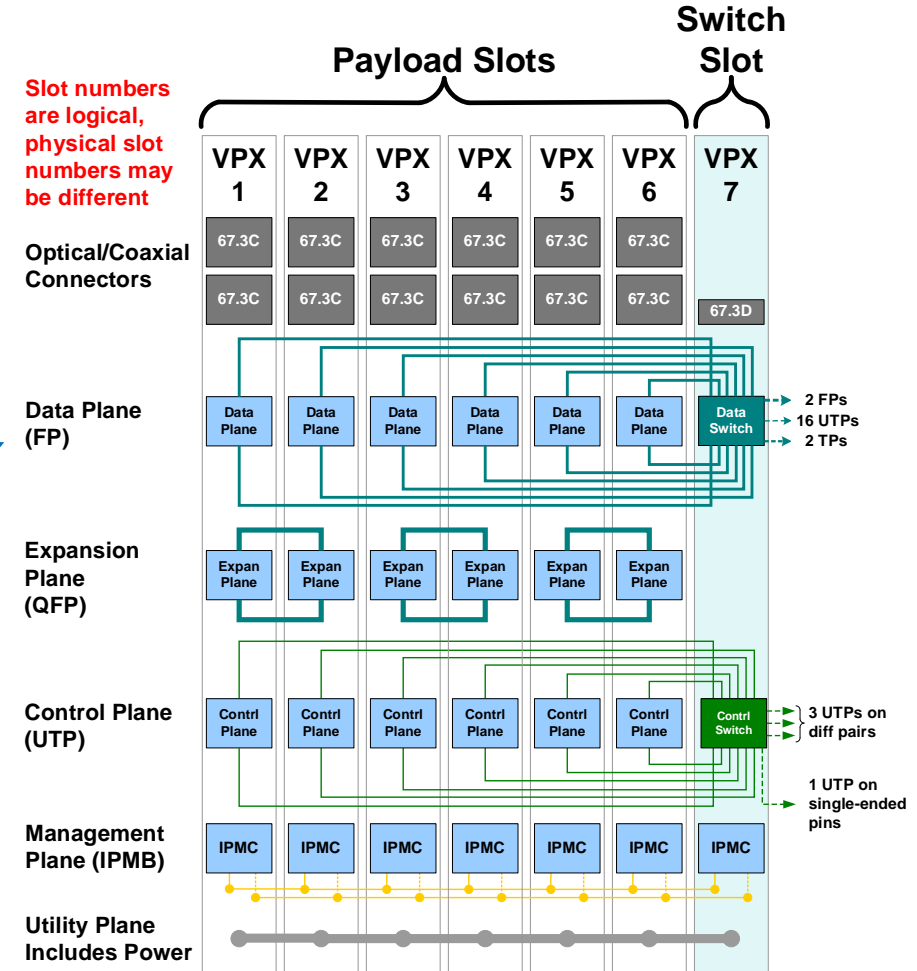
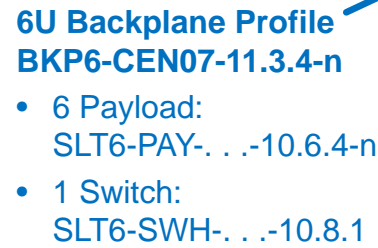
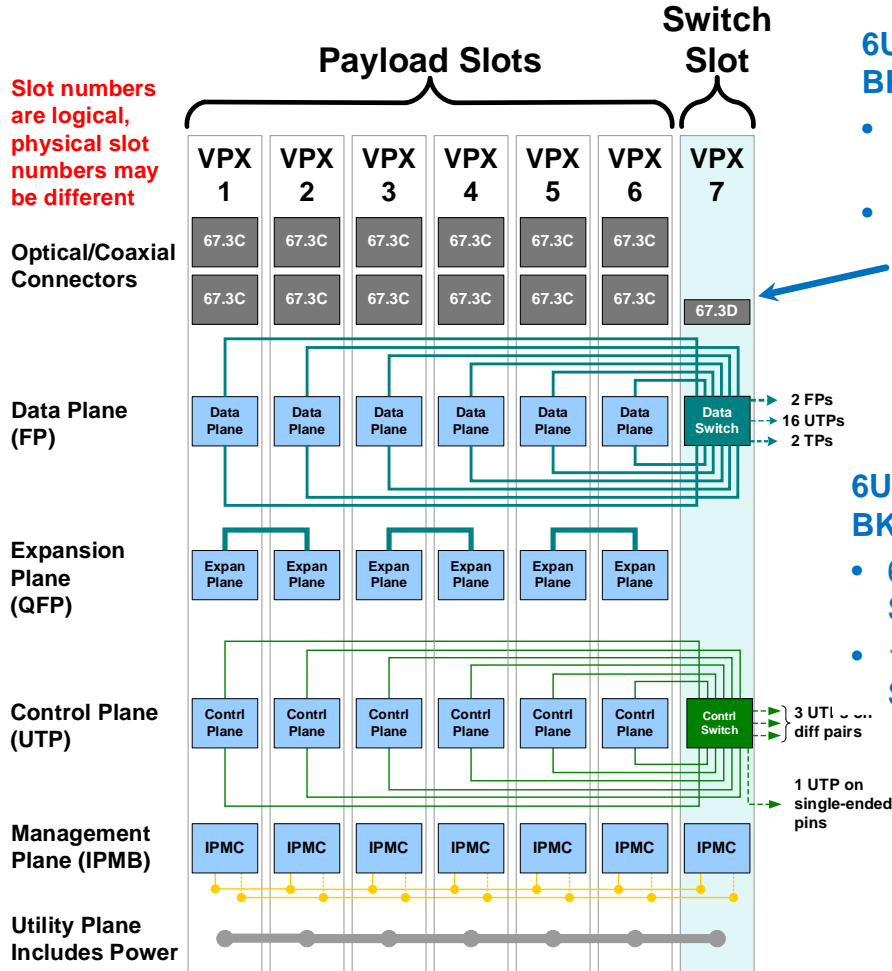
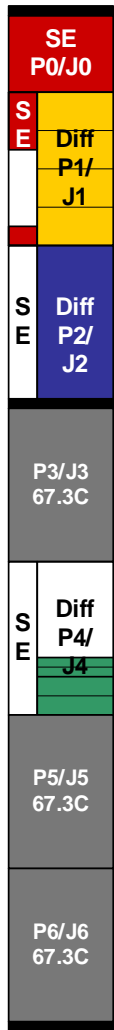


SLT3-PAY-14.9.2

- Module Profiles for these Slot Profiles only use the following for power from the backplane:
 - 12 VDC (VS1)
 - 3.3V_AUX
 - VBAT
- SLT3-PAY-2U2U-14.2.17 is the only one of these with UD (User Defined) pins



Slot and Backplane Profiles Added with ANSI/VITA 65.0-2021



SLT6-PAY-...-10.6.6

- 65.0-2021 added only one new Slot Profile and two Backplane Profiles other than dash options added to 65.1-2021
- 65.0-2023 did not add any Slot or Backplane Profiles other than Slot Profile dash options added to 65.1-2023



Protocol Sections Added With ANSI/VITA 65.0-2019 (1 of 2)

- **Ethernet sections added**
 - **5.1.14** 100BASE-TX (0.125 Gbaud Signaling)
 - **5.1.15** 25GBASE-KR (25.78125 Gbaud Signaling)
 - **5.1.16** 25GBASE-KR-S (25.78125 Gbaud Signaling)
 - **5.1.17** 25GBASE-SR (25.78125 Gbaud Signaling Over Multimode Optical Fiber)
 - **5.1.18** 100GBASE-KR4 (25.78125 Gbaud Signaling)
 - **5.1.19** 100GBASE-SR4 (25.78125 Gbaud Signaling Over Multimode Optical Fiber)
- **InfiniBand section added**
 - **5.4.6** InfiniBand EDR (25.78125 Gbaud Signaling)



Protocol Sections Added With ANSI/VITA 65.0-2019 (2 of 2)

- **5.9 USB (Universal Serial Bus)**
 - **5.9.1** High-Speed USB 2 (0.480 Gbaud Signaling)
 - **5.9.2** SuperSpeed USB 3 Gen 1 (5 Gbaud Signaling)
 - **5.9.3** SuperSpeed USB 3 Gen 2 (10 Gbaud Signaling)
- **5.13 General purpose serial ports**
 - **5.13.1** Asynchronous Serial Ports [TIA-422] and [TIA-232] (at least up to 115,200 baud)
 - **5.13.2** Asynchronous Serial Ports with LVCMOS Levels (at least up to 115,200 baud)
- **5.14 Signals Over Coax**
 - **5.14.1** Digital Over coax – Analog Levels
 - **5.14.2** Digital Over coax – CMOS/TTL levels
 - **5.14.3** GPS Antenna Input
- **5.15 General purpose electrical**
 - **5.15.1** GPIO – Single-Ended General Purpose I/O
 - **5.15.2** GPLVDS – Differential General Purpose I/O



Protocol Sections Added With ANSI/VITA 65.0-2021

- **Ethernet sections added**
 - **5.1.20** 50GBASE-KR2 (25.78125 Gbaud Signaling)
 - **5.1.21** 50GBASE-SR2 (25.78125 Gbaud Signaling Over Multi-Mode Optical Fiber)
- **Aurora sections added**
 - **5.7.3** Aurora with 64B/66B Encoding (up to 10.3125 Gbaud Signaling)
 - **5.7.4** Aurora with 64B/66B Encoding (up to 25.78125 Gbaud Signaling)
 - **5.7.5** Aurora with 64B/66B Encoding (up to 10.3125 Gbaud Signaling Over Multi-Mode Optical Fiber)
 - **5.7.6** Aurora with 64B/66B Encoding (up to 25.78125 Gbaud Signaling Over Multi-Mode Optical Fiber)
- **General purpose serial port sections added**
 - **5.13.3** Asynchronous Serial Ports [TIA-232]
 - **5.13.4** Asynchronous Serial Ports [TIA-422]
 - **5.13.5** Asynchronous Serial Ports [TIA-485]
- **General purpose electrical sections added**
 - **5.15.3** [TIA-485] Higher-voltage, Differential, Bi-Directional General Purpose I/O
 - **5.15.4** [TIA-422] Higher-voltage, lower-speed Differential General Purpose I/O
 - **5.15.5** CLK – Electrical requirements of radial clocks



Non-Video Protocol Sections Added With ANSI/VITA 65.0-2023

- **Ethernet sections added**
 - **5.1.22** 50GBASE-KR – (26.5625 Gbaud, PAM4 Signaling)
 - **5.1.23** 100GBASE-KR2 – (26.5625 Gbaud, PAM4 Signaling)
 - **5.1.24** 200GBASE-KR4 – (26.5625 Gbaud, PAM4 Signaling)
 - **5.1.25** 400GBASE-KR8 – (26.5625 Gbaud, PAM4 Signaling)
- **5.16 Serial Front Panel Data Port (sFPDP)**
 - **5.16.1** sFPDP with 8B/10B Encoding (up to 10.3125 Gbaud Signaling)
 - **5.16.2** sFPDP with 8B/10B Encoding (up to 10.3125 Gbaud Signaling Over Multi-Mode Optical Fiber)
 - **5.16.3** sFPDP with 64B/67B Encoding (up to 10.3125 Gbaud Signaling)
 - **5.16.4** sFPDP with 64B/67B Encoding (up to 25.78125 Gbaud Signaling)
 - **5.16.5** sFPDP with 64B/67B Encoding (up to 10.3125 Gbaud Signaling Over Multi-Mode Optical Fiber)
 - **5.16.6** sFPDP with 64B/67B Encoding (up to 25.78125 Gbaud Signaling Over Multi-Mode Optical Fiber)
- **General purpose electrical sections added**
 - **5.15.6** LVGPIO – Single-Ended General Purpose I/O
 - **5.15.7** GPLVDS15 – Differential General Purpose I/O Using 1.5V Logic



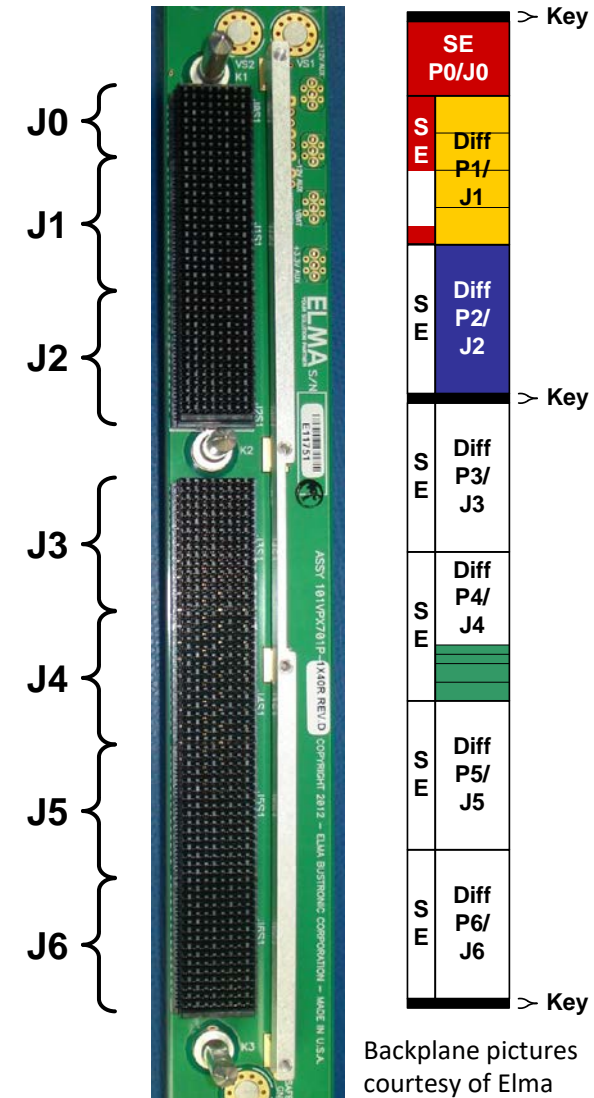
Video Protocol Sections Added With ANSI/VITA 65.0-2023

- **5.17 Composite Video Baseband Signal (CVBS)**
 - 5.17.1 National Television System Committee (NTSC)
- **5.18 Analog Video for Aircraft System**
 - 5.18.1 STANAG 3350 Class A – 875 lines, 60 Hz field frequency
 - 5.18.2 STANAG 3350 Class B – 625 lines, 50 Hz field frequency
 - 5.18.2 STANAG 3350 Class C – 525 lines, 60 Hz field frequency
- **5.19 Video Signal/Data Serial Interface (SDI)**
 - 5.19.1 High-Definition Serial Digital Interface (HD-SDI) . . . 5.19.4 12 Gbit/s Serial Data Interface (12G-SDI)
- **5.20 CoaXPress**
 - 5.20.1 CoaXPress CXP-1 – 1.250 Gbits/s . . . 5.20.7 CoaXPress CXP-12 – 12.500 Gbits/s
- **5.21 Avionics Digital Video Bus (ADVB)**
 - 5.21.1 ADVB At a Bit Rate of 1.0625 Gbit/s with 8B/10B encoding
 - . . .
 - 5.21.16 ADVB with 256B/257B encoding with 28.0500 Gbaud signaling



Summary

- **VITA, SOSA, HOST, and CMOSS communities giving input for revisions of OpenVPX standards**
- **ANSI/VITA 65.0-2023 and 65.1-2023 were published June 2023**
 - Added 2 Connector Modules with 75 ohm contacts to support video
 - Added more protocol sections including sections for both analog and digital video
 - No new Slot or Backplane Profiles other than additional dash options
- **With version of VITA 65.0 & 65.1, expected out early late 2024 or sometime 2025**
 - Optical Profiles to support Single-Mode optical fiber
 - Slot Profile dash options using these Optical Profiles
- **Starting with ANSI/VITA 65.1-2023 activity to add optical/coax Connector Modules has decreased**
- **Since 2019 only 1 new Slot Profile and 2 new Backplane Profiles added in 2021**
 - With ANSI/VITA 65.0-2023 and ANSI/VITA 65.1-2023, no new Slot or Backplane Profiles added, other than Slot Profile dash options



Backplane pictures courtesy of Elma