

# DEVICE PERFORMANCES AND PARAMETRIC STUDIES OF HIGH ENERGY IMPLANTATIONS WITH MULTIPLE CHARGED ION BEAMS

André GROUILLET<sup>a</sup>, Gerhard GÖLTZ<sup>a</sup>, Peter VAN DER MEULEN<sup>b</sup>, Sandeep MEHTA<sup>b</sup>

<sup>a</sup>Centre National d'Etudes des Télécommunications, Grenoble, FRANCE

<sup>b</sup>Varian Ion Implant Systems, Gloucester, MA01945, USA

Density of integration and latch-up properties of sub micron CMOS devices can be improved by a high energy retrograde well implant. The energy of the p-well implant (using Boron) remains in the easily accessible range of  $\leq 200$  keV. The typical energy for the n-well implant (using Phosphorus) is in the range  $\leq 1$  MeV. Traditionally, this application requires a specific high energy implanter. It is a challenge to extend the energy range of an existing medium current implanter to the high energy range and to compare its performance with a high energy implanter optimized for beam purity.

Studies with triple charged Phosphorus ions have been performed with the new Varian E500 ion implanter. In this paper, results concerning vacuum and beam purity will be presented and discussed. Furthermore electrical results of retrograde well implants performed with the E500 (at energies  $\leq 750$  keV) in a  $0.5 \mu\text{m}$  CMOS process will be compared with results obtained in a conventional high energy implanter. The key features of the E500 that extend the performance of the E220 implanter and distinguish it from other medium current implanters, will also be discussed.

## 1. INTRODUCTION

### 1.1. High energy implantations in CMOS

High energy ion implantation technology is being used for  $1 \mu\text{m}$  design rule based masks in ROMs, 16 Mbit DRAMs, and in CCD device technology. Other applications are in bipolar  $0.5 \mu\text{m}$  devices, where the use of high energy implants leads to higher switching speeds. The application of high energy implants in  $0.5 \mu\text{m}$  CMOS has led to quality improvements and cost reductions by eliminating masking steps [1].

In CMOS, the objective is to realize PMOS and NMOS transistors side by side on the same substrate, with a minimal number of processing steps. It is therefore necessary that microscopic regions exist in the substrate of opposite doping type for the complementary transistors. These regions are called n- or p-wells, depending on the type of the majority carrier (Fig. 1).

But other than just the difference in doping type, the substrate and the wells, and the wells themselves, have to be electrically isolated from each other, even when the devices are in active operation. The different device geometries that achieve this goal also have to prevent parasitic bipolar effects in the horizontal and vertical directions ("latch-up").

There are several geometries that achieve these goals: simple or double ("twin-tub") well structures of n- or p-type, that can be created by either diffusion or ion implantation. In the later case a high implantation energy creates an inversed doping profile ("retrograde wells"). The retrograde wells present a series of important advantages over conventional diffused wells such as: higher integration densities (compare the  $8\text{-}9 \mu\text{m}$  n+ to p+ distance for diffused wells to the  $4\text{-}6 \mu\text{m}$  in a retrograde well, Fig. 1), better latch-up protection, better lateral device isolation, and better control over the active device region [2].

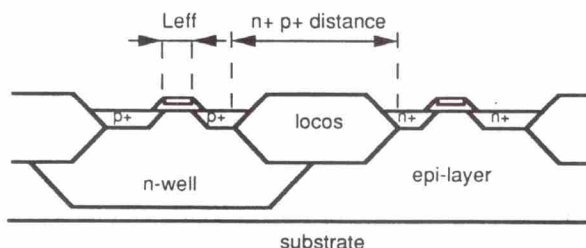


Fig. 1. Schematic of a CMOS n-well structure showing the definition of  $L_{\text{eff}}$  and the n+ to p+ distance.

In figure 2, we have shown that the difference between an implantation of Phosphorus single charged  $1e13$ , 400 keV (on a high energy machine) compared to the same implant using double charged or triple charged ions on the Varian E500 leads to

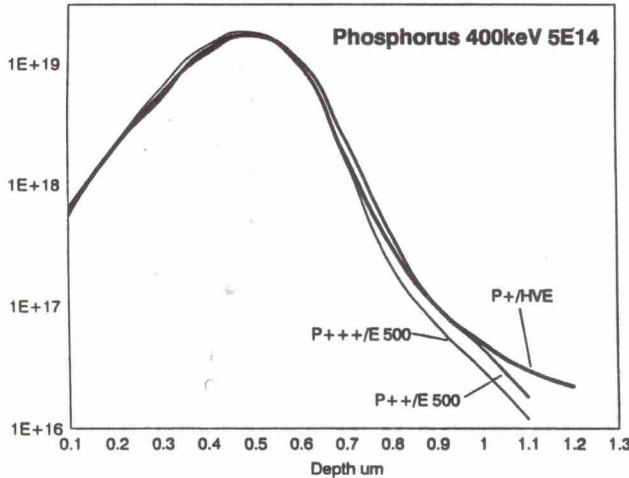


Fig. 2. Comparison of  $P^+(a)$ ,  $P^{++}(b)$  and  $P^{+++}(c)$  implants on the HVE 500 and the E500.

essentially the same depth profile, within the limits of accuracy of the SIMS measurement technique.

## 2.2. Vacuum- and beam performance

The improved performance of the E500 vacuum system is shown in figure 3. Profile (a) shows the result of the older E220 system. Profile (b) shows the identical implant on the E500 system. The higher extraction voltage and the presence of the 240 l/s resolving aperture turbo pump make a clear difference in the profile close to the surface, where energy contamination is expected. The higher extraction voltage results in a lower cross-section for charge exchange, and the lower pressure in the resolving aperture region reduces the chance of collisions with residual gas molecules in the beam line of the implanter. As compared to the E500 the E220 SIMS profile (Fig. 3, curve a) shows a contamination dose of 8%.

The contamination level on the E500 is believed to be below detection capabilities of SIMS analysis if compared to a single charged implant on the E500, as was demonstrated before in fig. 2.

Although Varian specifies a triple charged beam current of 10  $\mu A$ , it has been found that the actual

beam current varies with filament life to well above the specified limit. The specified beam current exists only during the first few hours of operation, after which it steadily increases to about 24  $\mu A$ . This means that implant time in production of a  $1e13$  dose in a 100 mm wafer takes on the average 2.5 min., compared to 6 min. if only 10  $\mu A$  were available; this compares quite favorably with the implant time of 8 min. necessary with the HVE 500.

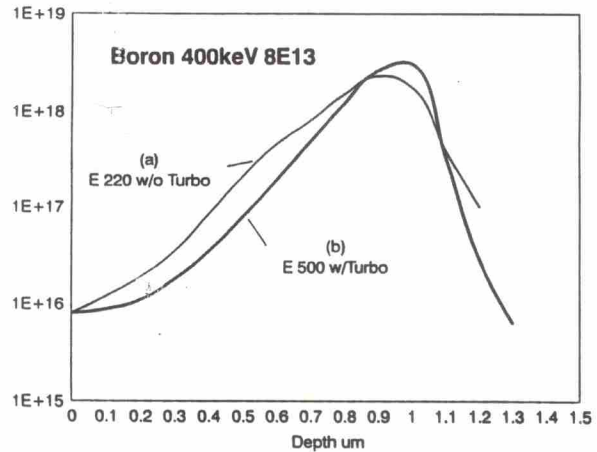


Fig. 3. SIMS profiles without (a-E220) and with (b-E500) resolving aperture turbo pump.

## 3. ELECTRICAL DEVICE RESULTS

The above advantages have allowed us to integrate the E500  $P^{+++}$ , 720 keV,  $1e13$  retrograde n-well process in a 0.5  $\mu m$  CMOS process line. The advantages are the following:

- Reduction of the n+/p+ distance down to 3  $\mu m$ .
- Substantial reduction of the well resistance ( $R_w$ ), in particular if compared to the diffused well process, by a factor 3, with a resulting improvement in latch-up holding current.
- The process allows a thinner epi wafer (4  $\mu m$ ) and thus improves the latch-up voltage characteristics for the bipolar transistor in the vertical direction.
- The lateral isolation between adjacent devices is excellent with a leakage current far less than 1 pA per micron.

Besides achieving the goal of a smaller n+/p+ distance, we have achieved an excellent



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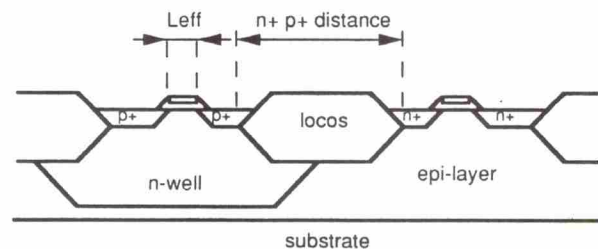


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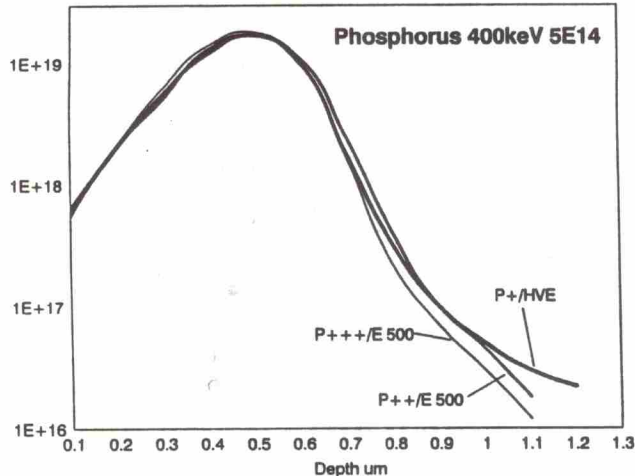


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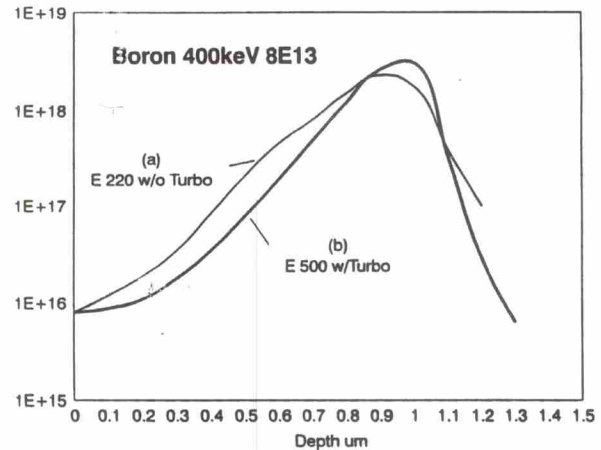


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