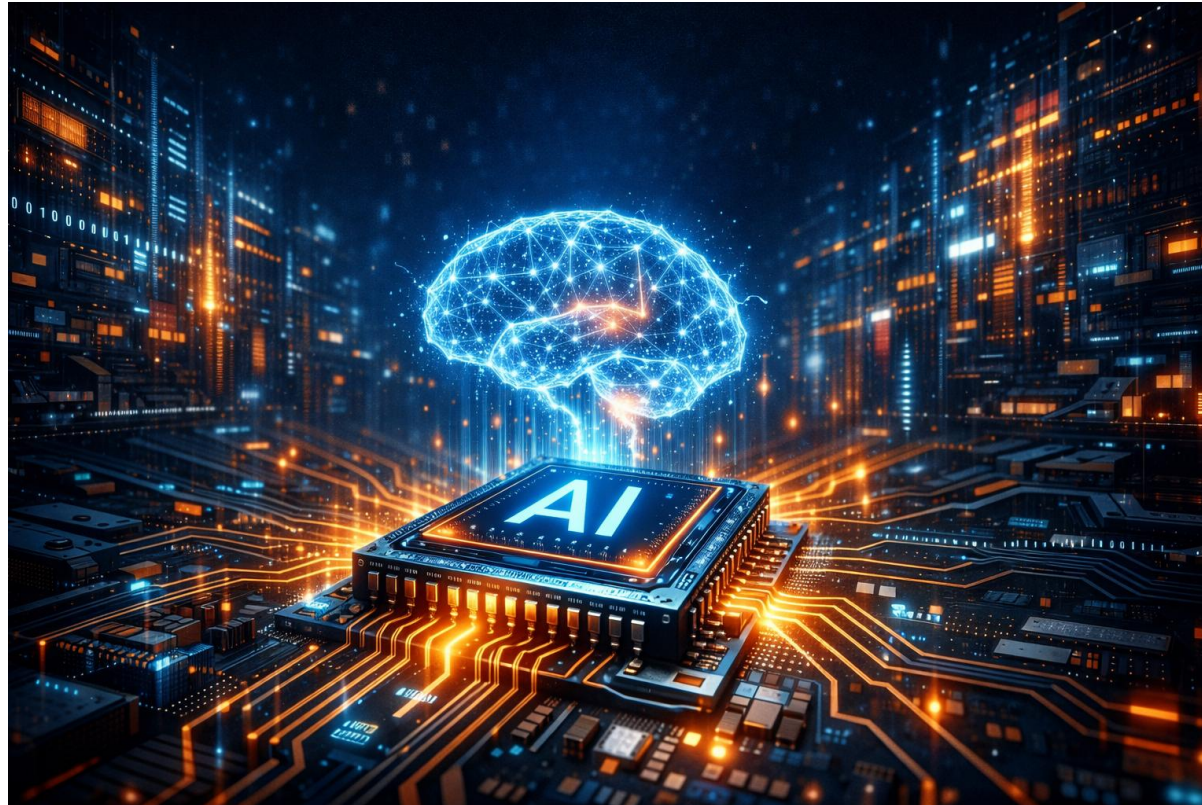


Semiconductors Chips: Powering the AI



Jaskaran Singh Dhiman (Jas)
Kulicke & Soffa, PA

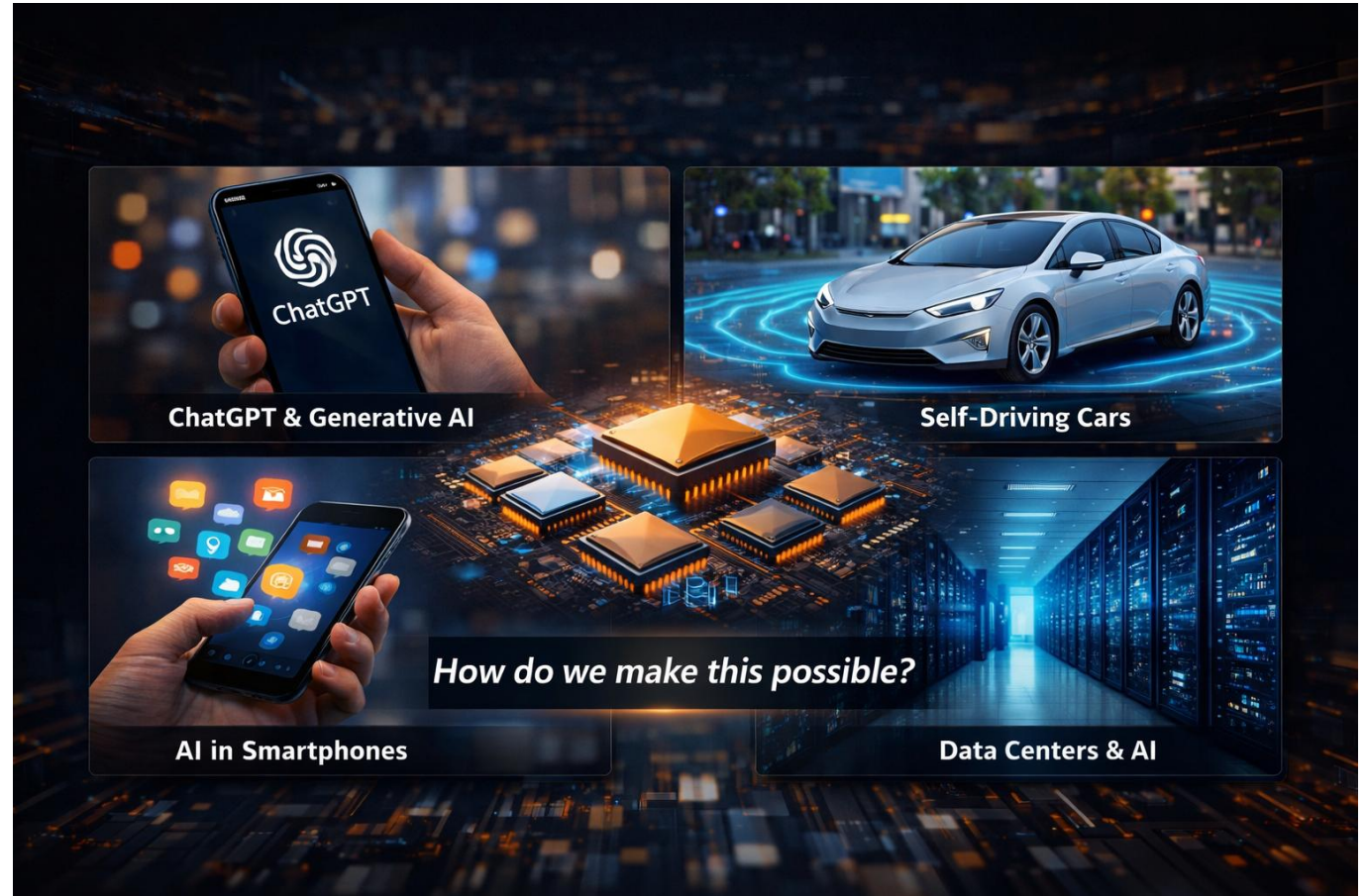
Topics

- Keynote
- Semi Fab
- Market & Ecosystem
- Interconnect Evolution
- Heterogenous Integration
- Career Paths
- Summary

Why AI feels Instant?

- GPT's
- AI on Devices

Computing Workloads



Inside the Fab



Credits: Intel, Link: <https://youtu.be/-KTKg0Y1snQ?si=OO68HyxCmmpohATK>

Market Outlook 2030

- **Computing & Data Storage**

- \$350B in 2024 → \$810B in 2030, adding \$460B
- AI Servers; Logic & Memory Chips
- ↑ Selling Price for Advance Node Chips

- **Wireless;**

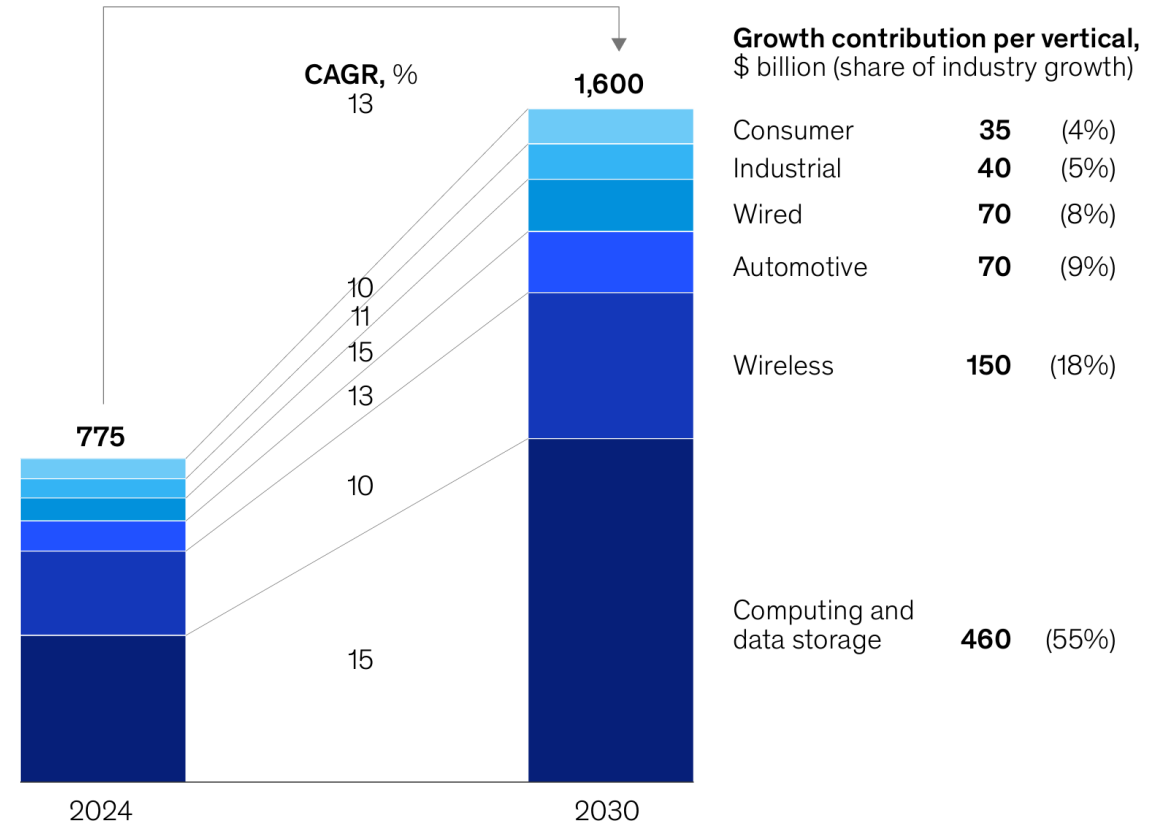
- Transition to smaller node sizes in wireless components, SoC's, modems & Wi-Fi chips, & memory controller

- **Automotive**

- ADAS(Advanced Driver Assistance System)

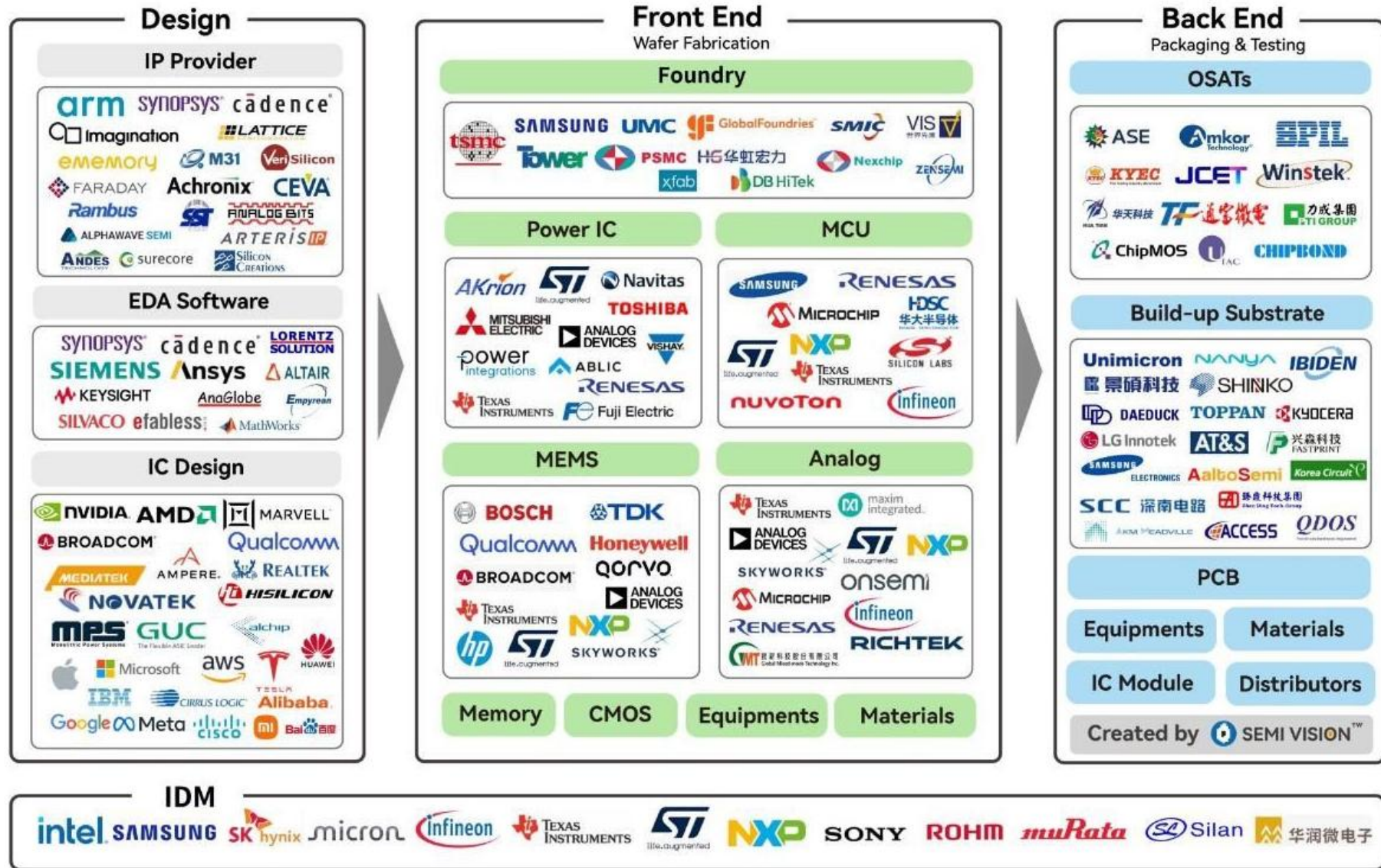
The semiconductor market could reach a value of **\$1.6 trillion** by 2030.

Global semiconductor market (base case),
\$ billion



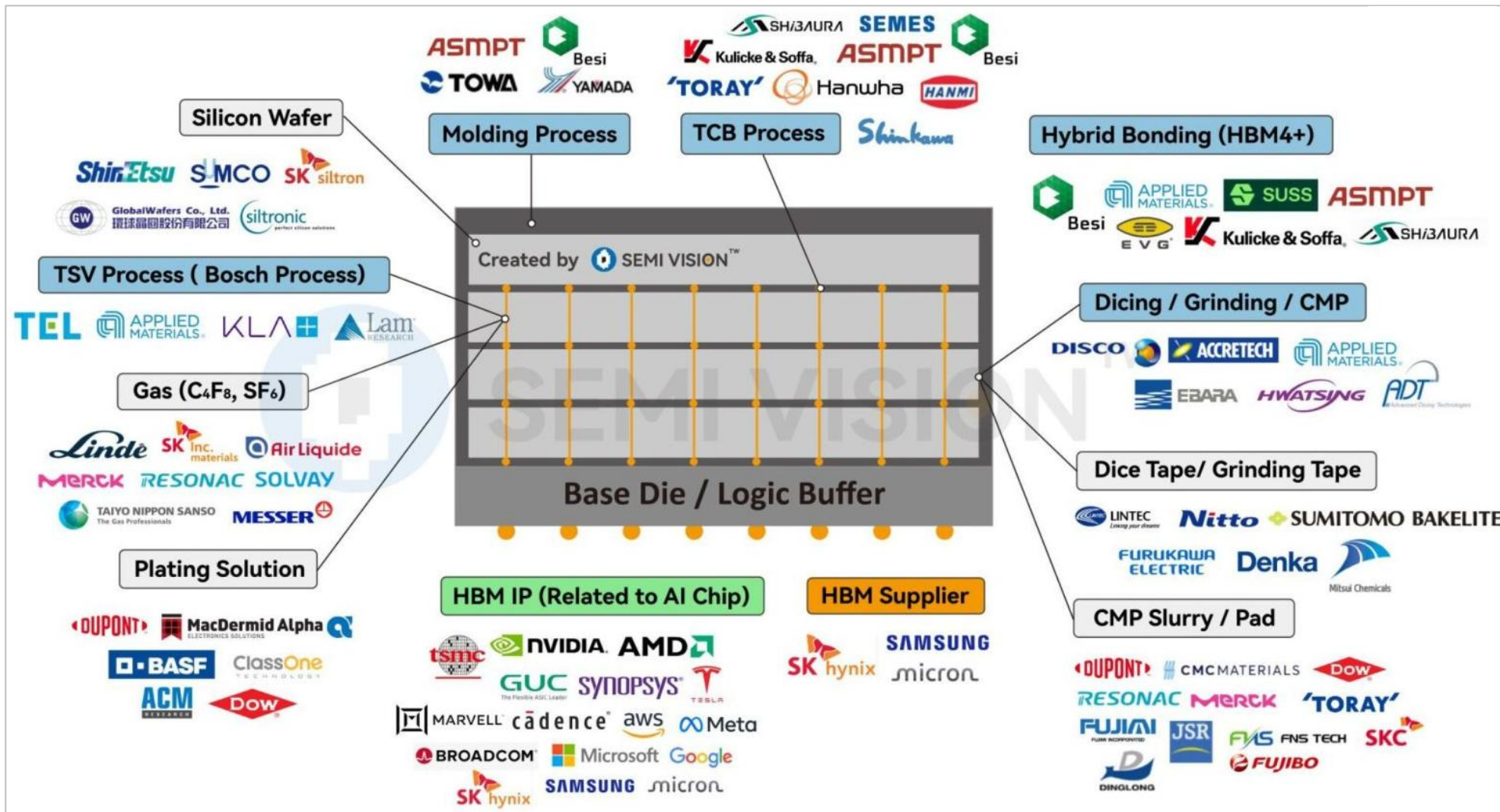
Note: Values rounded to nearest \$5 billion; percentages do not add to 100%, because of rounding.
Source: Omdia; McKinsey analysis

Semiconductor Ecosystem



- MCU – Micro controller unit
- MEMS – Microelectromechanical systems
- EDA – Electronic Design Software
- CMOS – Complementary Metal-Oxide-Semiconductor
- OSAT – Outsourced Semiconductor Assembly and Test
- IDM – Integrated Device Manufacturer

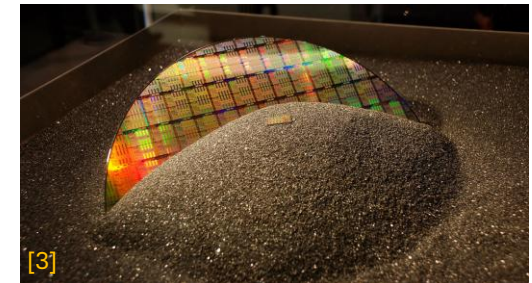
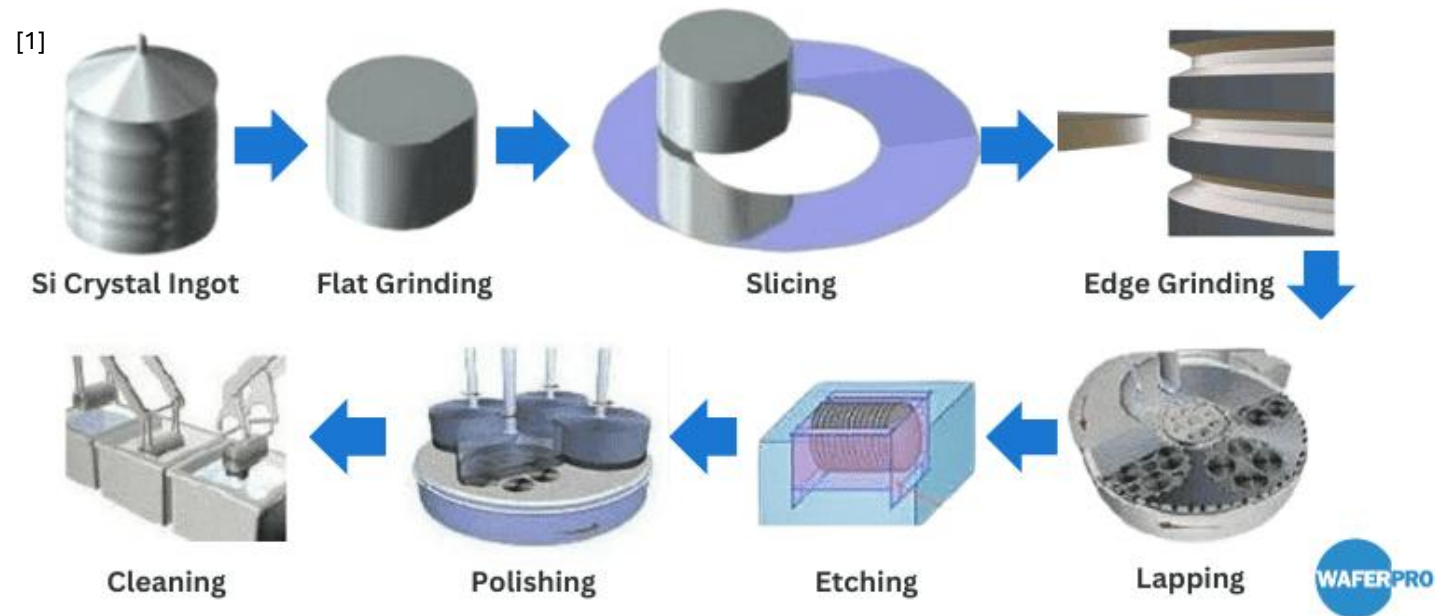
High Bandwidth Memory (HBM) Supply Chain



Credits; Semi Vision

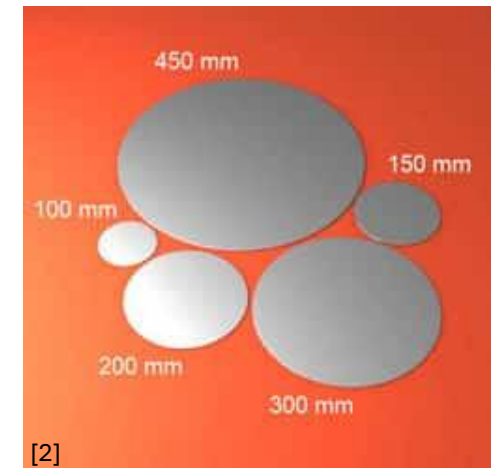
Link: <https://tspasemiconductor.substack.com/>

Semiconductor!



Silicon Wafer

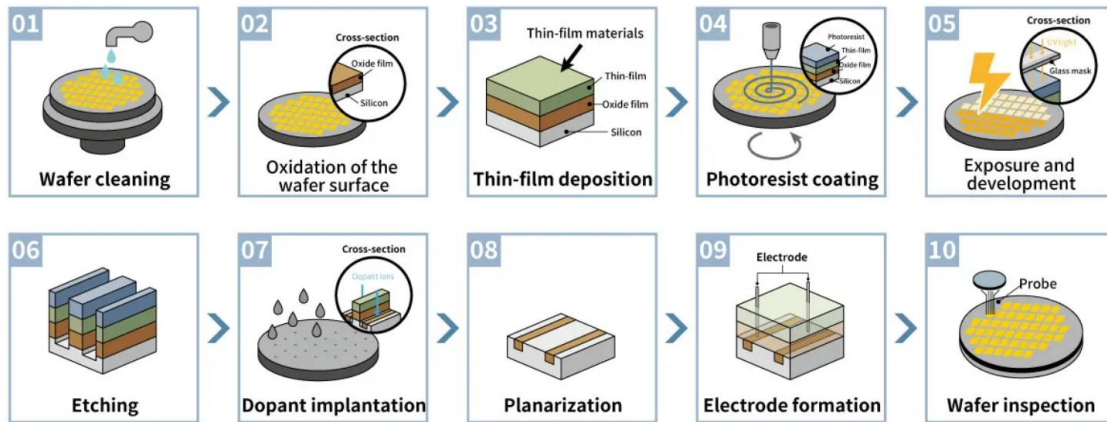
- Sizes; 1in -12 in, most common sizes are 150 mm, 200 mm & 300 mm
- Thickness; 0.2 – 1.5 mm
- Flatness ~ 1 μ m & Surface finish under 1nm
- Plain & Doped Options



1. https://waferpro.com/what-is-a-silicon-wafer/?srsltid=AfmBOoqeOFh0W_COY-wffSY9eDbunQQviCANNpbodvNUYkyMYdjvKBli
2. <https://waferpro.com/what-is-a-semiconductor-wafer/>
3. Micron Fabrication: <https://www.micron.com/content/dam/micron/educatorhub/fabrication/micron-intro-to-fabrication-presentation.pdf>
© 2020-2026 Micron Technology, Inc. All Rights Reserved. Used with permission.”

Process

Front End – making the chip



Back End – packaging of chip

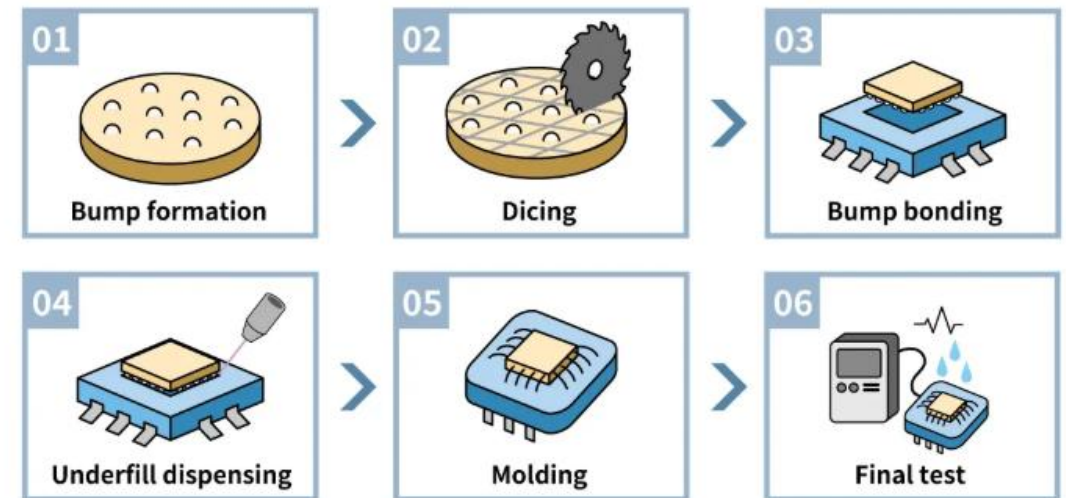


Image [1]

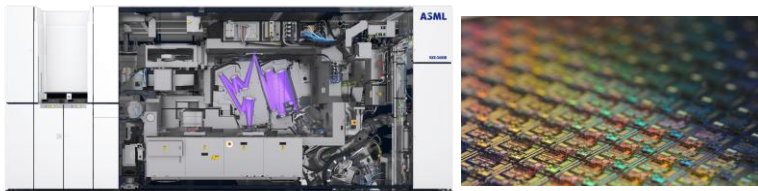




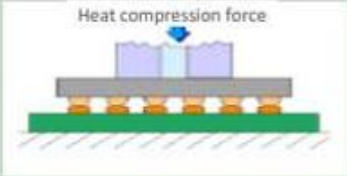

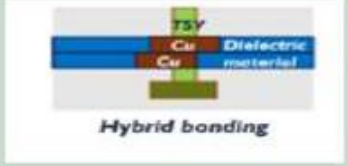





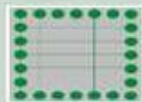




Image [2]

Credits:

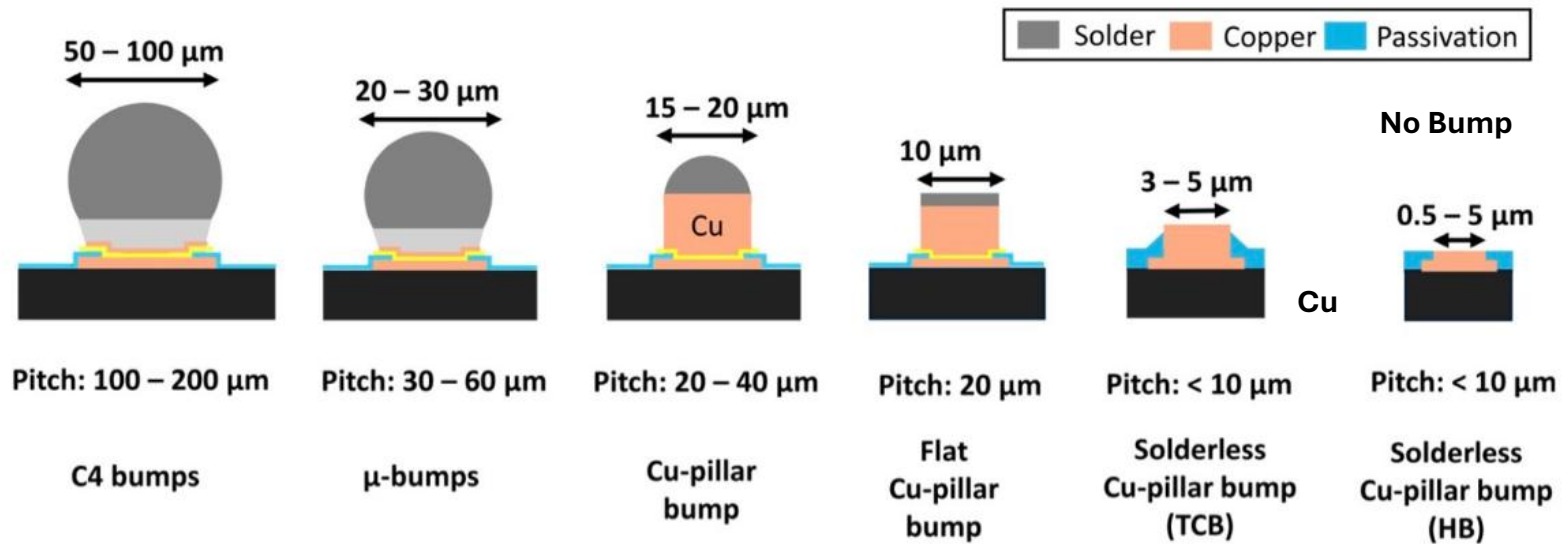
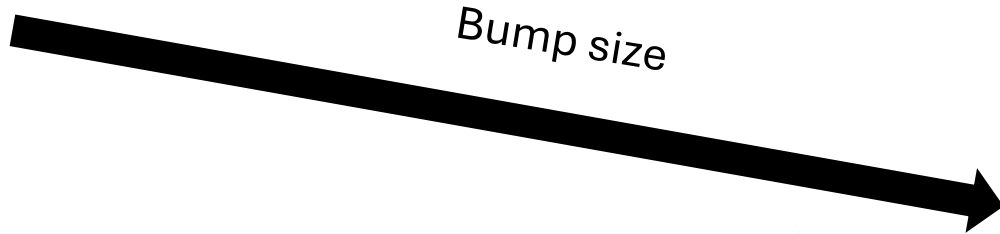
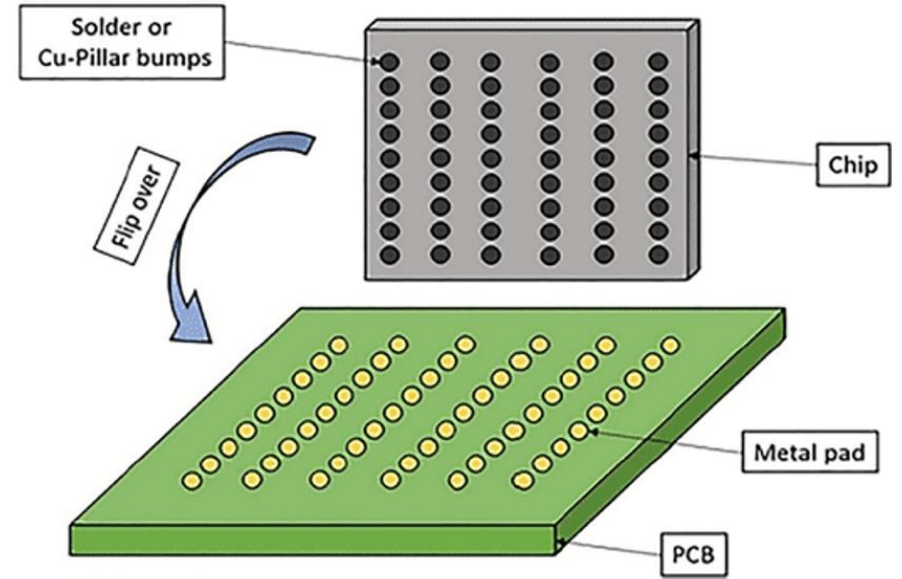
1. <https://www.rapidus.inc/en/tech/te0010/>

2. <https://www.cnn.com/2022/03/23/inside-asml-the-company-advanced-chipmakers-use-for-euv-lithography.html>

Evolution of Interconnects

	Wire Bond (1975)	Flip Chip (1995)	TCB Bonding (2012)	HD Fan Out (2015)	Hybrid Bonding (2018)
Architecture					
Contact Type	 Wire	 Solder ball or copper pillar	 Copper pillar	 RDL or copper pillar	 Copper to copper
Contact Density	 5-10/mm ²	 25-400/mm ²	 156-625/mm ²	 500+/mm ²	 10K-1MM/mm ²
Substrate	Organic/leadframe	Organic/leadframe	Organic /Silicon	None	None
Accuracy	20-10µm	10-5µm	5-1µm	5-1µm	0.5-0.1µm

Changes in Bumps



Credits

<https://techlevated.com/techterms/microbump/>

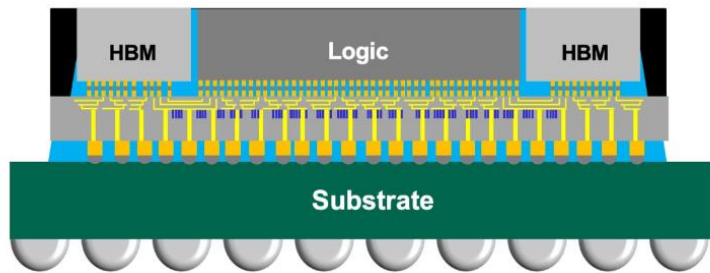
SemiVision; https://x.com/semivision_tw/status/1986087554685247796/photo/1

Heterogenous Integration (HI) Cont'd



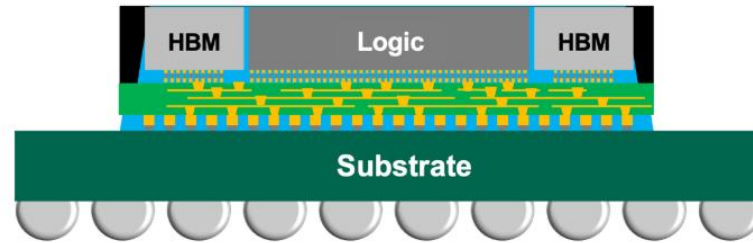
TSMC's Fabric- CoWoS (Chip on Wafer on Substrate)

CoWoS-S



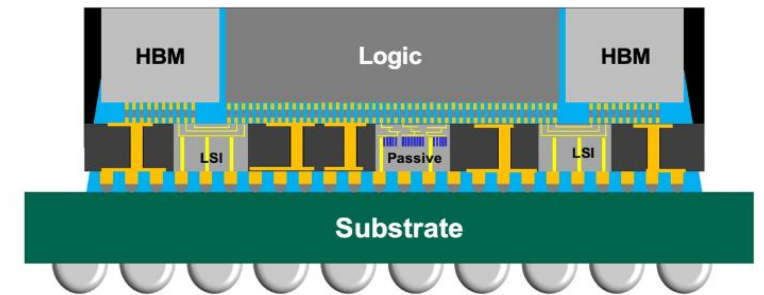
- AI & Supercomputing
- 3.3x reticle size or 2700mm²

CoWoS-R



- RDL Redistribution Layer Interposer
- Better C4 joints quality

CoWoS-L

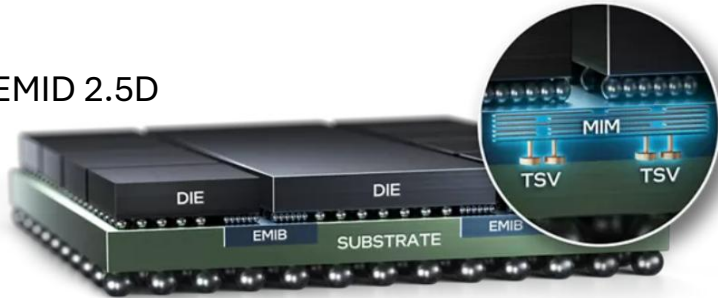


- LSI- Local Silicon Interconnect
- Accommodates variety of connection architects

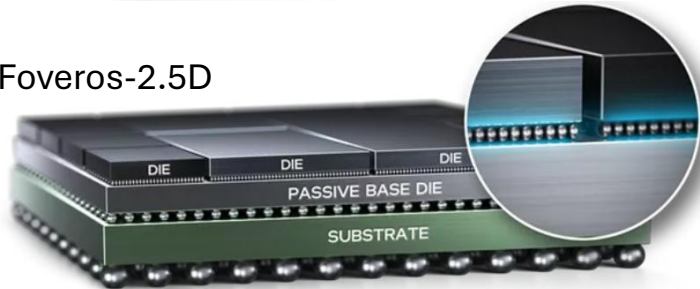
Intel's Packaging

2.5D

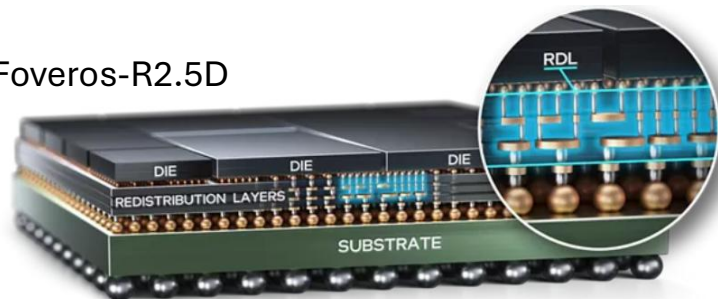
EMID 2.5D



Foveros-2.5D



Foveros-R2.5D

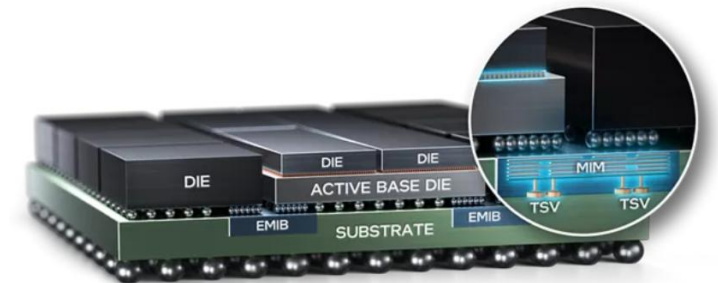


3D



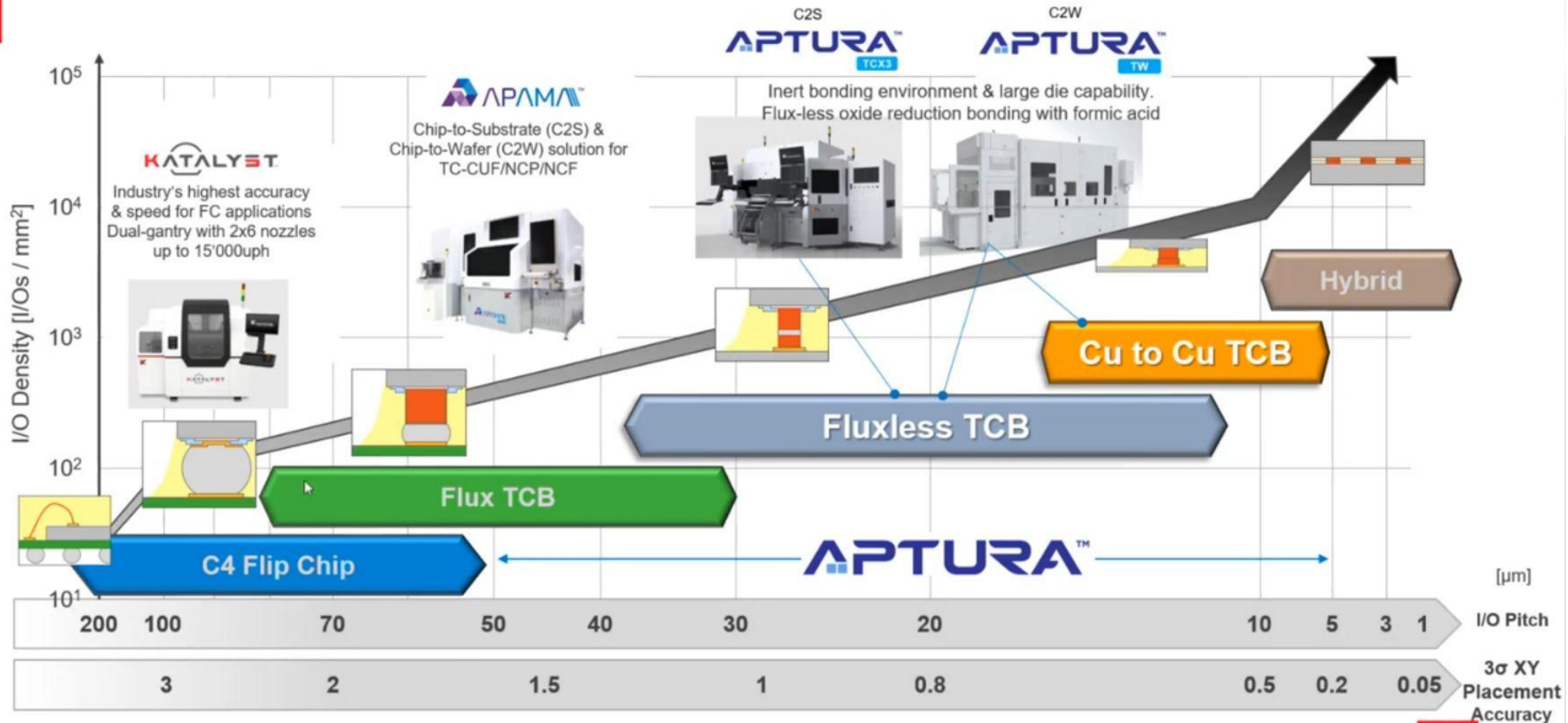
- Cu-Cu hybrid bonding interface(HBI)
- Data Center Application

3.5D



- Flexible Heterogenous Systems
- Capable of multiple 3D stacks in one single package

K&S Flip Chip and TCB Solutions



Which Packaging Technology to use?

- Power Efficiency & Delivery
- Routing Density
- Package Size
- Thermal Performance
- Cost
- Process Maturity
- Supply Chain

Career Pathways

- **IC Design Engineer**

- Designs the circuits that make chips compute, process signals, or manage power.

- **Hardware Roles**

- **R&D/Design Engineer;** Design Electro-Mechanical modules like material handling, optics, laser, vacuum systems, etc.
- **System/Equipment Engineer;** Review & analyzes the complete system/machine and define the specification(accuracy, die handling capabilities, bonding
- **Quality Engineer;** Test the packing system using metrology systems and other testing tools.

- **Process Engineer**

- Develops the packaging process on the machine by creating the recipes

- **SW Engineering**

- Developers and SVT(Software Verification Tests)

- **Field Service/Application Roles**

- **Facilities Engineer (Cleanroom, HVAC & Utilities)**

- Maintain & Design the facility(Cleanroom space)

- **Others**

Future Trends

CoPoS (Chips-on-Panel-on-Substrate)

- **Panel-level interposers** replace wafer-based interposers, enabling *much larger* package sizes for AI/HPC.
- **Better economics at scale:** rectangular panels reduce scrap and improve throughput vs. circular wafers.
- **Accommodates many logic dies & 4–12+ HBM stacks** with high I/O density.
- **Challenges:** warpage, die shift, PDN design, thermals, and board-level reliability for very large packages.

Co-packaged Optics

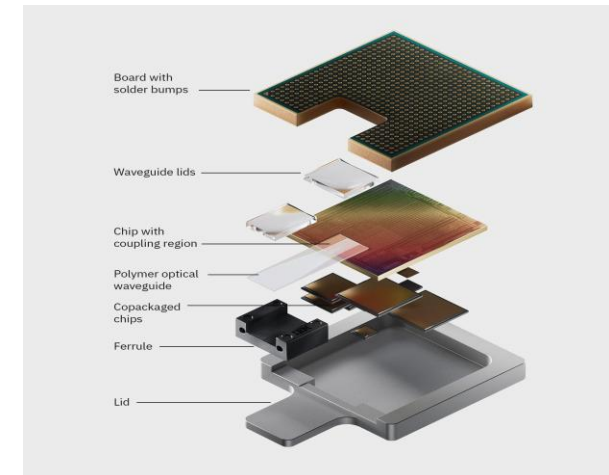
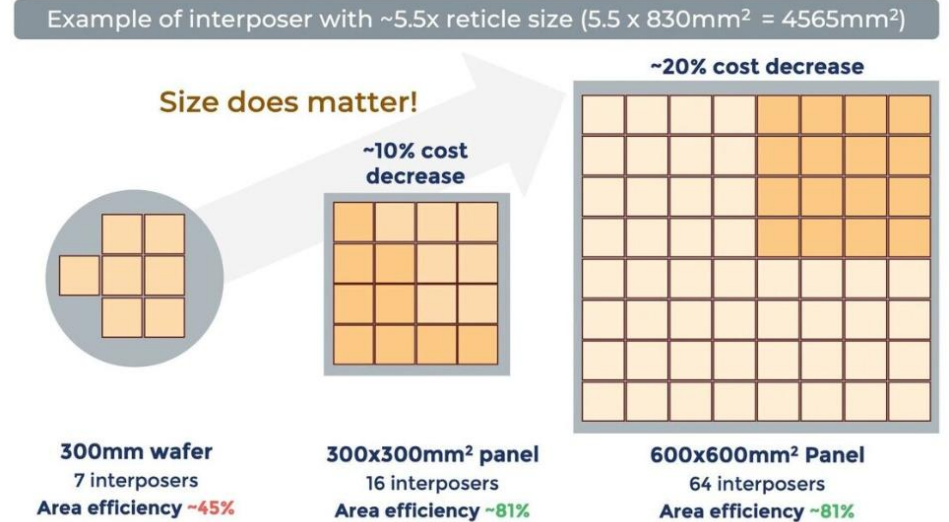
- Uses **light instead of electricity** to connect chips, enabling faster data transfer
- Potentially delivers **much higher bandwidth (10–80×)**
- Reduces energy consumption by **up to 80% per data transfer**
- Enables **denser connections (up to 6× more)**
- Critical for scaling AI systems where **data movement is the main bottleneck**

Sources

<https://research.ibm.com/blog/co-packaged-optics-to-supercharge-generative-ai-computing>

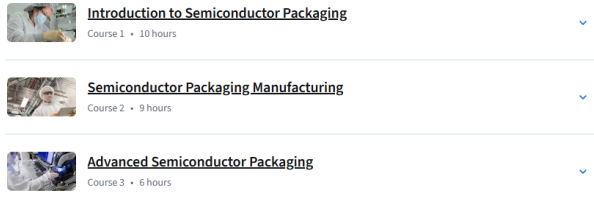
<https://semiwiki.com/wikis/industry-wikis/chip-on-panel-on-substrate-copos-wiki/>

<https://www.techpowerup.com/337960/tsmc-prepares-copos-next-gen-310-x-310-mm-packages>



Resources

- Online Course on Coursera by ASU : <https://www.coursera.org/specializations/semiconductor-packaging>



- YouTube Channels

- Intel Foundry; <https://www.youtube.com/watch?v=LgP35yX6nhI>
- Sand to Silicon; https://youtu.be/_VMYPLXnd7E?si=WRB7YcPwH-F_G60E
- Asianometry; <http://www.youtube.com/@Asianometry>
- Samsung Semiconductor; https://youtu.be/Bu52CE55BN0?si=v5TtJELY_TpSTMNI

- Societies & Organizations

- IMAPS(International Microelectronics and Packaging Society,); <https://imaps.org/>
- IEEE EPS(Electronics Packaging Society); <https://eps.ieee.org/>
- SIA (Semiconductor Industry Association); <https://www.semiconductors.org/>
- SEMI Foundation; <https://www.semi.org/>
- NSIT/Chips for America; <https://www.nist.gov/chips>

- Others(LinkedIn, Substack, etc.)

- Semi Vision; <https://tspasemiconductor.substack.com/>
- Semi Analysis; <https://newsletter.semianalysis.com/>
- Semiconductor Digest; <https://www.semiconductor-digest.com/>
- Trendforce; <https://www.trendforce.com/news/>

Thank You



LinkedIn: <https://www.linkedin.com/groups/13000252/>

Special Thanks

Velda Vaness Morris (Chapter Chair)



Jaskaran Singh Dhiman (Jas)
Kulicke & Soffa, PA

<https://www.linkedin.com/in/jaskaran-dhiman/>