Evaluation Package: Machine-Learning Surrogate Models for Analog Design

This evaluation package provides a hands-on introduction to Analog Intelligent Design's machine-learning–based approach for analog circuit analysis, using a **65nm folded-cascode operational amplifier** as a reference design. The package is intended to help prospective customers understand how ML surrogate models can be used to rapidly explore circuit performance across design parameters and operating conditions, with results available in seconds rather than through large numbers of iterative SPICE simulations.

The package includes trained ML models, a ready-to-run evaluation script, and supporting documentation that demonstrate how key specifications—such as gain, bandwidth, phase margin, power, noise, and settling behavior—can be evaluated across PVT corners and design tradeoffs. This approach enables much broader early-stage exploration, improves visibility into margins and sensitivities, and helps reduce design risk, late surprises, and costly respins.

What you'll see

- Rapid prediction of analog performance across design parameters and PVT
- Interactive exploration of key tradeoffs and sensitivities
- Comparison of operating points without running thousands of SPICE simulations
- Representative outputs and plots illustrating design-space coverage

This evaluation package reflects the same ML-based design and test methodology we apply in customer engagements for production analog and RF circuits. It is provided for evaluation purposes to support technical review and discussion. **Registration is required to obtain access to the package through our sales team.**

Legal Disclaimer

This material is provided for **evaluation and informational purposes only**. The machine-learning models, scripts, examples, and results contained herein are intended solely to illustrate a potential design and analysis methodology and do not constitute a final design, specification, guarantee, or commitment of performance.

All predictions, analyses, and outputs generated using this package are **model-based estimates** derived from trained surrogate models and are **not a substitute for full circuit simulation, verification, qualification, or silicon validation**. Actual circuit performance may vary due to implementation details, modeling assumptions, process variations, operating conditions, layout effects, aging, radiation effects, or other factors not fully captured by the models.

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