Introduction to GPIO pins

Soumick Majumdar

IIIT Bangalore

Contents

1 Introduction

GPIO stands for General-Purpose Input/Output. GPIO pins are versatile pins found on microcontrollers and other integrated circuits that can be configured to perform a wide range of input and output tasks. Unlike specialized pins that have fixed functions (such as power supply pins or communication interface pins like UART, SPI, or I2C), GPIO pins are general-purpose and can be used in multiple ways depending on how they are programmed and configured.

1.1 Key Features of GPIO Pins:

- Configurable Direction: Input: The pin can be configured to read signals from external devices. For example, it can detect whether a button is pressed or read the state of a sensor. Output: The pin can be configured to send signals to control external devices, such as turning an LED on or off or sending a signal to another circuit.

- Configurable Drive Modes: GPIO pins can be set to different drive modes, such as high-impedance, strong drive, open-drain, or resistive pull-up/pull-down. These modes determine how the pin interacts electrically with the circuit it's connected to.

- Interrupt Capabilities: GPIO pins can often be configured to trigger interrupts, which allow the microcontroller to respond immediately to changes in the state of the pin (e.g., when a button is pressed).

- Analog and Digital Functionality: Some GPIO pins can be configured to handle analog signals, either as inputs to an ADC (Analog-to-Digital Converter) or outputs from a DAC (Digital-to-Analog Converter). They can also be used as simple digital inputs or outputs.

- Multiplexing: GPIO pins may be multiplexed with other functions, meaning a single pin can perform multiple roles depending on the selected function (e.g., it might act as a UART TX/RX line or a simple digital input depending on how it's configured).

1.2 Common Uses of GPIO Pins:

- Controlling LEDs: Setting a pin as an output to turn an LED on or off.

- Reading Buttons: Configuring a pin as an input to detect whether a button is pressed.

- Interfacing with Sensors: Reading digital signals from sensors or providing control signals to actuators.

- Communication: Acting as simple bit-banged interfaces for communication protocols like SPI or I^2C (though dedicated hardware is preferred for these tasks).

- PWM (Pulse Width Modulation): Some GPIO pins can generate PWM signals for controlling motors, LEDs (for dimming), or other devices.

  General Purpose Input/Output (GPIO) pins in microcontrollers like those in the PSoC 4 family are highly configurable, allowing them to be tailored to a wide variety of applications. These configurations are often achieved using MOSFETs, specifically PMOS (P-channel Metal-Oxide-Semiconductor Field-Effect Transistor) and NMOS (N-channel MOSFET) transistors. Understanding the current flows, as well as the states and functionalities of these transistors, is crucial when explaining the eight different GPIO drive modes.

1.3 Drive Modes

There are 8 drive modes, namely,

- 1. High-impedance Analog

- 2. High-impedance Digital

- 3. Resistive Pull-Up

- 4.Resistive Pull-Down

- 5. Open Drain, Drives Low

- 6. Open Drain, Drives High

- 7. Strong Drive

- 8. Resistive Pull-Up and Resistive Pull-Down

2 Physical Structure of GPIO Pins

The physical structure of GPIO (General-Purpose Input/Output) pins in the PSoC 4 microcontroller family is designed to provide flexibility, enabling them to handle various analog and digital tasks. The GPIO pins connect to several internal resources within the PSoC 4, including the CPU, digital peripherals (like Timers, PWM, I²C), and analog peripherals (such as OpAmps and ADCs).

2.1 Key Components in the Physical Structure:

- Digital Input Buffer: The digital input buffer receives signals from external circuits connected to the GPIO pin. It can be configured to support different input thresholds, including CMOS, LVTTL, and 1.8-V CMOS, depending on the specific device in the PSoC 4 family. The input buffer presents high impedance to the external circuit, ensuring minimal loading and signal distortion.
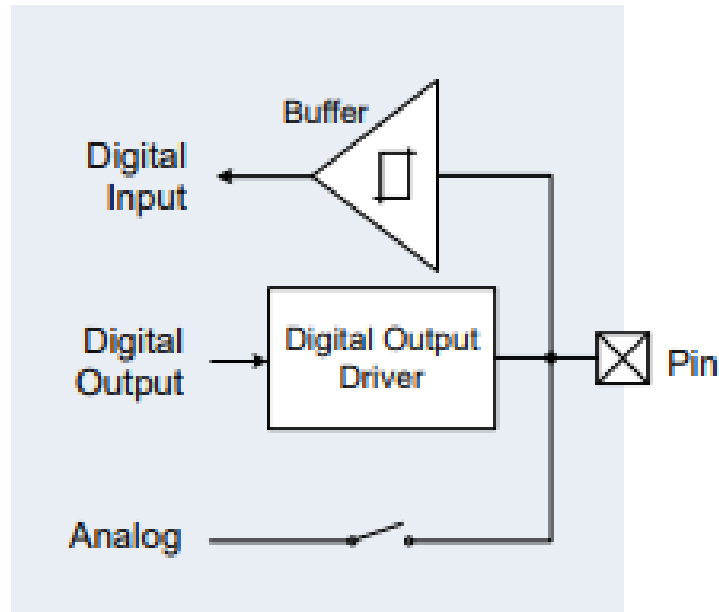
Figure 1: Block Diagram of GPIO pin

- Digital Output Driver: The digital output driver is responsible for driving signals from the microcontroller to external circuits. It can be configured in various drive modes (e.g., High-Impedance, Strong Drive, Open Drain), which determine how the pin behaves when it outputs a signal. The output driver includes circuitry to control the slew rate, which can be set to "Fast" or "Slow." Fast slew rates are useful for high-speed signals, while slow rates reduce EMI and cross-talk in less time-critical applications.

- Analog Pin: The GPIO can also function as an analog pin, connecting directly to internal analog resources like OpAmps, ADCs, or DACs. When configured for analog functionality, the pin bypasses the digital input/output buffers to ensure signal integrity for analog processing.

- Routing Capabilities: GPIO pins in the PSoC 4 have flexible routing capabilities. They can be connected to various internal resources via a high-speed I/O matrix (HSIOM) and a Digital System Interconnect (DSI). This allows the pin to interface with a wide range of peripherals, such as timers, communication blocks (I²C, UART, SPI), and PWM controllers.

3 Digital Output Driver of GPIO

The digital output driver within a GPIO pin in the PSoC 4 family is a crucial component that determines how the pin drives signals to the outside world.

Here's an in-depth look at its functionality:

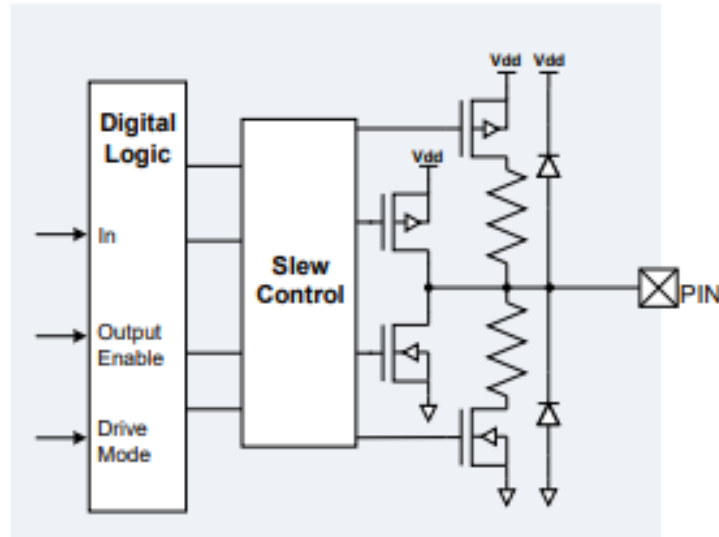## 3.1 Components and Functionality:

Figure 2: Digital Output Driver Circuit

Drive Modes:

- High-Impedance Analog (Hi-Z Analog): Both the PMOS and NMOS transistors are off, effectively disconnecting the pin from any digital drive. This mode is used for analog signal input/output where the pin should not affect the signal.

- High-Impedance Digital (Hi-Z Digital): The output driver is disabled, and the pin is not driven by any internal signal. This is ideal for input-only configurations where the pin should not source or sink any current.

- Resistive Pull-Up/Down: The output driver includes weak pull-up or pull-down resistors (5 k$_O mega$) that pull the pin to VDD or ground, respectively, when no active drive signal is present. These resistors prevent the pin from floating and ensure a defined logic level.

- Open Drain (Drives Low/High): The output driver can be configured to actively drive a strong logic low (NMOS on, PMOS off) or high (PMOS on, NMOS off) but remains in a high-impedance state otherwise. This mode is used for bus systems where multiple devices share a line.

- Strong Drive: Both the PMOS and NMOS transistors can actively drive the pin to a logic high or low, sourcing or sinking significant current. This

mode is used when the pin needs to drive heavy loads, such as LEDs or other logic devices.

Slew Rate Control:

The slew rate control feature allows you to adjust the rate at which the output signal changes from low to high or high to low. This control is essential in managing EMI and signal integrity, especially in high-speed digital circuits. A faster slew rate is suitable for high-frequency signals, while a slower rate reduces noise and cross-talk in more sensitive analog or mixed-signal circuits.

Output Enable:

The output enable control allows you to enable or disable the output driver dynamically. When disabled, the pin can function as an input or high-impedance state. This feature is useful in situations where a pin needs to be dynamically reconfigured between input and output modes during operation.
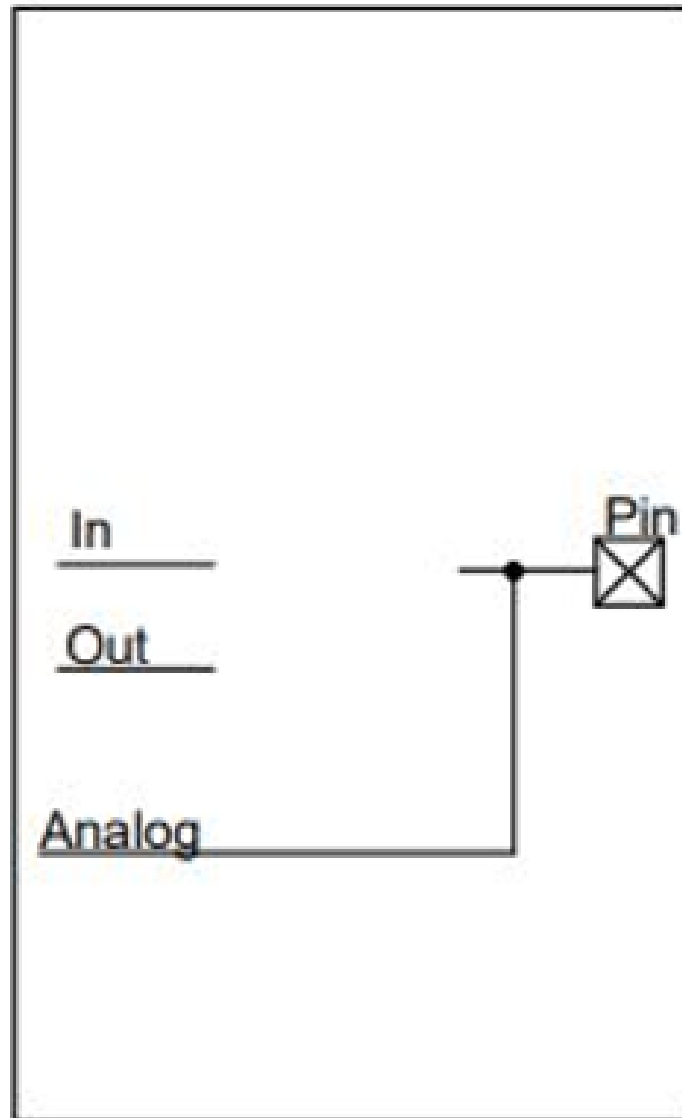
VDD Connection:

The output driver circuitry is powered by the microcontroller's VDD. This connection ensures that the output levels are consistent with the operating voltage of the PSoC 4, which is critical for interfacing with other components in the system.

Applications and Use Cases:

- Digital Communication: GPIO pins configured with strong drive modes are used in digital communication interfaces where fast and reliable signal transitions are necessary.

- Analog Interfaces: Hi-Z modes are employed in scenarios where the GPIO needs to interface with analog components without influencing the signal.

- Bus Systems: Open-drain configurations are commonly used in shared bus systems like I²C, where multiple devices can pull the line low without contention.

- Power-Sensitive Applications: In low-power modes, the slew rate control and output enable features help minimize power consumption by reducing unnecessary signal transitions and disabling unused outputs.

4 High-Impedance Analog (Hi-Z Analog)

- Circuitry: In this mode, both the input buffer and output driver are disabled. The pin is disconnected from any digital circuitry and can be used for analog signals.

- Current Flow: No significant current flows into or out of the pin. The pin presents very high impedance to the connected circuit.

- PMOS/NMOS State: Both PMOS and NMOS transistors are off, presenting a high impedance state.

In

Out

Analog

Pin

1. High-Impedance Analog

Figure 3: High-Impedance Analog

- Used for analog input or output, such as connecting to ADCs, DACs, or other analog circuitry where you need to avoid loading the analog signal.

- Functionality: In Hi-Z Analog mode, the GPIO pin is configured to have a very high impedance. Both the input buffer and output driver are disabled, making the pin appear "invisible" to the digital logic inside the microcontroller. The pin is thus isolated from the digital domain, allowing it to connect directly to analog circuits without interfering with the analog signal.

- Applications: Analog Signal Input: When the pin is connected to an ADC (Analog-to-Digital Converter), the high impedance prevents the pin from loading the circuit and altering the analog signal.

  Analog Signal Output: When connected to a DAC (Digital-to-Analog Converter) or other analog components, this mode ensures that the signal can pass through without digital interference.

  Capacitive Sensing (CapSense): Often used in touch-sensing applications where the pin's analog behavior is critical for detecting touch events.

5 High-Impedance Digital (Hi-Z Digital)

- Circuitry: The output driver is disabled, and the input buffer is enabled.

- Current Flow: The pin has a very high impedance to external circuits, acting as a digital input.

- PMOS/NMOS State: Both PMOS and NMOS transistors are off, preventing any active drive to the pin.

- Ideal for digital input signals where the pin should not affect the circuit it's reading from. It's commonly used in input pins that are not actively driven.

- Functionality: Similar to the Hi-Z Analog mode but intended for digital signals. The output driver is disabled, but the input buffer is enabled, allowing the pin to read digital inputs without driving the pin. The pin remains in a high-impedance state, meaning it won't interfere with other signals on the same line.

- Applications: Digital Inputs: Ideal for reading signals from external components or devices where the pin should not affect the circuit.

  Multiplexed Signals: Useful in systems where multiple devices share a bus, and only one device should drive the line at any given time.

In

Out

Analog

Pin
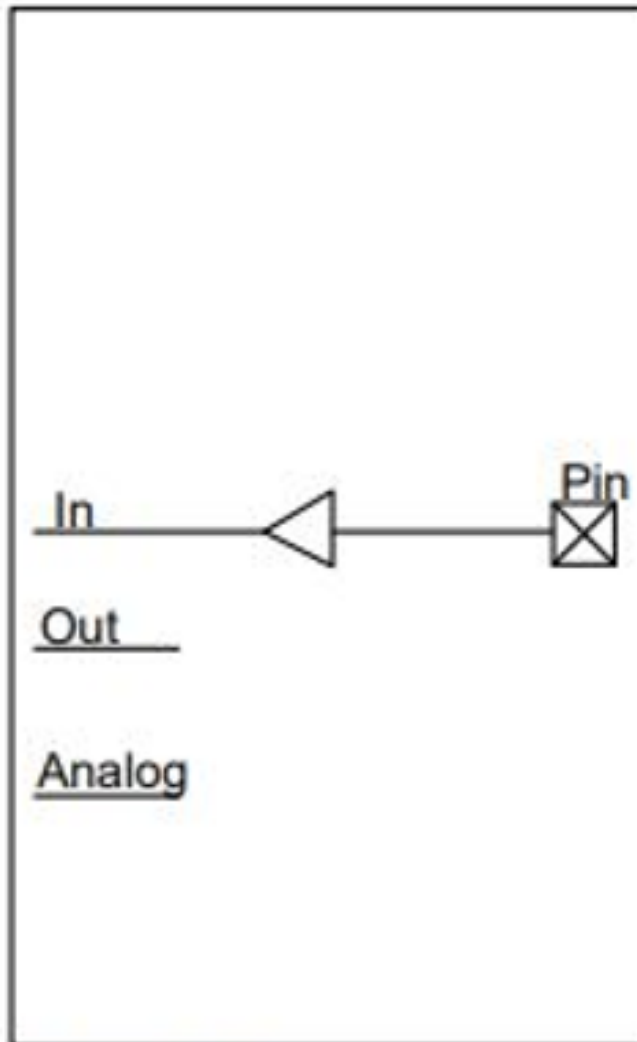
2. High-Impedance Digital

Figure 4: High-Impedance Digital

6 Resistive Pull-Up

- Circuitry: The output driver is disabled, and the pin is connected to VDD through a weak (5 kΩ) pull-up resistor.

- Current Flow: When no external device drives the pin low, it will be pulled up to VDD by the internal resistor.

- PMOS/NMOS State: The NMOS transistor is off; a weak pull-up is provided by the internal resistor.

- Useful for interfacing with open-drain or open-collector circuits, such as a switch connected to ground or a tachometer output from motors

- Functionality: The pin is internally connected to VDD through a weak pull-up resistor (5 k$_o mega$). This ensures that when no active signal is driving the pin, it will be pulled to a logic high level. The pull-up resistor helps prevent the pin from floating (an undefined state), which can lead to erratic behavior.

- Applications: Switches: When interfacing with a switch connected to ground, this mode ensures that the pin reads a high state when the switch is open (unpressed) and a low state when the switch is closed (pressed).

  Open-Drain Inputs: Often used with open-drain or open-collector outputs from other ICs, ensuring that the pin reads high when the external device is not pulling it low.

  Button Inputs: Commonly used in circuits with mechanical buttons to ensure a defined high state when the button is not pressed

7 Resistive Pull-Down

- Circuitry: The output driver is disabled, and the pin is connected to ground through a weak (5 kΩ) pull-down resistor.

- Current Flow: When no external device drives the pin high, it will be pulled down to ground by the internal resistor.

- PMOS/NMOS State: The PMOS transistor is off; a weak pull-down is provided by the internal resistor.

- Used when interfacing with circuits that can be left floating, ensuring the pin reads a low logic level when undriven.

- Functionality: The pin is connected to ground through a weak pull-down resistor (5 k$_o mega$). This keeps the pin at a logic low level when no active signal is driving it. Similar to the pull-up mode, this prevents the pin from floating but biases it towards a low logic level.
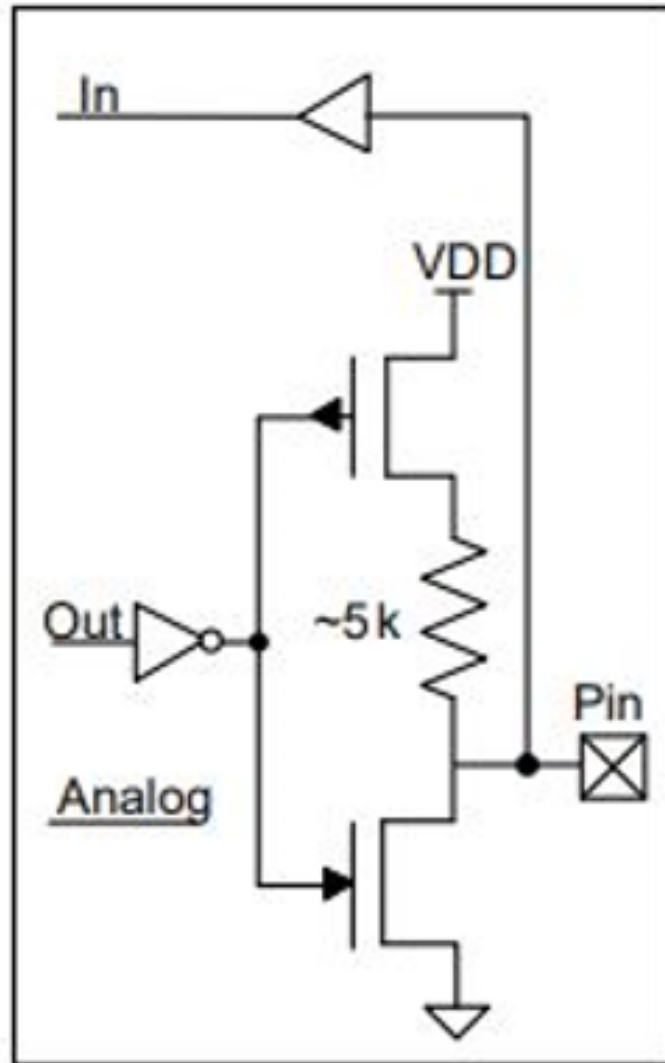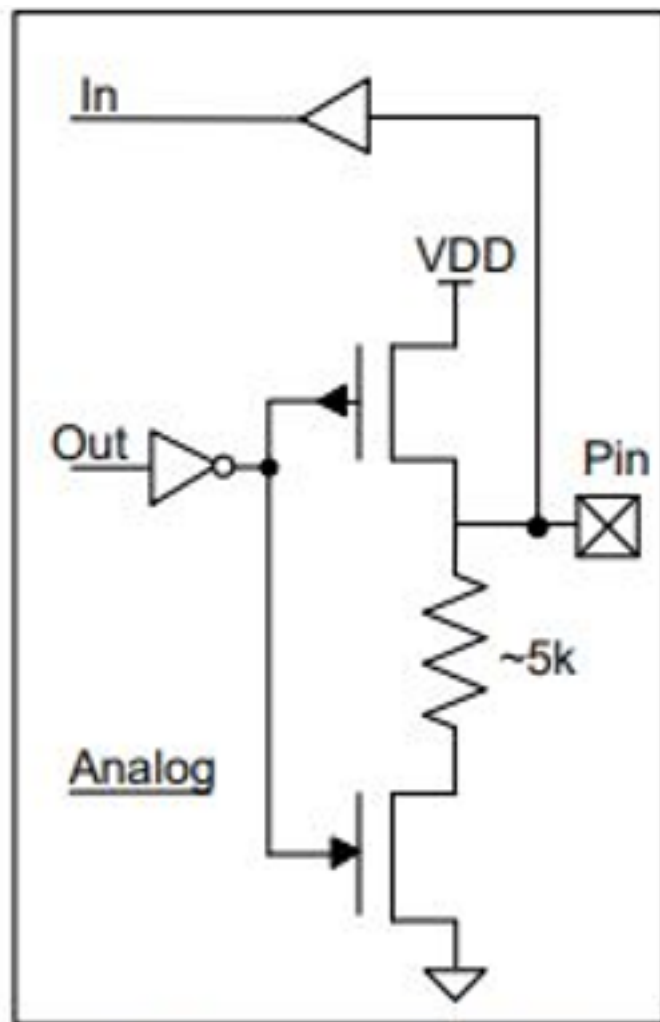
3. Resistive Pull Up

Figure 5: Resistive Pull-Up

- Applications: Switches: Useful when the switch is connected to VDD, so the pin reads a low state when the switch is open and a high state when closed.

  Input Stabilization: In circuits where a pin might be left unconnected at times, this mode ensures the pin reads low instead of floating.

  Digital Inputs: Helps in situations where a default low logic level is needed


Figure 6: Resistive Pull-Down

8 Open Drain, Drives Low

- Circuitry: The pin can drive a strong low signal (NMOS transistor on) but is high-impedance (both transistors off) when driving high.

- Current Flow: The pin can sink current when driving low, but it does not source current when high.

- PMOS/NMOS State: NMOS transistor is on when driving low; PMOS is always off.

- Commonly used in I^{2}C communication and other bus systems where multiple devices share a line and require pull-up resistors to VDD.

- Functionality: In this mode, the pin can drive a strong logic low (NMOS transistor is on) but is high-impedance (both transistors off) when trying to drive high. External pull-up resistors (or an internal pull-up in another device) are needed to pull the line high when the pin is not actively driving low.

- Applications: I^{2}C Communication: Standard for I^{2}C bus lines, where multiple devices can pull the line low, but no device actively drives it high.

  Interrupt Lines: Often used in systems where multiple devices need to pull a shared interrupt line low.

  LED Driving: Can be used in circuits where LEDs are connected between VDD and the pin, with the LED being turned on by pulling the pin low

9 Open Drain, Drives High

- Circuitry: The pin can drive a strong high signal (PMOS transistor on) but is high-impedance (both transistors off) when driving low.

- Current Flow: The pin can source current when driving high but does not sink current when low.

- PMOS/NMOS State: PMOS transistor is on when driving high; NMOS is always off.

- Used in cases where the circuit requires a strong high level, with an external pull-down resistor to bring the line low when necessary.

- Functionality: Opposite of the Open Drain, Drives Low mode. The pin can drive a strong logic high (PMOS transistor is on) but is high-impedance (both transistors off) when driving low. An external pull-down resistor is required to pull the line low when the pin is not actively driving high.

In

Out

Analog

Pin
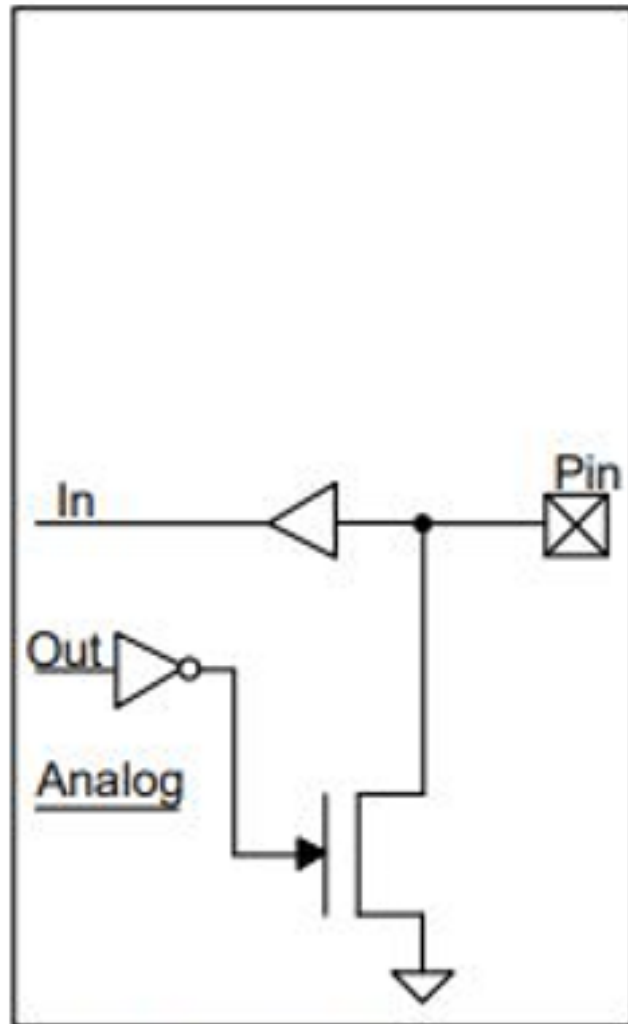
5. Open Drain, Drives Low

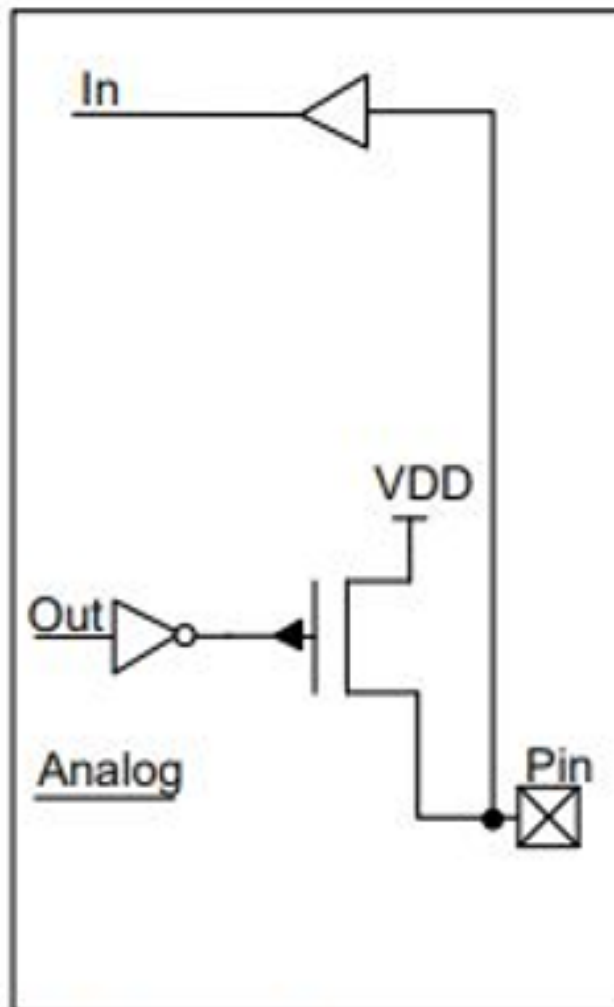Figure 7: Open Drain, Drives Low

14

- Applications: LED Driving: Useful for driving LEDs connected between the pin and ground, where the pin sources current to light the LED.

  Power Supply Control: Can be used to enable high-side switches or power supplies that require a strong high signal to turn on.

  Bus Systems: Less common than the low-driving counterpart but can be used in specific bus systems where a shared line needs to be driven high by one device.

10   Strong Drive

- Circuitry: The output driver is fully enabled, with both the PMOS and NMOS transistors being able to source and sink significant current.

- Current Flow: The pin can source and sink current actively, providing strong signals in both high and low states.

- PMOS/NMOS State: PMOS and NMOS transistors are on during their respective drive states.

- Suitable for driving LEDs, other logic devices, or any load that requires a strong, stable output.

- Functionality: The pin can source and sink significant current, providing a strong drive in both the high and low states. Both PMOS (for high) and NMOS (for low) transistors are actively driving the pin. This mode is useful when the pin needs to drive loads that require more current than what other modes can provide.

- Applications: LEDs: Directly driving LEDs, especially when multiple LEDs are connected or when a bright output is needed. Logic Circuits: Interfacing with other logic circuits that require strong, fast switching signals. Capacitive Loads: Driving capacitive loads where higher current is needed to charge/discharge the capacitor quickly.
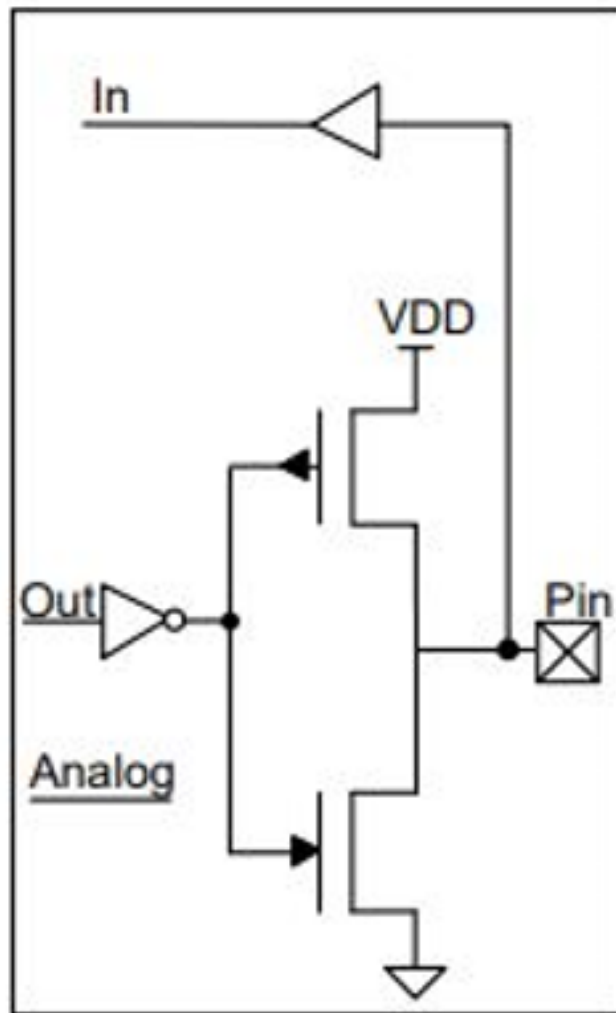
11   Resistive Pull-Up and Pull-Down

- Circuitry: The pin is connected to both VDD and ground through weak (5 kΩ) pull-up and pull-down resistors.

- Current Flow: The pin will tend to settle at a mid-point voltage when undriven by an external circuit due to the equal pull from both resistors.

- PMOS/NMOS State: Both transistors are off; resistive elements define the pin state.
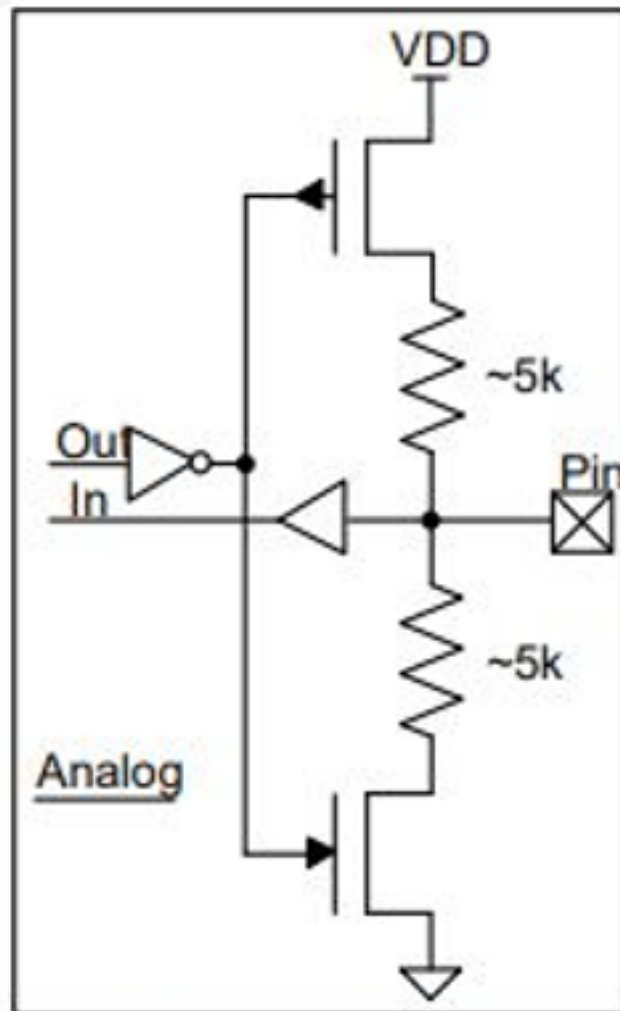
6. Open Drain
   Drives High

Figure 8: Open Drain, Drives High

7. Strong Drive

Figure 9: Strong Drive

Figure 10: Resistive Pull-Up and Pull-Down

- Often used in scenarios where the pin must be biased at a known state when undriven, or in analog-to-digital conversion where mid-level biasing is needed.

- Functionality: The pin has both a pull-up resistor to VDD and a pull-down resistor to ground. This creates a voltage divider, causing the pin to stabilize at a mid-point voltage when not actively driven. This mode is not typically used for pure digital signals but can be useful in certain mixed-signal applications.

- Applications: Analog Comparators: When used in conjunction with an analog comparator, the midpoint voltage can serve as a reference.

  Biasing Networks: In analog circuits, this mode can provide a steady bias voltage to a node.

  Debouncing Circuits: Helps in creating a stable, known state for pins in circuits that may experience noise or fluctuations

12   Conclusion

Understanding these drive modes requires a solid grasp of MOSFET operation, as the states of the PMOS and NMOS transistors directly influence the behavior of the GPIO pins. Each mode serves a specific purpose in ensuring reliable and predictable operation of digital and analog circuits interfaced with the microcontroller. By carefully selecting the appropriate drive mode, engineers can optimize their designs for power efficiency, signal integrity, and performance.