

DV Must Know

1

EdaPl

EdaPlayground

Do you know?

Edaplayground is a free website that let you access to all types of eda tools to compile your system verilog or verilog codes with or without UVM!

Create an account now and start picking up skills on coding!

https://www.edaplayground.com/

U ClueLogic

Do you know?

Cluelogic contains so much great information on UVM! We actually benefit from there as well, here we share you the link to it explaining on UVM RAL:

https://cluelogic.com/2013/02/uvm-tutorial-for-candy-lovers-register-access-methods/

RAL BACKDOOR ACCESS

To achieve RAL backdoor access, you need to prepare few things:

- 1. Add the slice of signals into your RAL
- 2. At the RAL parent, set the hdl path root
- 3. Then you may access via RAL:

You may see how we demonstrate inside our LVM AXI VIP!



VCS Partial Compilation

Do you know that Synopsys VCS prepared the tools to let user do to partial compilation? It let users to recompile the portion that get changed.

For example, when users just change the testbench files, then the RTL files and library files etc actually not needed to be recompiled again, this save engineer time and cpu also.

To see how we made it, you may just download our latest LVM AXI VIP, and copy the code directly to your testbench!

File Substitution

Do you know that you can modify files without opening them?

The magic cmd is as below:

```
perl -p -i -e 's/<before>/<after>/g' *
```

For example:

```
perl -p -i -e 's/old_task_name/new_task_name/g' *env*
```