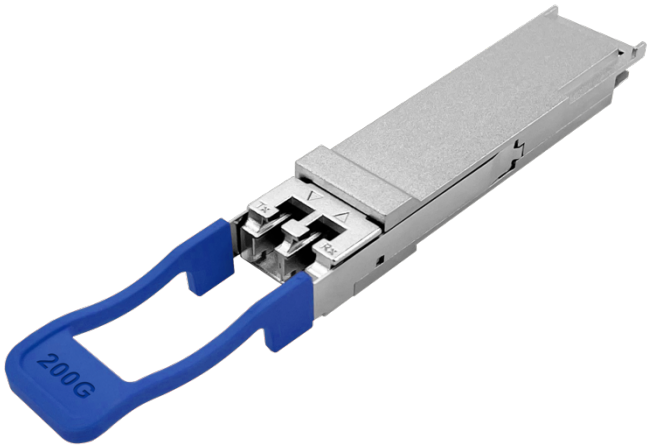
DUKEVILLA
DATA TRANSMISSION & SIGNAL PROCESSING

200 Gb/s QSFP56 LR4 Transceiver
QSFP56-200G-LR4

Features

- Hot-pluggable QSFP56 form factor
- Built-in 200G PAM4 DSP
- Supports 212.5Gb/s aggregate bit rates
- Maximum power dissipation < 7.5W
- Commercial case temperature range of 0°C to 70°C
- Single 3.3V power supply
- Maximum link length of 10km on SMF
- Cooled 4 channels EA-DFB TOSA
- 4 channels PIN ROSA
- 200GAUI-4 electrical interface
- Compliant with CMIS V4.0
- Built-in digital diagnostic functionality



Applications

- IEEE 802.3bs 200GBASE-LR4 Ethernet (PAM4)
- 5G Back-haul
- Data center

Description

DukeVilla's QSFP56-200G-LR4 200GE QSFP56 Optical Transceiver modules are designed for use in 200 Gigabit Ethernet links over SMF28 single-mode fiber. They are compliant with the QSFP MSA and with IEEE802.3bs 200GBASE-LR4 specification. Digital diagnostics functions are available via the I2C interface as specified by ACMIS4.0

Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Unit
Supply Voltage	V_{cc}	-0.3	3.6	V
Input Voltage	V_{in}	-0.3	V_{cc}+0.3	V

Storage Temperature	T_s	-20	85	ºC
Case Operating Temperature	T_c	0	70	ºC
Humidity (non-condensing)	Rh	5	95	%

Recommended Operating Conditions

Parameter	Symbol	Min	Typical	Max	Unit
Supply Voltage	V_{cc}	3.13	3.3	3.47	V
Operating Case Temperature	T_c	0		70	ºC
Baud Rate per Lane (PAM4)	fd		26.5625		GBaud/s
Humidity	Rh	5		85	%
Power Dissipation	P_m		6.8	7.5	W

Electrical Specifications

Parameter	Symbol	Min	Typical	Max	Unit
Differential Input Impedance	Z_{in}	90	100	110	ohm
Differential Output Impedance	Z_{out}	90	100	110	ohm
Differential Input Voltage Amplitude	ΔV_{in}	300		900	mVpp
Differential Output Voltage Amplitude	ΔV_{out}	300		900	mVpp
Bit Error Rate	BER			2.4E-4	
Input Logic Level High	V_{IH}	2.0		V_{cc}	V
Input Logic Level Low	V_{IL}	0		0.8	V
Output Logic Level High	V_{OH}	V_{cc}-0.5		V_{cc}	V
Output Logic Level Low	V_{OL}	0		0.4	V

Optical Characteristics

Parameter	Symbol	Min	Typical	Max	Unit
Transmitter					
Center Wavelength	L1	1294.53	1295.56	1296.59	nm
Center Wavelength	L2	1299.02	1300.05	1301.09	nm
Center Wavelength	L3	1303.54	1304.58	1305.63	nm
Center Wavelength	L4	1308.09	1309.14	1310.19	nm
SMSR	SMSR	30			nm
Average Launch Power (each lane)	P_{out}	-3.4		5.3	dBm
Average Launch Power (total)	Ptatal			11.3	dBm
Outer Optical Modulation Amplitude (each lane)	OMA_{out}	-0.4		5.1	dBm
Launch power in OMA_{outer} minus TDECQ	Ptdecq	-1.8			dBm
Transmitter and dispersion eye closure (each lane)	TDECQ			3.4	dB

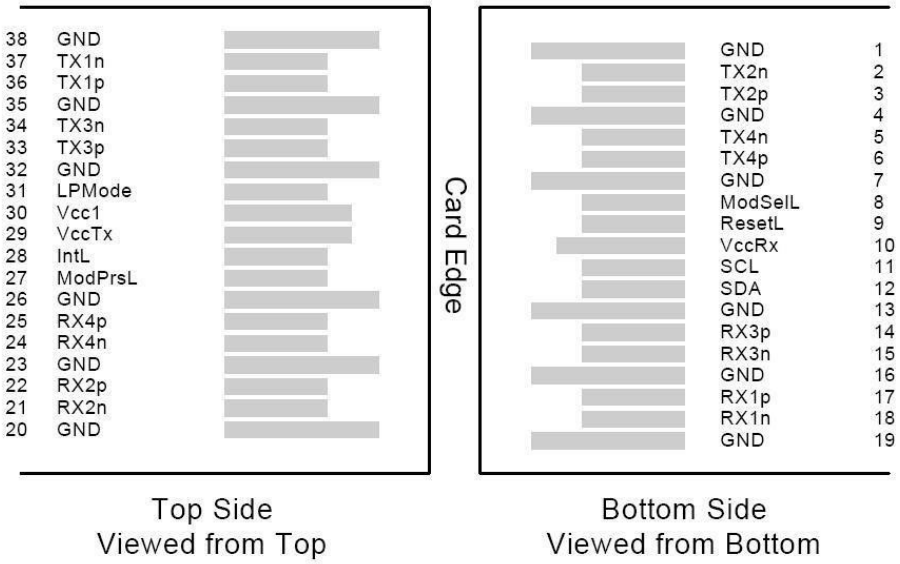
Average launch power of off transmitter(each lane)	P_{off}			-30	dBm
Outer Extinction Ratio	ER	3.5			dB
Optical Return Loss Tolerance	ORLT			15.1	dB
Receiver					
Center Wavelength	L1	1294.53	1295.56	1296.59	nm
Center Wavelength	L2	1299.02	1300.05	1301.09	nm
Center Wavelength	L3	1303.54	1304.58	1305.63	nm
Center Wavelength	L4	1308.09	1309.14	1310.19	nm
Damage threshold	Rdam	6.3			dBm
Average Receive Power (each lane)	Pin	-9.7		5.3	dBm
Input (each lane) Receiver Power (OMA_{outer}) (each lane)	OMA_{out}			5.1	dBm
Receiver reflectance	Pref			-26	dB
Stressed Receiver Sensitivity (OMA_{outer}) (each lane)	Sens			-5.2	dBm
Receiver Sensitivity (OMA_{outer}) (each lane) Note	Sen			-7.7	dBm

Note:
1.Measured with conformance test signal at TP3 for the BER specified in IEEE 802.3bs.

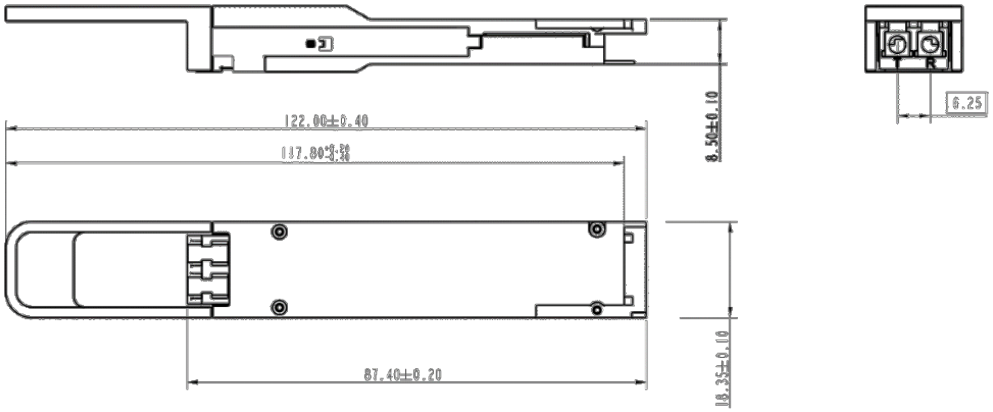
Pin Description

Pin	Logic	Symbol	Name/Description
1		GND	Module Ground
2	CML-I	Tx2-	Transmitter inverted data input
3	CML-I	Tx2+	Transmitter non-inverted data input
4		GND	Module Ground
5	CML-I	Tx4-	Transmitter inverted data input
6	CML-I	Tx4+	Transmitter non-inverted data input
7		GND	Module Ground
8	LVTTL-I	MODSEIL	Module Select
9	LVTTL-I	ResetL	Module Reset
10		VCCRx	+3.3V Receiver Power Supply
11	LVCMOS-I	SCL	2-wire Serial interface clock
12	LVCMOS-I/O	SDA	2-wire Serial interface data
13		GND	Module Ground
14	CML-O	RX3+	Receiver non-inverted data output
15	CML-O	RX3-	Receiver inverted data output
16		GND	Module Ground
17	CML-O	RX1+	Receiver non-inverted data output
18	CML-O	RX1-	Receiver inverted data output

19		GND	Module Ground
20		GND	Module Ground
21	CML-O	RX2-	Receiver inverted data output
22	CML-O	RX2+	Receiver non-inverted data output
23		GND	Module Ground
24	CML-O	RX4-	Receiver inverted data output
25	CML-O	RX4+	Receiver non-inverted data output
26		GND	Module Ground
27	LVTTL-O	ModPrsL	Module Present, internal pulled down to GND
28	LVTTL-O	IntL	Interrupt output, should be pulled up on host board[2]
29		VCCTx	+3.3V Transmitter Power Supply
30		VCC1	+3.3V Power Supply
31	LVTTL-I	LPMode	Low Power Mode
32		GND	Module Ground
33	CML-I	Tx3+	Transmitter non-inverted data input
34	CML-I	Tx3-	Transmitter inverted data input
35		GND	Module Ground
36	CML-I	Tx1+	Transmitter non-inverted data input
37	CML-I	Tx1-	Transmitter inverted data input
38		GND	Module Ground



Mechanical Specifications



Ordering Information

Part Number	Product Description
QSFP56-200G-LR4	QSFP56, 200GBASE-LR4 Transceiver, 10km over SMF, PAM4

Important Notice

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