ASIC (Application-Specific Integrated Circuit) design flow

1. **Chip Specification** – Define overall chip goals and architecture.

2. **Partitioning of Chip** – Divide the chip into functional blocks.

3. **Design Entry –**This is the process of writing the RTL code (using Verilog or VHDL) that describes the functionality of the chip.

   Functional Verification – This process checking whether the RTL design meets the intended specifications.
(It involves testbenches, simulations, and assertions to detect logical errors early in the design cycle.)

4. **RTL Synthesis** – Convert RTL code into a gate-level netlist.

5. **Design for Test (DFT) Insertion** – Insert scan chains and test logic.

6. **Floor planning** – Allocate chip area for blocks and define power/ground layout.

7. **Clock Tree Synthesis (CTS)** – Build a balanced clock distribution network.

8. **Place and Route (P&R)** – Route interconnections between placed components.

9. **Final Verification** – Perform checks: LVS, DRC, STA, etc.

10. **GDS II Generation** – Export the final layout for fabrication.