✅ RJ Semiconductor AXI Verification IP (VIP)

Overview

RJ Semiconductor's AXI Verification IP is designed to **speed up the verification process** for systems based on the AMBA AXI protocols — **AXI4, AXI3, and AXI4-Lite**. It offers rich features to ensure **protocol compliance, functional correctness**, and helps with **faster convergence** in the verification cycle.

This VIP integrates seamlessly with **Universal Verification Methodology (UVM)**, offering all standard components required for building a robust testbench for AXI interfaces.

With built-in protocol checks, debugging tools, sequencers, and coverage models, it ensures your SoC design meets protocol standards and performs as expected.

🔩 AXI Protocol Support & Features

- Full support for **AXI4, AXI4-Lite, and AXI3 protocols**
- **Configurable number of Masters (Managers) and Slaves (Subordinates)**
- Includes **Interconnect model** to simulate real SoC topologies
- **System Monitor** to track system-wide transactions
- **Protocol-aware sequencers** at port and system level
- Rich **sequence library** to create reusable and configurable traffic
- Built-in **protocol checks** to validate interface compliance
- **System-level data integrity checks** for end-to-end validation
- **Functional coverage model** included to track coverage goals
- Debug features:
    - **Transaction tracking** on waveforms
    - **Protocol analyzer** for in-depth debugging
- **Timing controls**:
    - Add delays for `VALID` and `READY` signals

    - Inject signal values during idle/bubble periods
- **Built-in scoreboarding** to compare expected vs actual data
- Support for both **directed and random** traffic generation
- Can be used in **UVM** environments.

🌟 Key Benefits of RJ AXI VIP

- 🚀 **Faster Verification Cycles** – Reduce time to reach verification closure
- 🔁 **Reusable & Scalable** – Use across projects and adapt to any system size
- 🧪 **Thorough Protocol Checking** – Ensures AXI compliance from start to end
- 🐞 **Easier Debugging** – Transaction-level tracking simplifies error finding
- 📊 **Built-in Coverage Tracking** – Helps ensure no test gaps
- 🔧 **Highly Configurable** – Easily adjust to simple or complex SoCs
- 🖥️ **Developer-Friendly** – Reduces manual effort and boosts productivity
- 🔄 **End-to-End Integration** – Ideal for verifying individual IP blocks or full SoC

💼 Where RJ AXI VIP is Used (Applications)

- ✅ SoC/ASIC functional verification
- ✅ AXI IP verification (e.g., DMA, BRAM, AXI bridge)
- ✅ FPGA/RTL-level AXI component testing
- ✅ System-level simulations and integration testing

- ✅ Used in industries like:
    - 📱 Mobile/IoT Chips
    - 🚗 Automotive SoCs
    - 🎮 Gaming and Graphics Processors
    - 📡 Networking and 5G Infrastructure
    - 🧠 AI/ML Accelerator Chips
    -

🔄 AXI Interface Signals

🟦 Write Address Channel (AW)

`AWID`, `AWADDR`, `AWLEN`, `AWSIZE`, `AWBURST`, `AWLOCK`, `AWCACHE`, `AWPROT`, `AWVALID`, `AWREADY`

🟩 Write Data Channel (W)

`WID` (AXI3 only), `WDATA`, `WSTRB`, `WLAST`, `WVALID`, `WREADY`

🟥 Write Response Channel (B)

`BID`, `BRESP`, `BVALID`, `BREADY`

🟨 Read Address Channel (AR)

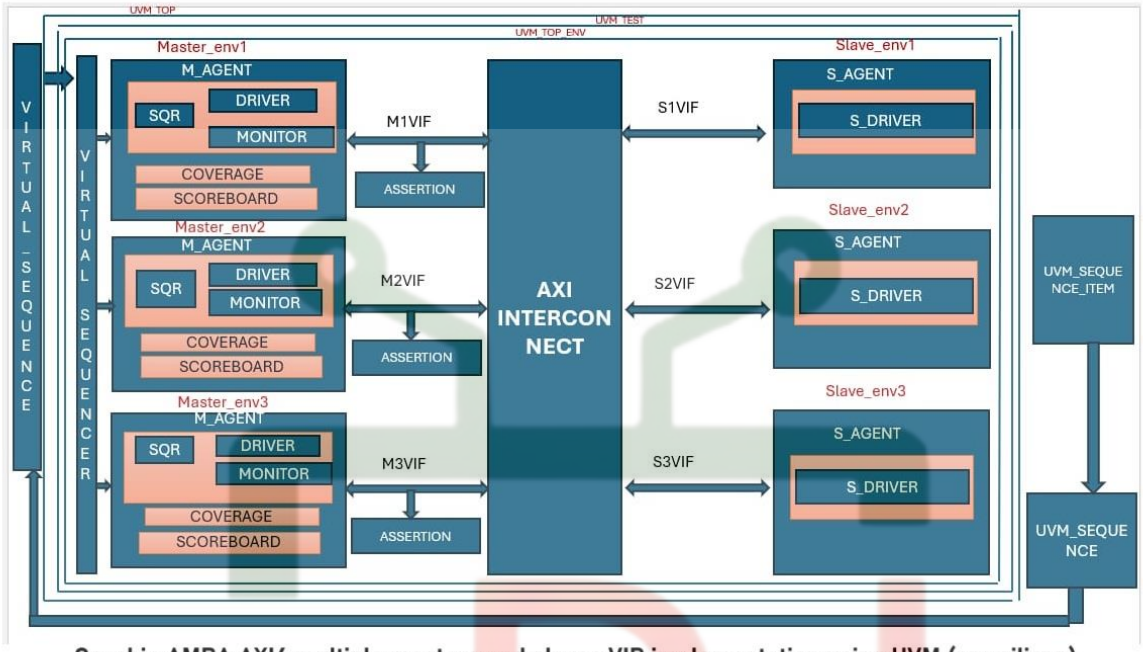
`ARID`, `ARADDR`, `ARLEN`, `ARSIZE`, `ARBURST`, `ARLOCK`, `ARCACHE`, `ARPROT`, `ARVALID`, `ARREADY`

🟪 Read Data Channel (R)

`RID`, `RDATA`, `RRESP`, `RLAST`, `RVALID`, `RREADY`

🧩 UVM Testbench Components

Component	Function
UVM Agent	Encapsulates driver, monitor, sequencer
UVM Driver	Drives AXI signals to DUT
UVM Sequencer	Issues AXI sequences
UVM Sequence/Item	Defines read/write AXI transactions
UVM Monitor	Observes DUT behavior passively
UVM Scoreboard	Compares actual vs expected behavior
UVM Environment	Manages all UVM components
UVM Test	Top-level stimulus generator
UVM Config DB	Parameter/control sharing across components
Coverage Collector	Monitors functional and protocol coverage



On-chip AMBA AXI4 multiple masters and slaves VIP implementation using UVM (pre silicon)