RJ Semiconductor DDR Solution.

Overview

RJ Semiconductor DDR IP is a family of high-speed interface solutions optimized for **High-Performance Computing (HPC)** and **data center** applications. The IP supports fast integration into any **System-on-Chip (SoC)** and works as a complete memory subsystem when paired with **Denali DDR Controller IP**.

Key Benefits

- **High-speed performance** up to **10 Gbps**
- Seamless integration with SoCs using AXI and DFI interfaces
- Product-optimized variants for **DDR3** and **DDR4**
- Verified and silicon-proven
- Extensive configuration options for power, performance, and area

DDR PHY IP Features

- **Supports DDR4/DDR3 training**:
  - Write-leveling
  - Data-eye training
- **Low power control** with **optional clock gating**
- **Loop-back modes**:
  - Internal
  - External datapath
- **Advanced I/O Pads**:

    - Impedance calibration logic
    - Data retention capability
- **Per-bit deskew (PVT compensated)** on read/write paths
- **RX and TX equalization** to support heavily loaded systems

DDR Controller IP Features

- **ECC Support**:
    - Sideband and in-line **SEC/DED ECC**
- **RAS Features**:
    - Error scrubbing
    - Parity check
- **Memory Compatibility**:
    - DDR5/4/3
    - LPDDR5/4X/4/3
- **DFI Compliance**:
    - Up to **DFI 5.0**
- **AXI Interface Support**:
    - **AMBA 4 AXI** protocol
    - Single & multi-port options
    - **QoS features**: Command prioritization

Applications

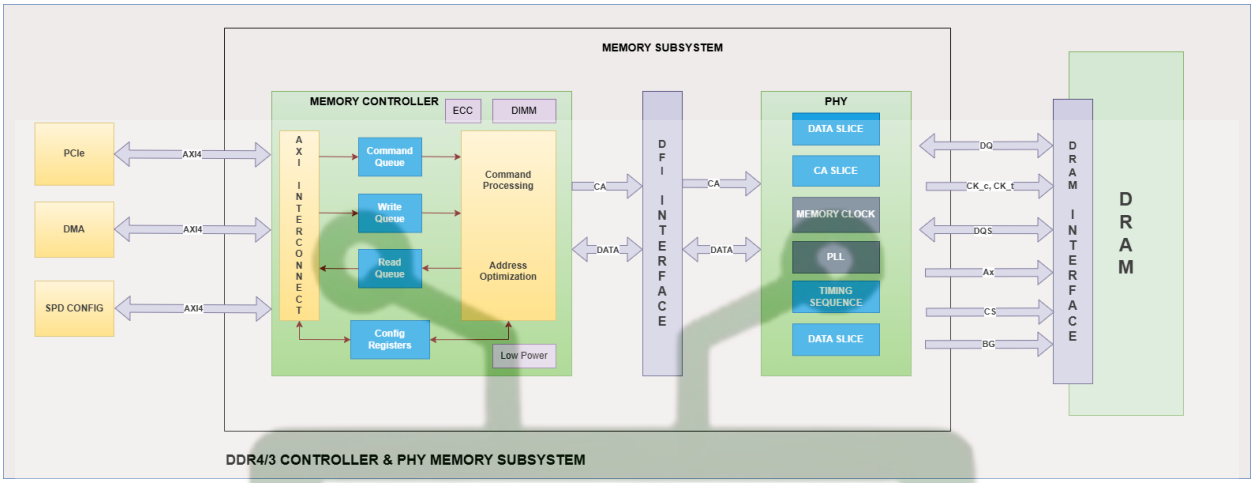
- High-performance computing (HPC) systems
- Data centers & server memory subsystems

- AI/ML accelerators
- Networking devices
- Automotive SoCs
- Storage controllers
- Embedded systems requiring fast DDR access

DDR3 vs DDR4 – Key Differences

Feature	DDR3	DDR4
Data Rate	800–2133 MT/s	1600–3200+ MT/s
Voltage	1.5V (typical), 1.35V (low)	1.2V (typical), 1.05V (low)
Prefetch Length	8n	8n
Bank Groups	Not Available	4 Bank Groups
Burst Chop	Yes (BC4, BL8)	No (Only BL8 supported)
Command/Address Bus	Single-ended	Differential (higher signal integrity)
Power Saving Features	Limited	Enhanced (self-refresh, gear-down)
CRC on Data	Not Supported	Supported

Complete DDR Interface Block Diagram Overview



- **Masters**: PCIe, DMA, SPD Controller act as masters initiating read/write transactions
- **AXI Interconnect**: Connects masters to the DDR controller
- **DDR Controller**: Manages protocol, RAS, ECC, and QoS features
- **DFI Interface**: Connects controller to PHY
- **DDR PHY**: Handles electrical signaling, training, and interface timing
- **DRAM Interface**: Physical signals between PHY and DDR memory

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DDR3/DDR4 DRAM Signal Overview

Common DDR Signals:

Signal Category	Signals
Command/Address	`CK`, `CK#`, `CS#`, `RAS#`, `CAS#`, `WE#`, `A[0:n]`, `BA[0:2]`
Control	`ODT`, `RESET#`, `CKE`
Data	`DQ[0:63]` (data lines), `DQS[n]`, `DQS#[n]` (strobe lines)
Power	`VDD`, `VSS`, `VDDQ`, `VSSQ`