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DATASHEET

MK.2TE Test System

ESD and latch-up test system

The MK.2TE Test System is a relay-based, exceptionally fast ESD and static latch-up test system used in the evaluation of advanced IC devices. It fully addresses today's JEDEC/ESDA standards, and can be configured with 128, 256, 384, or 768 test pins.

- Waveform network: 8-site HBM pulse source
- Human Body Model (HBM) and Machine Model (MM) testing to industry standards
- Latch-Up testing per current JEDEC EIA/JESD 78 method
- Preconditioning option allows DUT to be vectored with complex test and vector patterns for excellent control
- Highly repeatable, reproducible test data
- Enhanced data set features
- High voltage power supply chassis
- Power supply sequencing
- Event trigger output
- Comprehensive engineering vector debug
- Intuitive set-up and operation using the Thermo Scientific™ Scimitar™ software platform

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Rapid, high-throughput testing of complex IC devices

The Thermo Scientific™ MK.2TE™ ESD and Latch-up Test System provides users with advanced capabilities to test high pin count devices to today's Human Body Model (HBM) and Machine Model (MM) ESD standards. The system's pulse delivery design ensures waveform hazards noted in the standards, such as the trailing pulse and the pre-discharge voltage rise, are addressed. Trailing pulses have been shown to cause non-ESD related failures by exposing the DUT to an electrical overstress after the main HBM event. Pre-discharge voltage can cause voltage-triggered protection structures to fail, as the pin under test may not be at zero volts when the HBM event occurs. A user-selectable 10K Shunt can be connected during the pulse to eliminate any voltage prior to the actual HBM event. The MK.2TE Test System combination also performs Latch-Up testing per the JEDEC JESD 78 method. Its enhanced data set features provide the flexibility to meet the testing needs of today's system-on-chip designs.

Easy-to-use testing operations

The MK.2TE Scimitar Windows®-based software is both intuitive and comprehensive. Tests are set-up quickly, and user training requirements are minimal.

Consistent, precise ESD waveforms

By locating multiple discharge networks close to the test fixture board, unwanted stray inductance and capacitance is kept to a minimum at every pin. This ensures excellent in-test waveform quality and easily reproducible test data.

Advanced controller and communications

A powerful, extraordinarily fast embedded VME controller drives the highest Speed-of-Test execution available. Data transfer between the embedded controller and the tester's PC server, is handled through TCP/IP communication protocols, minimizing data transfer time. The tester's PC server can be accessed through internal networks, as well as through the Internet allowing remote access to the system to determine the systems status or to gather result information.

Define, achieve and sustain your test objectives

The MK.2TE Test System's flexible modular design and options enable you to upgrade on-site when corporate or industry standards change. Options include additional pins, V/I supplies, high speed vectoring capabilities, and test features.

Reach the next level of success

Experience the many benefits of working with recognized experts in the field of component reliability ESD and Static Latch-Up testing. Our goal is to support you with lifelong service — from applications support, calibration services, service contracts, and field service scheduling to full technical field support. We can help you reach that next level of success.

General specifications		
Test devices up to 768 pins; systems available configured as 128, 256, 384, 512 or 768 pins	Additional capability, faster throughput, multi-site testing, field upgradeable	
Relay-Based Operations	Enables test speeds 5 to 10 times faster than robotic-driven testers	
Waveform Network	8-site HBM pulse source with 100pF/1500Ω. Patented design ensures waveform compliance for technology generations to come	
High Voltage Power Supply Chassis	Modular chassis with patented HV isolation enables excellent pulse source performance	
Power Supply Sequencing	Additional flexibility to meet more demanding test needs of integrated system-on-chip designs	
Event Trigger Output	Manage your setup analysis with customized scope trigger capabilities	
Human Body Model (HBM)	100pF/1500Ω network, per ESDA, ESDA/JEDEC JS-001, MIL-STD 883, and AEC Q100-002 specs, 30V to 8kV Test to multiple industry standards in one integrated system; no changing or alignment of pulse sources	
Machine Model (MM)	200pF/0Ω network, per ESDA STM5.2, JEDEC JESD22-A115, and AEC Q100-003, 30V to 2kV Integrated pulse sources allow fast multi-site test execution	
Static Latch-Up Testing	Per JEDEC JESD 78 and AEC Q100-004. Optional static Latch-Up testing allows control of DUT pins using embedded bias supplies	
Pin Drivers	For use during Latch-up testing and parametric measurements. Vector input/export capability from standard tester platforms	
64k Vectors per Pin with Read-back Up to 10MHz Vector Rate Programmable from an Internal Clock	Full real-time bandwidth behind each of the matrix pins Quickly and accurately set the device into the desired state for testing	
Up to Six Separate V/I Supplies (1 stimulus and 5 bias)	DUT power, curve tracing, and Latch-up stimulus with 4-wire sensing at the DUT board for high accuracy. System design also provides high current capability through the V/I matrix	
Multiple Self-test Diagnostic Routines	Ensures system integrity throughout the entire relay matrix, right up to the test socket	
Test Reports	Pre-stress, pre-fail (ESD) and post-fail data, as well as full curve trace and specific data point measurements. Data can be exported for statistical evaluation and presentation	
Individual Pin Parametrics	Allows the user to define V/I levels, compliance ranges, and curve trace parameters for each pin individually	
Enhanced Data Set Features	Report all data gathered for off-line reduction and analysis; core test data is readily available; all data is stored in an easy-to-manipulate standard XML file structure	
Comprehensive Engineering Vector Debug	Debug difficult vectoring setups with flexibility	
Interlocked Safety Cover	Ensures no user access during test. All potentially lethal voltages are automatically terminated when cover is opened. Safety cover window can be easily modified to accept 3rd party thermal heads	
Dimensions / Weight	63 cm (23.5 in) W x 85 cm (33.5 in) D x 109 cm (43 in) H; 109 kg (240 lbs)	
Low resolution/high accuracy parametric measurements using an embedded Tektronix Keithley PSU	With the optional Tektronix Keithley PSU feature (replaces one V/I), nA measurements are achievable, allowing supply bus resistance measurement analysis to be performed	
Power Requirements	Operating Temperature Non-operating temperature Humidity Range	+15°C to +40°C (+59°F to +104°F) 4°C to +60°C (+40°F to +140°F) 30-60% non-condensing
Temperature Range	System Computer and Monitor	90-250 VAC, 10A, 50/60 Hz 100-240 VAC, 6.5A, 50/60 Hz

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Scimitar software features
Summary Panel with easy navigation among test plan and device plan components
Wizard-like prompts on multi-step user actions
Control of external devices through the use of Scimitar's user programmable Plug-in capabilities, in addition to the Event Trigger Outputs, which provide TTL control signals for external devices, such as power supplies or for triggering oscilloscopes
Flexible parametric tests that are defined and placed at an arbitrary position within the executable test plan
Comprehensive results viewer that provides: ESD and Static Latch-up data viewing capabilities Curves viewer with zooming capabilities and the ability to add user comments Data filtering on the following criteria – failed pins, failed results, final stress levels A complete set or subset of results using user defined parameters Sorting in ascending or descending order by various column criteria
Tree-like logical view of the tests and test plans
Flexible data storage that provides the ability for the end-user to query the data
Seamless support of existing ZapMaster, MK.2, MK.4, and Paragon test plans
Curve tracing with curve-to-curve and relative spot-to-spot comparison
Off-line curve analyzing, including third-party generated waveforms
Canned JESD78A test (static latch-up only) that can be defined automatically
Pause/Resume test capabilities
Intermediate results viewing
Automated waveform capture capability and analysis using the embedded EvaluWave software feature
Curve tracing with curve-to-curve and relative spot-to-spot comparison
Pause/Resume test capabilities
Full support for the latest JS-001 test standard combinations
Capability to induce a latch up condition using pulses compliant with standard test models (TLU test type)
Instrumentation support for third party instruments – oscilloscopes, source-meter units, power sources, heat streams, etc.
Realistic representation of the package under test. Variety of sources available for importing outlines into new or existing test plans
Wide range of device and result data visualizers; comprehensive waveform and statistical data analysis tools

Find out more at **thermofisher.com/EM-Sales**

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