Latch-up Characterization and Checking of a 55 nm CMOS Mixed Voltage Design

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Abstract: Mixed Voltage Design has become predominant in the semiconductor industry due to the integration of high voltage and low voltage circuits in the pad ring. Latch-up characterization and analysis of a 55 nm CMOS technology has been done to determine the effects of various protection strategies on the trigger and holding parameters of SCRs to develop a design rule checker.

I. Introduction

Latch-up [1-10] can be described as the formation of low resistance current carrying path between the power supply and ground terminals, through parasitic coupling of injecting junctions which form a PNPN Silicon Controlled Rectifier (SCR) structure as shown in Figure 1.

On the VDD-to-VSS transition the I/O can undershoot the VSS potential causing electrons to be injected into the p-well and collected by the n-well. The voltage drop across the n-well resistance R_W causes the vertical PNP to trigger and turn-on the SCR. The holes supplied by PNP provide base current for NPN thus forming a positive feedback loop. The positive feedback loop with a high enough loop gain [16,18], switches the SCR into a high conductivity state (holding condition) that is sustained mainly by the carriers injected from the p+ diffusion connected to VDD and the n+ diffusion connected to VSS. Even after the I/O voltage has returned to 0, the high conductivity state is maintained due to the presence of strong positive feedback and latch-up is said to have occurred. Such a latching condition triggered by a transient on an internal node of the SCR is referred to as internal latch-up [9]. Another latch-up scenario is external latch-up. This occurs if the node I/O1 in the SCR in Figure 1 is connected to VSS and the node I/O2 in the SCR is connected to VDD and the SCR is triggered by carriers emitted "elsewhere" (as in from an adjacent undershooting or overshooting I/O pad). Latch-up protection and verification has to account for both the aforementioned scenarios [9].

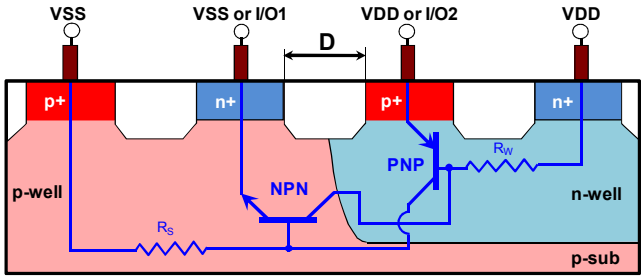

Figure 1: SCR Cross-Section Showing Parasitic Coupling between Diffusions Connected to VDD and VSS

The trigger and holding points are identified in the SCR IV characteristic as shown in Figure 2. The trigger point (T) defines the switching point of the SCR into its high conductivity state. The operation in the high conductivity state of the SCR is characterized by the holding point (H). The SCR holding voltage (*Vh*) is defined as the x-intercept (voltage axis) of the tangent line drawn at the minimum of the IV curve after snapback triggering. The necessary conditions for latch-up to occur are:

1. The power supply voltage (*VDD*) has to be greater than the holding voltage (*Vh*). The difference between the *Vh* and *VDD* defines the latch-up protection window.
2. The power supply must be able to supply current required to support the holding condition of the SCR.

Hence, latch-up protection and immunity can be characterized in terms of the difference between the supply voltage and the holding voltage of the parasitic PNPN. The strength of the positive feedback (loop gain) between the injecting emitters of the parasitic PNPN determines the holding voltage [16,18,19]. The positive feedback level in general depends on the spacing (*D*) between the injecting emitters. A smaller value of *D* leads to higher coupling (higher loop gain) and thus a lower holding voltage. A

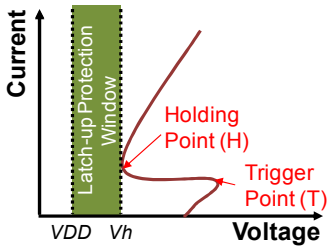

Figure 2: SCR IV Characteristic Showing the Latch-up Protection Window

lower holding voltage collapses the latch-up protection window and thus results in lower latch-up immunity.

The purpose of this work is to extract and construct layout and electrical (voltage based) design rules for latch-up free operation in a 55 nm CMOS technology through experimental characterization. The goal is to use candidate test structures which reflect the most commonly used latch-up protection strategies and extract the holding voltage. The focus is on the effects on the holding voltage of the lateral isolation/spacing *D* of p+ and n+ emitters (Figure 1) with and without efficient guard rings [1,2,4]. The rules are derived with the aim of pushing the holding voltage of any parasitic SCR in adjacent I/O pads above the supply voltage for the power domain under scrutiny. Experimental characterization is further supplemented with TCAD device simulation analysis of the trends for predictive design rule construction. Finally, implications for mixed voltage I/O design are discussed based on the analysis and related design rules.

II. Latch-up Risks in Mixed Voltage Applications

Latch-up protection and immunity has become more important with the increasing trend in the industry to embrace system-on-chip (SoC) designs. This has resulted in the integration of high voltage circuits on low voltage deep submicron CMOS technologies as required by the application environment. A few examples of such circuits are high-voltage tolerant I/O interfaces like the USB, on-chip charge pumps and regulators to support high voltage outputs. As a result of increasing integration, modern IC's can consist of multiple power domains in the pad ring. This has strong implications from the latch-up standpoint because in order to make the designs latch-up free, the holding voltage of any victim parasitic SCR must be pushed higher than the supply voltage of the domain that powers it. This can be illustrated with the following example shown in Figure 3.

The circuit shown in Figure 3 is a 2X charge pump. The function of this circuit is to create a high voltage 7.2V VDDH (2X VDDM) potential from the medium voltage (3.6V) VDDM supply voltage by switched capacitive voltage doubling using power MOSFETS MPHM, MPH, MPM, MNM and an external or internal capacitor. VDDH can be used as a power supply for output drivers in high voltage applications and systems. The fundamental circuit operation is as follows. During the first half of a clock cycle, MNM and MPHM are held 'on', and MPM and

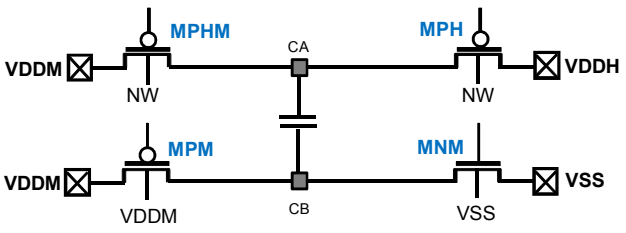

Figure 3: 2X Charge Pump

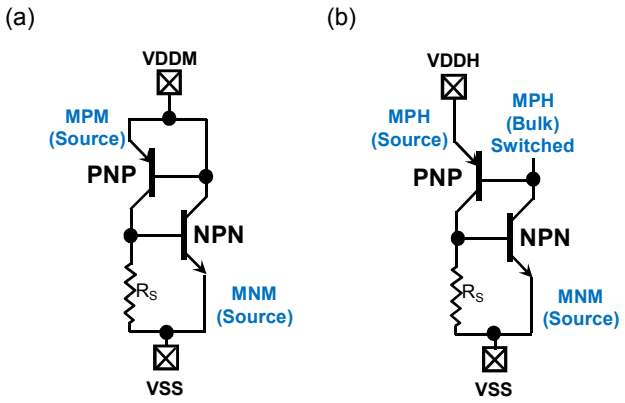

Figure 4: (a) MV VDDM-VSS SCR, (b) HV VDDH-VSS SCR.

MPH are 'off'. The capacitor is charged to voltage VDDM. During the second half of a clock cycle, MNM and MPHM are switched 'off', and MPM and MPH are switched 'on', placing the capacitor in series with VDDM, and pumping VDDH to 2X VDDM. The PMOS bulk, node NW, is dynamically switched to the highest on-chip potential. The power MOSFETs are laid out very close to the pads to reduce the contribution of metallization resistance to the output series resistance and hence are susceptible to latch-up triggering. There are two power domains in this circuit, VDDM and VDDH respectively. Parasitic SCRs device can be identified in each power domain:

- **VDDM-VSS SCR** (Figure 4a): MPM-MNM parasitic coupling between the p+ source of high side PMOS connected to VDDM and n+ source of the low side NMOS connected to VSS.
- **VDDH-VSS SCR** (Figure 4b): MPH-MNM parasitic coupling between the p+ source of high side PMOS connected to VDDH and n+ source of the low side NMOS connected to VSS. The bulk of the high side PMOS is switched to highest voltage on the chip during power-up of the charge pump. It is switched to VDDM initially when VDDH is 0 V and then switched to VDDH as VDDH becomes greater than VDDM. The relatively high-impedance connection of the bulk of MPH effectively lowers the trigger threshold for this SCR for any negative/electron injection in the neighborhood of this SCR.

The implementation of the gate-drive logic gates and the NW switching circuit for the charge pump power MOS devices are beyond the scope of this work, but these circuits can also have parasitic SCRs in both the VDDH and VDDM power supply domains. If these circuits are present near the pad-ring, they are susceptible to external latch-up triggering through current injected at nearby I/O pads. Due to VDDH value being twice as much as VDDM, any parasitic PNPN SCR present in the VDDH domain must be designed to have a higher holding voltage than the one present in the VDDM power domain. Hence, a larger spacing must be used to separate MPH and MNM as compared to that used for MPM and MNM isolation. Having separate rules for the two supply domains ensures

latch-up free operation while optimizing layout area by preventing the application of high-voltage domain isolation rules in the low-voltage domain.

III. Latch-up Protection Strategies and Verification/Rule Checking

The verification of latch-up protection networks in modern integrated circuits is a difficult challenge due to increasing design and process complexity, higher-pin counts and the overall computational difficulties in dealing with large data sets. Relying on manual verification alone poses a significant risk of missing hidden latch-up pitfalls. Consequently, automated latch-up rule checking is highly desired.

Traditional latch-up geometrical rule checks using DRC tools can only provide limited verification. These checks are typically focused on layout topology while electrical information for latch-up risk areas throughout the chip is not readily available.

Layout based rules are still very important for preventing latch-up. The most commonly used techniques/rules are [1,2,4,8,10]:

- Lateral separation (distance) of p and n emitters
- Lateral isolation of p and n emitters with guard rings (carrier collection) and well/substrate ties (potential control)
- Vertical isolation with the use of deep n-well if a deep n-well process option is available

While the presence of guard rings and well/substrate ties can be verified using layout based DRC, their effectiveness in collecting carries needs to be validated using additional resistance checks.

Values of supply voltage and I/O pad voltage are also very important to assess latch-up risk. The specification of the n+ to p+ emitter spacing value *D* depends on the I/O and VDD voltage. The strength of the coupling (spacing *D*) between the injecting emitters of the parasitic PNPN determines the holding voltage (*Vh*). Higher supply voltage domains, require higher holding voltage conditions to maintain the latch-up protection widow and thus the immunity. Higher holding voltages in parasitic PNPN structures require more isolation between injecting emitters i.e. a larger spacing *D*. Using voltage propagation capabilities [11] the latch-up risk for supply domain under scrutiny needs to be assessed and design rules constructed accordingly for latch-up free operation. This avoids the specification of overly conservative design rules which are based on the highest voltage level present in the system which requires the highest amount of isolation (i.e. a larger value of *D*).

An optimum latch-up verification flow should take into consideration both electrical and layout topology context to provide broad and flexible design rule coverage. It should also allow incremental verification as a design progresses, to avoid late-stage changes just before tape-out. The integration of latch-up checking tools into the standard design flow allows these rules to be used directly by IC designers to identify and correct most latch-up issues during the early design phase.

Figure 5 shows block diagram of an advanced latch-up verification flow which incorporates the above-mentioned features:

1. First, all external nodes are identified.
2. Secondly, externally connected diffusions are checked to identify possible latching paths.
3. This is followed by establishing latch-up electrical context, where voltage is propagated down to the diffusions to assess latch-up risk.
4. If diffusions are protected with guard rings, they are validated for their efficiency to collect injected carriers. This involves both guard ring continuity and resistance checks.
5. At the next verification step, full latch-up layout context for the path at risk is established. The checks at this step include verification of diffusion and well spacing, tie frequency rules, etc.
6. Based on the information collected in steps 1 through 5, an Electrical Design Automation (EDA) checker performs an analysis and either validates the layout or reports a latch-up error.

A detailed example of an automated latch-up check run on a 55 nm technology node using Mentor Graphics' PERC is shown in section V of this paper.

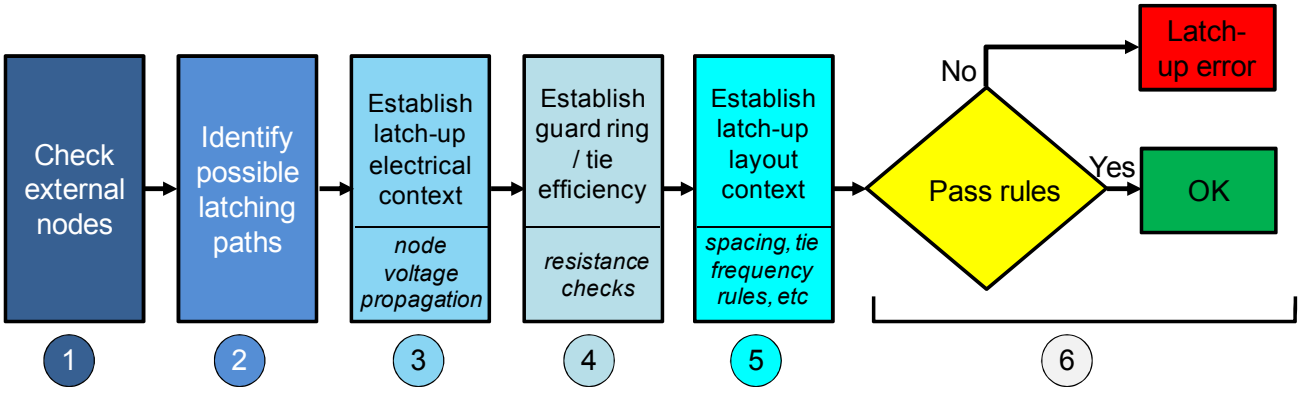

Figure 5: Block Diagram of an Advanced Latch-up Verification Flow

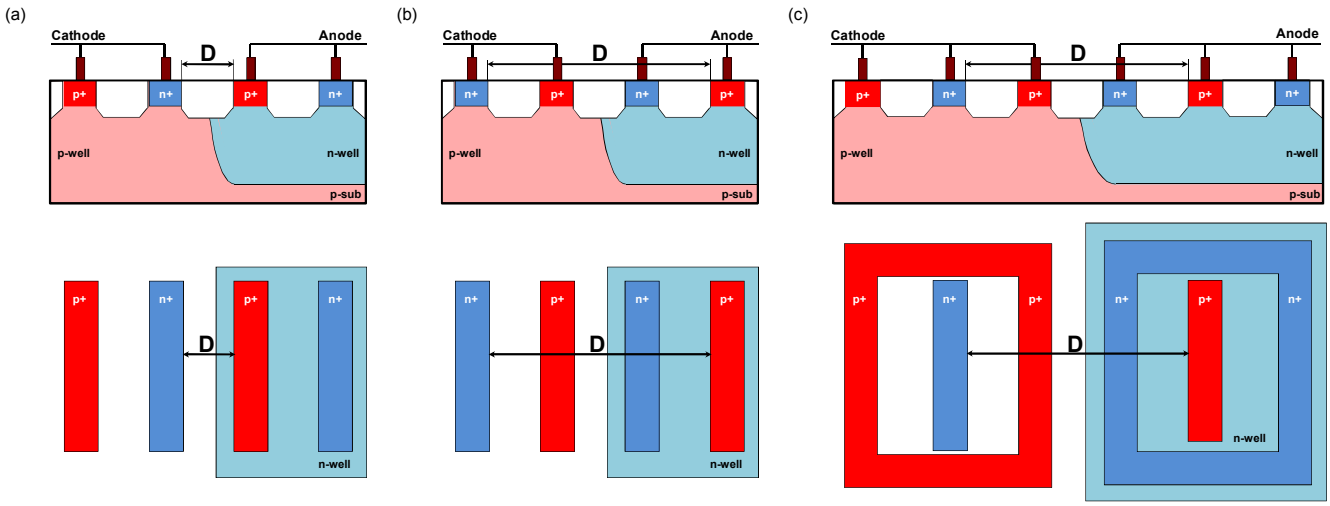

Figure 6: Latch-up Test Structures: (a) No Guard Ring; (b) Single Guard Ring Stripe; and (c) Single Guard Ring Enclosed Emitter

IV. Characterization and Analysis of a 55 nm CMOS Technology

A. Device Structure

Test structures in a 55 nm CMOS technology node are selected to emulate the most common latch-up protection scenarios. Figure 6 shows test structures for characterizing the p+ to n+ emitter latch-up isolation requirements for the following cases:

- No guard rings.
- Single guard stripes between p+ and n+ emitters.
- Single guard rings encircling the emitters: A p+ guard ring encloses a multi-finger NMOS device (n+ emitter) and an n+/n-well guard ring encloses a multi-finger PMOS device (p+ emitter).

All diffusions are 60 µm long. The p+ to n+ emitter spacing (*D*) is varied in the test structures to determine the effects on the holding voltage (*Vh*).

B. Experimental Data

An HPPI 50 Ω TLP programmable pulse generator with long pulse widths is used to apply voltage to the anode/n-guard ring terminal of the test structures with the cathode terminal grounded. This triggers snapback in the device under test (DUT) and the trigger current and holding voltage can be extracted from the snapback curve. Holding voltage for design rule derivation purposes was defined as the x-intercept of the tangent line to the high current portion of IV curve at the minimum voltage point after snapback**.** The TLP method with pulse-width control was chosen for experimental characterization to study structures with different levels of self-heating. This is especially important for probing the higher holding voltage structures (for example structures with guard rings and low tap spacings) as testing them under DC conditions with parameter analyzers can lead to failure caused by self-heating. Hence, in order to perform consistent comparisons of all the results the TLP method was chosen for IV data collection for all the structures. Long pulse widths are used to account for device self-heating and emulate the long pulses used in the static JESD78C latch-up current injection tests [15]. The use of 50 Ω load line was sufficient and justified for all the layout topologies. The test structures were made large by design and the resistance in the holding condition was found to be quite low. The extracted IV curves for the lower holding voltage structures (No guard rings) were found to be almost vertical and parallel to the tangent at the minimum voltage point after snapback triggering. For the higher holding voltage structures (with guard rings) the 50 Ω load line was able to capture the portion of negative differential resistance (NDR) region of the SCR IV curve preceding the holding point. Thus, the holding voltage determination based on the definition given in Section 1 was not affected by the 50 Ω load line.

Figures 7 and 8 illustrate the snapback I-V curves as a function of increasing p+ to n+ spacing, for the no guard ring and single guard ring cases. Spacing B is about 1.5 times spacing A1 and about 1.1 times spacing A2. The effect of inserting guard rings can be seen from Figure 9,

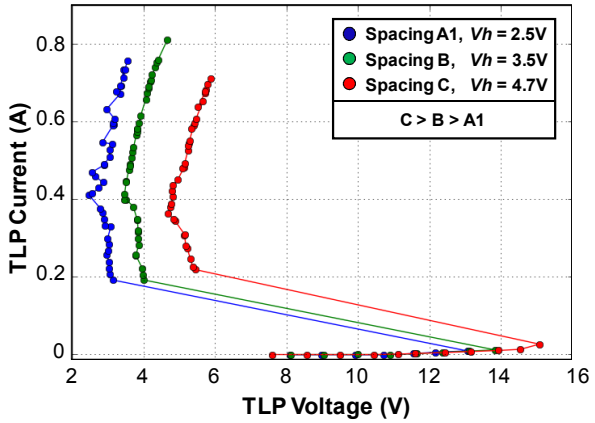

Figure 7: Measurements for No Guard Ring SCRs vs. p+ to n+ Emitter Spacing at 1.5 µs Pulse Width

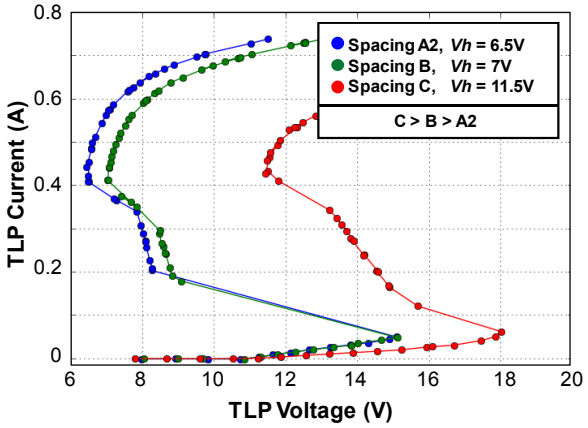

Figure 8: Measurements for Single Guard Ring SCR vs. p+ to n+ Emitter Spacing at 1.5 µs Pulse Width

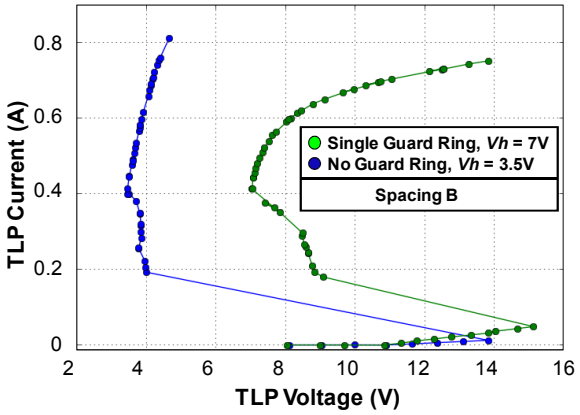

Figure 9: Holding Voltage vs. Guard Ring: For the Same n+ to p+ Emitter Spacing B the Insertion of a Single Guard Ring Increases the Holding Voltage from 3.5V to 7V

which shows the curves for the no and single guard ring SCR, with the same emitter to emitter spacing.

The holding voltage increases with p+ to n+ emitter spacing for the no guard ring and single guard ring test structures as shown in Figure 7 and 8. For the same p+ to n+ emitter isolation spacing *D*, the addition of guard rings increases the holding voltage as shown in Figure 9 from 3.5V to 7 V.

The effects of inserting guard rings and also the effects of self-heating on holding voltage are further illustrated in Figure 10. Here, 8 µm wide multi-finger NMOS and PMOS devices were used, each with a 0.5 µm wide single guard ring surrounding the transistors: p+ guard ring surrounding the NMOS n+ and n+/n-well guard ring surrounding the PMOS p+. The rationale behind the choice of these structures was to represent typical layouts in the I/O area and to compare it to the case of a just a single guard ring stripe present between potential emitters. Structures implementing guard rings which completely enclose the emitters (cf. Figure 6c) yield higher holding voltages than guard ring stripe structures (cf. Figure 6b), for comparable isolation (*D*) and tap spacings. This is a consequence of the

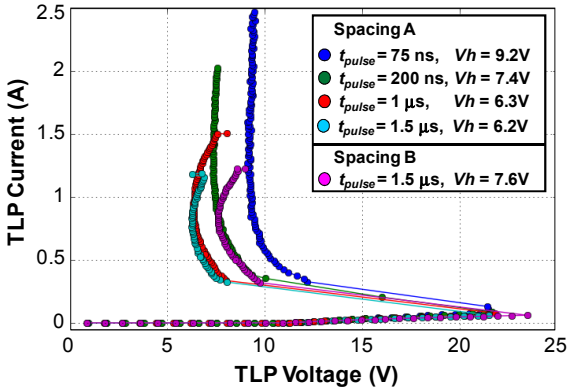

Figure 10: Single Guard Ring (Enclosing Emitter) Holding Voltage vs. Pulse Widths: The Holding Voltage for Spacing A Decreases from 9.2 V at a Pulse Width of 75 ns to 6.2 V at a Pulse Width of 1.5 µs Due to the Device Self-Heating. For 1.5 µs Pulses Device Failure is Observed Beyond 1.3 A for Both Spacing A and B

reduction in guard ring resistance (increase in collection efficiency) for the enclosed emitter structures.

The holding voltage decreases as a function of pulse width due to more self-heating and the subsequent rise in temperature associated with longer pulse widths. For instance, to account for self-heating in a 7.2 V supply voltage domain, a spacing greater than B with single guard ring would have to be employed to ensure latch-up free operation, as spacing A yields a holding voltage of 6.2V, which is less than the operating supply voltage. However, spacing B could be used, since it results in a holding voltage of 7.6V at long pulse widths, which exceeds the desired power supply operating voltage. Spacing B is 1.4 times Spacing A. It is also evident from Figure 10 that holding voltage difference between 1 µs and 1.5 µs is very small. Thus measurements taken at 1.5 µs are sufficient for design rule definitions.

The effect of temperature/pulse-widths on holding voltage has also been studied in [17,19]. It is clearly shown in these studies that higher temperature/self-heating causes the holding voltage of the SCRs to decrease. This is due to the following reasons [16-18,20]:

- An increase of the emitter injection efficiency due to reduction of the band-gap narrowing effect with temperature leads to stronger coupling/positive feedback between the n+ and p+ emitters and thus higher level of space charge neutralization.
- Higher resistivity of the wells due to reduction in carrier mobility.

The impact ionization coefficients decrease with an increase in temperature [18]. However, this effect is overcompensated by the increase in positive feedback (loop gain) between the n+ and p+ emitters due to the reasons given above.

C. TCAD Analysis

Experimental characterization of the various SCR topologies/test structures described above established the dependence of holding voltage (*Vh*) on emitter to emitter spacing (*D*) and the layout topology (single guard ring / no guard ring). To gain a better physical understanding of these trends 2-D mixed mode device simulations are performed using the DECIMM simulator [14]. A physical understanding of the holding voltage trends helps in holding voltage interpolation/extrapolation as a function of spacing *D* and the layout configurations. Since the experimental characterization was performed on a limited number of test structures, holding voltage interpolation helps in filling the gaps due to inadequate coverage of layout configurations and isolation spacings. This facilitates the creation of robust and optimal design rules for different layout topologies.

As mentioned earlier, the holding voltage is a function of the strength of positive feedback between the injecting n+ and p+ diffusions in a parasitic PNPN thyristor. The goal of the TCAD simulations is to uncover and illuminate the current flow paths/regions for the electrons and holes so that the strength of the positive feedback coupling between injectors, i.e. loop gain, can be analyzed. This aids in discerning the coupling/positive feedback level between the p+ and n+ emitter as a function of isolation spacing and the guard ring configuration.

The level of positive feedback has a direct impact on the degree of space charge neutralization [16,17,19] and consequently on the electric field and the holding voltage. Thus, the dependence of holding voltage on the underlying current transport physics in conjunction with the experimental characterization data can be exploited to define optimized design rules based on layout topology and the supply voltage.

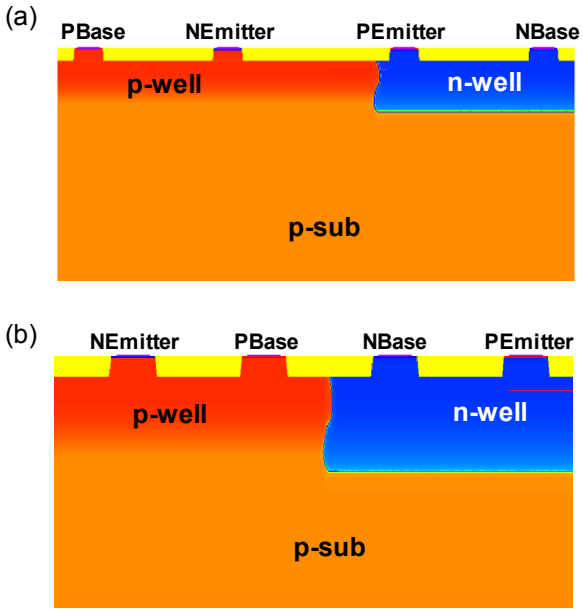

Figure 11: Simulation Test Structure Devices: (a) Baseline No Guard Ring; (b) Single Guard Ring

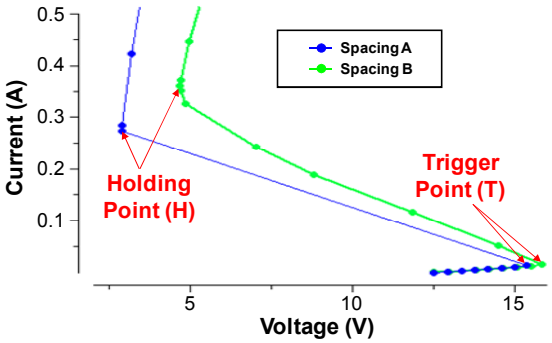

Figure 12: No Guard Ring, TLP Device Simulations.

The device cross-sections for the baseline no guard ring test structure and single guard ring test structure are shown in Figure 11. IV curves are simulated for these 2-D cross-sections by using ramped TLP source in the quasi-static IV simulation setup.

The baseline four-stripe no guard ring test structure is simulated with two different p+ to n+ emitter spacing corresponding to Spacing A1 and B in Figure 7. The simulated TLP IV curves are shown in Figure 12 and the simulation holding voltage is in reasonable agreement with the experimentally derived holding voltage data collected under equivalent conditions.

The electric field at the front side p-well/n-well junction is extracted for devices with spacing A and B, at the Trigger (T) and Holding (H) points, as shown in Figure 12 to gain an understanding of the increase in holding voltage. Lateral electric field (Ex) and electrostatic potential are measured across the junction along a cutline which intersects the high field region, as shown in Figures 13 and 14.

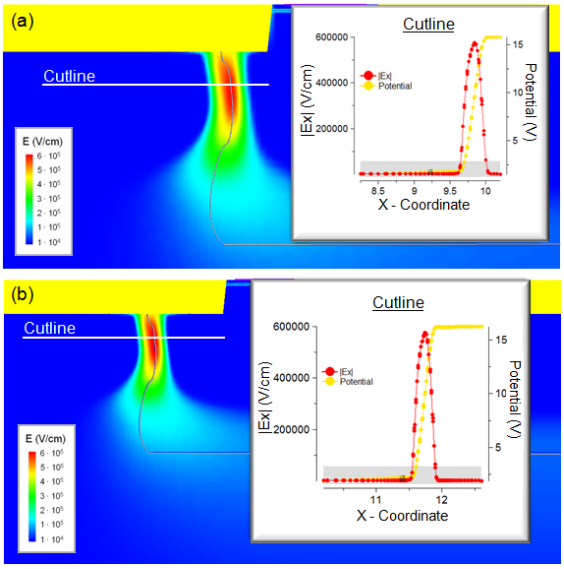

Figure 13: Simulated Electric Field and Potential at Trigger Point (T) for No Guard Ring Device with (a) Spacing A and (b) Spacing B

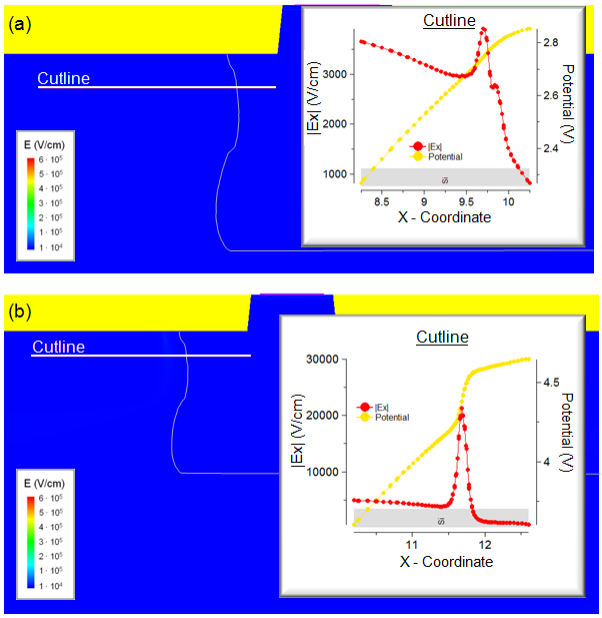

Figure 14: Simulated Electric Field and Potential at Holding Point (H) for No Guard Ring Device with (a) Spacing A and (b) Spacing B

At trigger point T (Figure 13), the field is very high for both spacing A and B test structures. This reflects the presence of space-charge and impact ionization regions [16]. The current flow at the trigger point is mostly sustained by avalanche injection from the high field impact ionization region at p-well/n-well junction.

The situation changes drastically at the holding point (H), as shown in Figure 14. The electric field decreases by almost two orders of magnitude for both spacing A1 and spacing B structures. Most of the potential variation is due to drift across the quasi-neutral regions. A high degree of positive feedback between the injecting emitters results in significant electron and hole current injection from the forward biased junctions. This leads to space charge neutralization and the decrease of the electric field [16]. The structure with smaller spacing A has stronger coupling between the forward biased injecting junctions and thus more space charge neutralization. As a result, the peak electric field is lower for smaller spacing A as compared to spacing B.

Simulation results for single guard ring structure with spacing B, including the IV curve, terminal currents, electric field and potential contours at the holding point, are shown in Figure 15. The high holding voltage as compared to the no guard ring case is due to the presence of a high electric field region due to a lower level of space charge neutralization. This is caused by the carrier loss at the n+/n-well and p+/p-well contact [16,19] as well as reduced positive feedback/coupling between the n+ and p+ emitters due to vertical current flow. The loss of carriers through the guard ring contacts is reflected in the high NBase current contribution of almost 54% at a holding current of 3mA/µm in Figure 15b. This implies that a majority of the electrons are collected at the n+/n-well contact, thereby reducing the

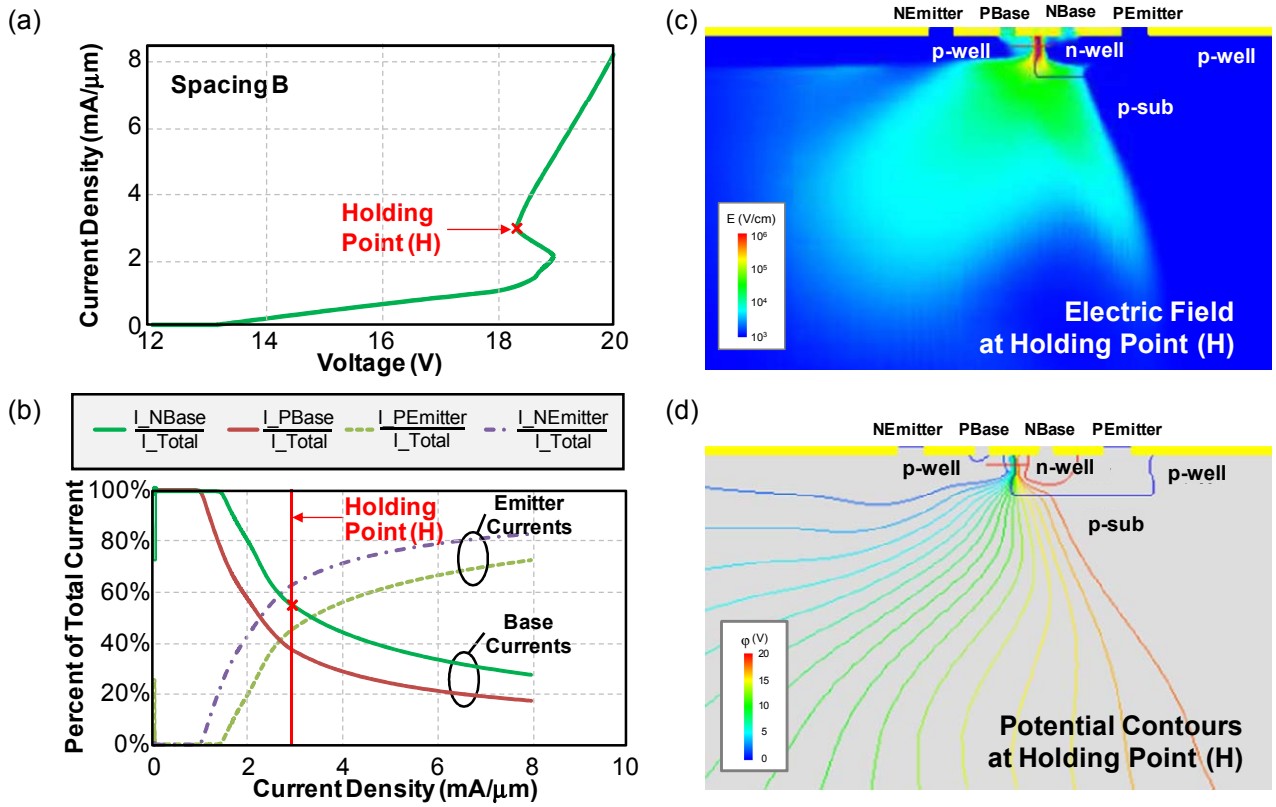

Figure 15: Simulation Results for Single Guard Ring Case: (a) IV Curve; (b) Normalized Terminal Currents; (c) Electric Field at Holding Point; (d) Potential Contours at Holding Point

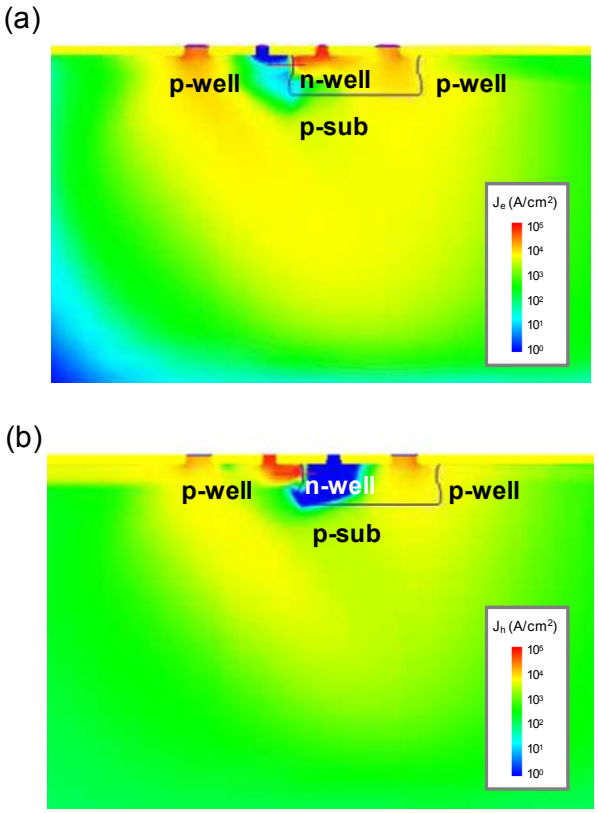

Figure 16: (a) Electron Current Density Distribution and (b) Hole Current Density Distribution at Holding Point for Single Guard Ring Case

electron base current flowing into the p+ emitter. This leads to reduced hole injection from the p+ emitter.

Current flow is predominantly vertical due to the field effect [8]. This is visible in the current density plots in Figure 16. The vertical electron current flowing through the n-well to the n+/n-well contact creates an electric field (potential gradient) that enhances the hole drift current in the opposite direction and degrades the transport of holes laterally. Similarly, the vertical hole current in the p-sub/p-well region enhances electron drift in the opposite direction and reduces the lateral electron current. Also as shown in Figure 16, the hole current flowing through the p-well on the right/backside side of the structure, enhances electron current in that region. Vertical hole current flow through the lightly doped p-sub also induces base push-out due to Kirk effect [18]. The quasi-neutral region extension is visible in the electric field and potential contour plots in Figure 15. The loss of lateral coupling between the injecting n+ and p+ diffusions and hole current induced base push-out cause a reduction in the overall level of positive feedback, thereby contributing to an increase in holding voltage.

While the simulated holding voltage for the no guard ring case was in good agreement with measurements, single guard ring simulation produced a holding voltage about 7V higher than the experimentally determined value. This discrepancy can be explained by the 2-D limitation of the performed simulations, whilst the real current flow is 3-D. Single guard ring stripe structure (as shown in Figure 6b) triggers in an inhomogeneous fashion with enhanced current conduction through the short sides and backside [21]. Due to the presence of highly doped p-well all around the n-well, the hole conduction through the sides does not suffer from Kirk effect. The n-well overlap of p+ is also very small at the short sides and back side in the single guard stripe test structure layouts further augmenting the hole current conduction through that region due to reduction of base width. Thus, a higher level of positive feedback is present in the 3-D configuration as compared to the 2-D one resulting in a lower holding voltage condition**.**

D. Holding Voltage Trend Summary

Holding voltage trends observed in experimental characterization and TCAD simulations have the following implications for the construction of robust and optimal design rules:

- Layout topologies with no guard rings show significant positive feedback coupling between the injecting diffusions in the PNPN thyristor structures. The current is entirely supported by carriers emitted from the injecting p+ and n+ diffusions in the holding state due to the absence of a high field impact ionization region. Higher supply voltage domains would require large spacings *D* for latch-up immunity. For example, even a large spacing C is not sufficient for a 7.2V supply domain (cf. Figure 7). As such, the use of guard rings encircling the emitters is advised.
- Single guard ring layout topologies show significantly less positive feedback coupling as compared to the no guard ring case. The loss of carriers flowing out of the guard ring contacts reduces the positive feedback loop gain due to reduction of base currents. Also, the presence of guard rings weakens lateral current transport through the front side n-well/p-well junction due to the field effect [8]. These observations can be exploited to construct design rules which ensure a low coupling high holding voltage PNPN configuration. For instance, fully encircling single guard ring based design rules can be defined with a reduced value of spacing *D* as compared to the no guard ring case. In particular, in a 7.2V supply domain n+ to p+ emitter spacing B can be employed (cf. Figure 10), while spacing A can be used for a 3.6V domain.
- The width of a guard ring can also be exploited for optimal design rule construction. Wider guard rings would cause more carrier loss and reduced lateral transport, further weakening the coupling between the emitters.
- Double encircling guard rings can be considered as further extension of a single guard ring case. Emitter-to-emitter spacing *D* in this case can be further reduced.

V. Latch-up Protection Checks in Mixed Voltage I/O Design

The 55 nm latch-up characterization and analysis reveals holding voltage trends which can be employed to achieve latch-up free operation in mixed voltage designs while saving area by the context sensitive construction and application of design rules. The 2X charge pump circuit described earlier in Figure 3 can be used to illustrate this. A slice of the layout of the power transistor area is shown in Figure 17. It is assumed for the sake of illustration that the total power transistor device size is large enough to sustain the holding current condition. Assuming an input voltage VDDM = 3.6V and output voltage VDDH = 7.2V the following can be deduced:

- VDDH–connected devices: the holding voltage needs to be made higher than 7.2V for latch-up free operation. If p+ to n+ emitter isolation with no guard ring is employed Spacing larger than C has to be used (see Figure 7) while spacing B can be used with the single guard ring scheme (see Figure 10).
- VDDM–connected devices: the holding voltage needs to be made higher than 3.6V for latch-up free operation. If p+ to n+ emitter isolation is used with no guard ring, spacing C has to be used (see Figure 7) for all the logic gates and power devices while spacing A can be used if the single guard ring scheme is implemented (see Figure 10).

The above rules are exemplary only and are for the Mentor Graphics' PERC-LDL flow for checking an exemplary 2X charge pump design, which was laid out following a single guard ring protection scheme. PERC-LDL checker run results are illustrated in Figure 17:

1. In accordance with the established verification flow (Figure 5), an external node VSS was identified.
2. The n+ source diffusion of transistor MNM was flagged as a potential latch-up emitter when forming paths to p+ diffusions of transistors MPH, MPHM and MPM.
3. This was followed by establishing latch-up electrical context: transistor MPH belongs to HV power domain (VDDH, 7.2V), while transistors MPHM and MPM belong to MV power domain (VDDM, 3.6V).
4. Guard rings surrounding diffusions were checked and validated.
5. After that, a full latch-up layout context for the path at risk was established. In particular, since n+ diffusion of transistor MNM is surrounded by a single guard ring, spacing rule A was checked for the MNM - MPM and MNM - MPHM diffusion separation, while spacing B was checked for the MNM - MPH diffusion separation.
6. As indicated by red arrows in Figure 17, a number of diffusions in the first version of the layout did not meet spacing requirements and layout modification to move diffusion regions apart was required to avoid latch-up risk.

In the absence of checking capability differentiating MV and HV connected devices, a more conservative spacing B rule would have to be applied to MNM - MPM and MNM – MPHM diffusions. This would have resulted in block area increase by about 50%. Thus context based design rule construction and application can be used to save area in the VDDM domain.

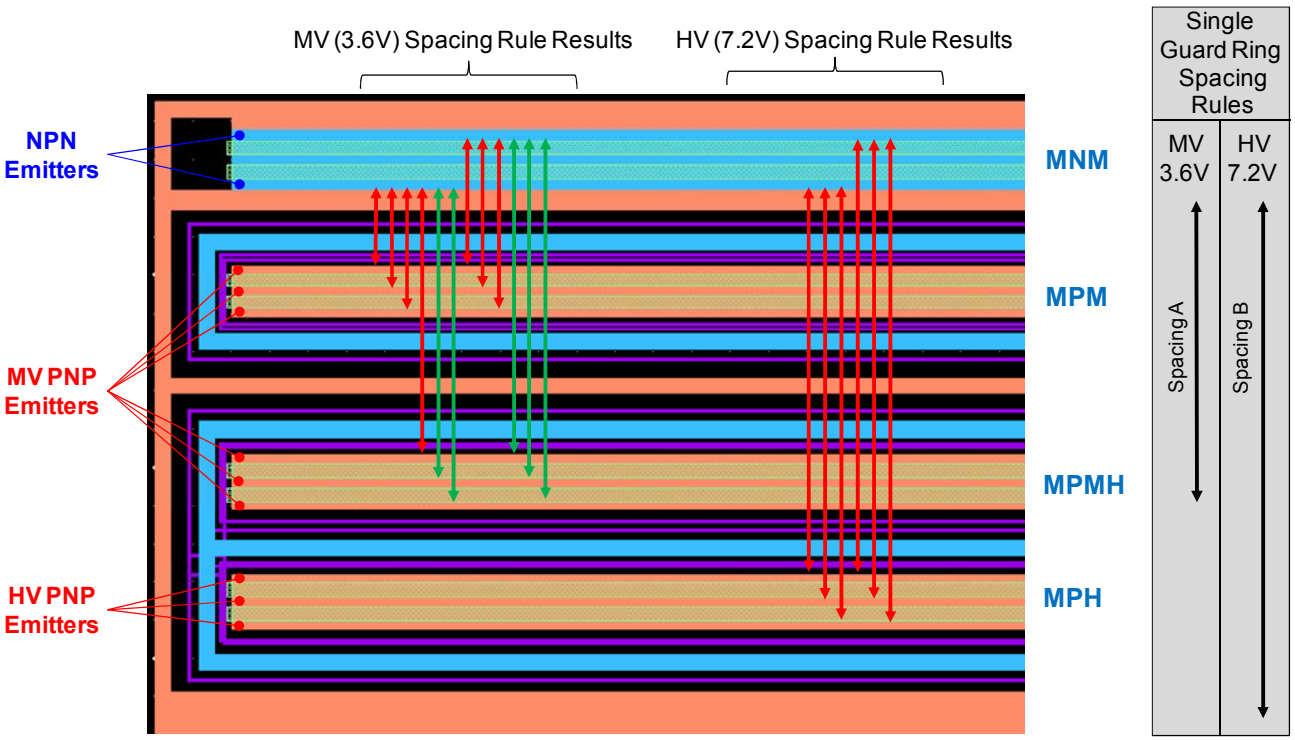

Figure 17: PERC-LDL Run Results for the 2X Charge Pump Circuit Slice Layout. Arrows Indicate Checked Spacing Rules: Green Arrows – Pass, Red Arrow – Fail

VI. Conclusions

In this study, experimental latch-up characterization and analysis was done for a 55 nm CMOS technology node to derive layout and electrical context based design rules. The relationship between the holding voltage and emitter-to-emitter isolation and guard ring strategy was extracted. It was shown that through context sensitive construction and application of latch-up design rules, area savings could be achieved in mixed voltage designs where high and low supply voltages intermingle as was illustrated in a 2X charge pump example.

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