

Application Note

HBM-TP01

Secondary EOS Event in HBM Systems

Executive Summary – This application note focuses on a recently discovered secondary EOS event on HBM test systems and its effects on certain types of protection structures, mainly designs using snapback protection. It also discusses how the secondary pulse is generated, how it can be measured and how a method (patent applied) has been developed to eliminate the secondary event in our latest tester technologies.

Characteristics of the phenomena

Since the Human Body Model (HBM) test was first standardized in MIL-STD-883 Method 3015 in 1979, many commercial HBM simulators have been introduced to the semiconductor industry. These HBM test systems have proven to be a valuable tool in improving the EOS/ESD robustness of semiconductor process technologies and device designs.

Today, most commercial HBM test systems employ a specifically designed high voltage relay to deliver the HBM discharge waveform to the device under test (DUT). The relay contains sulphur hexafluoride (SF₆), at pressure, to mask the effects of contact bounce and ensure waveform fidelity. When the relay is actuated, ionization of the gas causes a low resistance electrical continuity between all contacts to occur. The HBM discharge current waveform is delivered when an arc forms between the discharge capacitor and the DUT, however, any parasitic or residual current from the high voltage supply circuit is also delivered to the load when the gas is ionized. This transient leakage occurs after the main HBM event, so it has been referred to as the “trailing pulse”. The period between the intended ESD event and the “trailing pulse” event is dependant on the selected discharge voltage, the higher the voltage the longer the period between the ESD event and the “trailing pulse” event. The current level of the trailing pulse is several orders of magnitude less than the main HBM pulse, but still significant enough to cause damage to thin gate oxides at the 130nm node and below. This was the case for a 3.3 V input pin on a 0.13 μm geometry CMOS device, which began the investigations by C. Duvvury et al., [1]. The trailing pulses described in this note have always existed at

various levels but now may be problematic in particular topologies as scaling of the gate oxides continues downward.

The secondary waveform cannot be seen during normal ESD waveform verification procedures specified in today’s various standards as the current level is orders of magnitude smaller than that of the ESD pulse and is significantly below the current sensitivity of the specified measurement probes. The time domain of the ESD event also precedes that of the secondary waveform by some microseconds.

How to measure the event and qualify your testers

The trailing pulse can not be captured using the standard current waveform capture methods listed in the various standards, other verification loads have been devised to display the event and the appropriate time domain measurements follow.

When verifying waveforms at charge voltages up to 4000 volts, a measurement artifact consisting of a 10KΩ resistor in parallel with a zener diode (type IN5236B) should be used as the verification load. When verifying waveforms above 4000 volts, a 5KΩ resistor in parallel with the zener diode should be used as the verification load. Each of the above loads allows convenient viewing of the “trailing pulse event” on any oscilloscope with a 500MHz or greater bandwidth with identical vertical resolution for measurement of the event. Figure 1 shows an equivalent HBM circuit and the correct placement of the load. A Tektronix CT1 current probe, placed on the Terminal A side of the verification load is used to trigger the oscilloscope.

An additional 10 MΩ voltage probe is also connected to Terminal A and used to capture the trailing pulse on another channel of the oscilloscope (Figure 1).

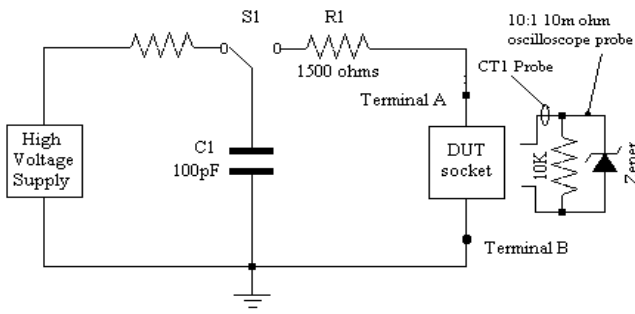


Figure 1: Equivalent HBM Circuit with 10 KΩ//Zener load used to characterize the trailing pulse at or below 4000 volts

At this time, the relevant industry standards [2,3] are being modify to include a single voltage level verification limit for the trailing pulse phenomena, which will allow users to verify whether or not their systems meet this latest industry requirement.

Suggested Specification levels:

Any trailing pulse artifact after the HBM pulse must be less than 4μA at positive and negative 4000 volt stress levels using the 10 KΩ//Zener, as shown in Figure 1. Scanning for the presence of any trailing pulse shall cover a period of at least 1 msec after the HBM pulse.

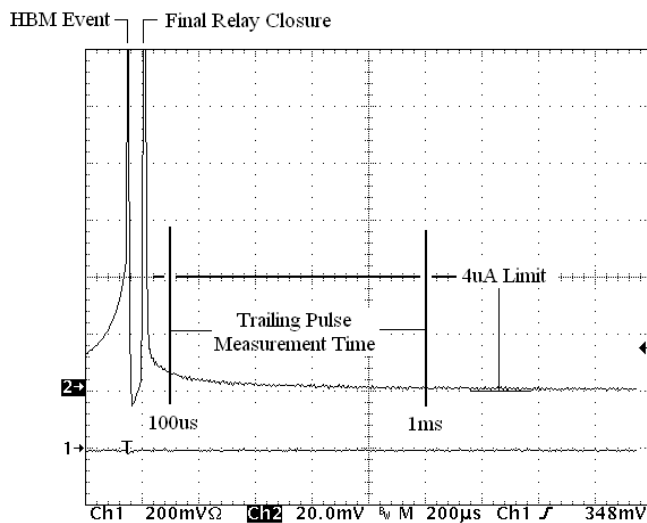


Figure 2: 4kV trailing pulse waveform on an Mk.2 system demonstrating the measurement area and showing performance well below the proposed 4μA level.

What structure types and topologies are suspect

The thin gate oxides of device I/O structures have been shown to be susceptible to the EOS of the “trailing pulse”. The problem is exasperated by the response of the ESD supression device. Some supression structures which are designed to have a limited ‘on’ or conduction time, such as avalanche or snapback type structures which quench very quickly and have high hold potentials do not dissipate the remaining paracitic charge. Because of this, the EOS affect of the trailing pulse can cause soft failure to the gate oxide without causing typical hard failures of the ESD event.

The input protection scheme shown in Figure 3 is an input protection structure called a Fail-Safe (FS) device, because a *diode to Vdd is not present*. Although the FS pins are shown to be susceptible, the same could happen for I/O pins stressed negative to V_{DD}. If the V_{DD} capacitance is not large enough the voltage from the V_{DD} protection device could also lead to a trailing pulse and cause degradation of the pMOS gate. Also, any input pins using SCR’s, GGNMOS, GCNMOS, etc. would be equally vulnerable.

Failure signatures and the failure mechanisms

The HBM failures were not evident with simple, post-stress I-V curve tracing or open/short testing. The failures were only traceable to the degradation of the following input pin parameters: minimum logic high voltage level (VIH) and maximum logic low voltage level (VIL). After HBM stressing, VIH/VIL levels shifted as much 700mV causing them to exceed the products specification.

From the known fundamental physics of oxide stress, it is the charge fluence along with available energy that can degrade an oxide before any real leakage paths are formed. That is, if sufficient current flows through the oxide for long enough duration, interface traps are created which in turn shift the threshold voltage (Vt) of the input buffer devices. The increase in Vt for either or both the nMOS and the pMOS would result in shift of the input high and input low (VIH and VIL) parameters. While trapped charges in the oxide such as those that occur with CDM pulses can be annealed, effects from the interface trap can only be partially baked out, indicating a more permanent damage.

In another study using various test structure analyses, it was concluded that the cause of oxide degradation was an over-voltage at the input gate due to inefficient input protection design. Consider the case of a typical input protection with a secondary clamp as shown in Figure 3. The paper by Chaine et al., [4] concluded that if the isolation resistor is excessively large the bipolar current to the secondary clamp is choked off during the long decaying current of the HBM pulse and gives rise to an unexpected rise in V_{t1} . This would then cause stress on the input gate oxide.

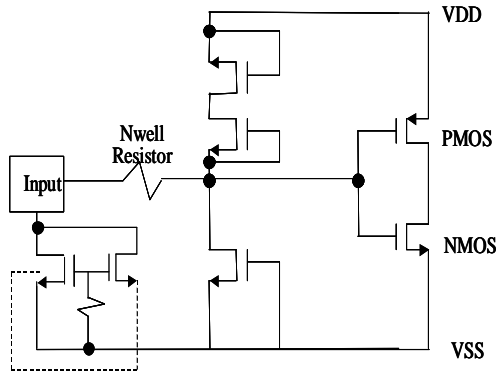


Figure 3. Input protection scheme with gate oxide clamps

Conclusions

The trailing pulse phenomena is real and has always existed at various levels in ESD tester hardware. Not all suppression structures allow the EOS event near the structures being protected. The EOS triggered by the “trailing pulse” may now be potentially problematic as the scaling of thinner gate oxides continues. This phenomena has been shown to cause failures in certain protection structures, those which incorporate snapback or avalanche designs.

This also may point to weaknesses in some of today’s protection structure designs, posing the question of the scaleability of avalanche style structures. If the structures are designed for test, should they be able to shunt this type of energy and suppress the phenomenon?

With the work performed by Thermo in cooperation with Texas Instruments, we have been able to fully understand the root cause of the trailing pulse and initiate changes to our tester technologies to provide idealised tester performance within the boundaries of available relay performance.

Upgrade paths for the ZapMaster Mk.2 and the Paragon systems will be offered by Thermo. We will also provide trade-up programs for our older technology systems, such as the ZapMaster.

References

- [1] C. Duvvury, et al., Gate Oxide Failures Due to Anomalous Stress from HBM ESD Testers, in Proceedings of EOS/ESD Symposium EOS/ESD Symposium, pp. 132-140, 2004.
- [2] “ESDA STM 5.1-2001, Electrostatic Discharge Sensitivity Testing – Human Body Model (HBM) Component Level” 2001
- [3] JEDEC JESD22-114-B, Electrostatic Discharge (ESD) Sensitivity Testing Human Body Model (HBM)”, June 2001
- [4] M. Chaine et al., “TLP analysis of 0.125 μ m CMOS ESD Input Protection Circuit”, in Proceedings of EOS/ESD Symposium EOS/ESD Symposium, pp. 70-79, 2003.

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