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RadPC Single-Board Computer (RadPC-SBC-001)

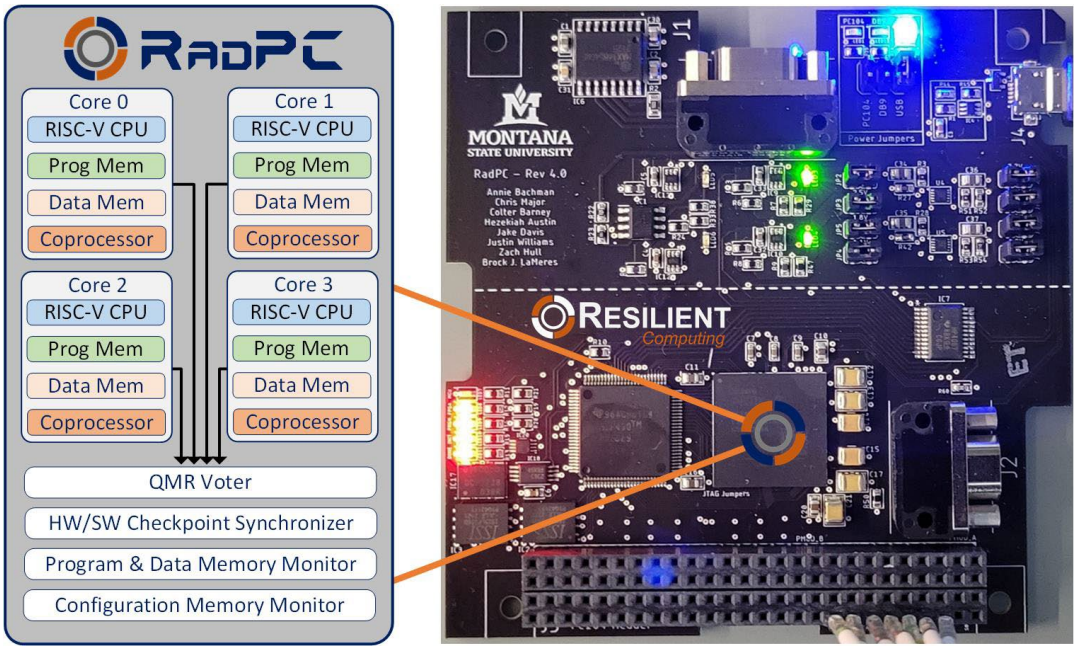
Revised December 1, 2022
This document replaces all prior versions for RadPC-SBC-001.

PRELIMINARY

Overview

The RadPC Single-Board Computer (SBC) provides radiation-tolerant computing for space applications. The RadPC SBC implements a set of redundant computing cores on a commercial Field Programmable Array (FPGA) and deploys a series of proprietary recovery algorithms to automatically detect, recover, and repair faults caused by single event effects (SEEs). The recovery procedures are abstracted from the user allowing the software developer to treat the RadPC SBC as a traditional embedded computer without worrying about SEEs. The RadPC CPU implements a 32-bit RISC-V computing architecture, which is gaining popularity for aerospace applications. This allows RadPC to use the open-source RISC-V development tools with custom plug-ins to adapt it for the fault-tolerant RadPC architecture.

The RadPC-SBC-001 version is optimized for small spacecraft applications by providing low power consumption and increased computation relative to other commercially available SmallSat computers. The RadPC computer is implemented on an industrial-grade Xilinx Artix-7 200T FPGA with an operating temperature of -40C to +100C. This commercial off-the-shelf FPGA is fabricated using a 28nm process node. This reduced feature size provides inherent immunity to total ionizing dose (TID) with a predicated rating exceeding 100krad. Reliability models show the RadPC architecture implemented on an Artix-7 FPGA provides a significant improvement to the Mean Time Before Failure (MTBF) over a simplex system, a system using triple modular redundancy (TMR), and a system using TMR+repair.



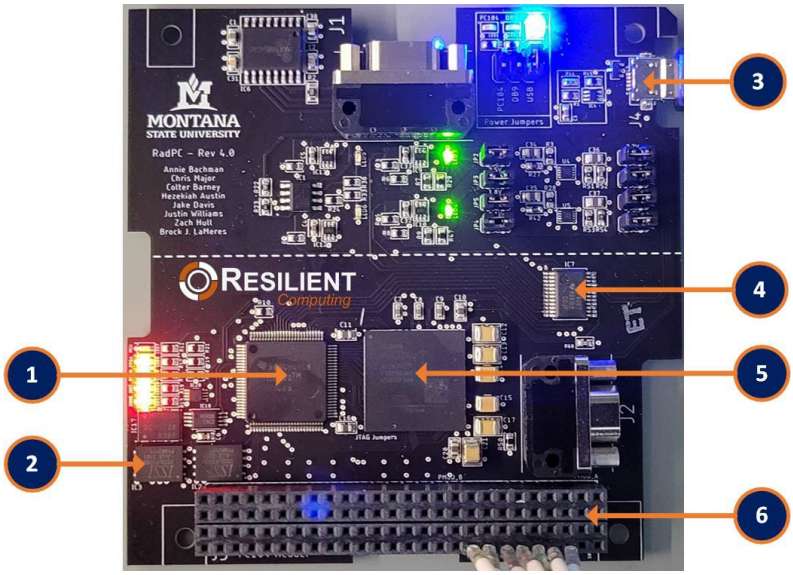
RadPC Features

- 50 MIPs of Computational Performance.
- 2k Data Memory; 8k Program Memory.
- +5 VDC Single-Input Power Supply.
- 1 W Total System Power Consumption.
- 100mm x 100mm CubeSat form factor.
- PC/104 Compatible
- 32 GP Parallel I/O Ports.
- 2 UART Serial Peripherals.
- 2 SPI Serial Peripherals.
- LEO Reliability: 1556% improvement of MTBF beyond a simplex system and 331% improvement beyond TMR.
- Lunar Reliability: 337% improvement of MTBF beyond a simplex system and 67% improvement beyond TMR.
- Tested under a comprehensive suite of buffer overflow cyberattacks.

Flight Heritage

RadPC has been developed under NASA funding over the past decade. The RadPC fault tolerant computing architecture has been tested on high altitude balloons (8x), sounding rockets (2x), on the International Space Station (3x), and on small satellites (2x). In 2024, RadPC will be tested on the surface of the moon through NASA's Commercial Lander Services (CLPS) program.

RadPC SBC Hardware Details



Callout	Component Description	Callout	Component Description
1	TI MSP430 Housekeeping MCU (MSP430FR5969-SP Rad-Hard Option Available)	4	On-Board Current/Voltage Monitoring
2	SEE Recovery Memory for FPGA	5	Xilinx Artix-7 200T FPGA Running RadPC
3	+5V Input Voltage Supply	6	PC104 Compatible

Development Environment

Software is developed using the open-source RISC-V tools with a custom RadPC plug-in. This allows software to be written in a widely popular development environment with a growing number of open-source libraries and tools. Implementation on the RadPC architecture is abstracted from the developer so the system is treated as any standard embedded flight computer.