Detecting remapped DRAM chips

Advanced diagnostic methods can detect "remapped" or "non-spec" DRAM chips. These chips are often components that failed original manufacturer (OEM) speed or reliability tests but were "remapped" to hide defects or "remarked" to appear higher-performing than they actually are.

1. **Thermal Stress and Burn-In Testing (TDBI):** Applies extreme high and low temperatures (typically ranging from -40°C to +95°C).
   The Detection: Remapped chips often have weakened cells that only fail when heated. By applying thermal stress, labs can identify retention failures—where a cell cannot hold a charge for the required 64ms—that would otherwise be hidden by the chip's internal error-management logic at room temperature.
2. **Voltage and Timing Margining:** The module's operating parameters are pushed beyond standard specifications to find "weak" chips.
   The Detection: By slightly raising or lowering the I/O voltage, testers can trigger failures in chips that have been improperly binned or remapped to hide electrical sensitivities.
3. **Timing Checks:** High-speed tests validate specific operational timing specs (e.g., tAC, tRCD).
   The Detection: Remapped chips often exhibit marginal timing that causes intermittent "soft errors" under heavy load, even if they pass basic "Pass/Fail" tests.
4. **Advanced Algorithmic Pattern Testing:** Instead of simple linear reads/writes, complex patterns find faults hidden by remapping:
   a) **March C- Algorithm:** This is a gold-standard academic and industry test that involves five reads and five writes at each address to catch "coupling faults," where writing to one address flips a bit at a different address.
   b) **Moving Inversions:** These patterns detect Address Faults (AF), ensuring the internal address decoding logic hasn't been tampered with to bypass known "dead" sections of the DRAM array.
5. **Application-Specific Platform Validation:** Unlike using only generic testers, tests are performed on a specific enterprise server platform.
   The Detection: A module might "pass" on a standalone tester but fail when the platform memory controller (which has its own proprietary timing and voltage curves) interacts with the chip. This identifies "non-spec" components that lack the electrical "headroom" required for stable enterprise operation.
6. **Signature and Physical Inspection SPD (Serial Presence Detect) Verification:**
   a) Testing labs check the SPD data on the module for inconsistencies. Discrepancies between the chip's physical markings and the digital identification programmed into the SPD often reveal remarked or remapped stock.
   b) **Advanced Imaging:** For high-stakes enterprise audits, techniques like X-ray imaging can detect structural defects or evidence of recycled/remarked chips that standard electrical tests might miss.