Contributor: Raji Tannouri

Industry Background

2017-2007 - CMTL (Computer Memory Test Labs, Inc.): Irvine, CA -General Manager
Primary Responsibilities:

1. Insure efficient and maximum through-put of lab operation.
2. Manage all operations of the lab including employees, contractors, website and testing procedures.
3. Primary technical contact for Intel TMEs (Technical Marketing Engineers).
4. Primary technical contact for all motherboard, platform, system and memory module manufacturers.
5. Coordinate receipt of required materials to test all Intel and clone motherboards and platforms.
6. Provide Intel update on all certified & tested memory parts to post on CMTL and Intel websites.

2006-2005- Intel Corporation: Hillsboro, OR- Sr. Validation & Test Engineer
Primary Responsibilities:

1. Review server system/board level validation and memory module qualification process.
2. Work with engineering team leads, programs mangers, and vendors to resolve technical issues.
3. Write qualification test procedures/test plans to support new product development for environmental validation and memory qualifications-Intel Enterprise Products Server Division].
4. Establish and execute test procedures, analyze results, create and maintain records, log defects analyze data, perform testing, recommend process improvements, review test procedures.
5. Identify hardware and software bugs at board/system level failures related to design stability by utilizing 4-corner testing, power sequencing, power cycling and board level vibration and thermal stressing.

2005-2004- Intel Corporation, Hillsboro, OR- Sr. Quality & Reliability Engineer
Primary Responsibilities

1. Develop plan and risk assessment to ensure compliance with Intel quality and reliability requirements.
2. Ensure Intel, Dell, and FSC quality goals are achieved and maintained.
3. Interface with Dell reliability team to ensure Dell reliability requirements are understood and executed.
4. Maintain communication product development teams to define quality & reliability goals criteria.
5. Manage risk mitigation plans, resolve quality and reliability challenges.

2004-1997-Intel Corporation, Hillsboro, OR- Sr. Test Engineer:
Primary Responsibilities

1. Develop “Universal Test Platform”
2. Develop “Mixed Memory Testing Process”
3. Manage environmental validation process to provide improvements.
4. Manage memory module regression and sustaining testing for Intel TME’s
5. Manage OEM memory suppliers [Samsung, Micron, Infineon, Hynix .....]
6. Support CMTL, Intel TMEs and Intel PMO (Platform Memory Organization).
7. Perform 4-corner, power cycling, shock, vibration memory validation testing.

1997-1996- Intel Corporation, Hillsboro, OR- Failure Analysis Center Debug Technician:
Primary Responsibilities

1. Verify reported customer Intel platform failures.
2. Audit inspection of outgoing failure analysis center products.
3. Perform incoming quality inspection for Intel desktop mother boards.

Education

Bachelor of Science in Electrical Engineering, Portland State University, 1994
Associate of Science, Portland Community College, 1989