Sawblade Cyber Defense EDA

Cyber Security
Cyber Defense

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Sawblade Ventures, LLC

Austin, Texas

January 25, 2019

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Sawblade Ventures Product Statement

Sawblade Ventures Product:

A fully functional patented method
for improving cyber-security
by integrating
small flexible, re-configurable, distributed
and networked hardware
into microelectronic systems!

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Sawblade Ventures History

- Sawblade Ventures (SbV) began in January 2015.
- Sawblade Ventures, LLC is the managing partner of SaW Ventures, LP

- SbV is based on roadmap previously implemented by DAFCA, Inc
  - Validation and Verification DAFCA focus
  - Cyber-Security

- DAFCA
  - Began in 2003; Inactive in 2012

- SbV manages the technology including all rights, patents, IP, hardware and software previously owned by DAFCA.
  - 10 years of research with over $25M of investments in the IP

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SbV Product Offering

- SbV is offering a *HARDWARE* solution for securing integrated circuits.
- SbV can be used to augment other solutions including hardware and software techniques to improve security.
- SbV goes into the DNA of the chip, deep into the design.
- The best security is ….. *MORE* security!

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SbV Product Offering

SbV includes:

- Patented methods for placing and configuring security
- Custom Digital IP library – ClearBlue™ ReDi
- EDA tool used during design integration – ClearBlue™
- Tutorial for use in building a secure chip with Sawblade

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SbV Offering – The Basics

SbV Basics for System on Chip

Normal Design Flow

- Market need drives a product definition- any market
- Customer defines requirements, vendor develops spec
    - Security definition can ***not*** be an afterthought
- SoC is designed using HDL/RTL/Verilog, chip is verified/Verilog
- Semiconductor process compiles into gates/transistors.
- DFT scan chains are added
- Timing, power, physical design is completed.
- ***ALL WORKS per requirements and spec in this normal flow! Now,***

Adding security

- **Sawblade security is integrated and verified / only creator knows the secrets.**
- Chip is re-verified for original functionality, timing, power ***and security***.
- Tape out or FPGA programed and into production.

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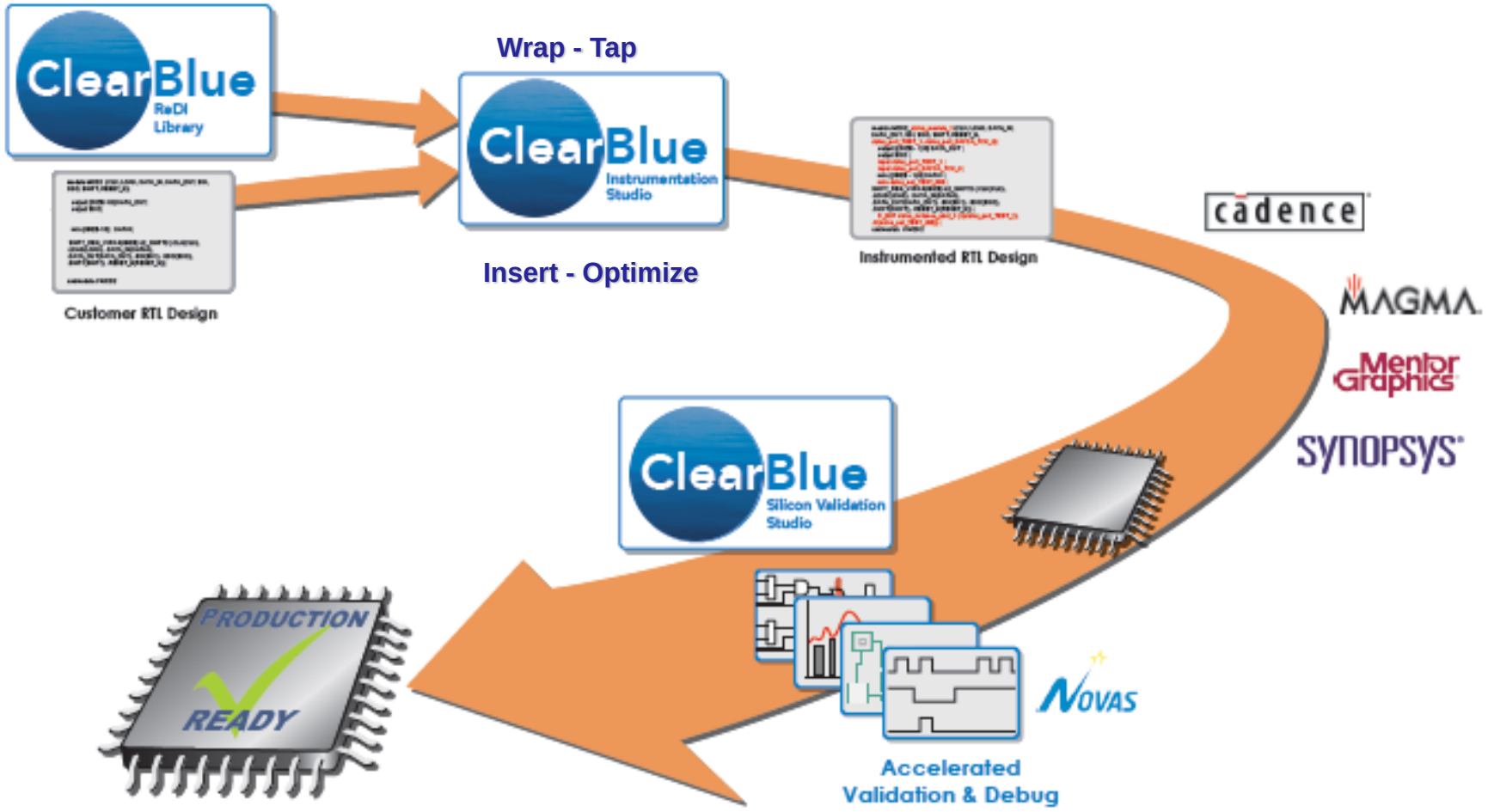
ClearBlue™ Accelerated In-System Silicon Validation



Seeing is Believing!

Integrates with normal design flow

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Ventures

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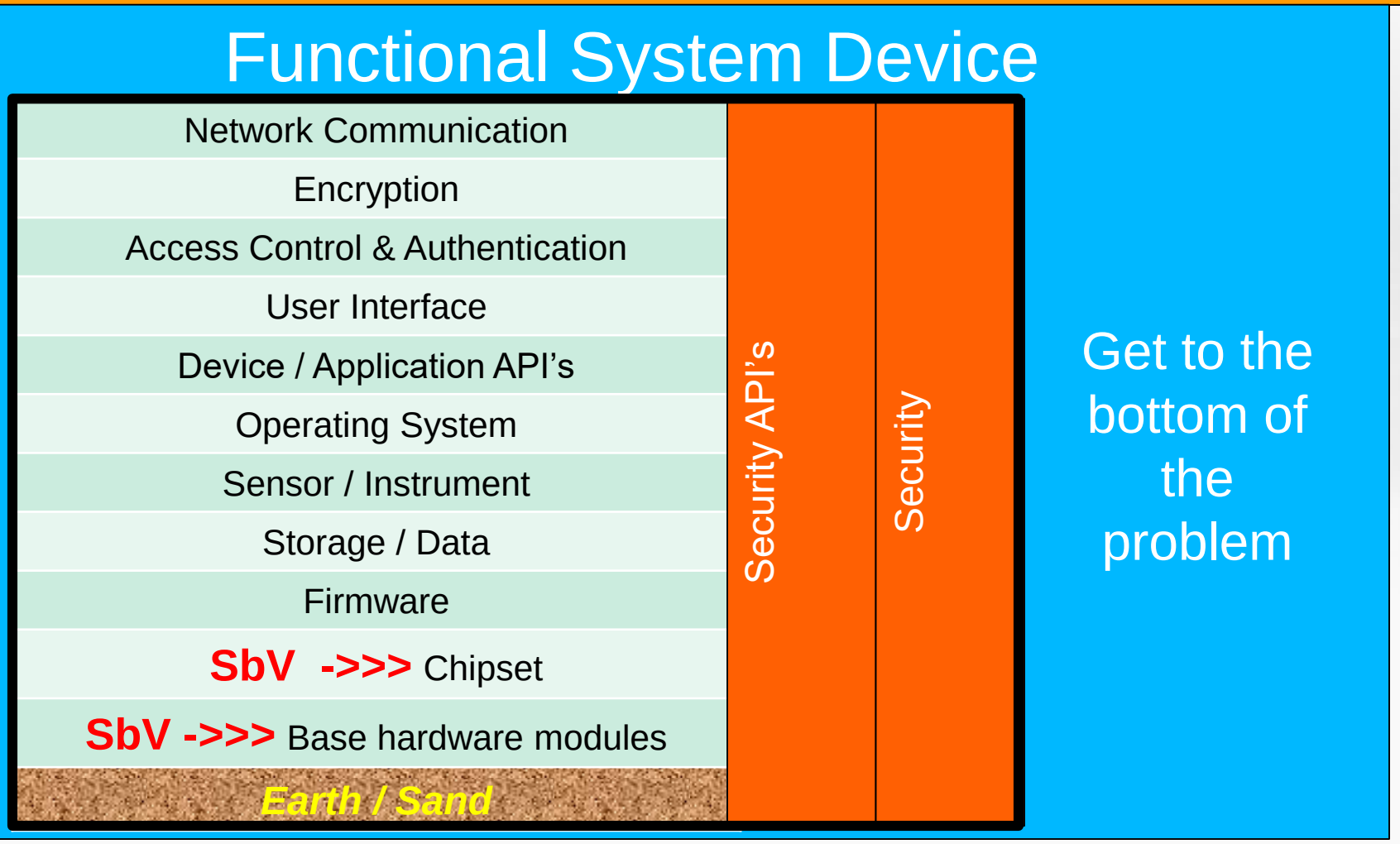
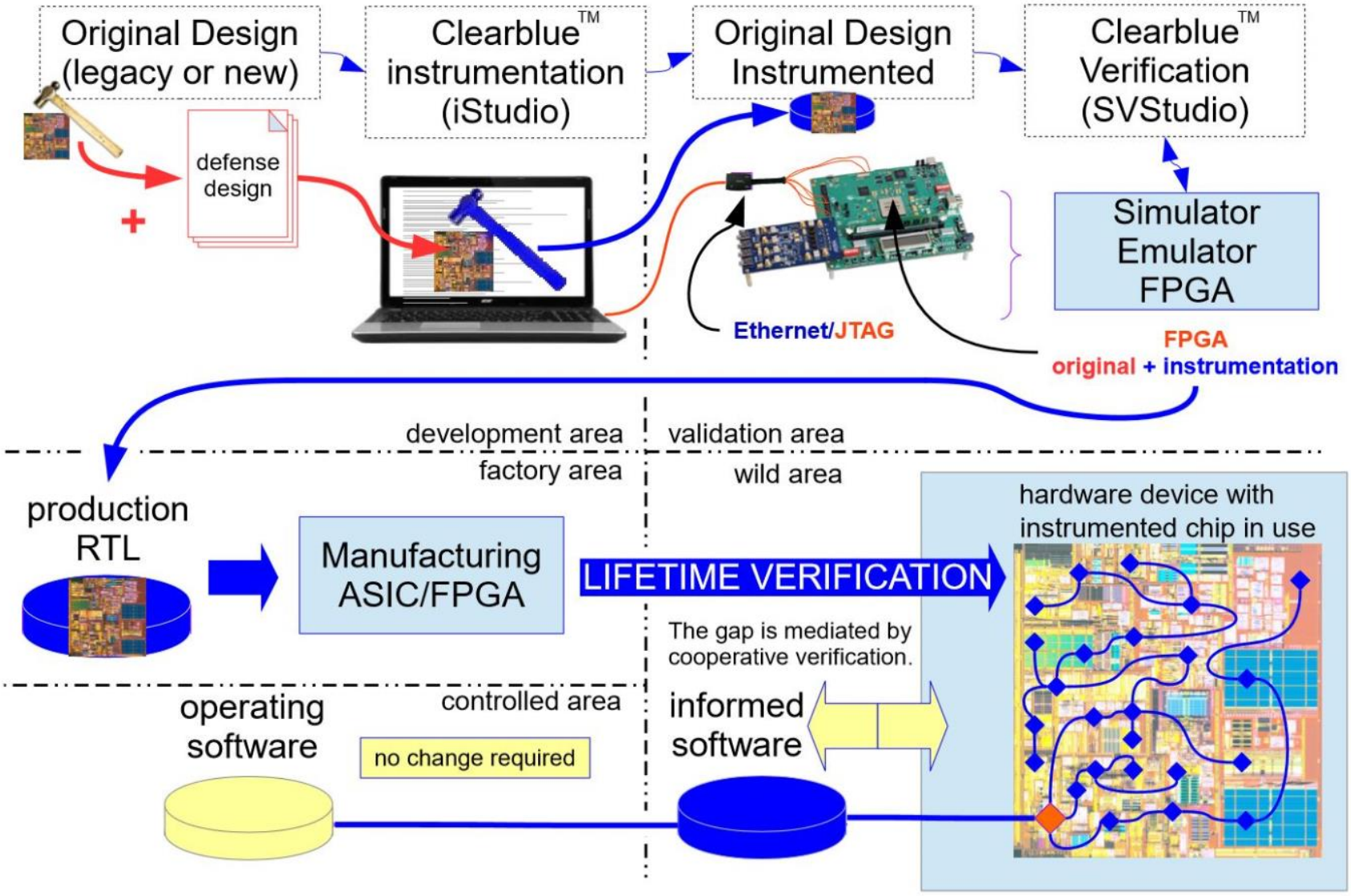
Application System Layers



SbV ClearBlue™ Workflow

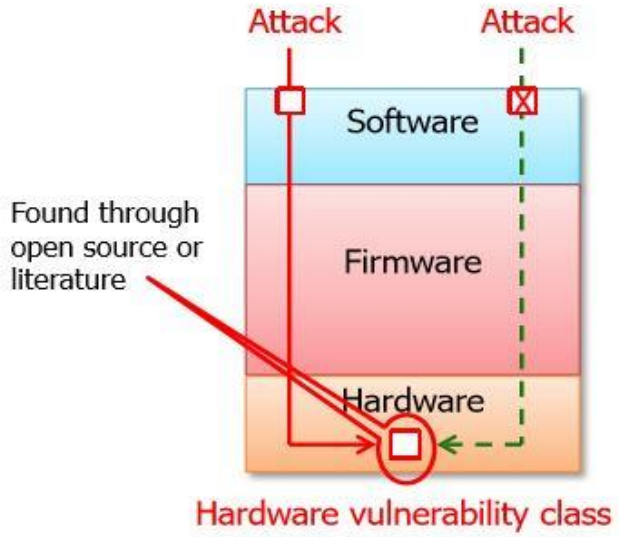


Electronic Systems Need Better Hardware Protection

SbV predicate:

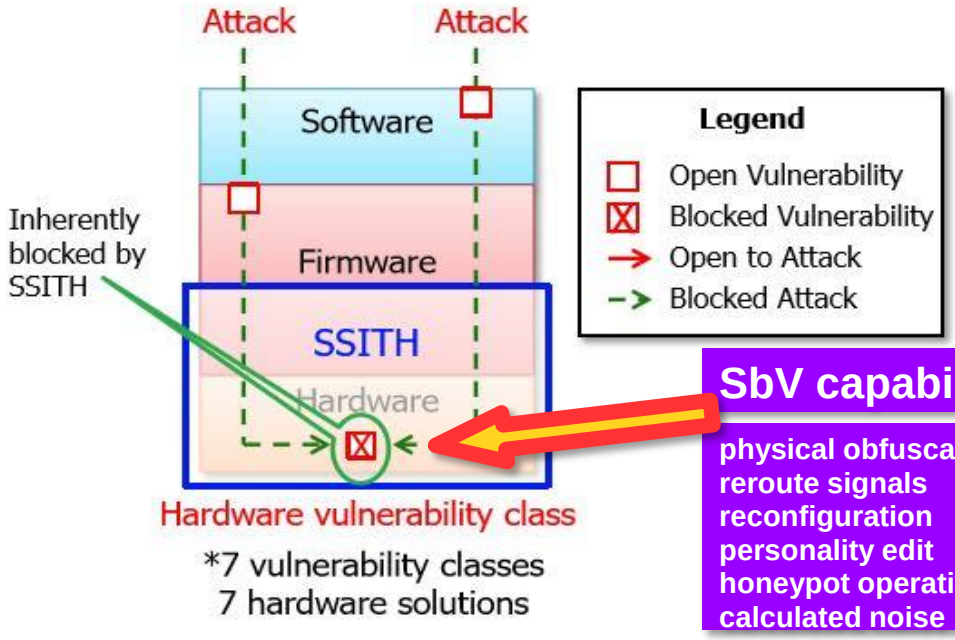
Today: Patch and Pray

*2800 vulnerability instances
2800 software patches



Future: SSITH

SSITH will protect against all 7 hardware classes



SbV capability:

physical obfuscation:
reroute signals
reconfiguration
personality edit
honeypot operations
calculated noise

SSITH addresses hardware vulnerabilities at their source and will address current and future vulnerabilities

*2015 MITRE-recorded hardware vulnerabilities (CVE)

2017

2

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SbV How it Should work

New Design IC's – Adding Security

- Requirements are defined
  - Assuming security is a critical need
- Architecture is defined / Specification written
  - Security specification is a separate document
- Design is created, RTL, hardblocks, memories
- Design is verified through traditional methods
- Gates synthesized and verified.
- SbV security now can be added per specification
  - RTL netlist is read into ClearBlue™ iStudio (EDA tool)
  - IP blocks: Monitors, capture, trace, trigger engines inserted as per security strategy and spec.
  - SVStudio is used to verify security scheme
  - New netlist is created.
- Re-verification of base circuit, synthesis, timing, power, DFT
- Tape out

SbV How it Could work

New Design IC's – Design is in process……

OMG – I have a weakness and we are about to tape out !!!

- **STOP** the tape out and prepare to **run Sawblade's ClearBlue™ !!!**
- Define weakness plus some more thought of …. What else….
- Document the entry weakness
- SbV security is added per specification
  - RTL netlist is read into ClearBlue™ EDA tool
  - Monitors, capture, trace, trigger engines added
  - SVStudio is used to verify security scheme
  - New net list is created.
- Re-verification of base circuit, synthesis, timing, power, DFT
- Tape out with
  - ***MINIMAL TIME LOST***
  - ***Gap Closed***

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SbV How it Could work

Modifying Existing Designed IC's

- At risk design features are identified
- Security specification is defined and documented
- SbV security is added per specification
  - RTL netlist is read into ClearBlue™ EDA tool
  - Monitors, capture, trace, trigger engines added
  - SVStudio is used to verify security scheme
  - New net list is created.
- Reverification of base circuit, synthesis, timing, power, DFT
- Tape out

Note: This can be done with same pin out / same package / same performance as before but now with *internal monitor and counter measures* added.

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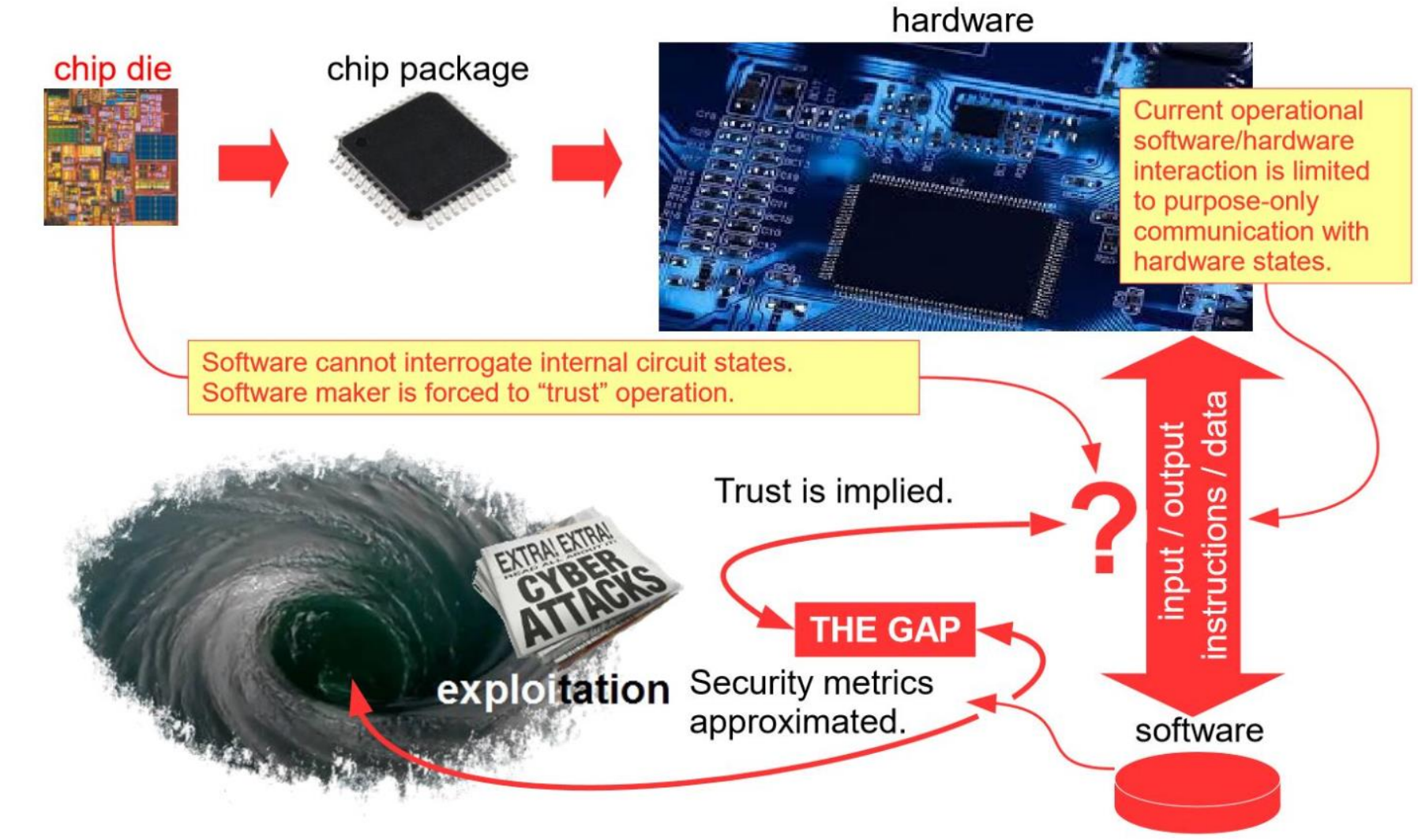
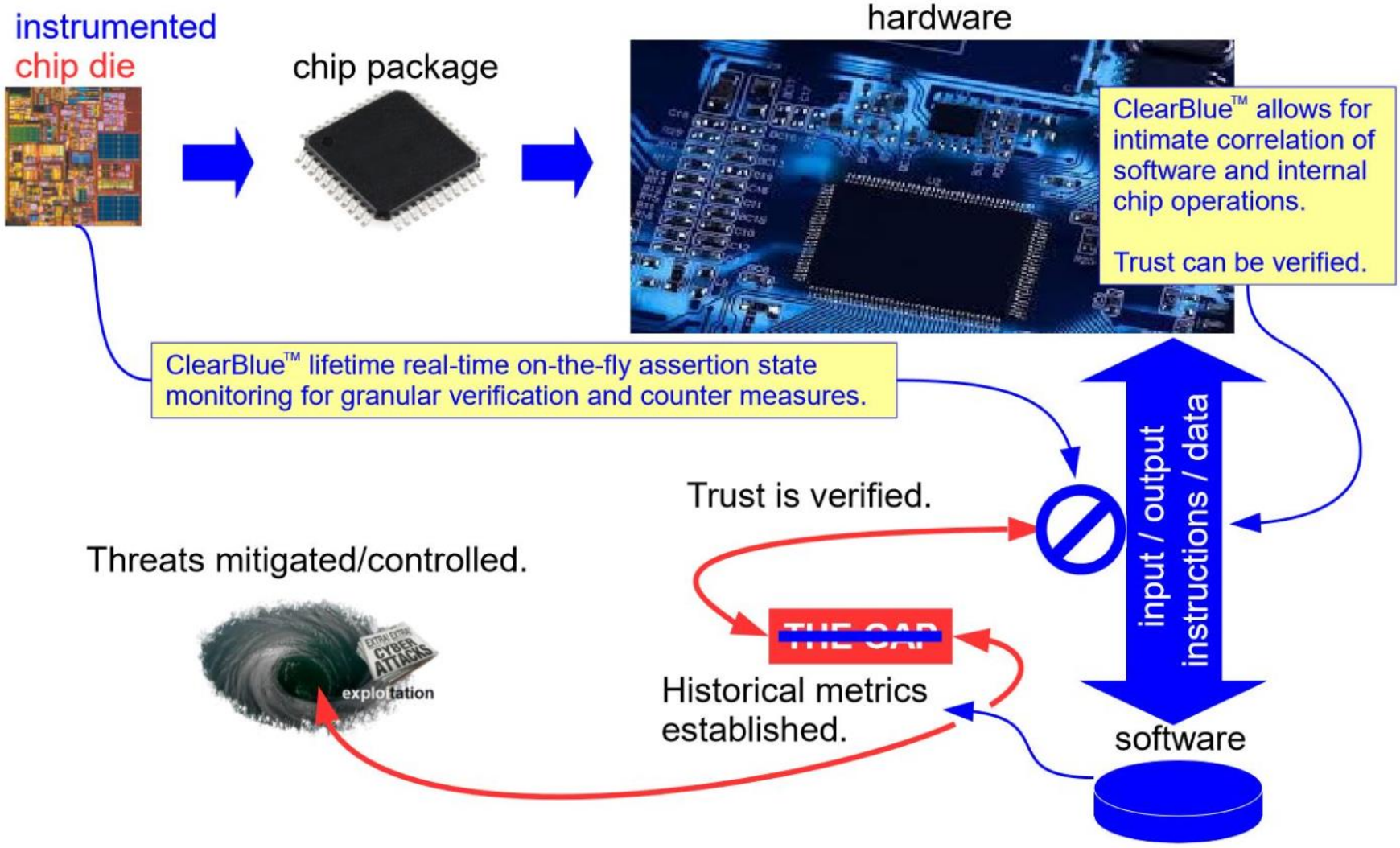
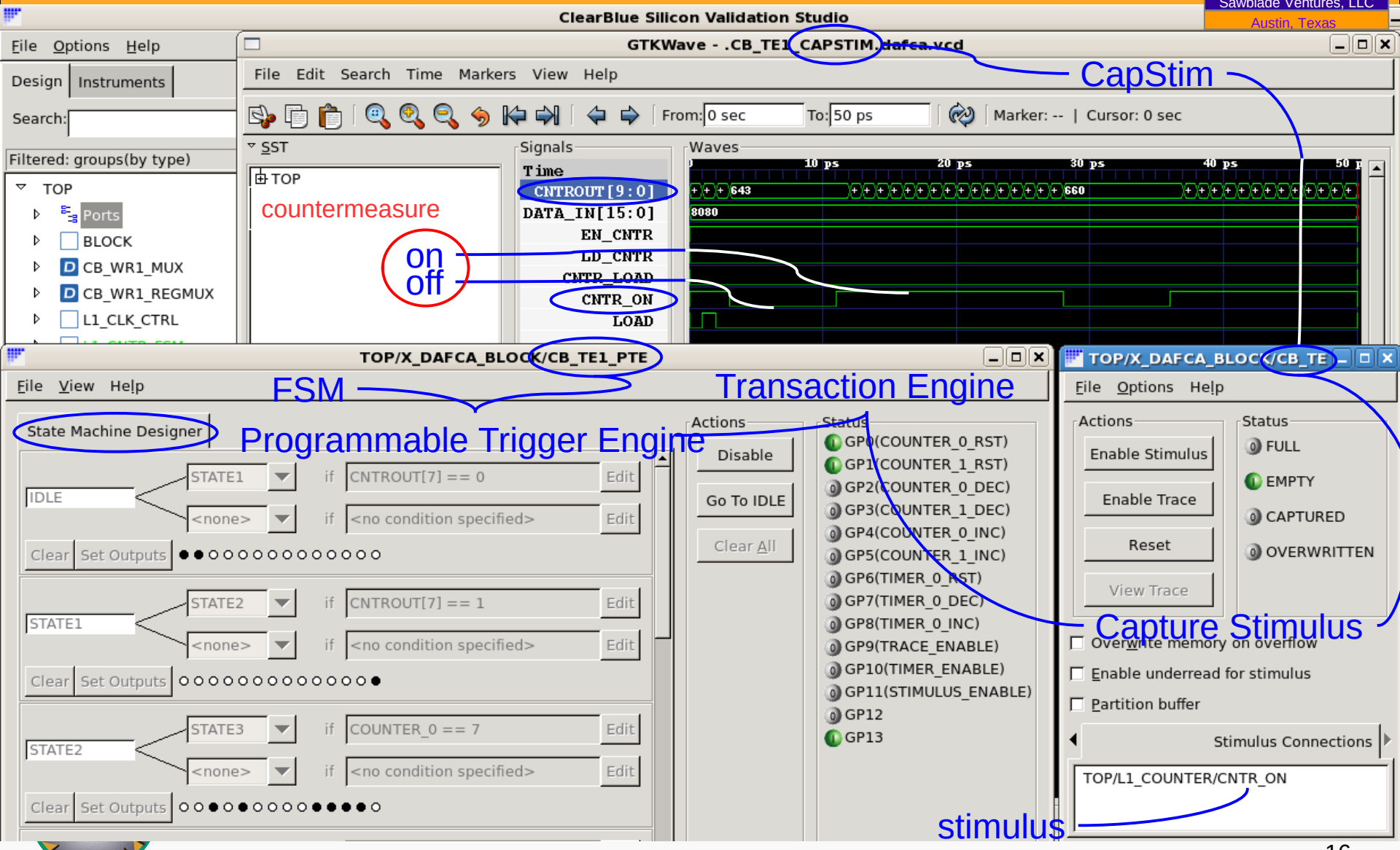
IT Industry Security Problem



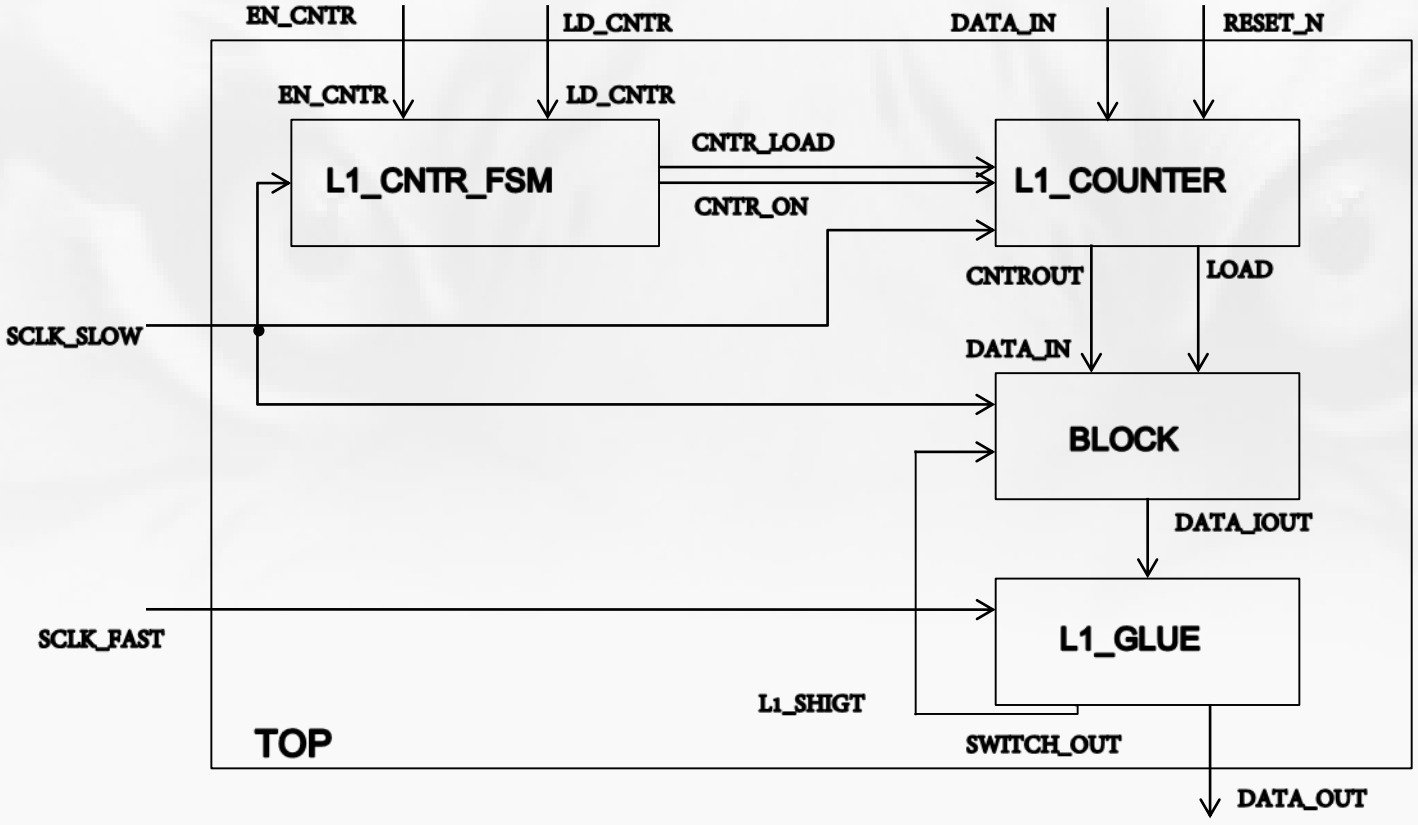
SbV ClearBlue™ Solution



Example SVStudio Run



A Typical Circuit



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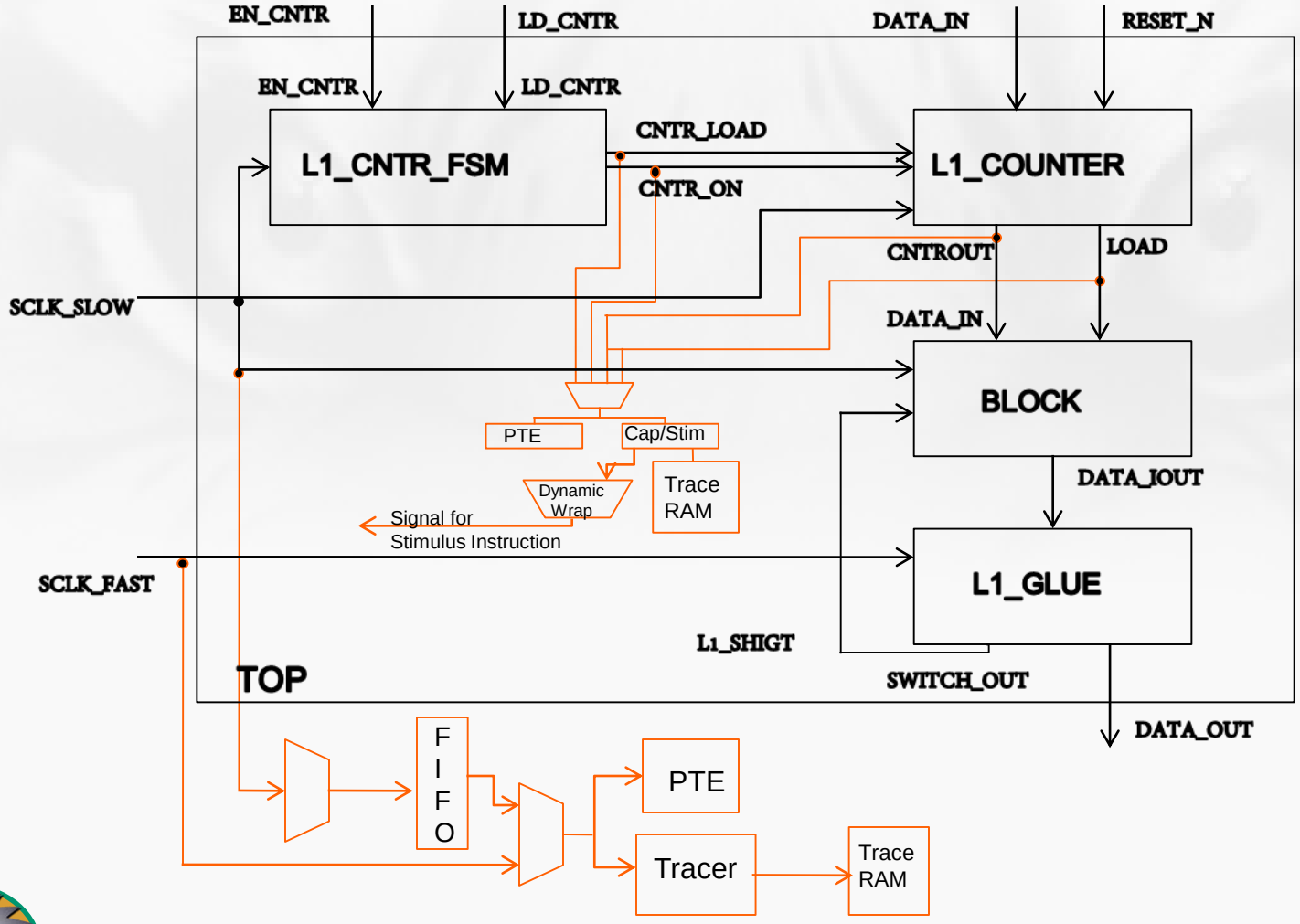
Typical Circuit with SbV Instruments Added



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Reconfiguration Circuit Example

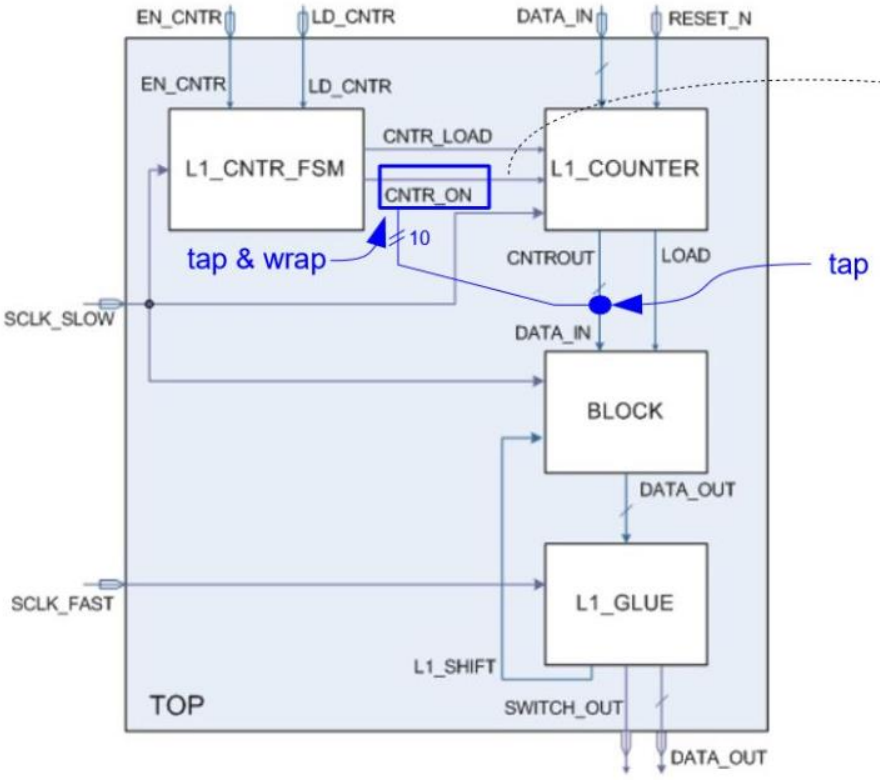
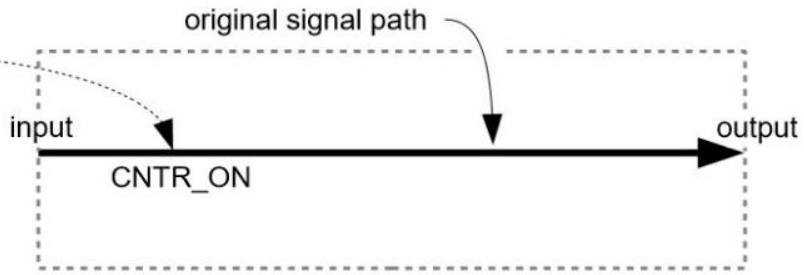
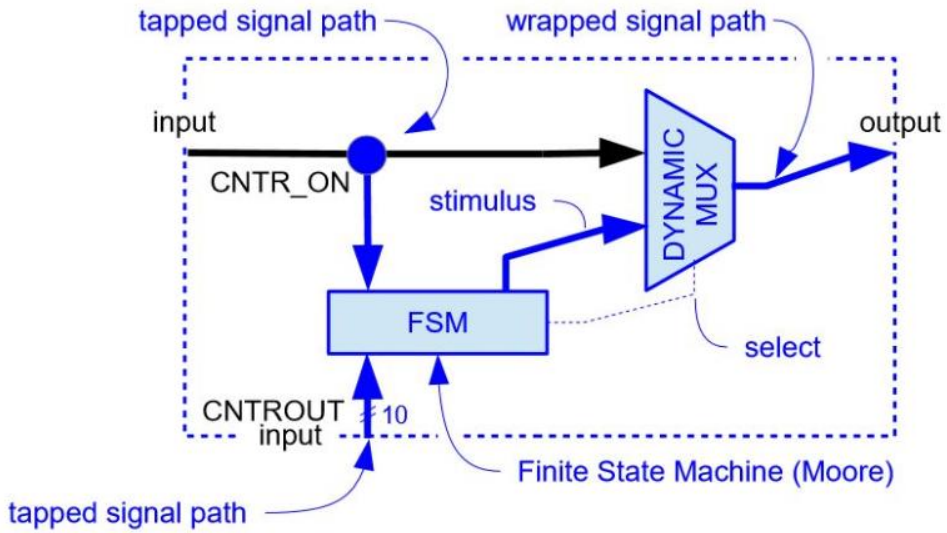


Figure 1-1 Tutorial circuit top-level block diagram





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Cyber Security with Sawblade Ventures

Small, distributed, integrated HARDWARE

END of Presentation

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