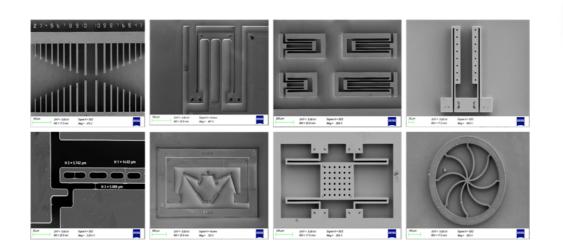


INFAB SEMICONDUCTOR PVT LTD

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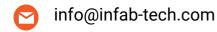
SILICON ON INSULATOR (SOI)
PROCESS GUIDE



Microstructures (Cantilevers, Thermal actuators, Folded-beam suspensions, Ring resonator, etc.) fabricated using SOI-MEMS process with a minimum feature size of $3~\mu m$

SUPPORTED SOI-MEMS DEVICES

Accelerometer
Gyroscope
Micro-mirror
DC-RF Switch
Optical waveguide
Electrothermal Actuator
Microchannels, etc.







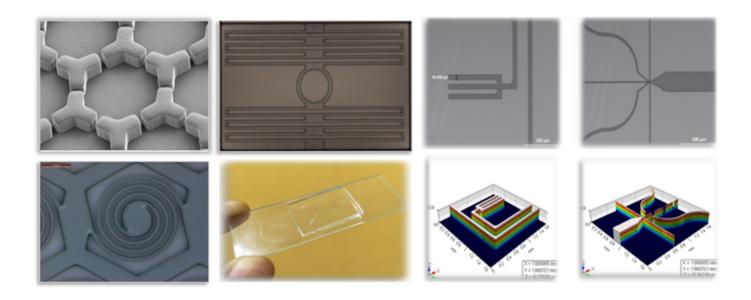
SUPPORTED MICROFLUIDIC DEVICES

PDMS-based Devices

- Various thickness ranging from 100 µm to 5 mm (max.)
- Micro-channel width ranging from 10 μm to 250 μm

SU-8 Devices/Mould

- Various thickness ranging from 5 μm to 150 μm (max.)
- Micro-channel width ranging from 10 μm to 250 μm



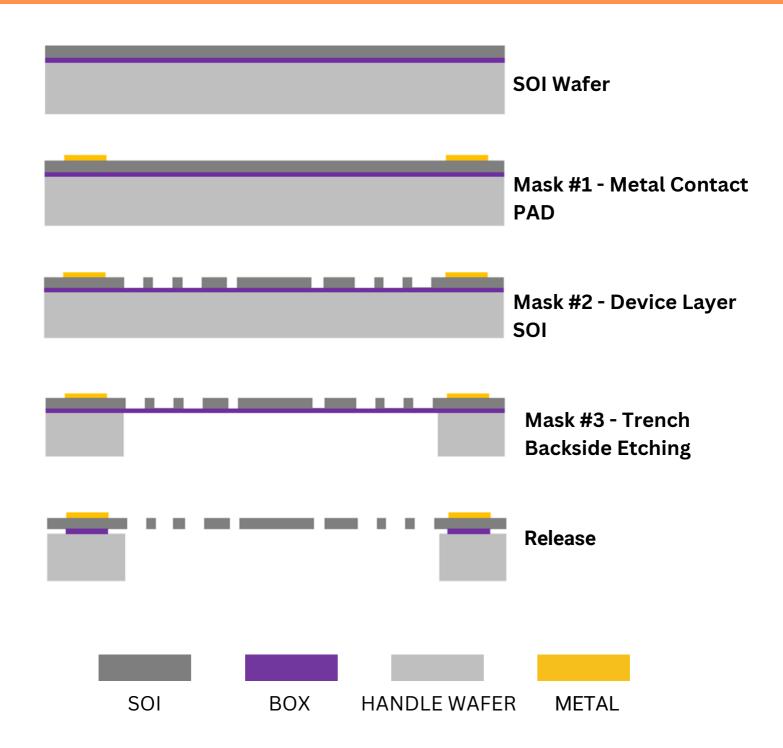
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SOI-MEMS PROCESS FLOW





LAYER PROPERTIES

The statement describes the overall process for manufacturing MEMS devices on a Silicon-On-Insulator (SOI) wafer using a three-mask level process. The process involves the use of three different masks: PAD METAL, SOI, and TRENCH.

The PAD METAL mask is used for creating contact pads on the wafer. These contact pads provide electrical connections to the MEMS devices that are being fabricated on the wafer.

The SOI mask is used for creating the MEMS devices themselves. This mask defines the features of the devices, such as their shapes and dimensions. The SOI layer is where the MEMS devices are fabricated, and it sits on top of a buried oxide layer, which provides insulation between the devices and the underlying substrate.

The TRENCH mask is used for back-side etching, which is a process that removes material from the backside of the SOI wafer. This step is necessary to release the MEMS devices from the substrate and allow them to move freely.

Overall, the process of manufacturing MEMS devices using these three masks involves precise microfabrication techniques to create intricate structures on the SOI wafer. This process requires careful control over the deposition and etching of different layers and the alignment of the different masks used to create the devices. Once fabricated, the MEMS devices can be used in a wide range of applications, from sensors and actuators to microfluidics and lab-on-a-chip devices.

Layer	Material	Thickness (µm)	Remark
Contact PAD	Metal – Au/Cr	up to 0.5	Used for electrical contact
SOI	Si	10, 20, 30	Device layer for Si-based microstructures
Oxide	BOX	1-2	Sacrificial layer for gap
Handle wafer	Silicon	400 – 550	Provide mechanical support



DEVICE LAYER PROPERTIES

The statement refers to the use of Single-Crystal-Silicon (SCS) as a structural layer and SOI wafers of different thicknesses as device layers in a microfabrication process. The device layer is the layer of the SOI wafer where the MEMS devices are actually fabricated.

SCS is used as the structural layer because it provides a strong and stable base for the MEMS devices to be built upon. SCS is a high-quality material that is commonly used in the semiconductor industry due to its excellent mechanical, electrical, and thermal properties.

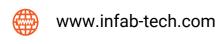
The device layer of the SOI wafer comes in three different thicknesses: 10 μ m, 20 μ m, and 30 μ m. The thickness of the device layer is an important parameter that affects the performance of the MEMS devices. Thinner device layers allow for greater sensitivity and faster response times, while thicker device layers provide greater structural stability.

The resistivity of the device layer (Si) is also an important parameter that affects the performance of the MEMS devices. The resistivity of the device layer can range from 1 to 20 ohm-cm in bulk, depending on the thickness of the layer. The user can request a specific thickness of the device layer based on their device and design requirements, and the resistivity will be within this range.

Overall, the use of SCS as the structural layer and SOI wafers of different thicknesses as the device layer provides a solid foundation for the fabrication of high-quality MEMS devices. The ability to customize the thickness and resistivity of the device layer allows for greater flexibility in designing and optimizing MEMS devices for specific applications.

Layer	Name	Minimum Feature (μm)
Contact PAD	CPAD	5
Device	SOI	3
Trench Backside	TRENCH	200 X 200

Layer to Layer	Minimum Overlay
	(µm)
CPAD to SOI	5
Trench	5
Backside to SOI	







DESIGN RULES

Firstly, the recommended design format for microstructure design is CIF (Caltech Intermediate Form) and GDS-II (Graphic Data System II).

Secondly, it's important to consider the minimum feature size of the microstructures. In general, the minimum feature size is the smallest dimension that can be resolved in the fabrication process. For example, if the minimum feature size is 3 μ m, then the smallest width or spacing of a structure should be 3 μ m or greater. Going below the minimum feature size can lead to inaccuracies in the fabrication process and may result in unusable devices.

Finally, it's important to consider the minimum spacing between adjacent microstructures. For example, in the case of an electrostatic comb-drive actuator, the minimum spacing between two adjacent comb fingers should not be less than 5 μ m. This spacing ensures that there is no unwanted electrical coupling between the fingers and that the actuator functions as intended. In extreme cases, a user may be able to reduce the spacing to 4 μ m, but it's important not to go below this limit to avoid any issues with functionality.

Overall, it's important to consider these factors and others when designing microstructures. Attention to detail and adherence to industry standards can lead to successful fabrication and functional devices.

Contact PAD (Metal Layer)

Recommended dimensions for contact PAD

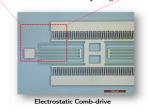
- $100 \mu m \times 100 \mu m$ (On wafer probe)
- 200 μm × 200 μm (Wire Bonding



Fig. Contact PAD (yellow in color) onto the device.



Example. 1 – Minimum feature size and spacing between comb fingers

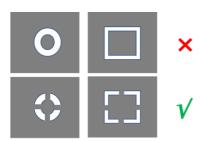






DO'S AND DON'T

When using the trench layer for backside etching, it's important to keep in mind that the minimum feature size is 200 μ m. Additionally, it's recommended to avoid unanchored designs underneath the trench region to ensure proper support and functionality. Please refer to the instructions below for more information on anchoring designs.



Example. 3 – NO un-supported/un-anchored structure under TRENCH area

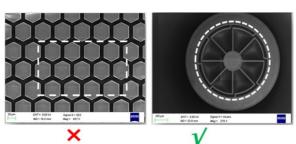


Fig. Microstructure with trench region (dashed line)

To ensure proper layer-to-layer alignment, it's important to avoid any overlap between two adjacent layers. Overlapping layers can cause inaccuracies and inconsistencies in the fabrication process and may result in unusable devices. Therefore, it's recommended to ensure that there is no overlap between layers during the design stage.



Example. 2 - Metal layer on top device layer



DIE SITE RESERVATION

Our SOI-MEMS process is designed to support a wide range of MEMS (microelectromechanical systems). This process allows for the creation of high-precision, high-quality microstructures and devices for various applications.

The die site available for our process is **11** mm × **11** mm, with a design area of **9** mm × **9** mm. We require a minimum booking of 2 sites for each order.

To submit your design for fabrication, we provide an online submission portal with submission deadlines listed on our website. The supported design file formats are GDS-II and CIF.

After submission, the expected delivery time for completed devices is approximately 12 weeks.

Design Area
(9mm X 9mm)
Chip Size
11mm X 11mm

We understand that designing and fabricating MEMS devices can be a complex process, so we offer design assistance upon request. Additionally, technical assistance is provided during characterization and measurement. However, the facility usage charge will be borne by the user.

Overall, we strive to provide a comprehensive and efficient service for the design and fabrication of MEMS devices, and we are committed to supporting our clients throughout the entire process.