1.2: Working with Boost Converters and Duty Cycles (Part I)

a. First, you will begin your state machine design by assigning values of state variables Q1 and Q0 to four different duty cycles in an equally spaced interval between 0% to 75%. In this case, we cannot utilize a 100% duty cycle because this will make our input S constantly active, which in turn will prevent the transfer of charge from the inductor to the capacitor and will likely damage the inductor. Complete the table below with the corresponding duty cycles for each state variable values. For this part, 0% and 75% duty cycles have been specified for you.

Q1Q0	Duty Cycle
00	0%
01	25%
10	50%
11	75%

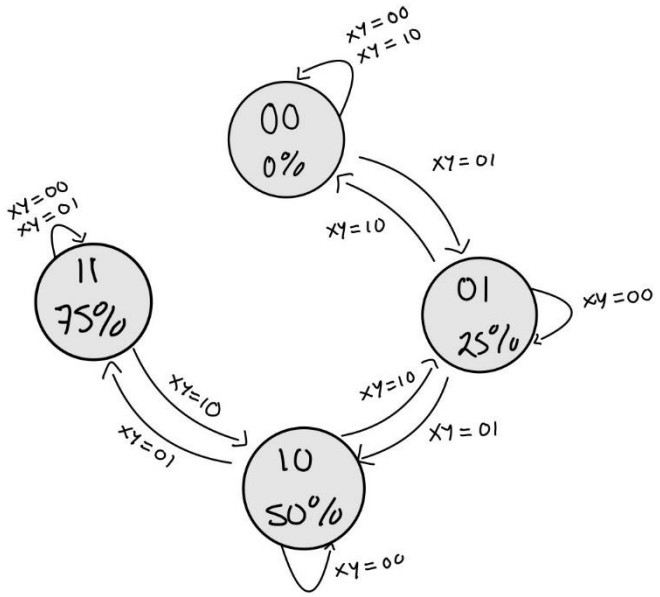
b. For the second part, you will be focusing on the voltage control section of the boost converter circuit. This section basically changes the duty cycle based on the value of V_{boost}. Here, you will notice there are three main signals labeled X, Y, and R which are inputs to your state machine. Whenever X is true or high, this means that V_{boost} is too high whereas when Y is true or high, this means that V_{boost} is too low. Lastly, R is an active-low asynchronous reset signal that is true (low) whenever V_{boost} is significantly low, which will in turn increase the duty cycle to its maximum value in order to raise the voltage. Complete the table below that describes the behavior of signal X, Y, and R based on V_{boost} and the outcome of this behavior.

Condition	Value of Inputs	Outcome
V_{boost} < 1.8 V	R = 0	Increase duty cycle to its maximum value (75%)
1.8 V <= V_{boost} < 1.9 V	R = 1, X =0, Y =1	Increase duty cycle to the next highest value
1.9 V <= V_{boost} < 2.1 V	R = 1, X = 0, Y = 0	Nothing occurs
V_{boost} >= 2.1 V	R = 1, X = 1, Y = 0	Decrease duty cycle to the next lowest value

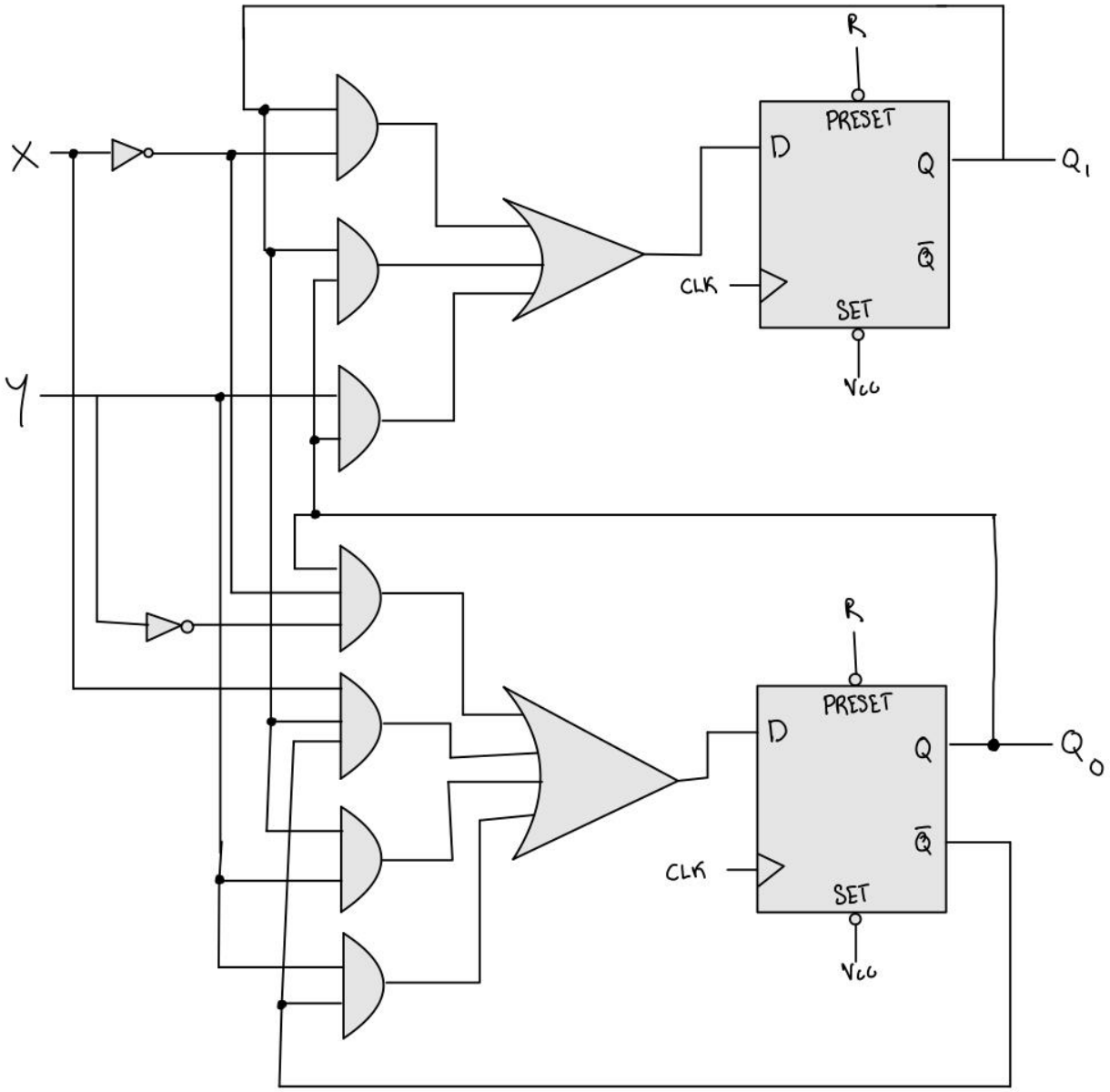
c. Complete a state transition table showing the current and next states of variables Q1 and Q0 based on the input values of X, Y, and R. Assume that an outcome that results in a decrease of the duty cycle when it is currently at 0%, will result in 0% being the next state. On the other hand, an outcome to increase the duty cycle when it is currently at 75%, will result in 75% being the next state.

Inputs		Current State		Next State	
X	Y	Q1	Q0	Q1+	Q0+
0	0	0	0	0	0
0	0	0	1	0	1
0	0	1	0	1	0
0	0	1	1	1	1
0	1	0	0	0	1
0	1	0	1	1	0
0	1	1	0	1	1
0	1	1	1	1	1
1	0	0	0	0	0
1	0	0	1	0	0
1	0	1	0	0	1
1	0	1	1	1	0
1	1	0	0	d	d
1	1	0	1	d	d
1	1	1	0	d	d
1	1	1	1	d	d

d. Draw, on paper, a state machine diagram that corresponds to your state transition table from part c.



e. Design and draw, on paper, your state machine circuit based on your answer from parts c and d.
Q1+ = Q0Y+Q1/X+Q1Q0, **Q0+** = /Q0Y+Q1Y+Q0/X/Y+Q1/Q0X



f. Why is it important to guarantee that the duty cycle stays at 0% when the outcome is set to decrease the duty cycle and at 75% when the outcome is set to increase the duty cycle?

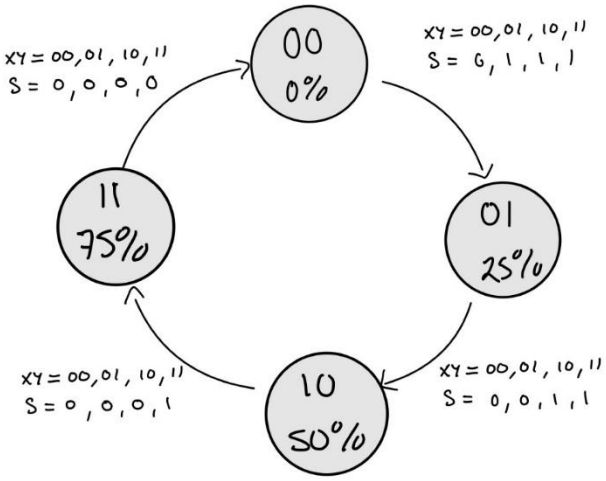
Whenever the duty cycle is at 0%, the voltage in the circuit is too high, therefore, whenever the inputs indicate a reduction in the duty cycle, we must stay at 0% duty cycle because otherwise, the circuit will have voltage that is extremely high and could cause damages to components in the circuit. On the contrary, if the duty cycle is at 75%, the voltage is too low, therefore, whenever the inputs indicate an increase in duty cycle, we must stay at 75% duty cycle because otherwise, the circuit will have voltage that is too low and lead to not maximizing the voltage conversion (for example in the cause of a battery input that is almost discharged).

1.3: Working with Boost Converters and Duty Cycles (Part II)

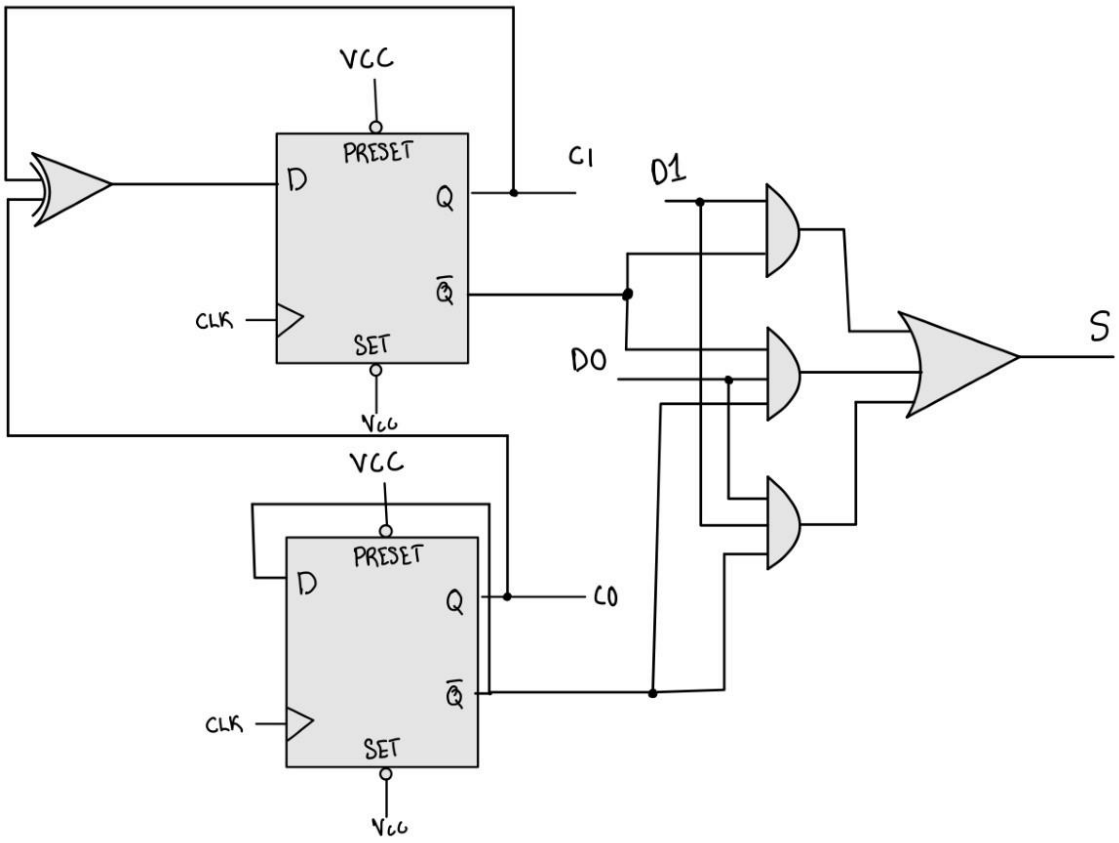
a. Create a state transition table for your 2-bit counter design that follows the pattern 00, 01, 10, 11 and goes back to 00, with inputs d1d0 and output S.

Inputs		Current State		Next State		Output
D1	**D0**	**C1**	**C0**	**Q1+**	**Q0+**	**S**
0	0	0	0	0	1	0
0	0	0	1	1	0	0
0	0	1	0	1	1	0
0	0	1	1	0	0	0
0	1	0	0	0	1	1
0	1	0	1	1	0	0
0	1	1	0	1	1	0
0	1	1	1	0	0	0
1	0	0	0	0	1	1
1	0	0	1	1	0	1
1	0	1	0	1	1	1
1	0	1	1	0	0	0
1	1	0	0	0	1	1
1	1	0	1	1	0	1
1	1	1	0	1	1	0
1	1	1	1	0	0	0

b. Draw, on paper, a state machine diagram based on your state transition table from part a.



c. Based on your answer from part a and b, design the logic circuit that corresponds to this counter. Before doing this, remember to define the logic expressions for your D flip-flops.
   Q1+ = C1 XOR C0, Q0+ = /C0, S = D1/C1+/C1/C0DO+D1D0/C0
d. Lastly, build your circuit from part c on the DEB. Use the OUT LEDs for your



outputs and time how long they are ON/OFF and compare this to the CLOCK signal on the DEB. This will help you demonstrate that the duty cycle follows the expected behavior.