1.3: Learning About Shift Registers

a. What are the benefits of each shift register configuration described in section 1.3?
   1. Serial In Serial Out Shift Register (SISO)
      The benefit of the SISO configuration is that it can delay the output of a system by various clock cycles depending on how many flip-flops are utilized.
   2. Serial In Parallel Out Shift Register (SIPO)
      The benefit of the SIPO configuration is that it is able to expand communication lines and I/O ports by translating a single communication line to multiple communication lines.
   3. Parallel In Serial Out Shift Register (PISO)
      The benefit of the PISO configuration is that it can input data from several communication lines and transform it into a single communication line.
   4. Parallel In Parallel Out Shift Register (PIPO)
      The benefit of the PIPO shift register is that it inputs data from several communication lines and the output does not have to be delayed by clock cycles, meaning that as soon as the flip-flop receives the digital input, it is able to output it faster than serial configurations.

1.4: Learning About the MSGEQ7

a. Design and construct your graphic equalizer circuit on the DEB using the devices specified above. You can test out your circuit by initially sending an audio signal of a single frequency (e.g. a 65 Hz frequency audio from YouTube). After this has successfully worked, try testing your circuit with any song you would like to make sure that the frequencies are shown as expected.