Practice Problems - Lab 7: Duty Cycle Controller/Power Electronic CKT

Duty Cycles/Boost Converters

1. What is a boost converter? What is it used for?

2. What is a duty cycle? What is it used for?

3. Draw, on paper, a square wave for an 85% duty cycle. Make sure to include what percentage the signal is on and off.

4. In lab 7 part II, you were asked to build a 2-bit counter. What would be the maximum switching frequency of the converter (signal S) if you wanted the maximum clock frequency for your counter to be 1MHz?

5. Draw, on paper, a timing diagram for the signal S from your duty cycle controller that shows the 25% and 75% duty cycles and includes the 2-bit counter clock and the counter current states.

6. Propose an equation for obtaining the maximum switching frequency in terms of the counter's clock frequency and the number of bits of the counter.

7. What is the tradeoff between the duty cycle precision (number of bits) and the maximum clock frequency? What is the benefit of less precise duty cycles?

Finite State Machines

1. Consider a circuit that repeats the sequence 01→11→00→10 and has an input A. If A is false or 0, the state machine does not transition to the next state. If A is true or 1, the state machine transitions to the next state.

    a. Draw, on paper, a state transition diagram for the FSM described above.
    b. Create a state transition table.
    c. Derive the logic equations for the outputs of the FSM flip-flops. Use D flip-flops in your design.
    d. Design, on paper, a circuit for the FSM using your answers from part a, b, and c.

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Solutions

Duty Cycles/Boost Converters

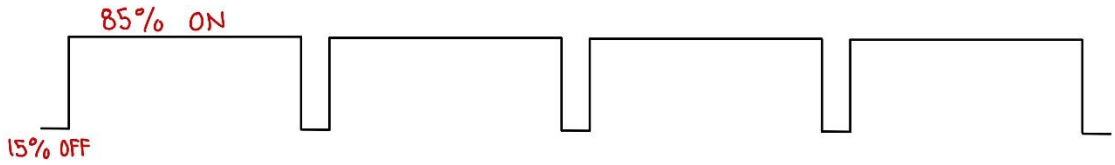
Question 1

A boost converter is a type of power circuit that is used for converting lower voltages to higher voltages for uses that include medical and wearable devices.

Question 2

A duty cycle is a percentage or ratio that is used for describing the period of time when a signal is active and inactive.

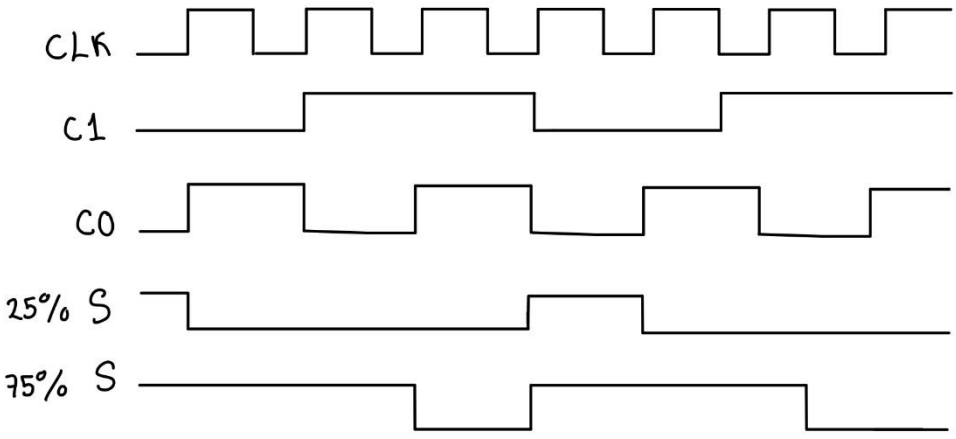
Question 3



Question 4

f_{max} = 1MHz / 4 = 250 kHz

Question 5



Question 6

$f_{max} = f_{clock} / 2^n$, where n = number of bits

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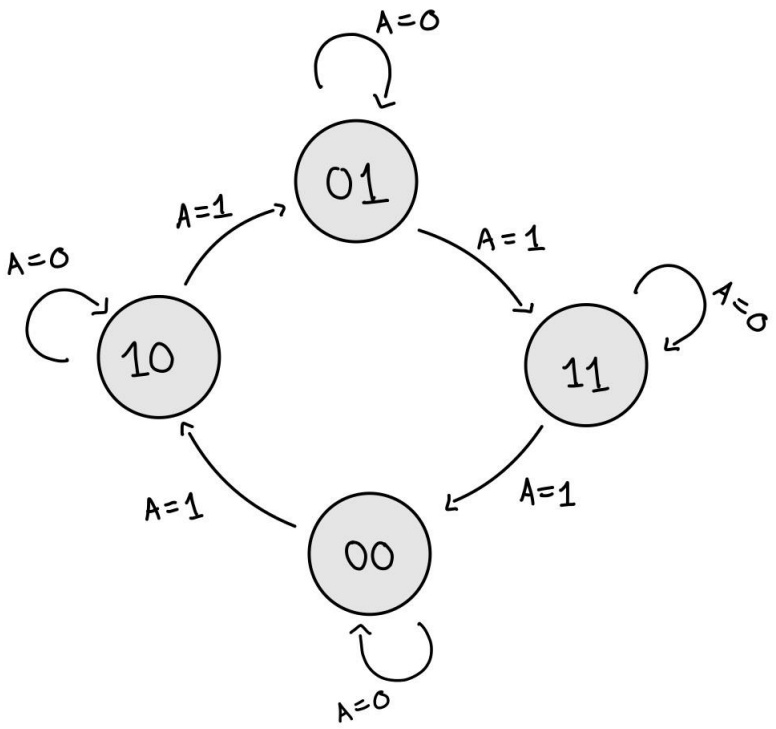
Question 7

Better precision is obtained with an increase in the number of bits. For example, if the number of bits is equal to 3, then d, which represents the duty cycle, can have values 0%, 12.5%, 25%, 37.5%, …, 87.5%, etc. This, however, leads to a higher clock frequency, which means that more power is consumed.

Finite State Machines

Question 1 part a



Question 1 part b

Current State		Input	Next State	
C1	C0	A	D1	D0
0	1	0	0	1
0	1	1	1	1
1	1	0	1	1
1	1	1	0	0
0	0	0	0	0
0	0	1	1	0
1	0	0	1	0
1	0	1	0	1

Question 1 part c

D1 = /C1C0A + C1C0/A + /C1/C0A + C1/C0/A

D0 = /C1C0/A + /C1C0A + C1C0/A + C1/C0A

Question 1 part d