Guideline for Design Development of Ball Grid or Column Grid Arrays with Pad Pitch of .5 mm or less.

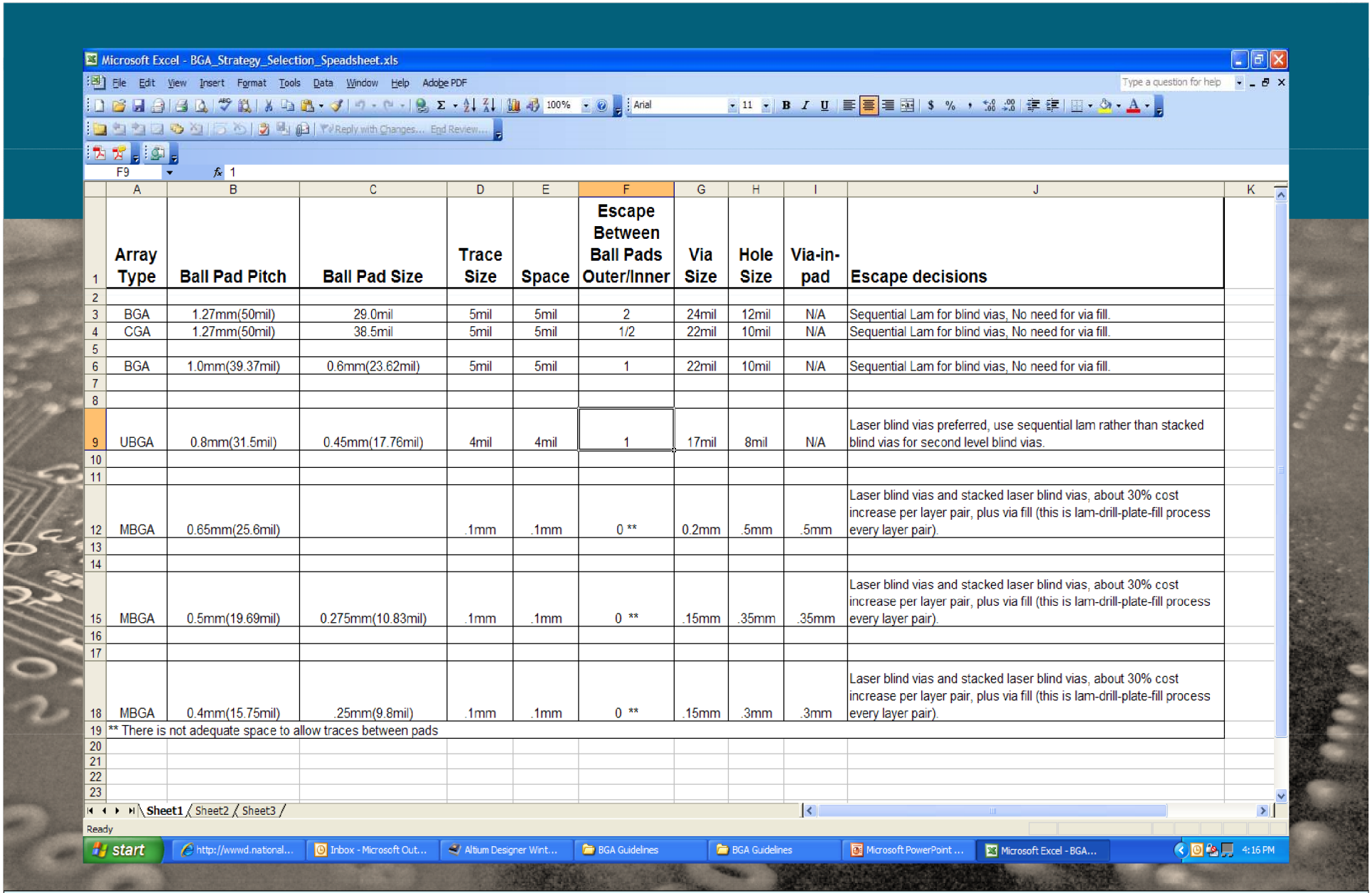
In most cases, if a BGA (Ball Grid Array) exists on your design, the escape requirement for the device will usually determine the stack-up needed for the design. Most large pin-count arrays are either 1.27mm, 1.0mm, or 0.8mm ball pitch that allows traces between pads. When you encounter an MBGA with a pad pitch of .65mm, .5mm or .4mm, traces between pads no longer work and a different design/stack-up strategy must be created.

These smaller pad-pitch devices generally have lower pin counts with fewer rows of pads to escape. However, they will require via-in-pad technology since there is no room for dog-boned vias next to each component pad. If pin swapping is allowed on the I/O pins, and especially if all the I/O pins are not used, you can work with the engineer to improve the escape strategy for the part. Your first concern should be any controlled impedance traces, their relationship to their reference plane, and whether you plan to use stripline or micro-strip routing techniques.

At this point, there are some important fabrication reliability and cost considerations to be reviewed. Selecting the fabricator that you wish to use for the board is important at this stage since interface with the fabricator will help to ensure high reliability and lowest cost for the technology, process and stack-up decisions made. For instance, blind via technology will almost certainly be required but whether to use laser micro-vias or mechanically drilled vias must be decided as well as which vias will be through and which will be blind. Another consideration at this stage is whether to use sequential lamination or additive layers (stacked blind vias). These decisions and the costs and reliability associated with them cannot be made without a fabrication partner. Even the small variations in equipment and methodologies from one fabricator to another could dramatically affect your product.

Since a laser drilled blind via should not exceed an aspect ratio of 1:1 (the preferred ratio is only 0.5:1), stacked vias would be required to get to inner layers more than about 6 mils deep (one or two layers). Mechanically drilled vias of 4.7 mils, 5.9 mils and 7.9 mils can be drilled when using sequential lamination. Be sure that the sub-part overall thickness is substantially below 10:1 aspect ratio to achieve good hole wall plating properties.

Now for .4 mm MBGA escape strategies. Use the spreadsheet in Figure 1. as a starting point for ball pad size, via size, and trace and space width to begin configuring a stack-up and your escape strategy.



Array Type	Ball Pad Pitch	Ball Pad Size	Trace Size	Space	Escape Between Ball Pads Outer/Inner	Via Size	Hole Size	Via-in-pad	Escape decisions
BGA	1.27mm(50mil)	29.0mil	5mil	5mil	2	24mil	12mil	N/A	Sequential Lam for blind vias, No need for via fill.
CGA	1.27mm(50mil)	38.5mil	5mil	5mil	1/2	22mil	10mil	N/A	Sequential Lam for blind vias, No need for via fill.
BGA	1.0mm(39.37mil)	0.6mm(23.62mil)	5mil	5mil	1	22mil	10mil	N/A	Sequential Lam for blind vias, No need for via fill.
UBGA	0.8mm(31.5mil)	0.45mm(17.76mil)	4mil	4mil	1	17mil	8mil	N/A	Laser blind vias preferred, use sequential lam rather than stacked blind vias for second level blind vias.
MBGA	0.65mm(25.6mil)		.1mm	.1mm	0 **	0.2mm	.5mm	.5mm	Laser blind vias and stacked laser blind vias, about 30% cost increase per layer pair, plus via fill (this is lam-drill-plate-fill process every layer pair).
MBGA	0.5mm(19.69mil)	0.275mm(10.83mil)	.1mm	.1mm	0 **	.15mm	.35mm	.35mm	Laser blind vias and stacked laser blind vias, about 30% cost increase per layer pair, plus via fill (this is lam-drill-plate-fill process every layer pair).
MBGA	0.4mm(15.75mil)	.25mm(9.8mil)	.1mm	.1mm	0 **	.15mm	.3mm	.3mm	Laser blind vias and stacked laser blind vias, about 30% cost increase per layer pair, plus via fill (this is lam-drill-plate-fill process every layer pair).

** There is not adequate space to allow traces between pads

Figure 1.

After choosing pad and trace sizes and planning an escape strategy, configure an evenly structured stack-up the same as you would with larger components only in this case you'll need to consider what pads or via stacks must be cleared to get at each successive row of pins. Figure 2 shows the stack-up used for the example part.

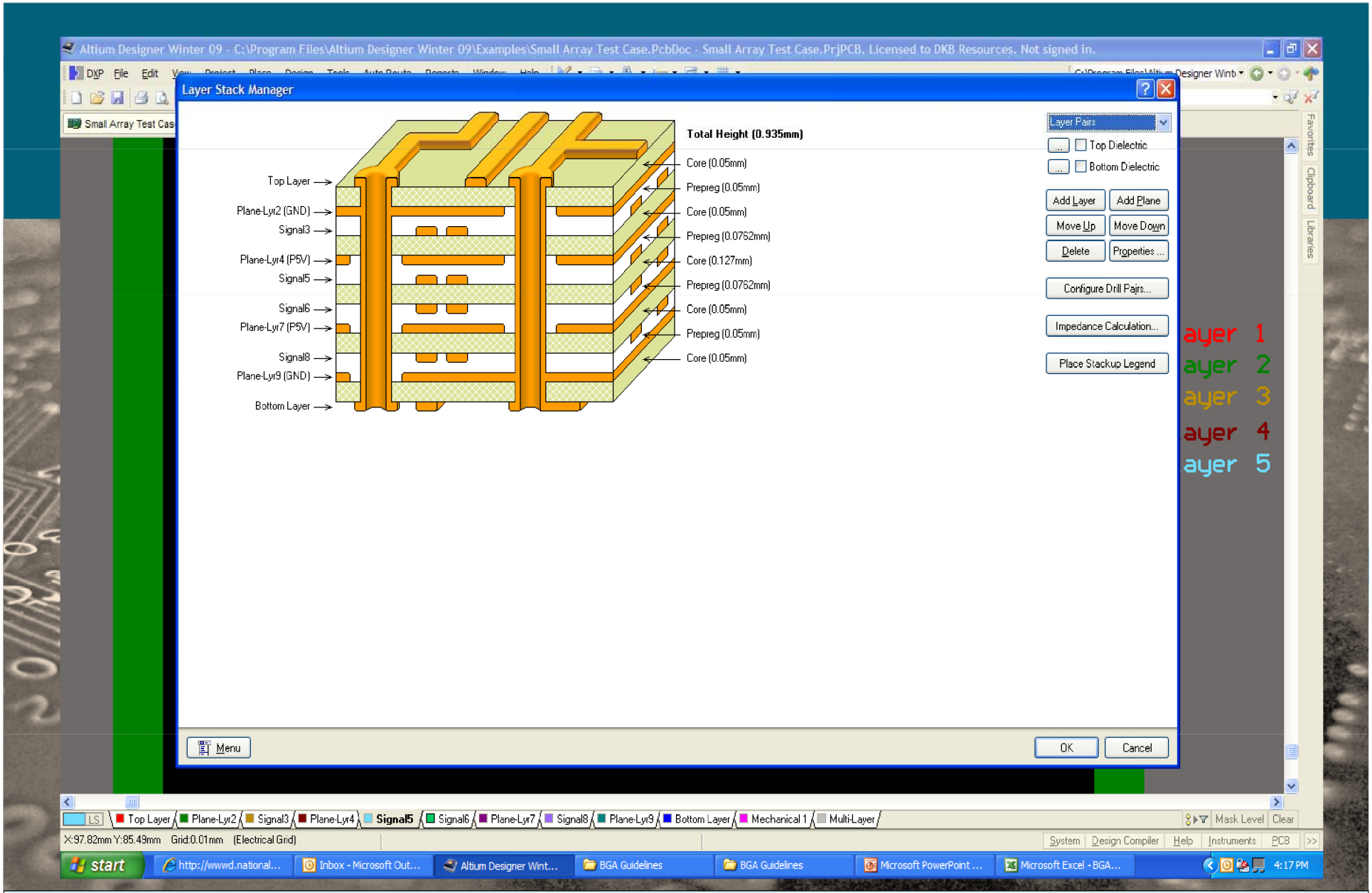

Altium Designer Winter 09 - C:\Program Files\Altium Designer Winter 09\Examples\Small Array Test Case.PcbDoc - Small Array Test Case.PrjPCB. Licensed to DKB Resources. Not signed in.
Layer Stack Manager
Total Height (0.935mm)
Top Layer
Plane-Lyr2 (GND)
Signal3
Plane-Lyr4 (P5V)
Signal5
Signal6
Plane-Lyr7 (P5V)
Signal8
Plane-Lyr9 (GND)
Bottom Layer
Core (0.05mm)
Prepreg (0.05mm)
Core (0.05mm)
Prepreg (0.0762mm)
Core (0.127mm)
Prepreg (0.0762mm)
Core (0.05mm)
Prepreg (0.05mm)
Core (0.05mm)
Layer Pairs
Top Dielectric
Bottom Dielectric
Add Layer
Add Plane
Move Up
Move Down
Delete
Properties ...
Configure Drill Pairs...
Impedance Calculation...
Place Stackup Legend
Menu
OK
Cancel
ayer 1
ayer 2
ayer 3
ayer 4
ayer 5
Top Layer
Plane-Lyr2
Signal3
Plane-Lyr4
Signal5
Signal6
Plane-Lyr7
Signal8
Plane-Lyr9
Bottom Layer
Mechanical 1
Multi-Layer
X:97.82mm Y:85.49mm Grid:0.01mm (Electrical Grid)
start
4:17 PM

Figure 2.

This design is a ten layer stack up using a four layer core composite (all .5 oz copper) and with 3 pairs of additive layers successively added pair by pair to achieve the 1, 2, 3, and 4 deep stacked via sets and then through vias needed for this design. The stacked vias are laser drilled, filled with non-conductive resin and then plated to mate with the next via above. They are called out at .15mm (6mils) allowing the fabricator to use an optimum hole size between .1 and .15mm. The through vias are 6 mil mechanically drilled vias. The overall board thickness must be held to no more than about 1.4mm, an aspect ratio of < 10:1 hole size to maximum board thickness, not nominal thickness.

To create the stacked vias, beginning with the four layer core part, each set of vias must be laser drilled then plated, filled, imaged, and etched, after each successive pair of pre-preg and foil layer pairs is added.

This particular board must go through four press runs, pointing up the need to have even build up of signal and plain layers to reduce and copper distribution to ease stress during the lamination cycles and reduce the possibility of warpage in the finished product.

The example in Figure 3 is a .4mm pad pitch array with 209 pins. This is a fairly large pin count for a .4mm part for today s' technologies. It should demonstrate most of the issues and problems you might encounter during your own design effort. On this design, the ball pads are .3mm, the traces are .1mm as are the spaces. The vias are also .3mm with a .15mm hole. That includes the through vias.

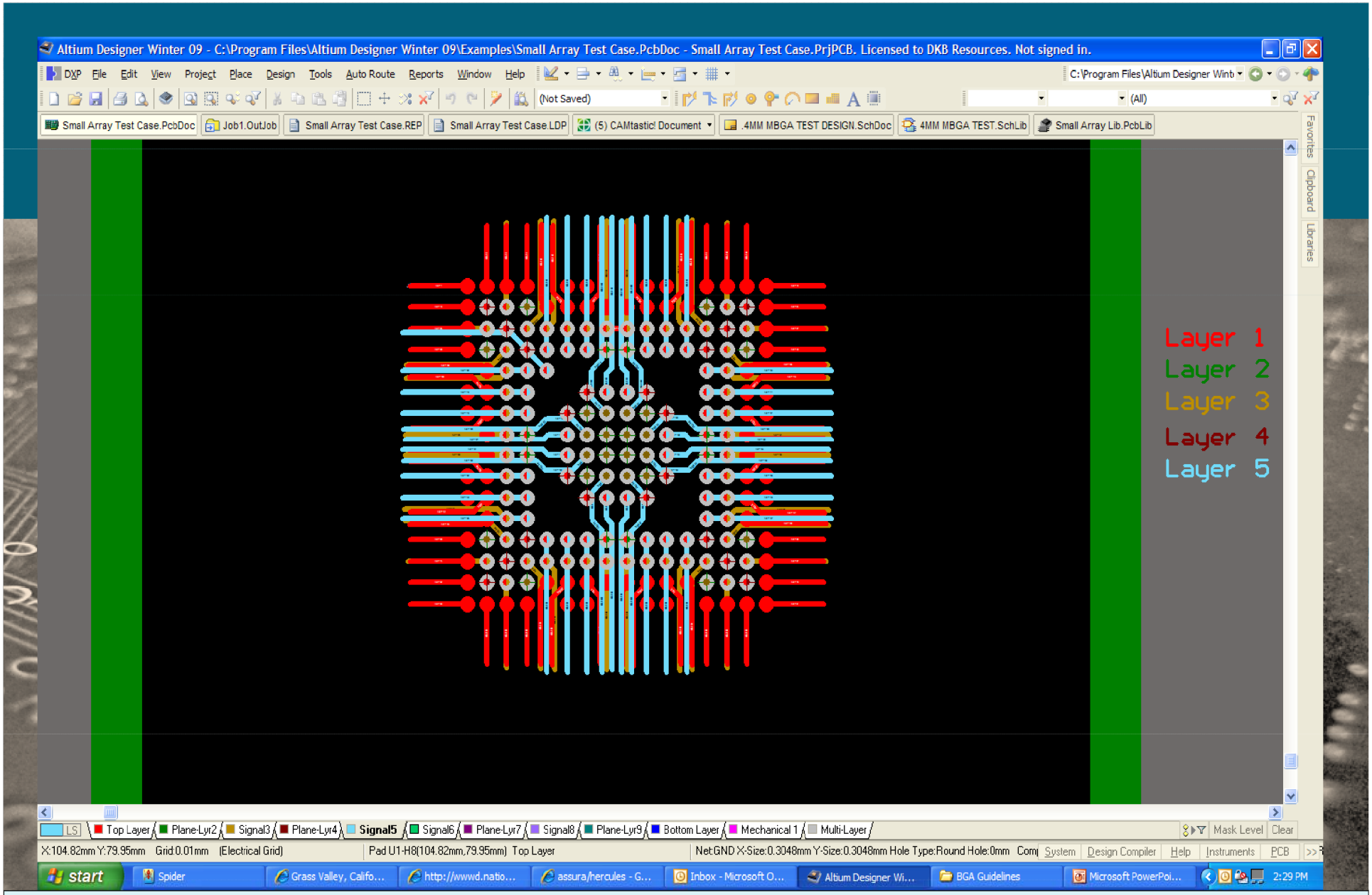


Figure 3.

All of the pins from the outer most row and most pins the second row can escape on layer one. Since a pad must remain in place for every ball on the array, an ideal condition would be to have all of the surface accessible pins used. The escape for layer one is shown in Figure 4.

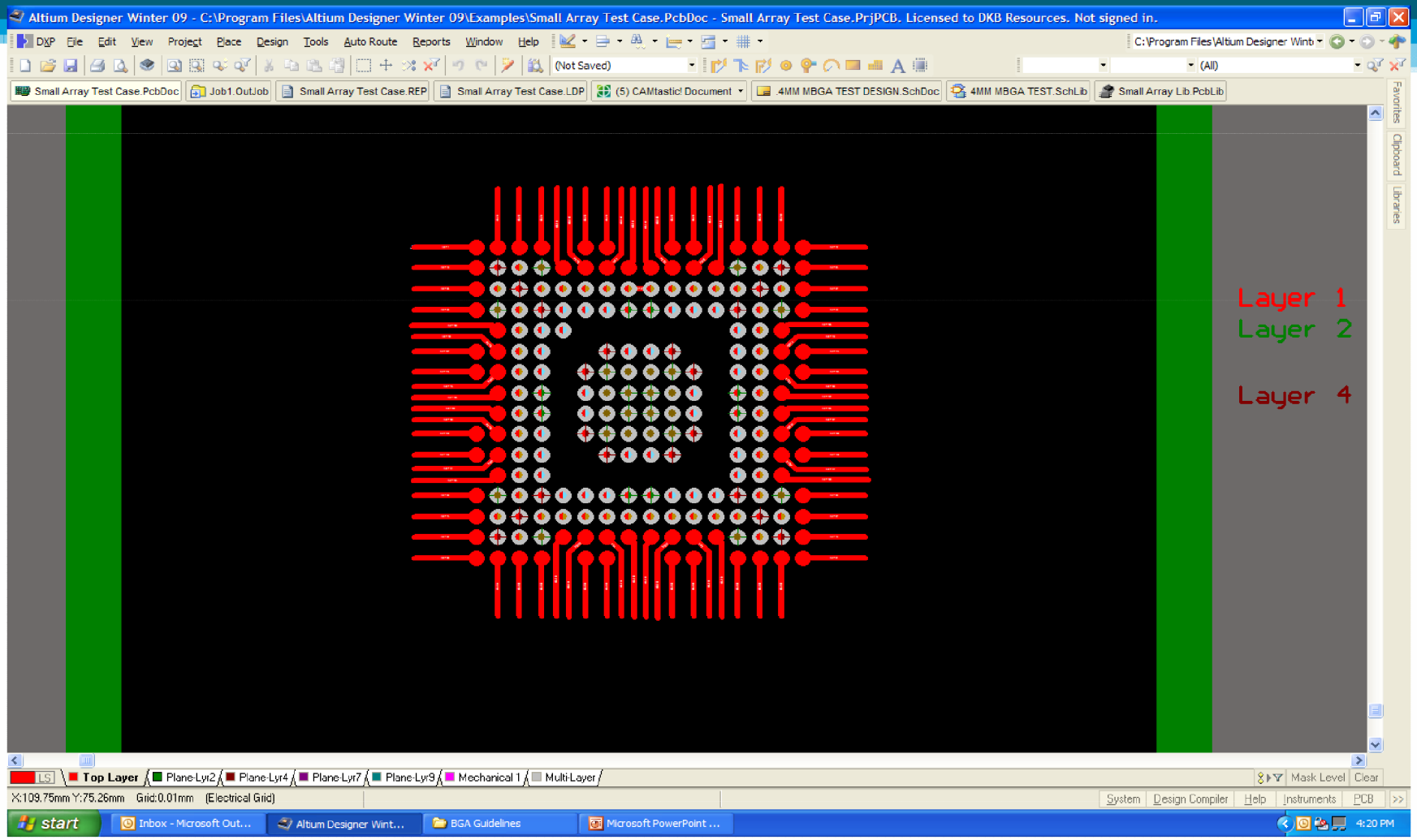


Figure 4.

The third row and the inaccessible pads from the second row now must be accessed through the shallowest vias used. This would either be layer two or three depending on whether you need a ground layer next to the surface for a reference plane or EMI protection. In this example, layer 2 is a ground plane as shown in Figure 5. Note that the ground connections are spread throughout the design to allow adequate copper to as many thermal relief ports as possible. The ground and power connections must have thermals rather than solid connections as in larger arrays because you're connecting a ball pad, not a dog-boned via. Remember, what you are trying to achieve is to escape under successive vias or pads from the layer above and move from the outside edge of the component inward.

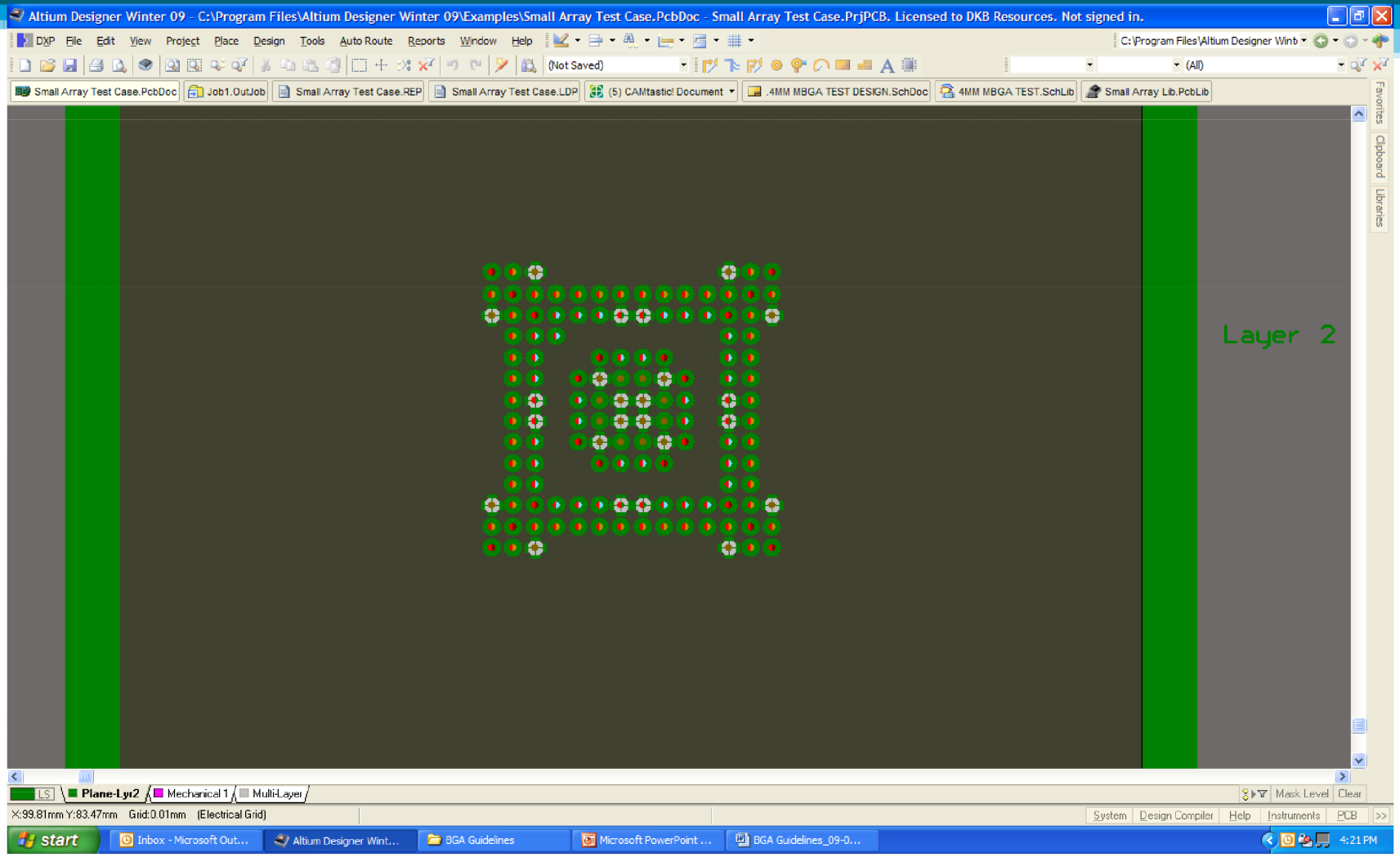


Figure 5.

Now the second escape layer becomes layer 3 as shown in figure 6.

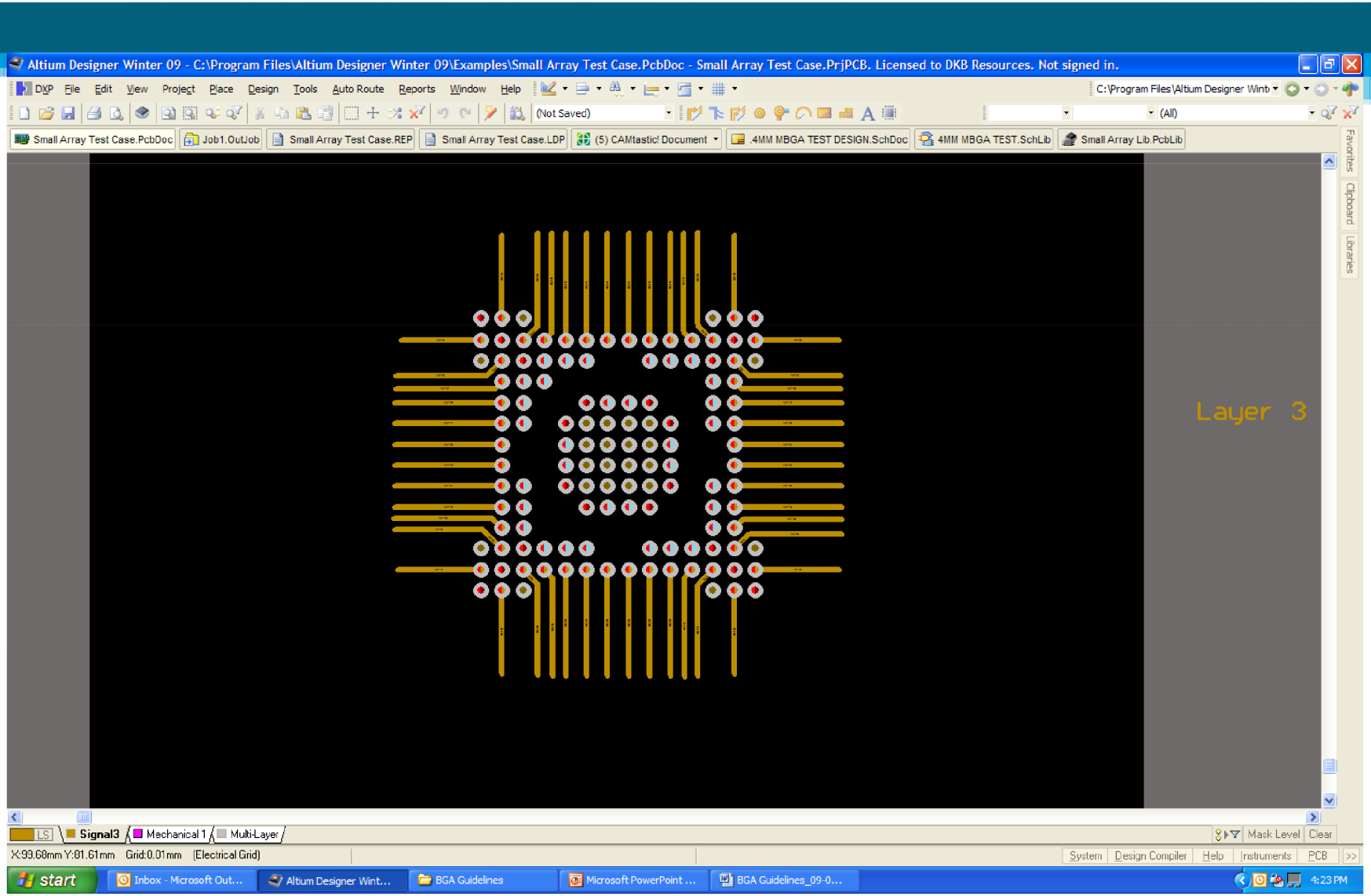


Figure 6.

You are now able to escape from the third layer by traveling directly beneath the first and second row pads on the layers above. Also note on Figure 6 that two pads from the center of each of row four are missing. These were ground connections that only dropped to layer two and do not go through to the lower ground plane as all of the other ground pins do. You can see why this is necessary in Figure 8 later on. Next, layer 4 is a plane and carries power (P5V) shown in figure 7.

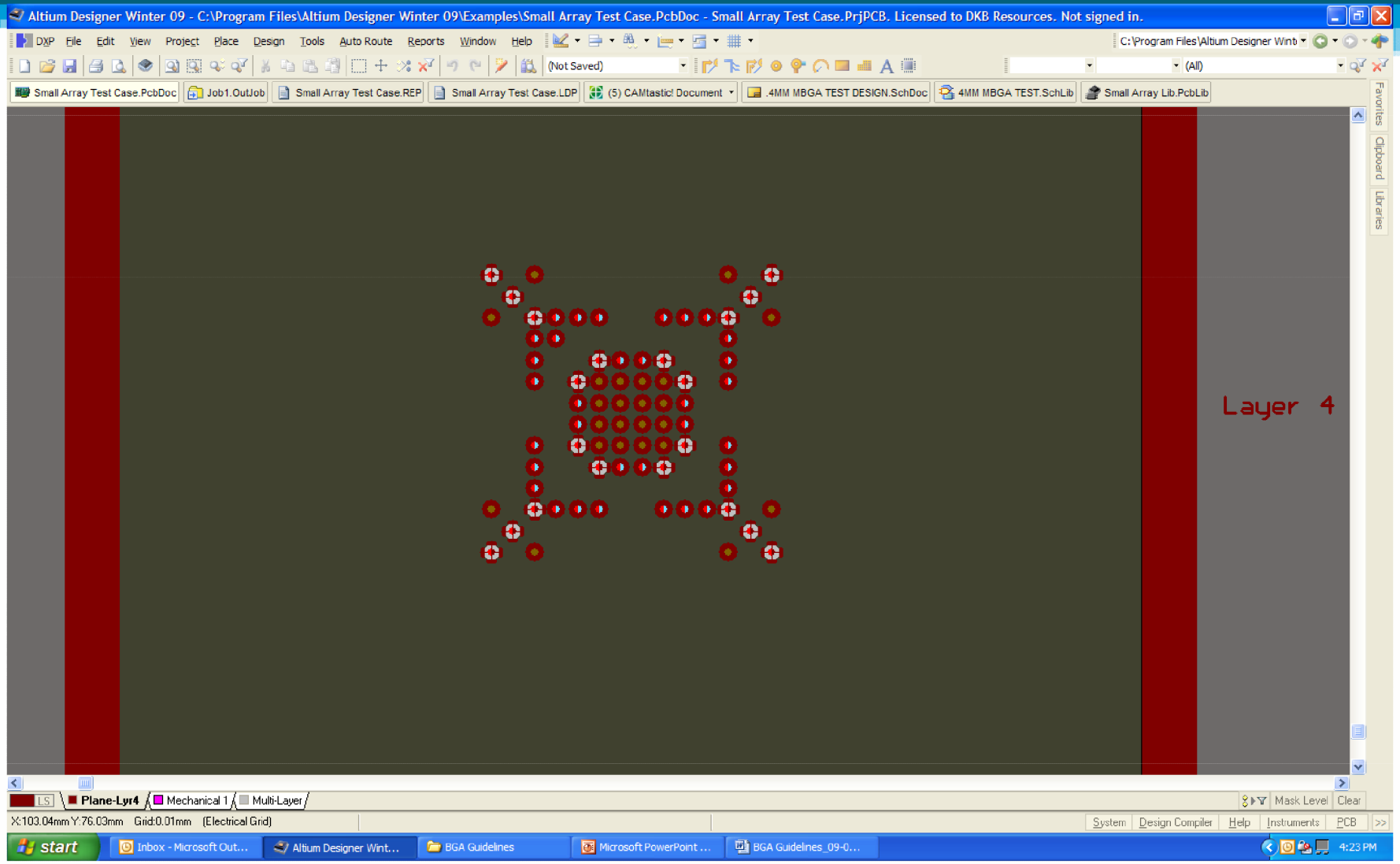


Figure 7.

You'll notice that on the power plane, the power pins are spread widely to once again achieve optimum copper connection. The only remaining cleared pads are ground pins going through the board and the remaining un-escaped I/O pins. These escapes are on layer 5 and are shown in Figure 8.

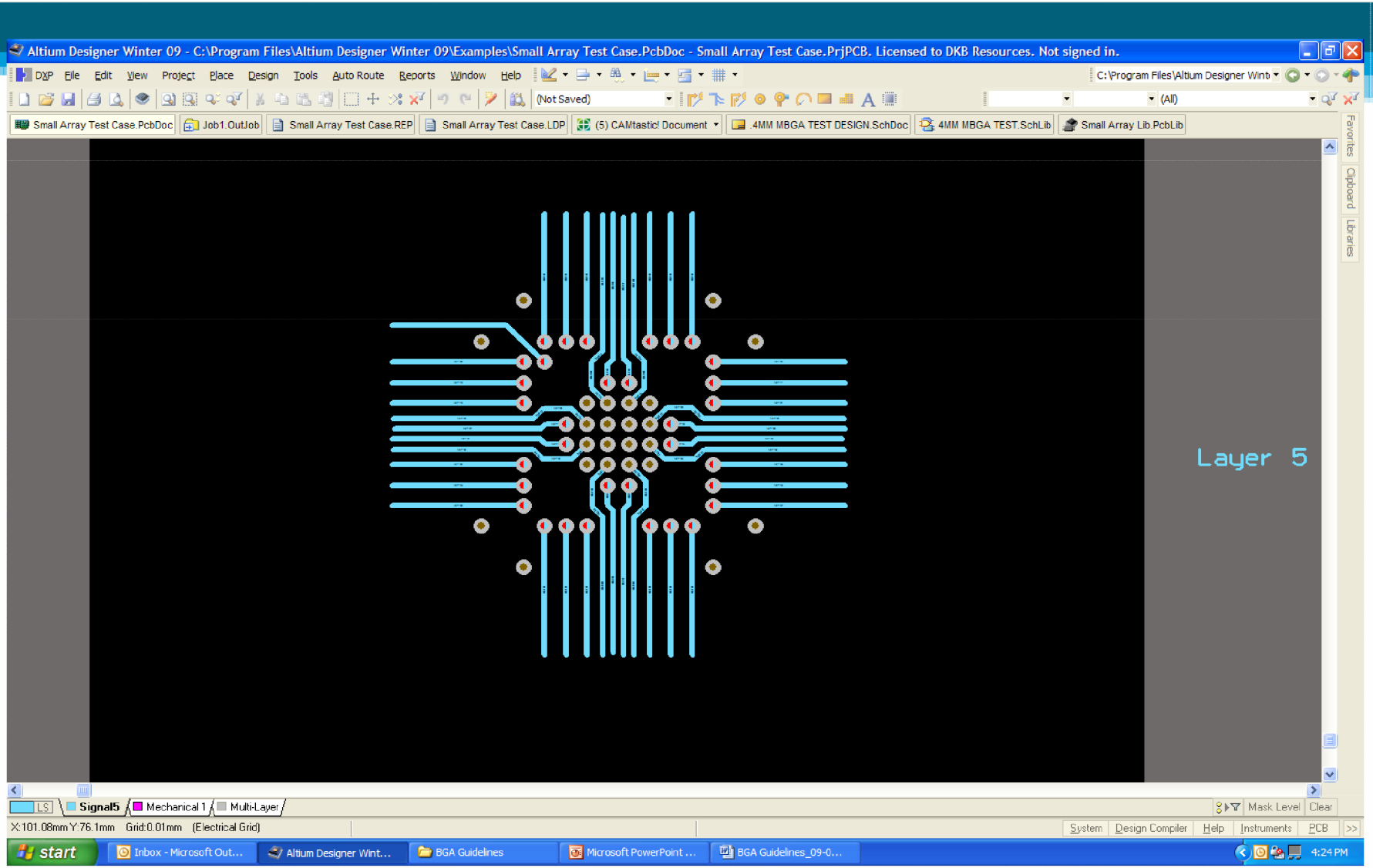


Figure 8.

In viewing Figure 8 it now becomes evident why the 2 ground pins in each of the fourth rows were stopped at layer 2. This gives us a path to escape the sixteen I/O pins in the center pad group. At this point the part is fully escaped. In most cases, all pins on an array are not used. This will make the escape plan easier. However, it is important to remember that all the balls are always on the pins, connected or not, so you must have a ball pad for each regardless of which ones need to be escaped.

There are two conditions that are of concern when using stacked vias. These items have been mentioned earlier but bear repeating. First, all of the connections for power and ground, if connected to a plane rather than trace, must be thermally relieved on the plane layers. At fabrication, all vias whether through or blind must be filled and plated to receive the array ball. You're likely to get cold or open connections when the part is soldered if thermal relief is not provided.

Second, the power and ground connections should be alternated rather than next to each other in the pattern. Although there will probably be some restrictions placed on the location of these pins from the array manufacturer and possibly by the engineer as well, it is critical that they are arranged to optimize copper connection as part of your escape strategy from the start.