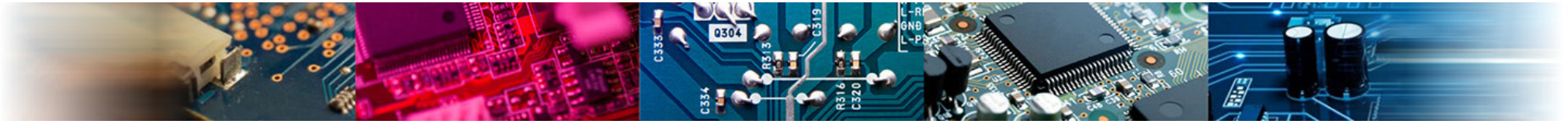
Tech Microvias & SMV Technology

TECH DRIVEN
Electronic Manufacturing Solutions

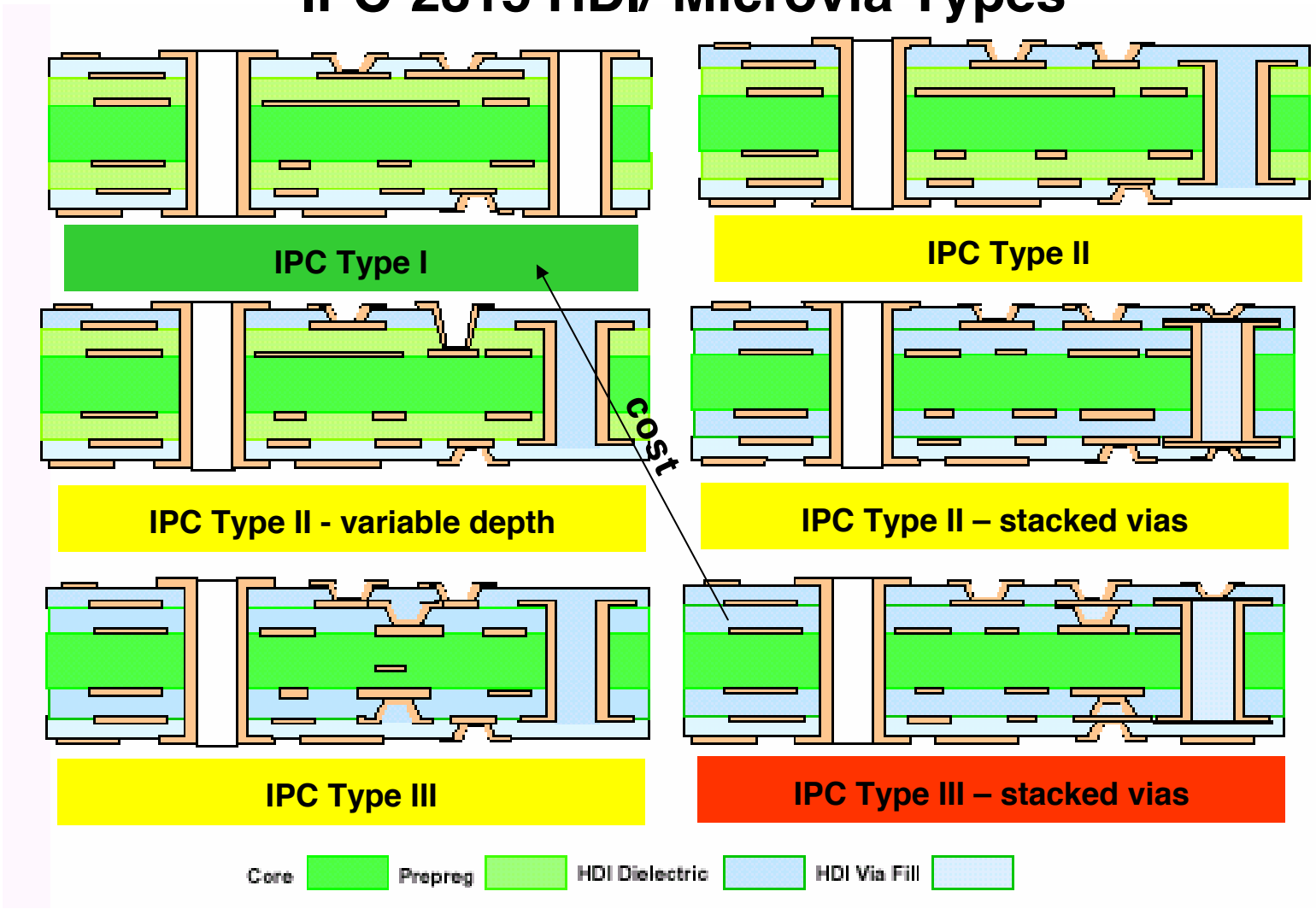
Your Full Circuit Solution.



TD Technology

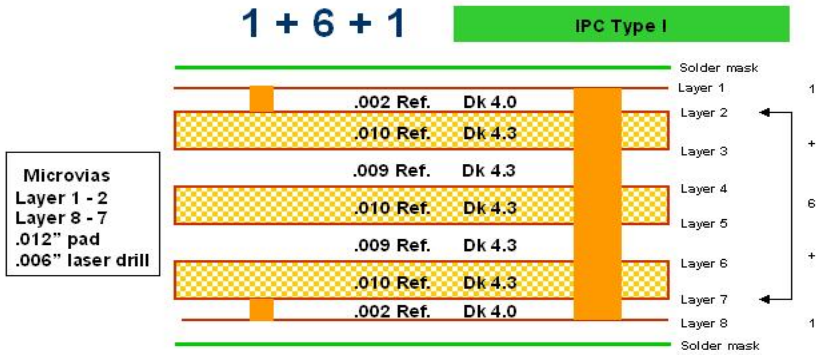
Laser Drilled Blind & Buried Microvias

IPC-2315 HDI/ Microvia Types



TD Technology

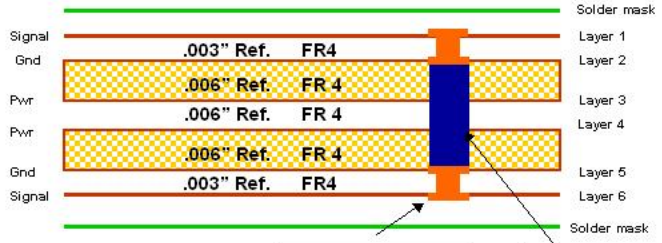
1 + 6 + 1 — IPC Type I



Finish Thickness = .062 +/- .006
Material = High Temp FR4

Layer 1 – 8 through vias
.020" pad & .010" drill

1 + 4 + 1 — IPC Type II – stacked vias

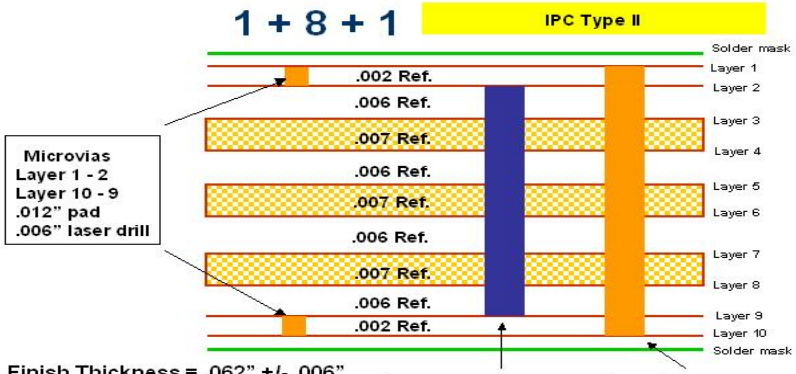


Stacked Microvias
Layer 1 - 2
Layer 6 - 5
.010" pad
.004" laser drill

Buried vias
Layer 2-5
.010" drill
.020" pad
Fill with conductive epoxy

Finish Thickness = .032" +/- .003"

1 + 8 + 1 — IPC Type II

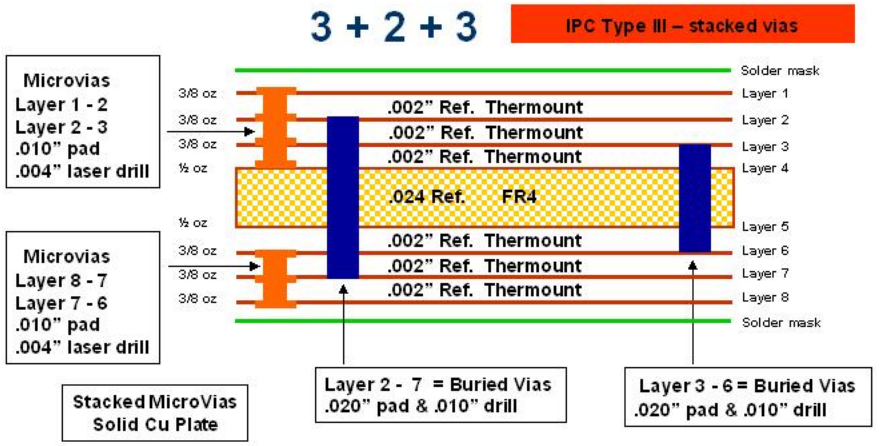


Finish Thickness = .062" +/- .006"
Material = High Temp FR4

Layer 2 - 9 buried vias
.018" pad & .008" drill

Layer 1 - 10 through vias
.020" pad & .010" drill

3 + 2 + 3 — IPC Type III – stacked vias



Stacked MicroVias
Solid Cu Plate

Layer 2 - 7 = Buried Vias
.020" pad & .010" drill

Layer 3 - 6 = Buried Vias
.020" pad & .010" drill

Finish Thickness = .048 +/- .004
4 175° C Tg & Thermount

TD Technology

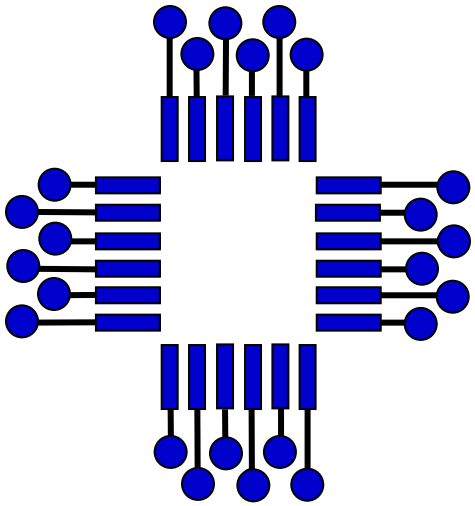
Microvia Materials

- RCC™ Resin Coated Copper
  - single stage, double stage or B & C stage
- RCF Resin Coated Foil Single stage
- Glass Reinforced Prepreg FR4 = 106, 1080
- Thermount®
- SpeedBoard ™ C

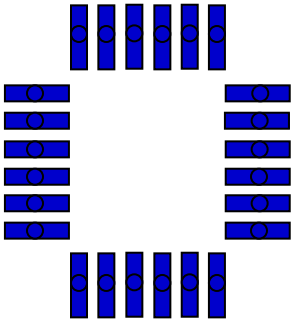
TD Technology

Via-in-Pad Microvia Technology

Present Technology

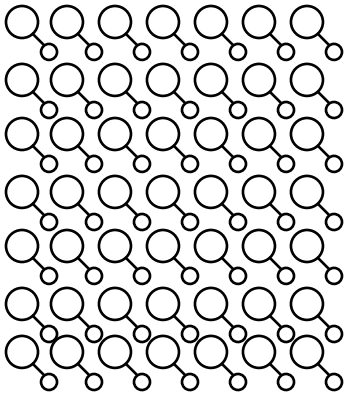


Via-in-Pad Technology

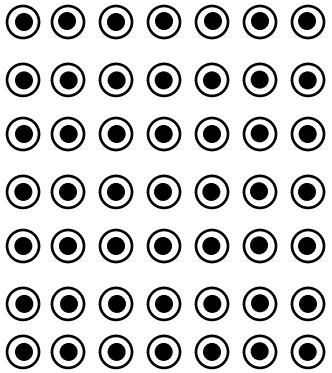


QFP Land Pattern

Present Technology



Via-in-Pad Technology

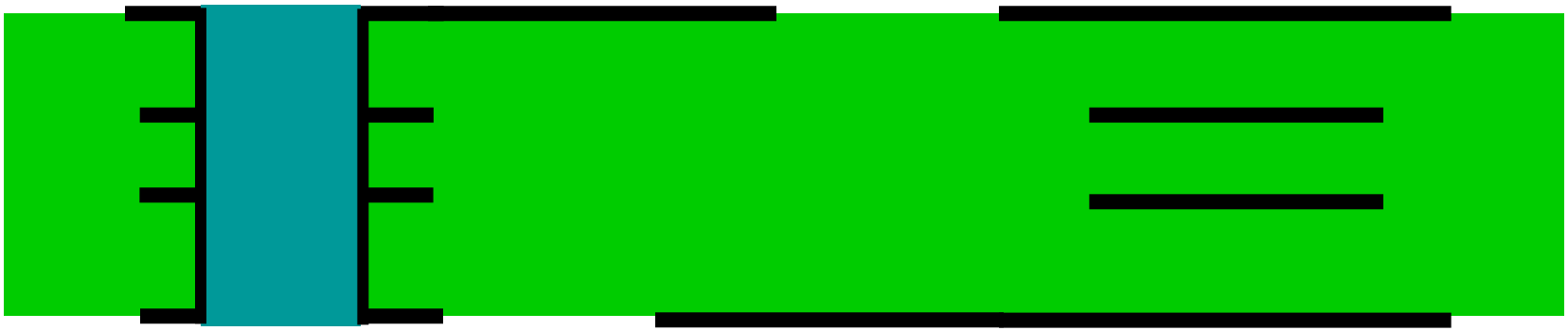


BGA Land Pattern

Fine Pitch-SMT and BGA area array with Via-in-Pad

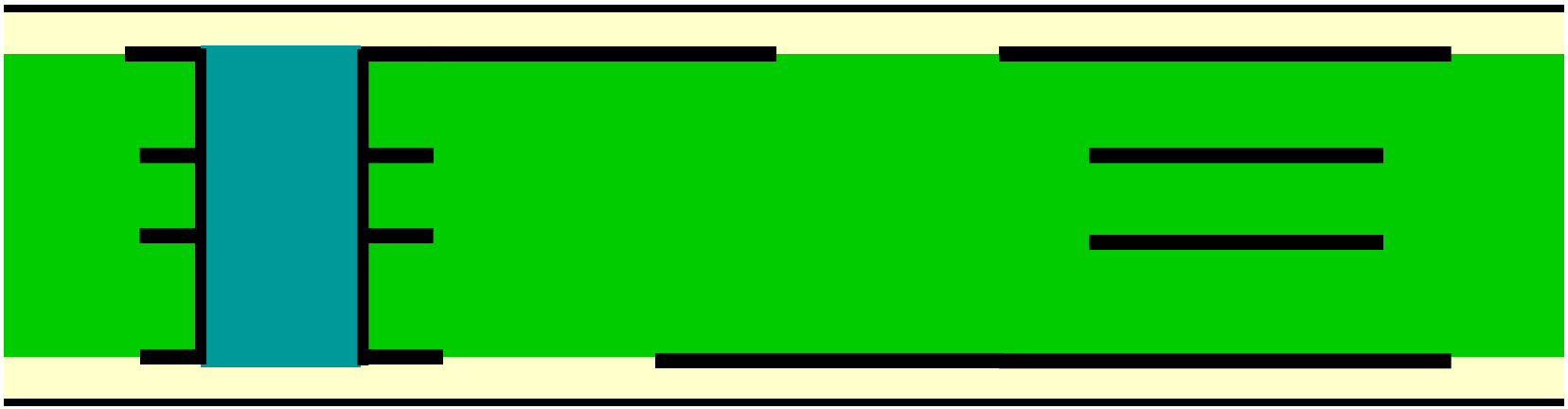
TD Technology

Build-Up-Multilayer (BUM)



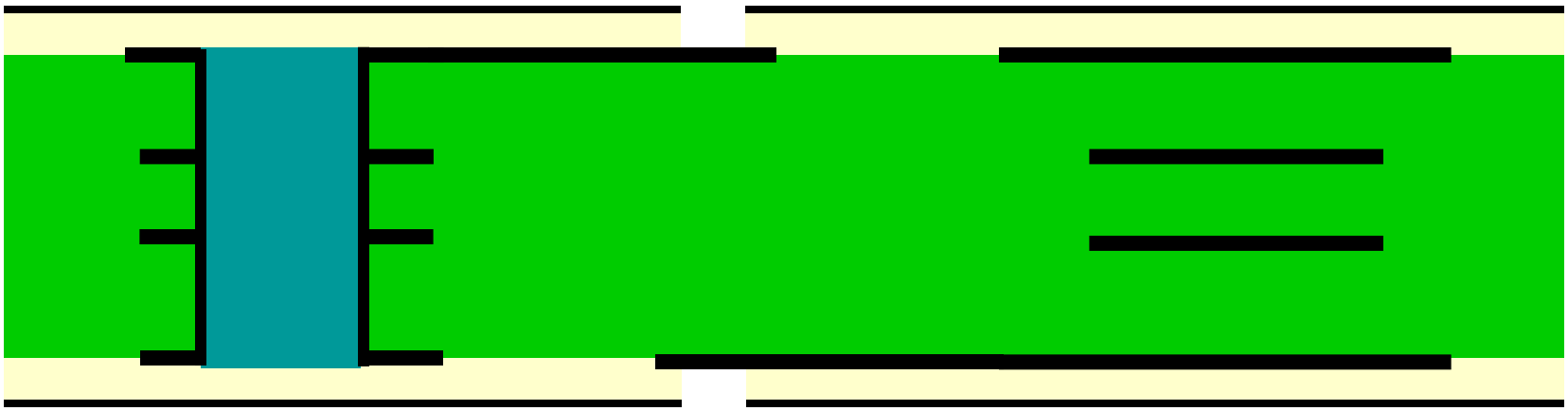
1. Fabricate multilayer PCB (2 - 38 layers)
2. Fill plated through holes with non-conductive epoxy fill

TD Technology



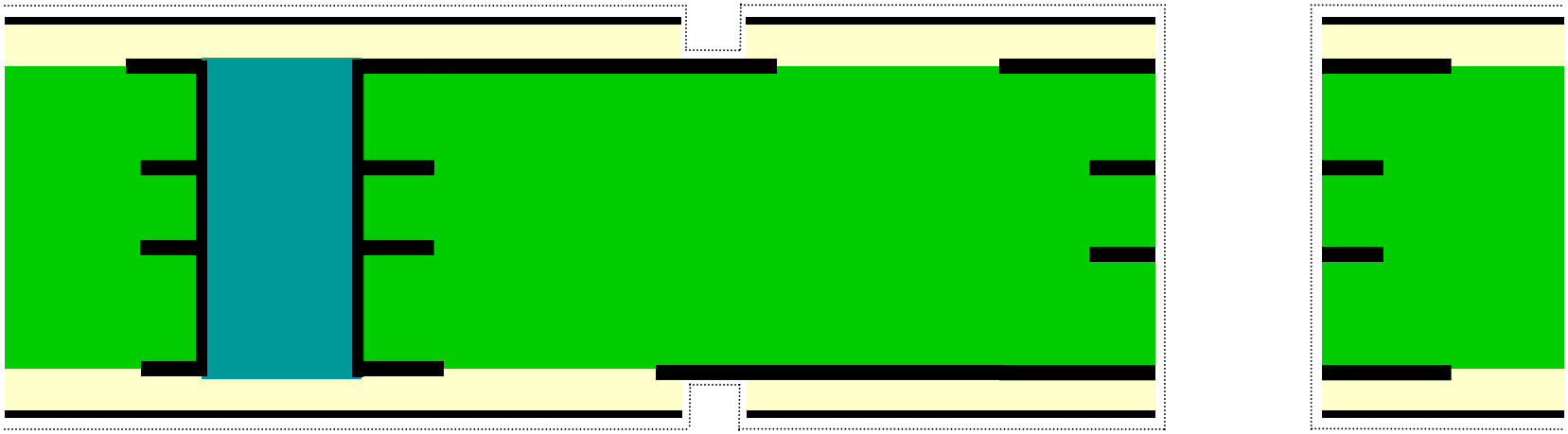
1. Fabricate multilayer PCB (2 - 38 layers)
2. Fill plated through holes with non-conductive epoxy fill
3. Laminate Microvia material (FR4, RCF, Thermount™, Speedboard C)

TD Technology



1. Fabricate multilayer PCB (2 - 38 layers)
2. Fill plated through holes with non-conductive epoxy fill
3. Laminate Microvia material (FR4, RCF, Thermount™, Speedboard C)
4. Laser Drill Microvias (150 microns down to 100 microns)

TD Technology



1. Fabricate multilayer PCB (2 - 38 layers)
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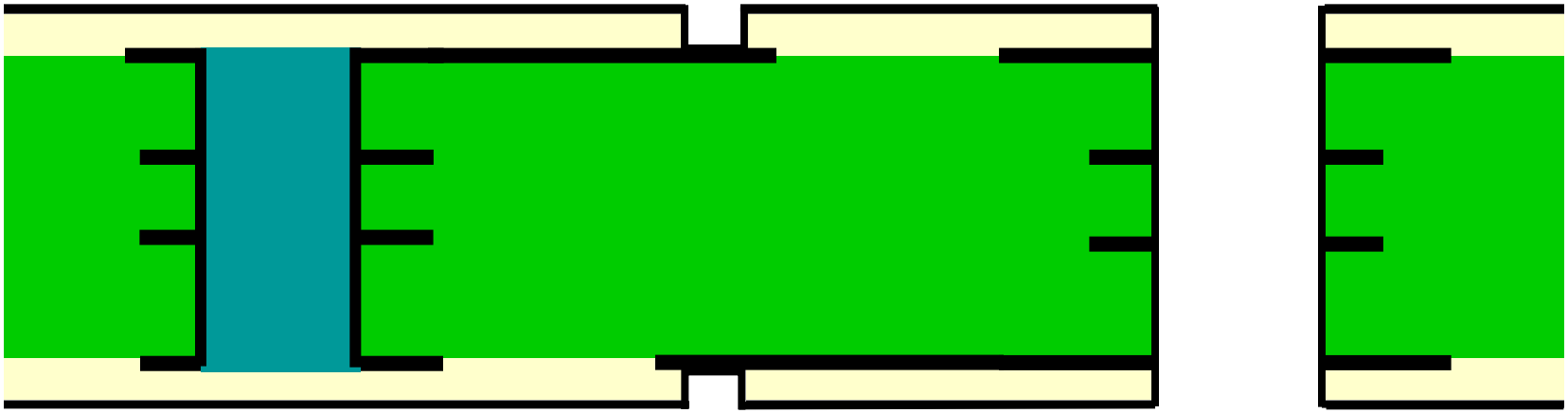
3. Laminate Microvia material (FR4, RCF, Thermount™, Speedboard C)
4. Laser Drill Microvias (150 microns down to 100 microns)
5. Mechanical Drill through-holes
6. Desmear through holes and microvias to roughen dielectric surface prior to plating

TD Technology



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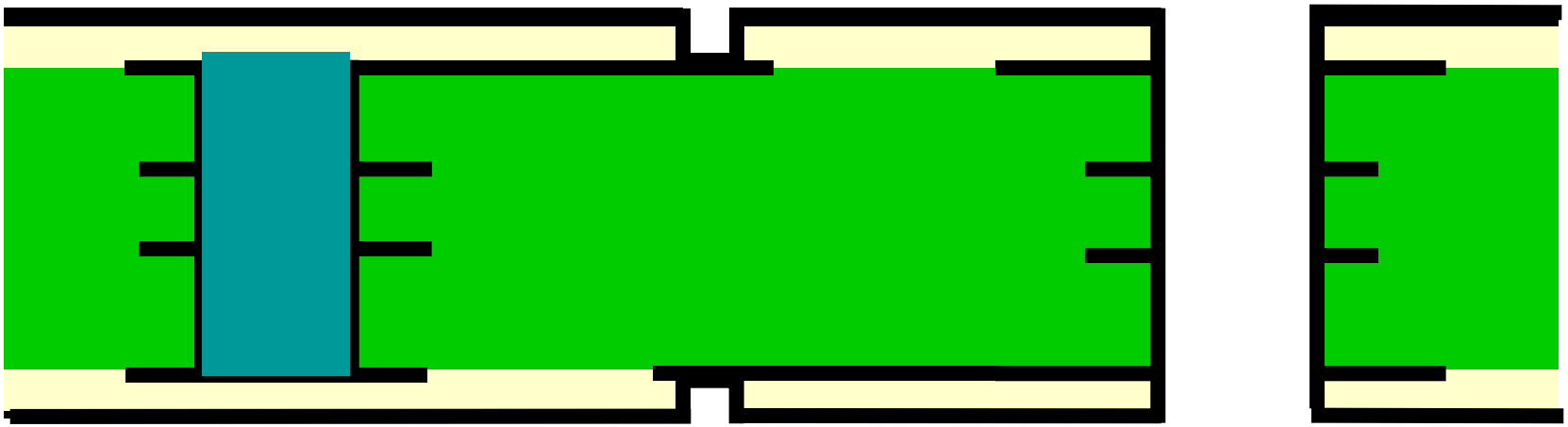
2. Fill plated through holes with non-conductive epoxy fill
3. Laminate Microvia material (FR4, RCF, Thermount™, Speedboard C)
4. Laser Drill Microvias (150 microns down to 100 microns)
5. Mechanical Drill through-holes
6. Desmear through holes and microvias to roughen dielectric surface prior to plating
7. Electroless copper plate through holes, Microvias, and surface areas

TD Technology



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4. Laser Drill Microvias (150 microns down to 100 microns)
5. Mechanical Drill through-holes
6. Desmear through holes and microvias to roughen dielectric surface prior to plating
7. Electroless copper plate through holes, Microvias, and surface areas
8. Pattern Plate outer layer circuits

TD Technology

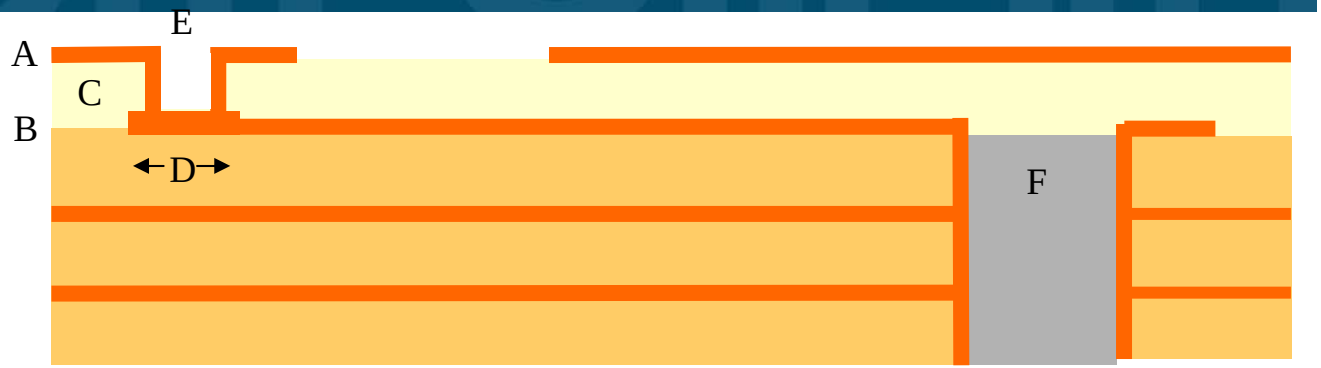
Microvia Design Guidelines

Prior to the Design of Microvia Technology, Consult with your assembly Team to ensure they have experience with the assembly of Microvia or Via-in-Pad Technology

TD Microvia Technology

Laser Drilled Microvias

Layer 1 to 2



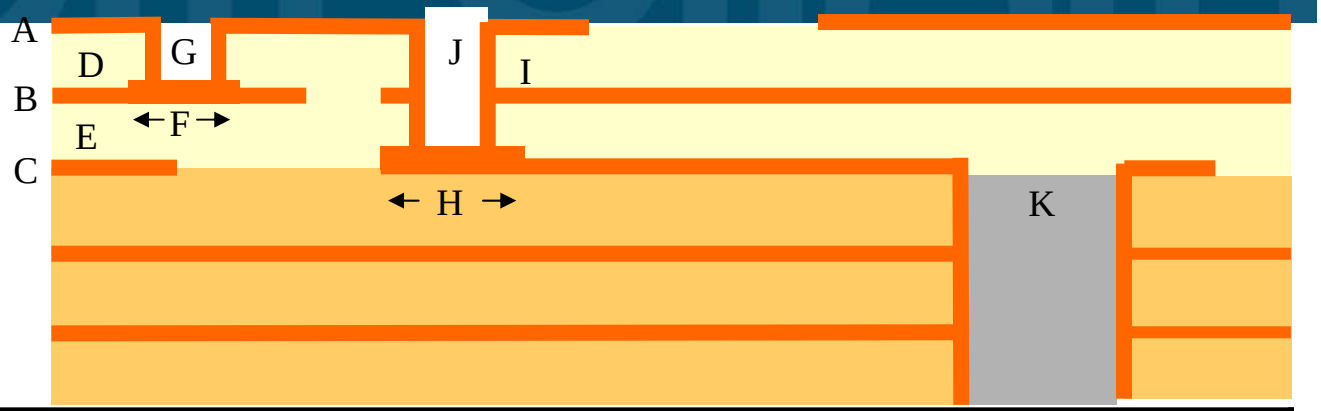
#	Description	Standard Microvia		Advanced Microvia	
		µm	+/-	µm	+/-
A	Minimum Layer 1 copper thickness	52	20%	45	10%
B	Minimum Layer 2 copper thickness	40	20%	40	10%
C	Layer 1 – 2 dielectric thickness	25 to 50	10%	25 to 75	10%
D	Minimum Layer 2 pad for Layer 1 to 2 Microvia	300	NA	300	NA
E	Minimum Layer 1 pad for Layer 1 to 2 Microvia	250	NA	250	NA
F	Minimum drill diameter for buried via	250	NA	200	NA
G	Minimum Line width on Layer 1	75	+/-0.6	50	+/- 0.3
H	Minimum Line width on Layer 2	75	+/- 0.6	50	+/- 0.3
I	Laser drilled Microvia diameter from layer 1 to 2	125 to 150	NA	125 to 150	NA
J	Aspect ratio	0.3 to 0.4: 1	NA	0.5 to 0.6:1	NA

TD Microvia Technology

Laser Drilled Microvias

Layer 1 to 2 & Layer 1 to 3

Aspect Ratio: 0.3 to 0.6:1



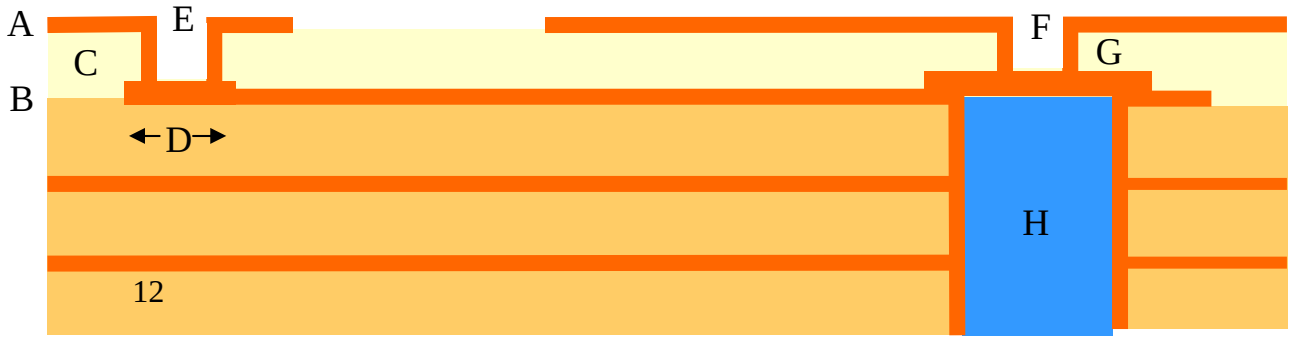
#	Description	Standard Microvia		Advanced Microvia	
		µm	+/-	µm	+/-
A	Minimum Layer 1 copper thickness	52	+- 20%	45	10%
B	Minimum Layer 2 copper thickness	40	+- 20%	40	10%
C	Minimum Layer 3 copper thickness	40	+- 20%	40	10%
D	Layer 1-2 dielectric thickness	25 to 50	+- 10%	25 to 75	10%
E	Layer 2-3 dielectric thickness	25 to 50	+- 10%	25 to 75	10%
F	Minimum Layer 2 pad for Layer 1 to 2 Microvia	300	NA	300	NA
G	Minimum Layer 1 pad for Layer 1 to 2 Microvia	250	NA	250	NA
H	Minimum Layer 3 pad for Layer 1 to 3 Microvia	400	NA	450	NA
I	Minimum Layer 2 pad for Layer 1 to 3 Microvia	350	NA	400	NA
J	Minimum Layer 1 pad for Layer 1 to 3 Microvia	300	NA	350	NA
K	Minimum drill diameter for buried via	300	NA	250	NA
L	Minimum Line Width/Space on Layers 1, 2, & 3	75	+/- 20%	50	+/- 10%

Laser Drilled Microvia from layer 1 to 2 = 150 µm diameter From 1 to 3 = 200 – 250 µm diameter

TD Microvia Technology

Laser Drilled Microvias

Layer 1 to 2 & Stacked Vias



#	Description	Standard Microvia		Advanced Microvia	
		µm	+/-	µm	+/-
A	Minimum Layer 1 copper thickness	52	20%	45	10%
B	Minimum Layer 2 copper thickness	40	20%	40	10%
C	Layer 1 – 2 dielectric thickness	25 to 50	10%	25 to 75	10%
D	Minimum Layer 2 pad for Layer 1 to 2 Microvia	300	NA	300	NA
E	Minimum Layer 1 pad for Layer 1 to 2 Microvia	250	NA	250	NA
F	Minimum Layer 1 pad for Stacked Microvia	NA	NA	250	NA
G	Minimum Layer 2 pad for Stacked Microvia	NA	NA	250	NA
H	Minimum drill diameter for buried via	300	NA	250	NA
I	Minimum Pad diameter for buried via			500	NA
J	Laser drilled Microvia diameter from layer 1 to 2	125 or 150	NA	125	NA
K	Aspect ratio	0.3 to 0.4: 1	NA	0.5 to 0.6:1	NA

Laser Drilling Technology

Combination ND:YAG CO_2
Forms holes by removing copper with the ND:YAG laser and the dielectric and re-enforcing material with the CO_2 laser (Approximately 3,500 to 13,000 holes per minute dependant on material and hole size)

$C0_2$ (Infrared)
Capable of drilling most re-enforcing materials and laminate resin systems. Not effective for drilling copper (copper is reflective in the infrared spectrum and must be window etched) Forms holes by pulsing a larger high energy beam (Approximately 17,000 holes per minute)

ND:YAG (Ultra-Violet)
Capable of drilling copper, all re-enforcing materials and all laminate resin systems. 25 to 50 micron beam forms holes by spiraling of trepaning the beam (Approximately 600 to 1,400 holes per minute dependant on material and hole size)

Limitations of Conventional Microvia Structures

- Dielectric thickness limited by plating aspect ratio with typical dielectric thickness ranging from 50 to 75 mm
- Thin dielectric layers often result in impedance issues due to reduced line with and tolerance
- Microvia in pad is considered a risk for potential solder voiding and increases as the solder volume is decreased with smaller pitch BGA’s
- Connections to deeper than one layer require “stair-Case” geometries presentation design challenge and potential copper voiding in planes
- Conventional microvia structures can not be vertically stacked

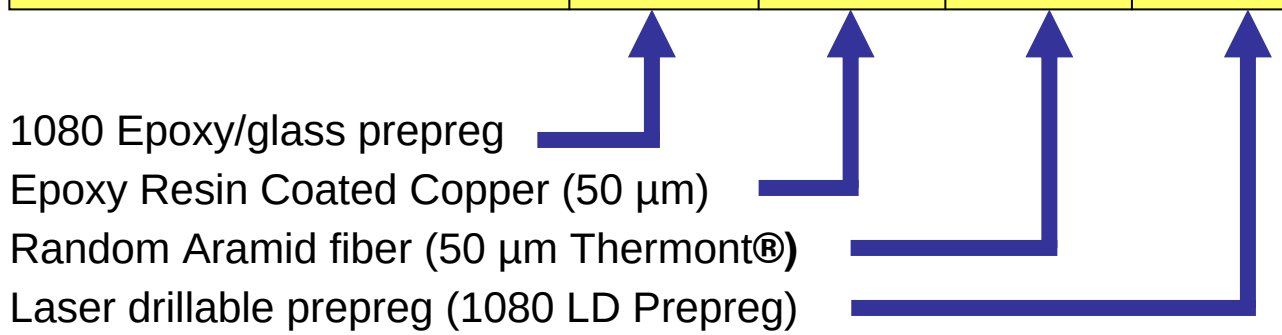
Laser Drilling Technology

Factors Impacting Laser Drilling Time & Cost

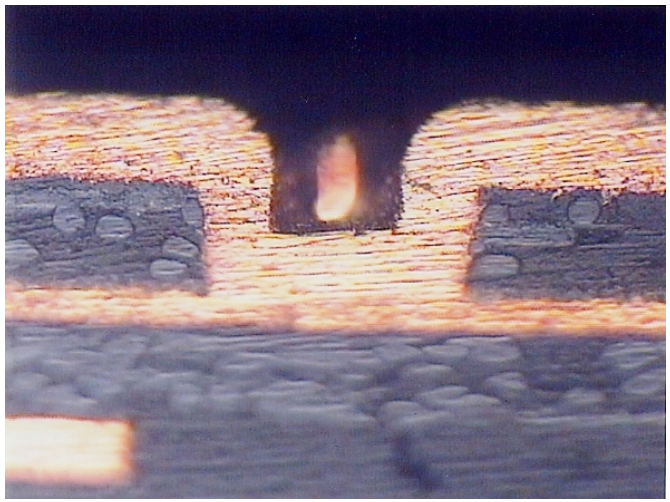
- Copper foil thickness
- Dielectric thickness
- Hole diameter
- Dielectric composition
  - Non-reinforced resin (RCC)
  - Non-woven reinforcement (Thermont ®)
  - Woven (106 , 1080 glass)
- System Optimization = increases velocity and power

Typical ND:YAG Laser Drilling Speeds

Cu Thick.	Via Dia.	Drilling Speed Holes/sec.			
9 µm	100 µm	76	97	94	57
9 µm	150 µm	47	54	53	38
9 µm	200 µm	30	32	30	28



Tech Driven Microvia Technology



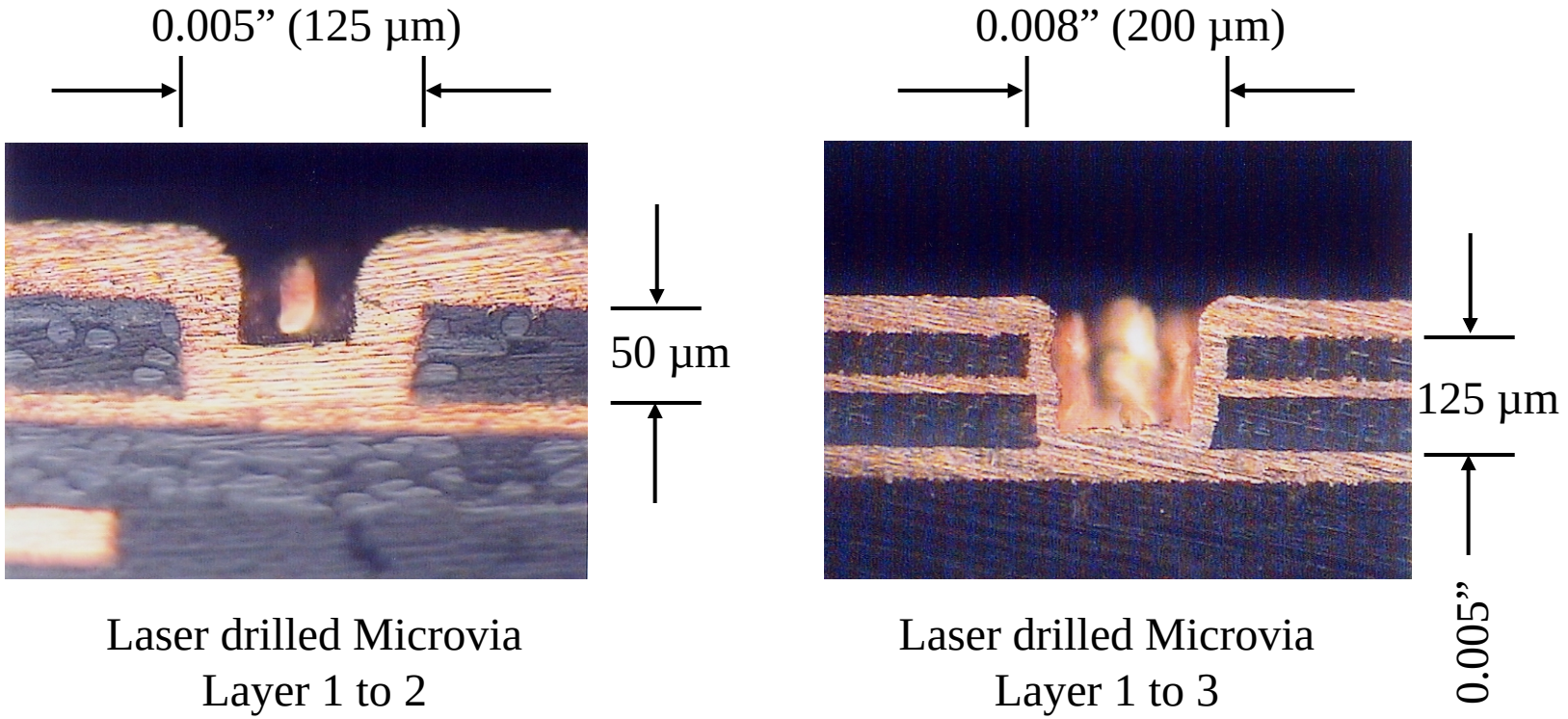
Laser Drilled Micro-via (ESI Equipment)

Characteristics

- Laser drilling can be performed in any laminate.
- Typical thickness requested is .002 in and may be drilled to multiple layers
- Picture indicates UV Laser drilling through surface copper and .002 laminate.

Microvia Technology

Traditional laser drilled Microvia geometry



Laser drilled Microvia
Layer 1 to 2

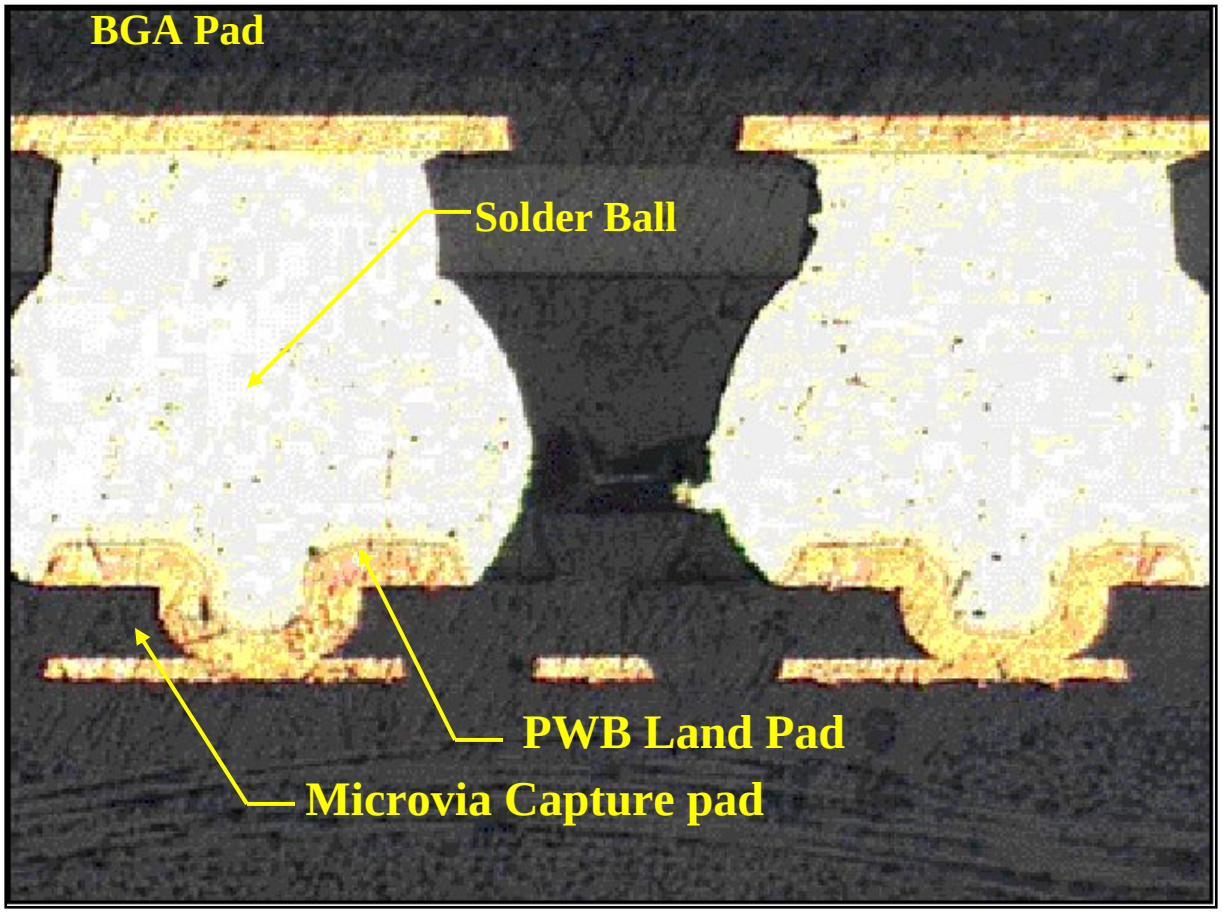
Laser drilled Microvia
Layer 1 to 3

Note: Typical aspect ratio on laser drilled holes is 0.5:1 to 0.8:1 max

Microvia Technology

Via-in-Pad

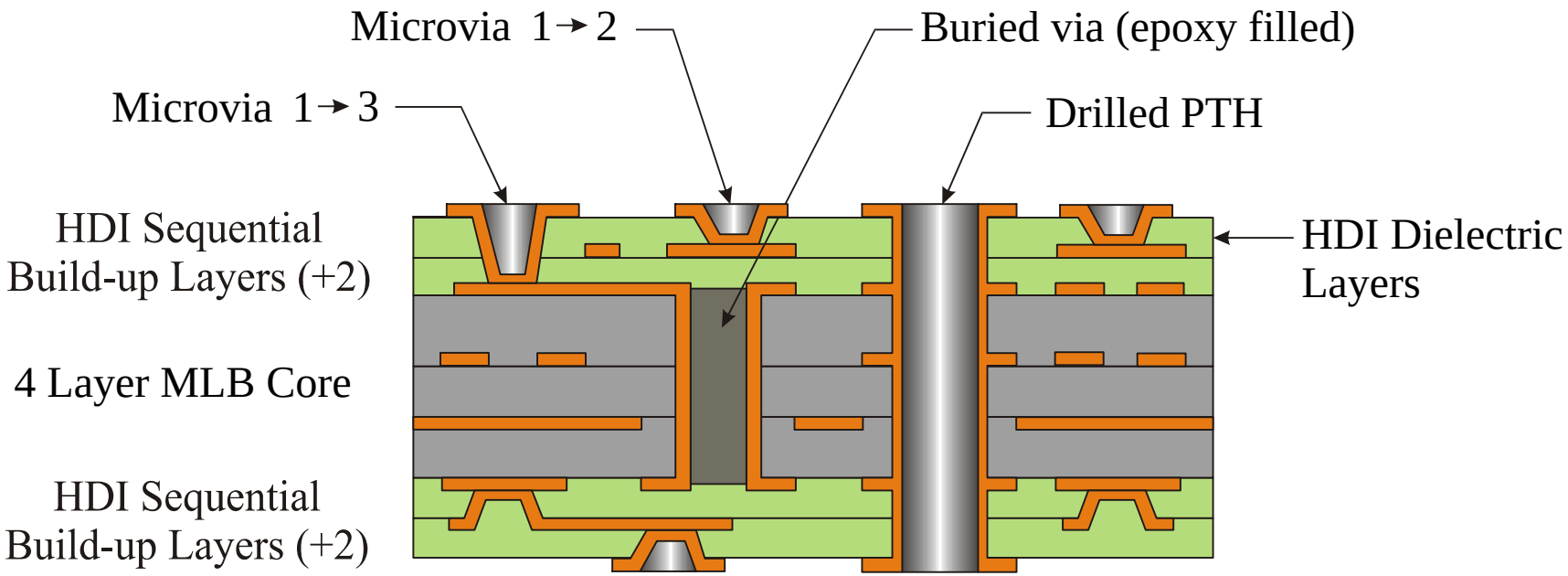
Ideal Solder Joint



Chip Scale BGA Package with Microvia in Pad

Microvia Technology

Traditional Laser Drilled hole Geometry



2+4+2 HDI Substrate

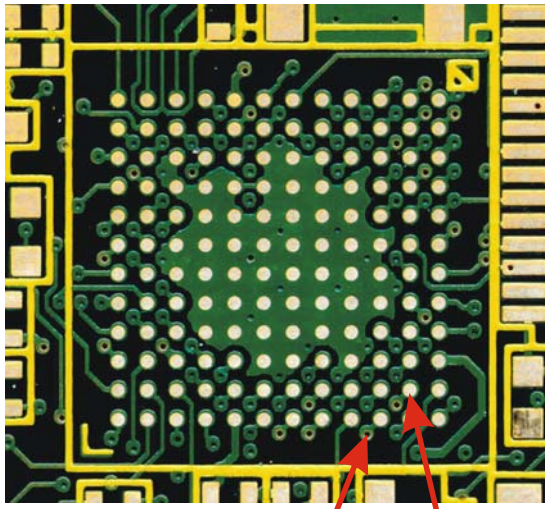
- Aspect ratio on Microvia's approximately 0.5:1max.
- Microvia 1→3 require larger hole diameter

Microvia Technology

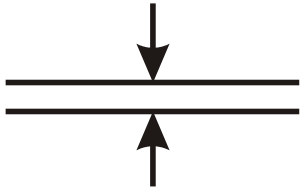
Conventional MLB vs HDI

0.8 mm μBGA

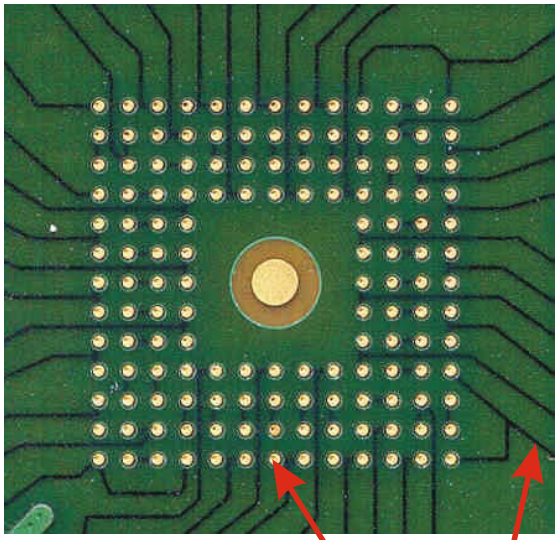
Conventional MLB Substrate



0.8 mm



HDI Substrate



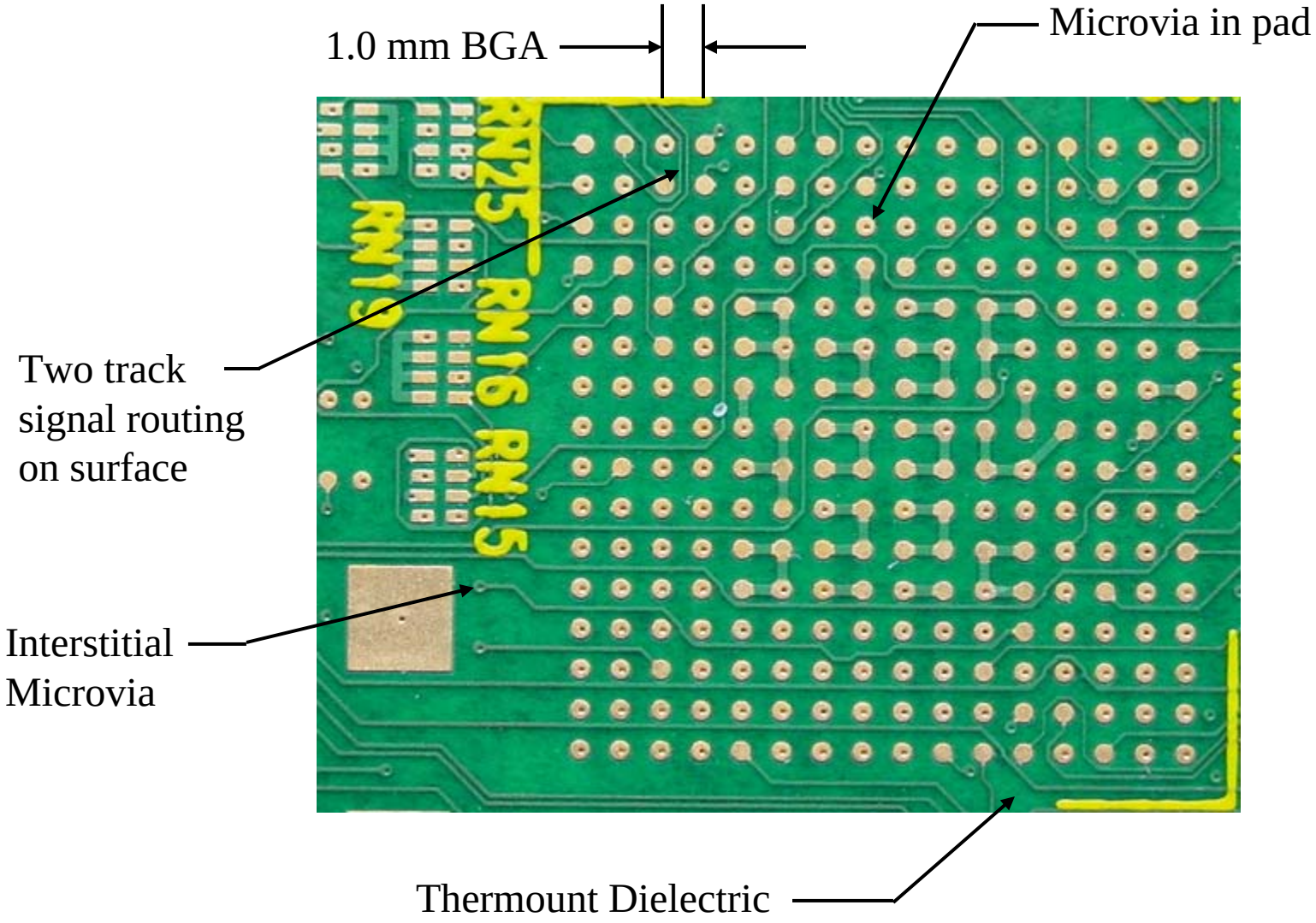
Mechanical drilled via's offset from attachment pad

Solder mask defined pad

Laser drilled via in pad (Solder mask defined attachment pad layer # 1)

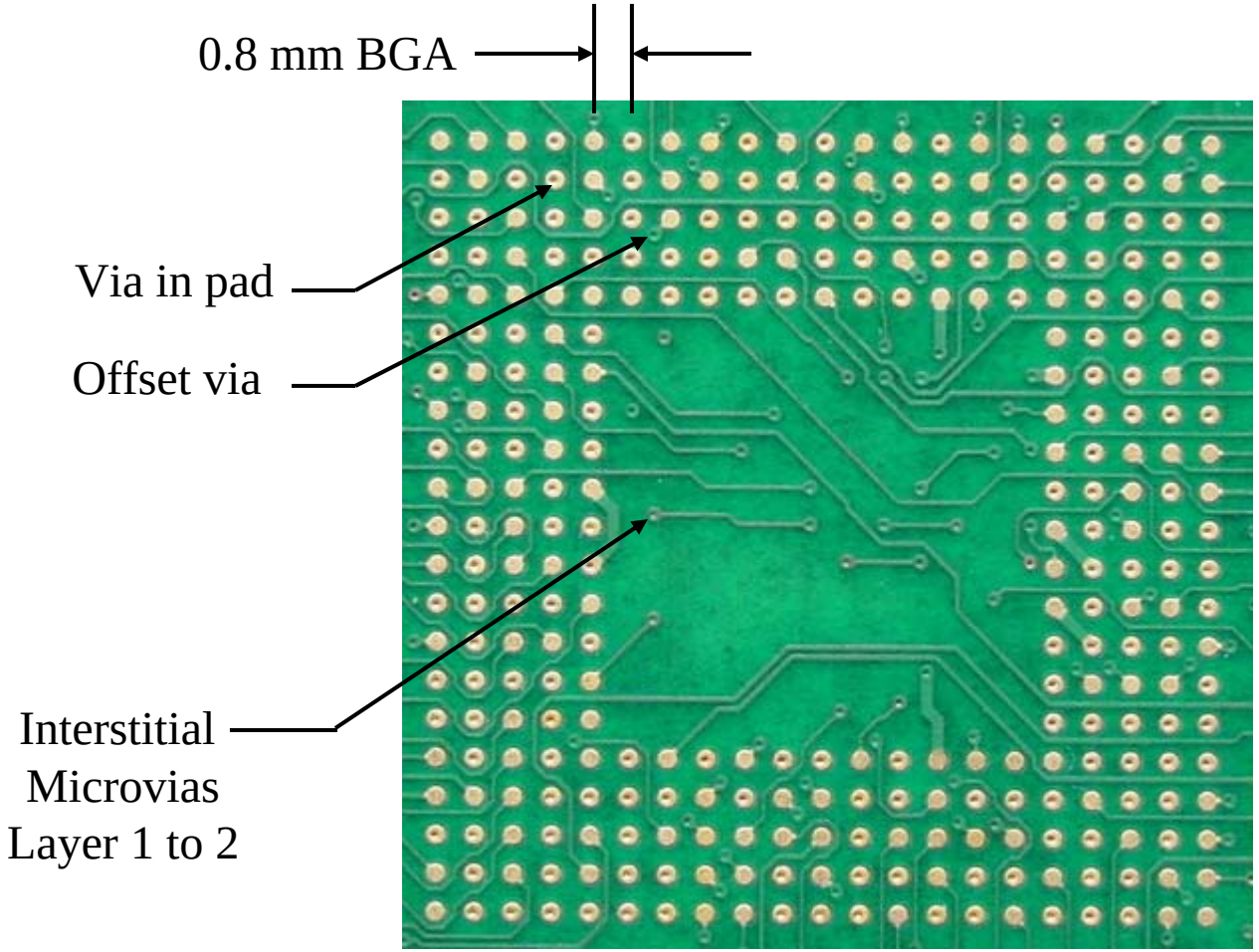
Signal routing on layer # 2

Microvia Technology



Microvia Technology

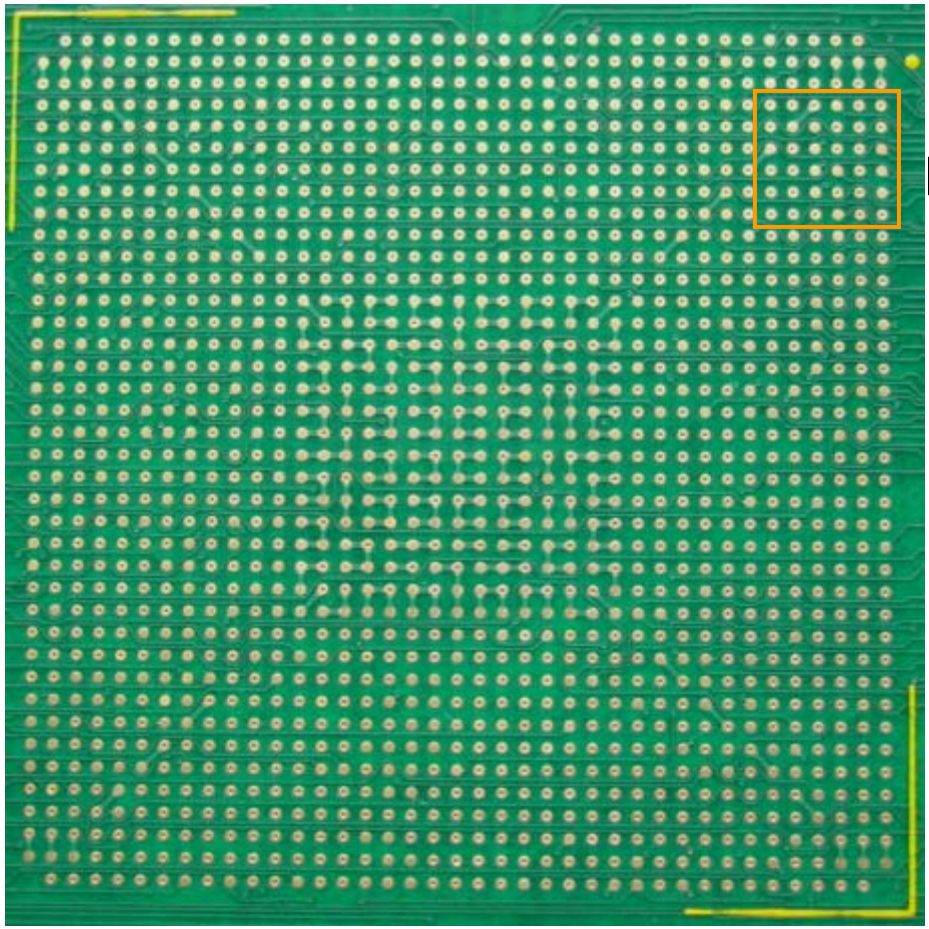
Microvia Technology - Via-in-Pad

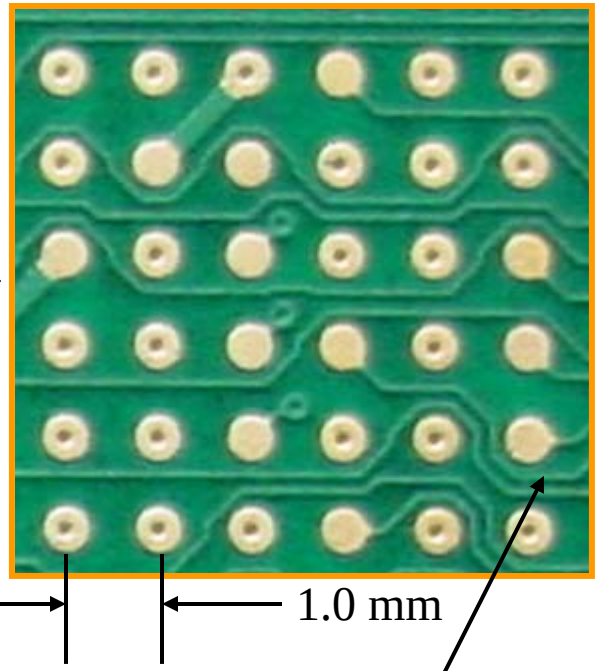


Microvia Technology

Microvia Technology - Via-in-Pad

39 x 39 1.0 mm BGA

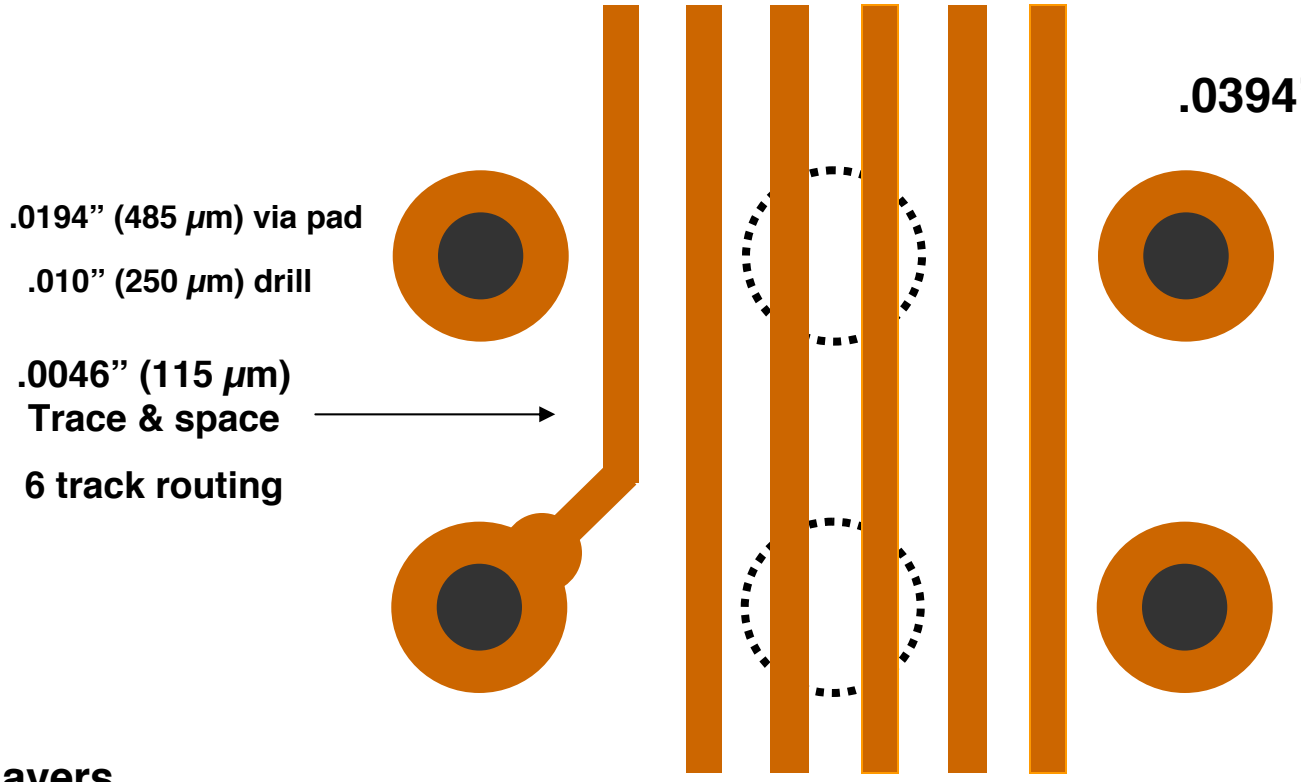




Microvia Technology

Hybrid Approach

1 mm BGA



Internal Layers

Thickness of .093” (2.362 mm) - .100” (2.54 mm)

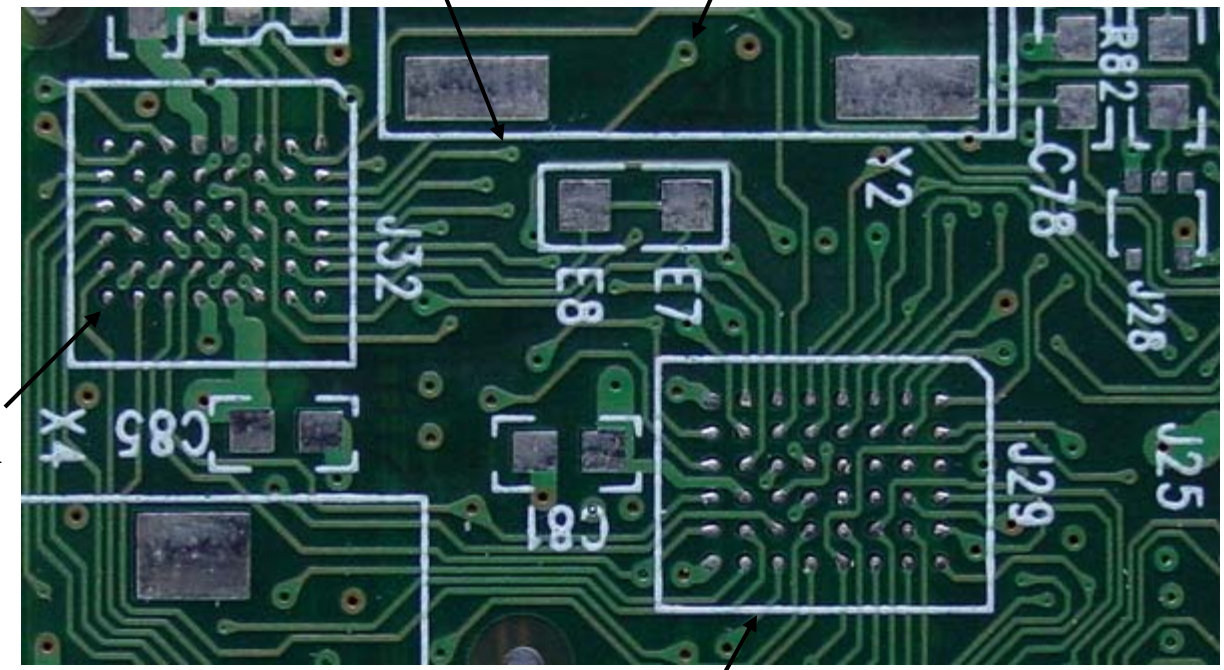
Aspect Ratio 10:1

Microvia Technology

Microvia Technology - Via-in-Pad

Laser drilled via's

Mechanically drilled via

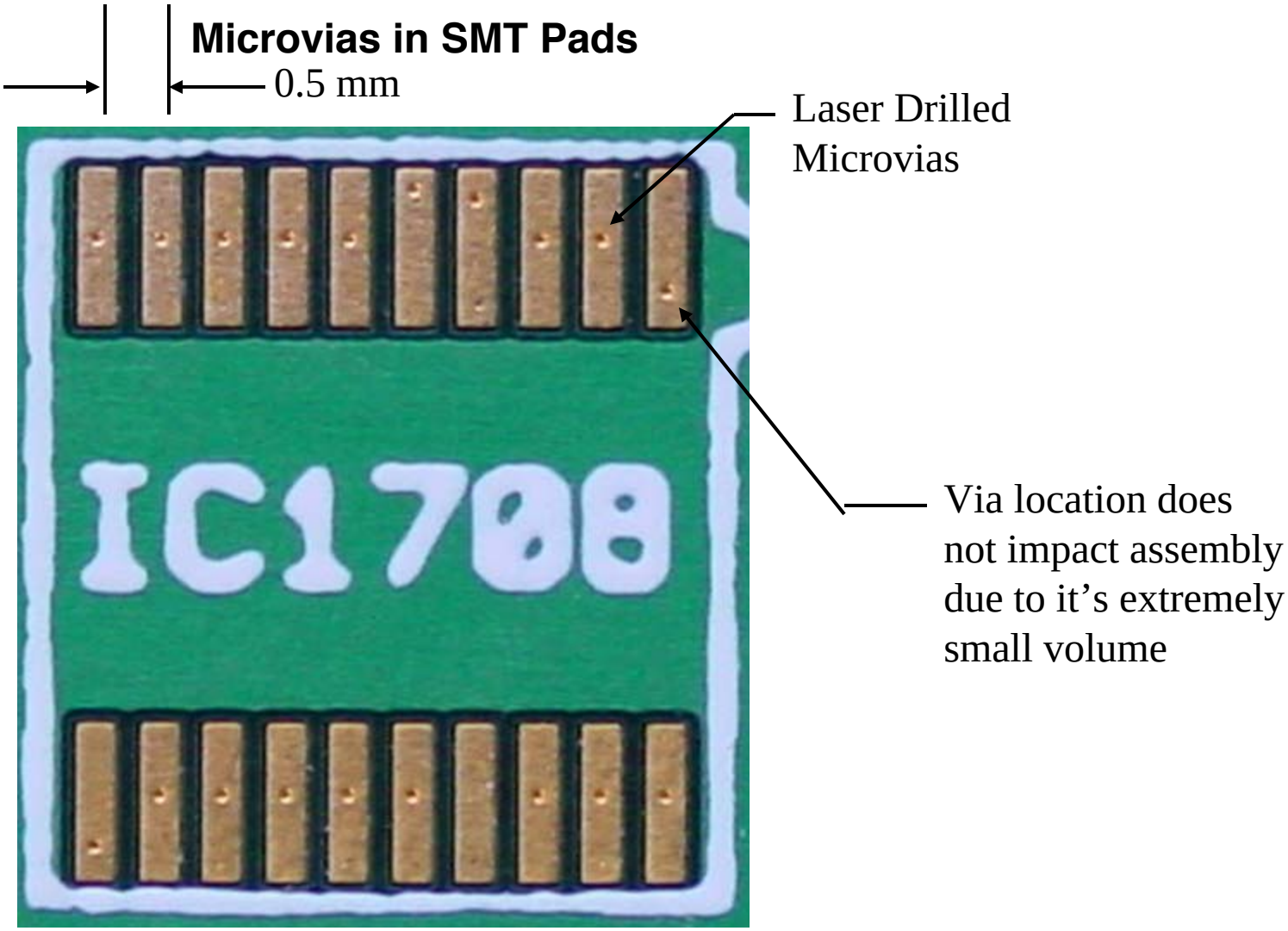


0.8 mm BGA

0.8 mm BGA

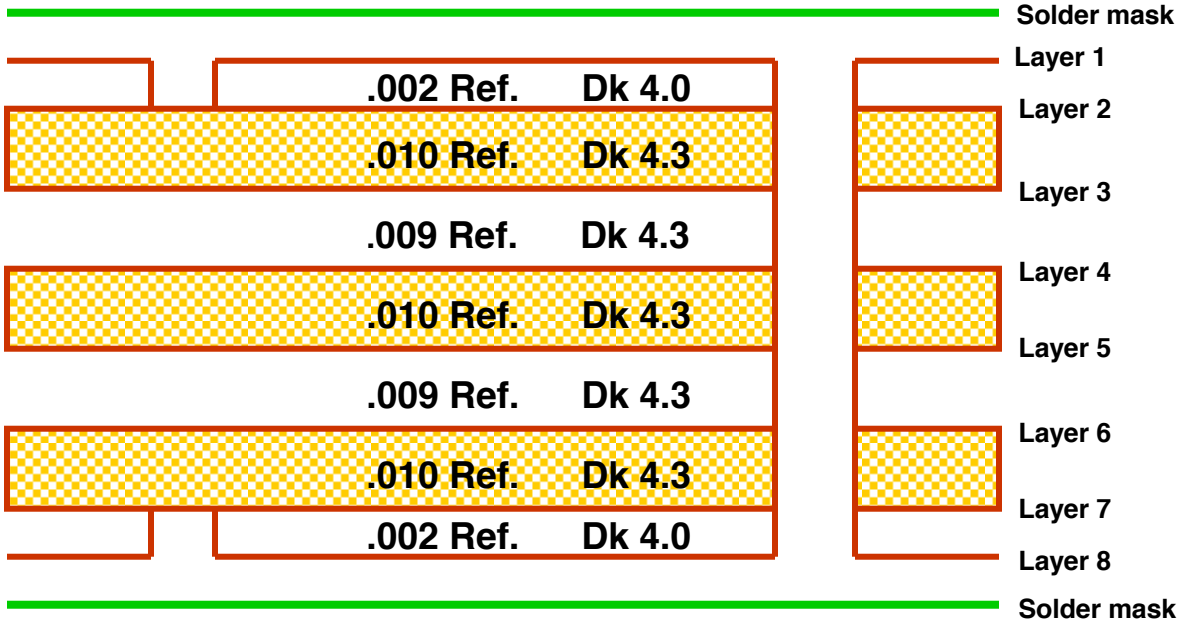
Tin/Lead Surface Finish

Microvia Technology



Microvia Technology

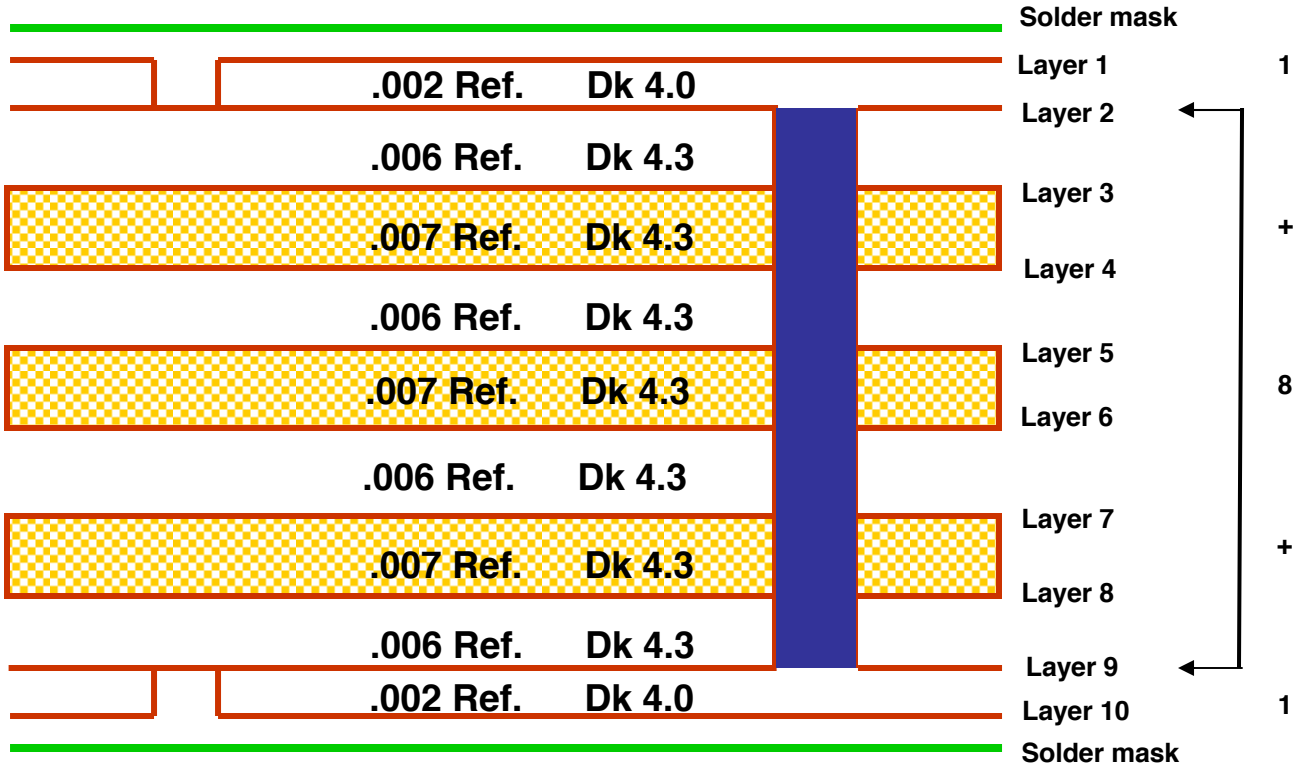
1 + 6 + 1
Single Lamination Construction



Nominal Lam Tolerance = .058 +/- .004
Finish Thickness = .062 +/- .006

Microvia Technology

1 + 8 + 1
Buried Via Construction
2 Lamination Cycles

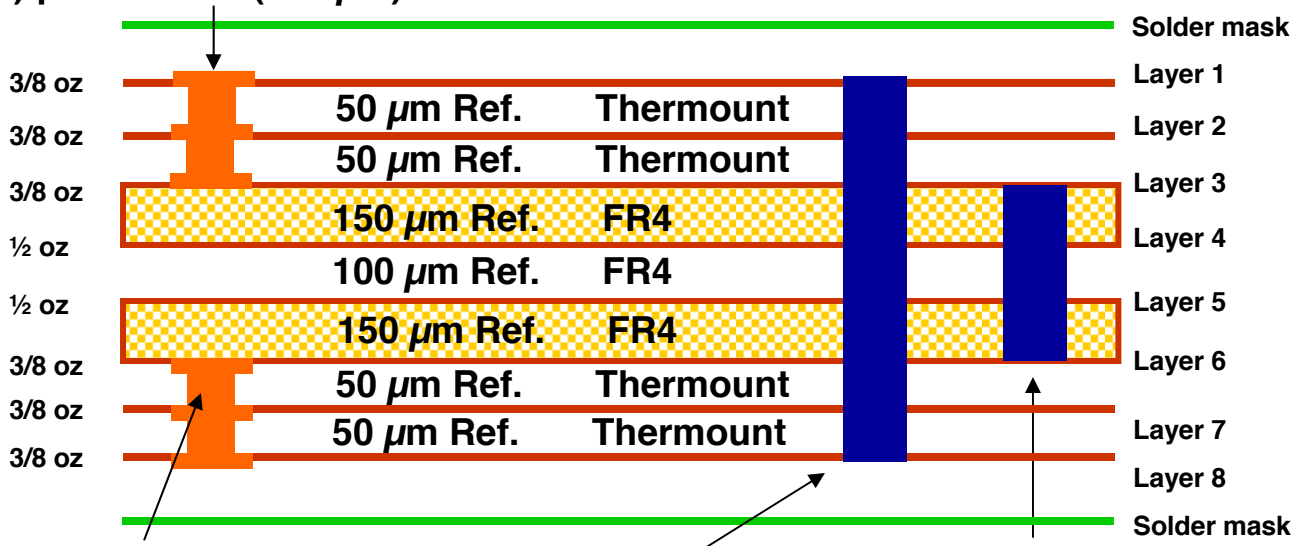


Nominal Lam Tolerance = .058 +/- .004
Finish Thickness = .062 +/- .006

Microvia Technology

2 + 4 + 2
Three Lamination Construction

Layer 1 - 2 & 8-7 = Stacked MicroVias
L1 .010” (250 µm) pad & .005” (125 µm) laser drill



Layer 2 – 3 & 6 - 7 = Microvias
.010” (250 µm) pad & .005” (125 µm) laser drill

Layer 3 - 6 = Buried Vias
.018” (450 µm) pad & .008” (200 µm) drill

Finish Thickness = .038” +/- .004”
Material = High Temp FR4

Layer 1 - 8 = Through-hole
.020” (500 µm) pad & .010” (250 µm) drill

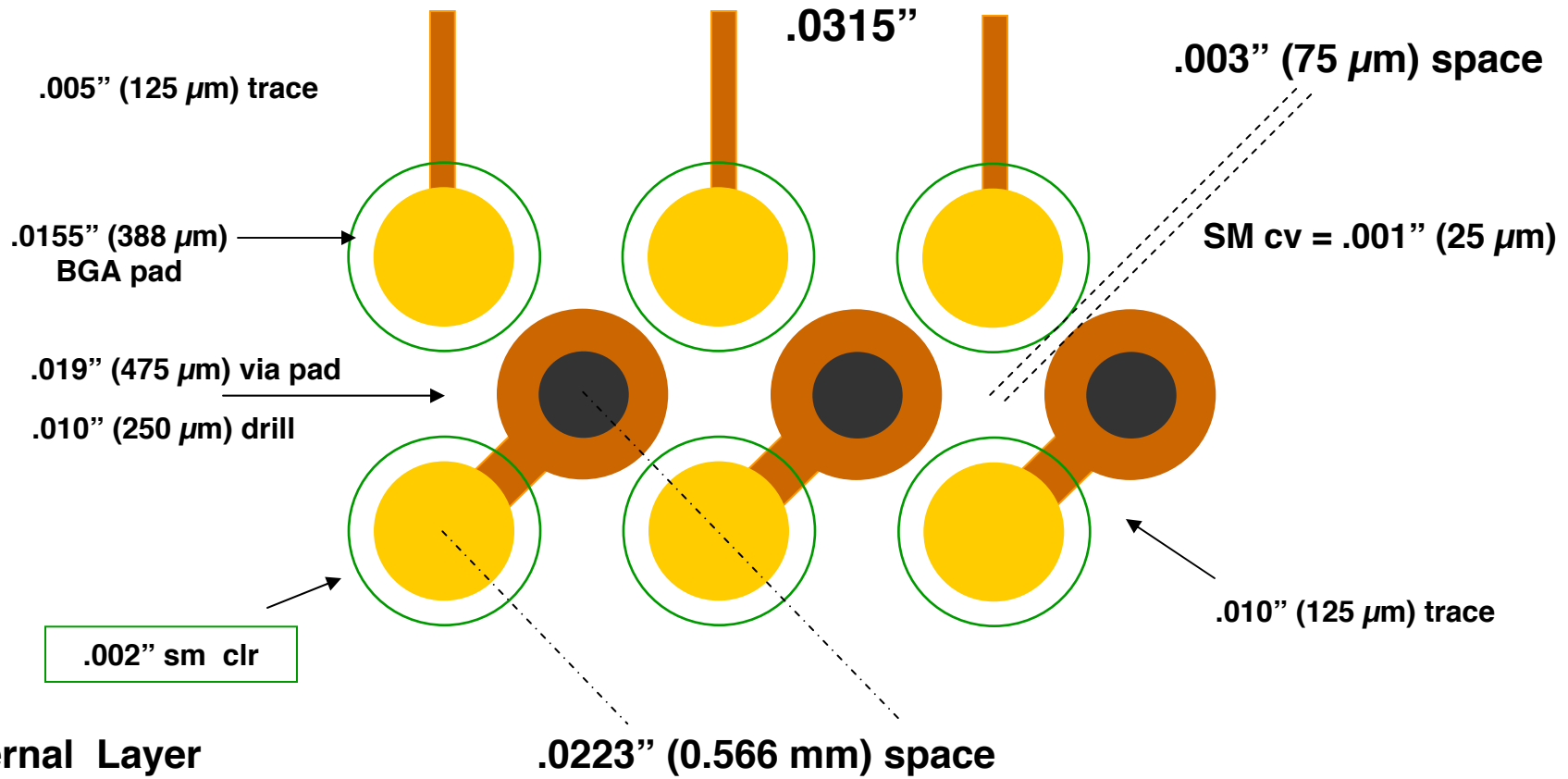
Microvia Technology

0.8 mm BGA

Design Guidelines

TD Technology

0.8 mm BGA



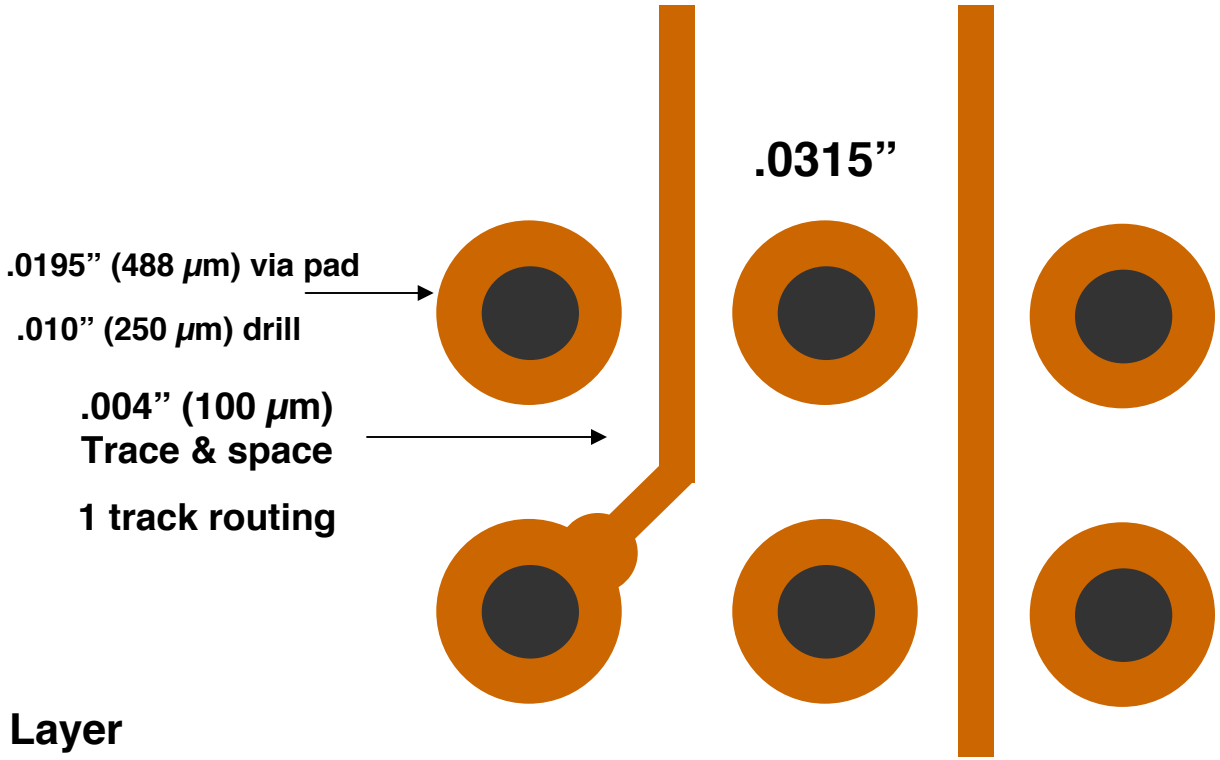
Thickness of .093” (2.362 mm) - .100” (2.54 mm)

Aspect Ratio 10:1

TD Technology

0.8 mm BGA

IPC 6011/6012 Class 2



Internal Layer

Thickness of .093” (2.362 mm) - .100” (2.54 mm)

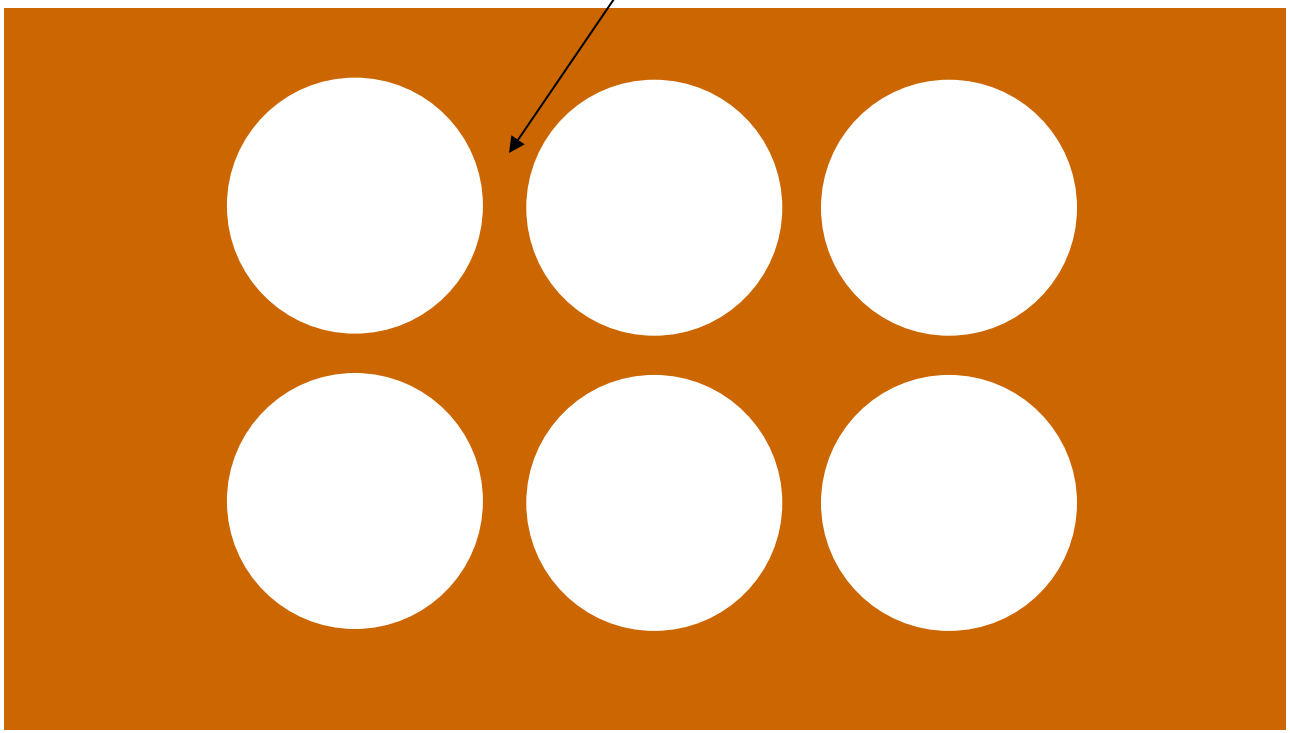
Aspect Ratio 10:1

TD Technology

0.8 mm BGA

IPC 6011/6012 Class 2
.028” (0.711 mm) clearance

.0035” (88 μm) copper



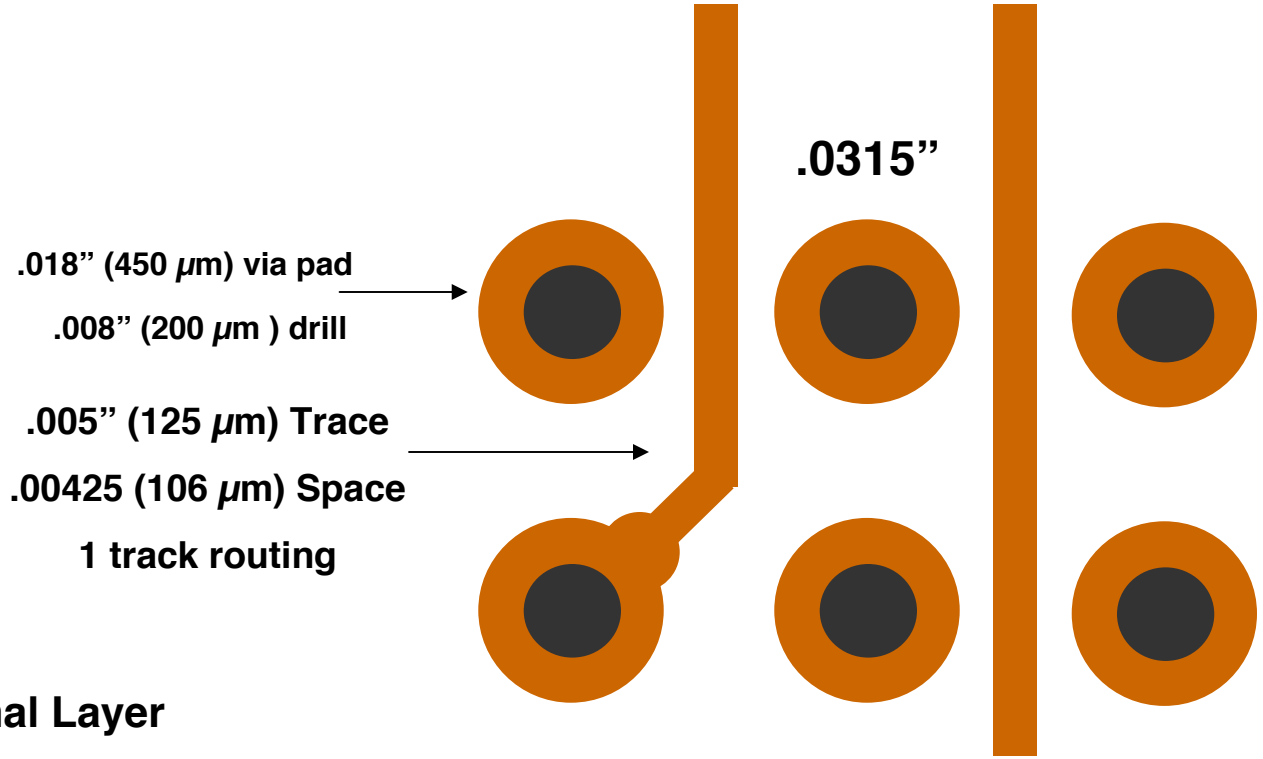
Thickness of .093” (2.362 mm) - .100” (2.54 mm)

Aspect Ratio 10:1

TD Technology

0.8 mm BGA

IPC 6011/6012 Class 2



Internal Layer

Thickness of .028” (0.711 mm) - .062” (1.575 mm)

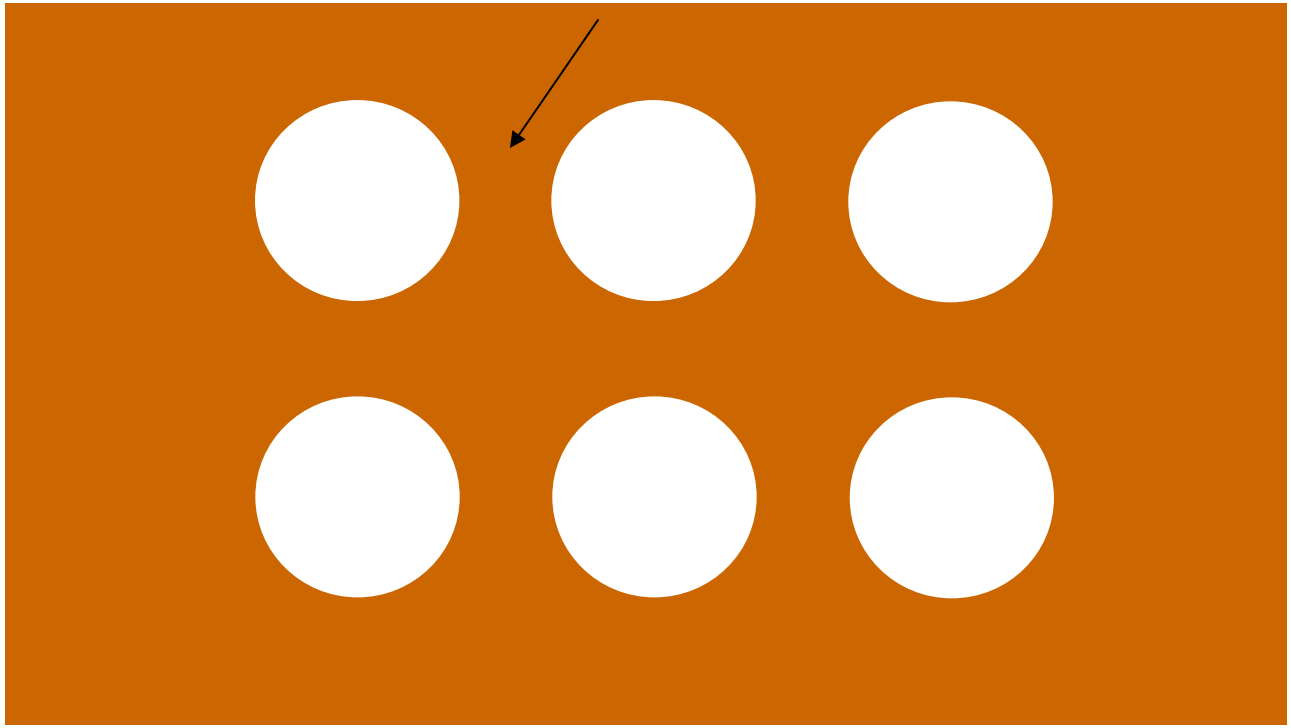
Aspect Ratio 10:1

TD Technology

0.8 mm BGA

IPC 6011/6012 Class 2
.026” (0.660 mm) clearance

.0055” (138 *µ*m) copper



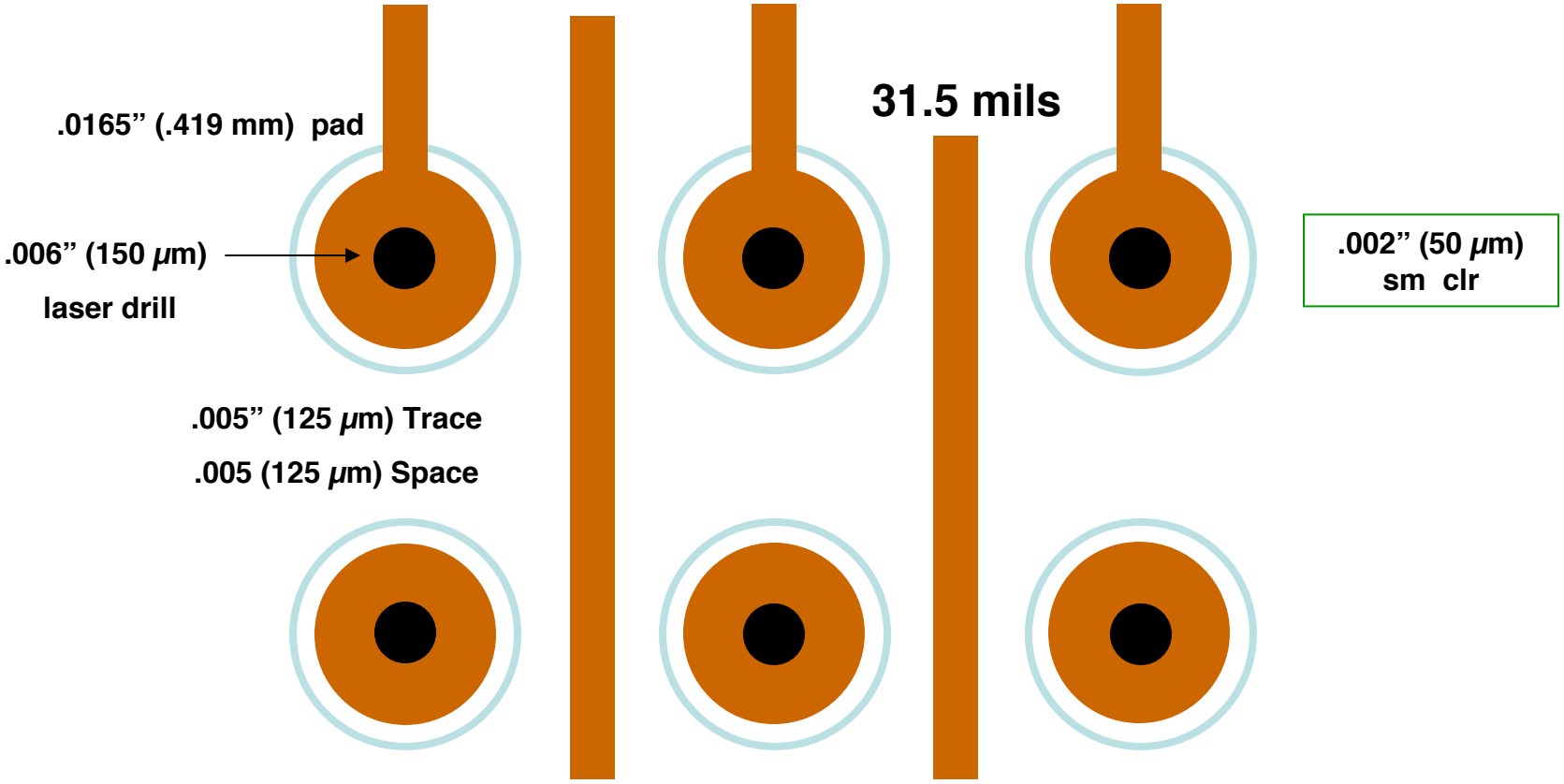
Thickness of .028” (0.711 mm) - .062” (1.575 mm)

Aspect Ratio 7.75:1

Microvia Technology

0.8 mm BGA – Microvia Via-in-Pad

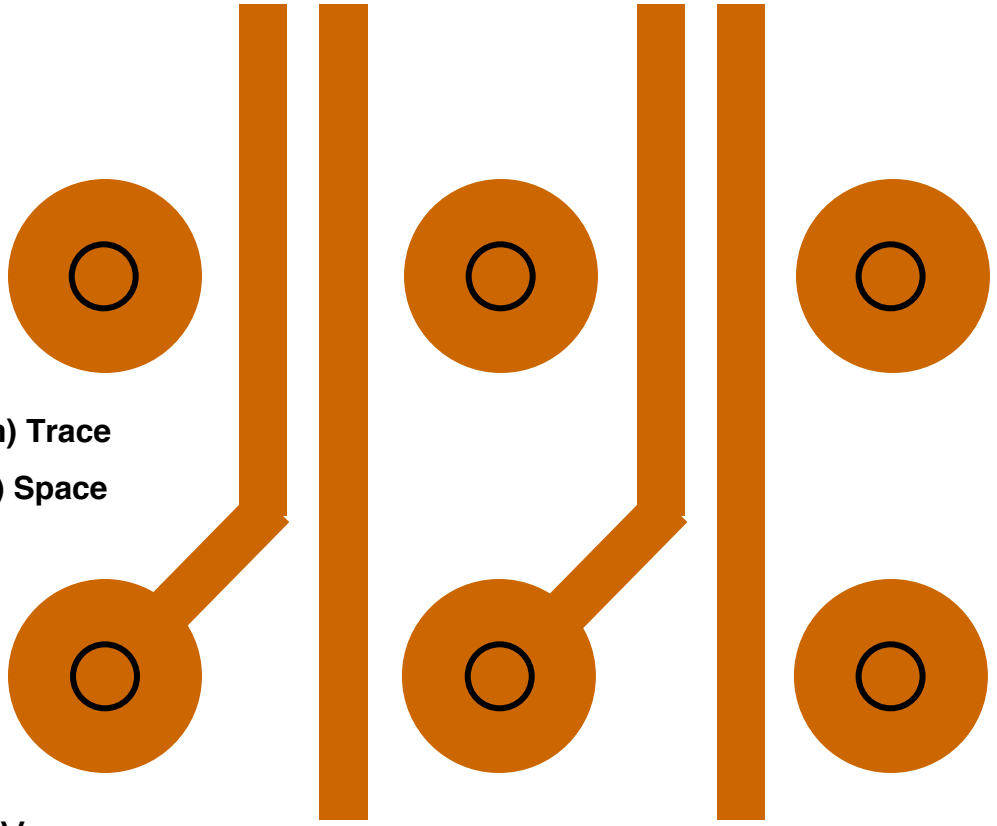
Layer 1



Microvia Via-in-Pad Technology = Eliminates through vias

Microvia Technology

0.8 mm BGA



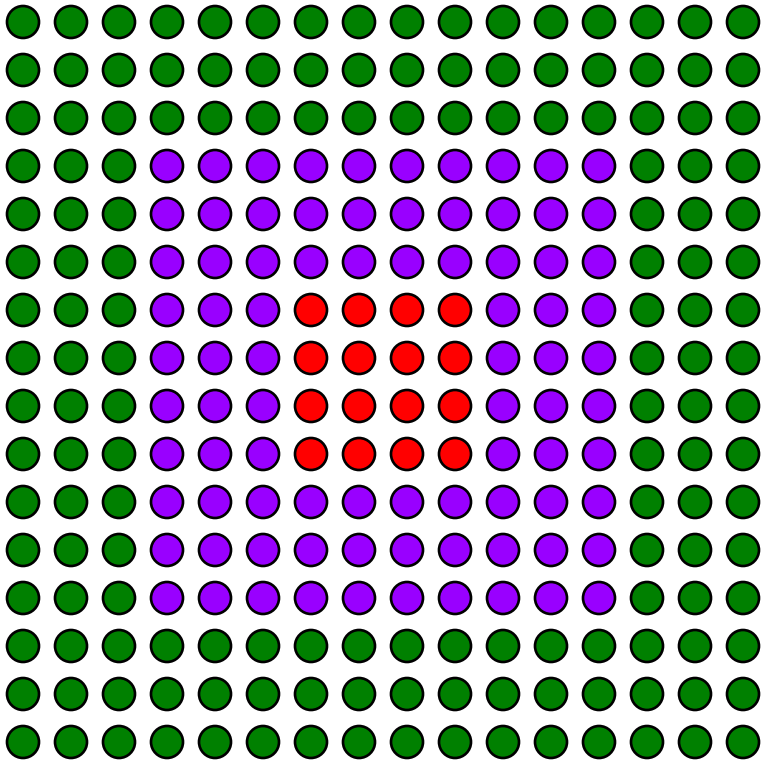
Microvia Technology

0.8 mm BGA Design

No clearance required

Microvia Technology

0.8 mm BGA 256 I/O Full Array

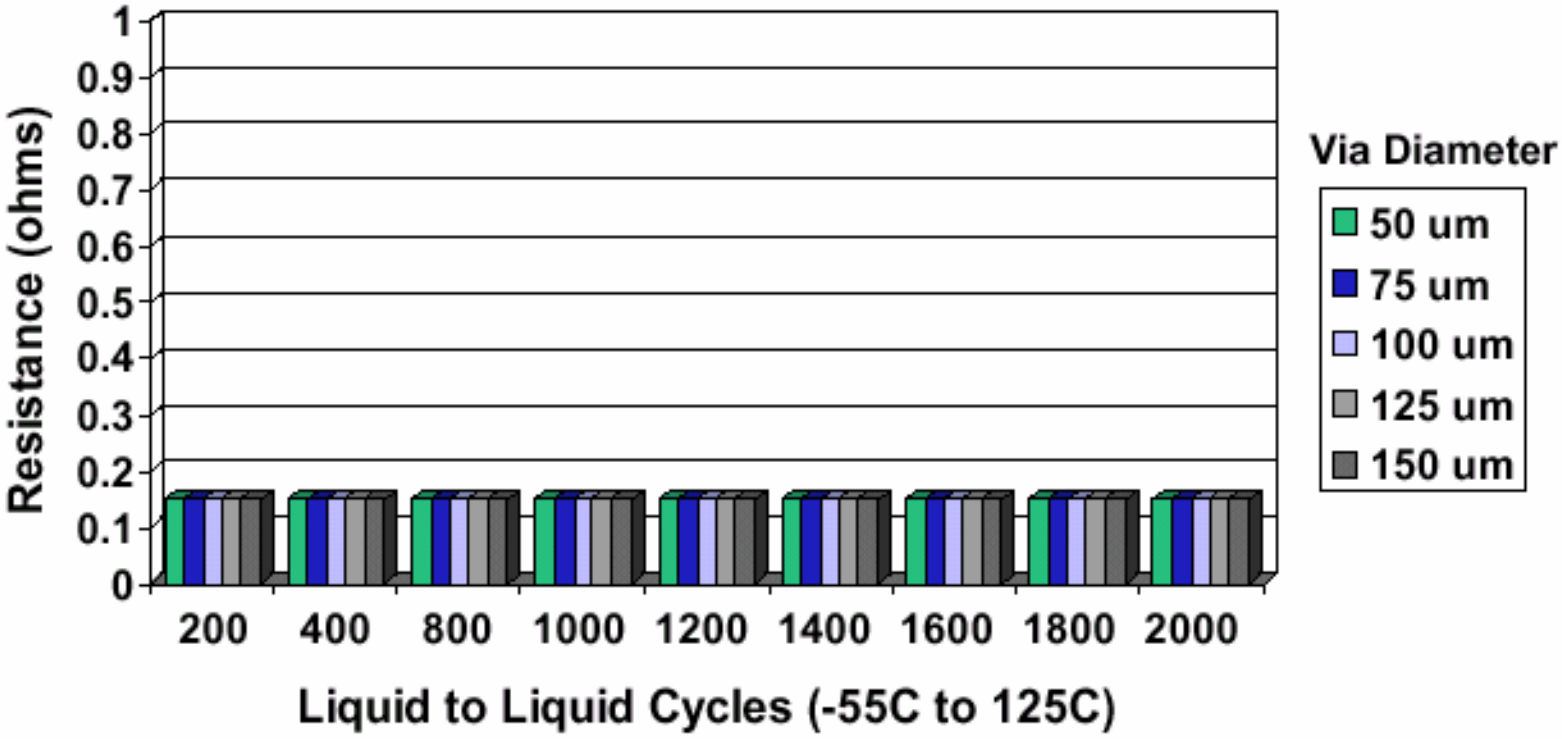


Layer 1 Layer 2 Layer 3

Option = 2 layers with 3/3 & .010 pad = 3 track

Microvia Technology

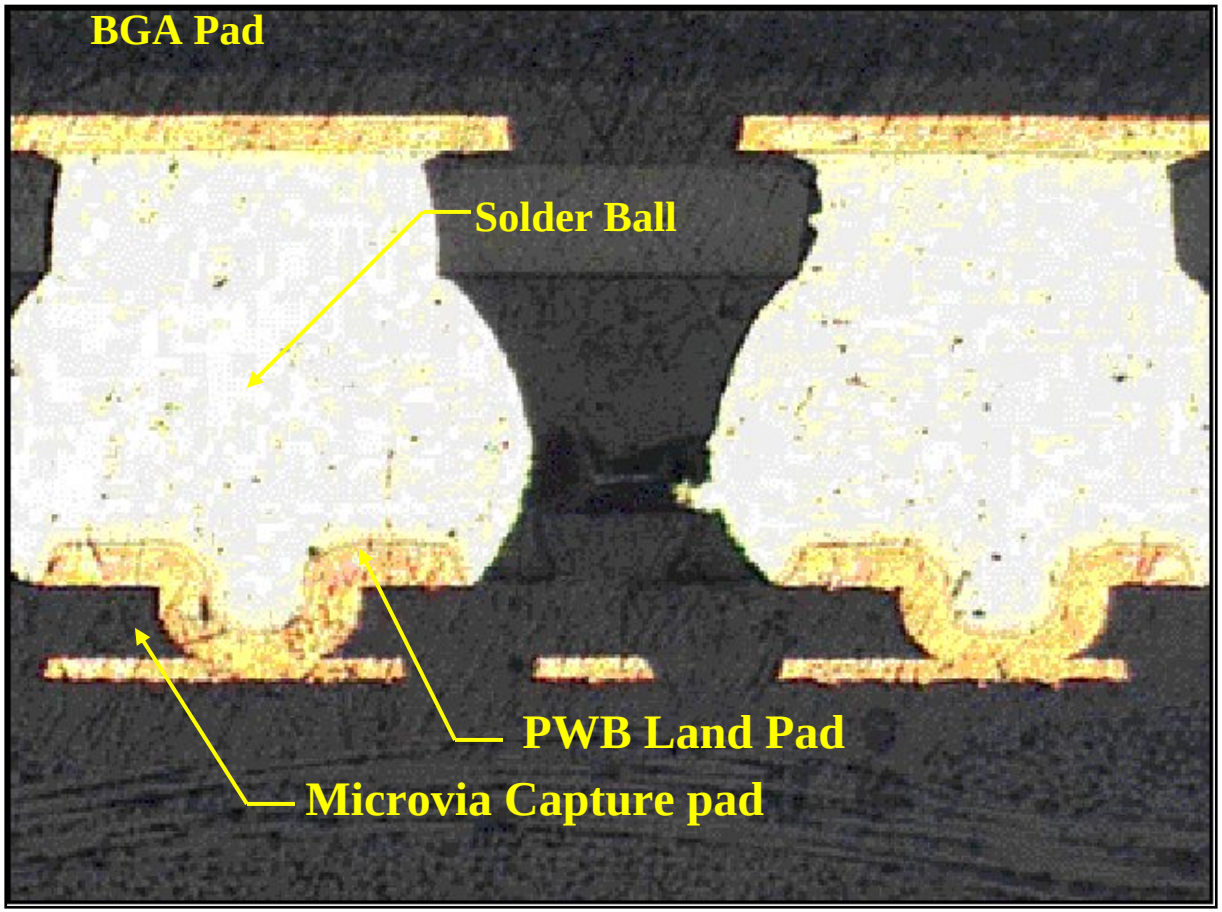
Reliability Data



Microvia Technology

Via-in-Pad

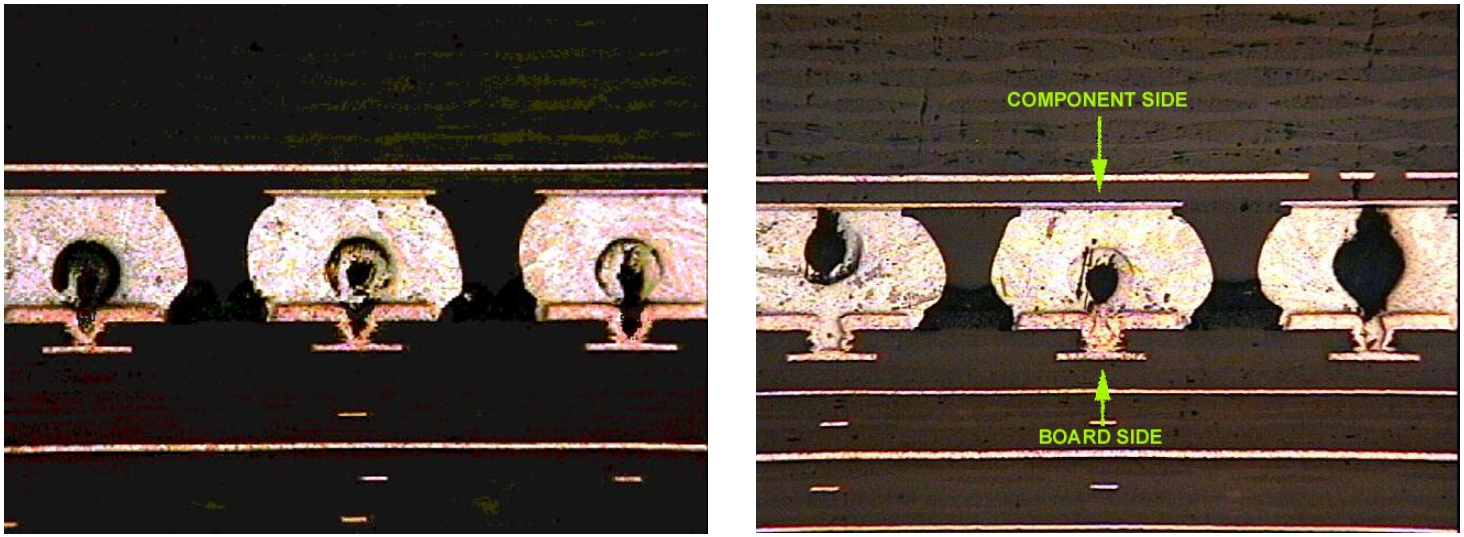
Ideal Solder Joint



Chip Scale BGA Package with Microvia in Pad

Microvia Technology

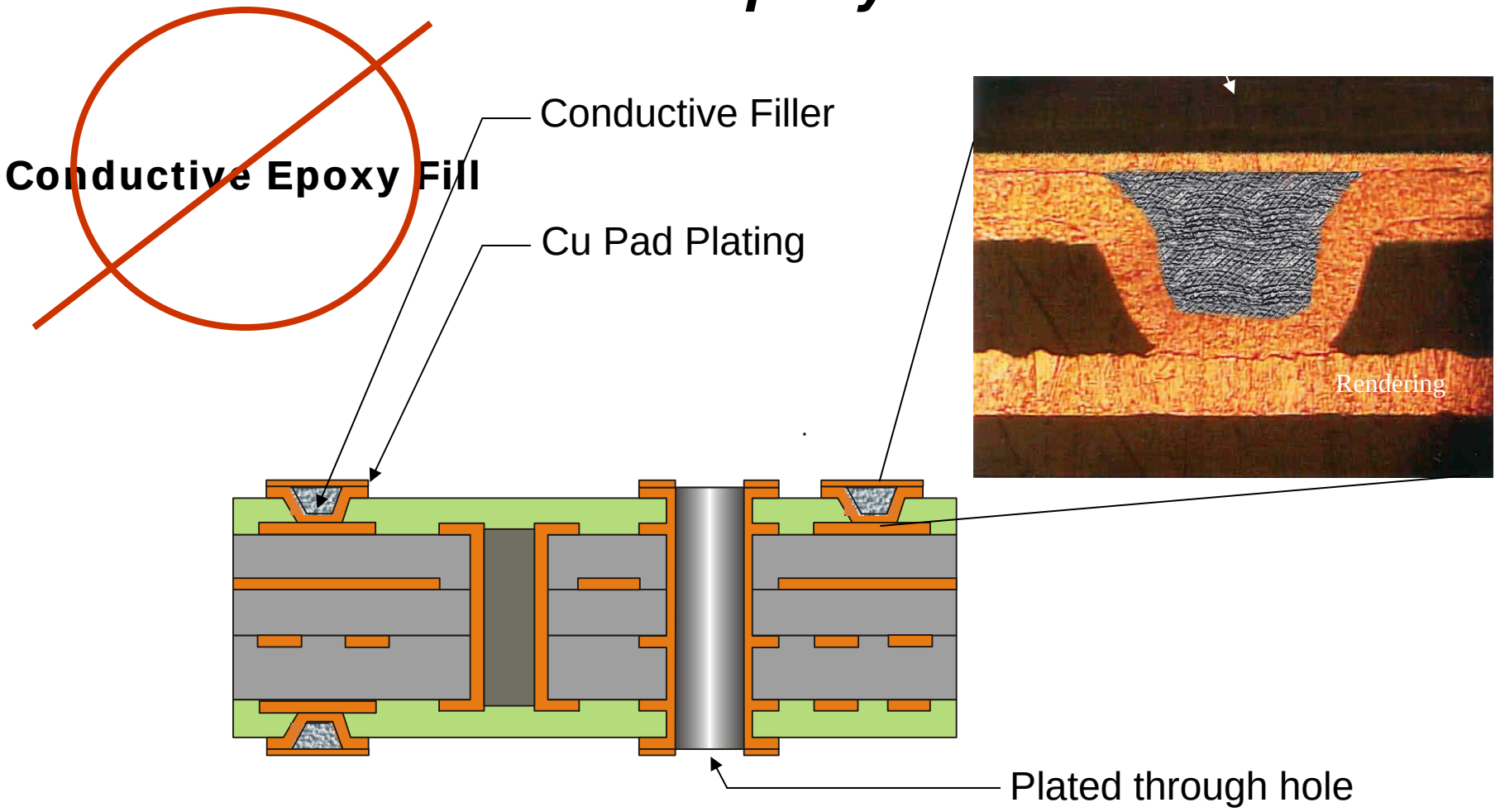
Unacceptable Via-in-Pad Solder Joints



Microvias with <u>solder voids</u> after assembly

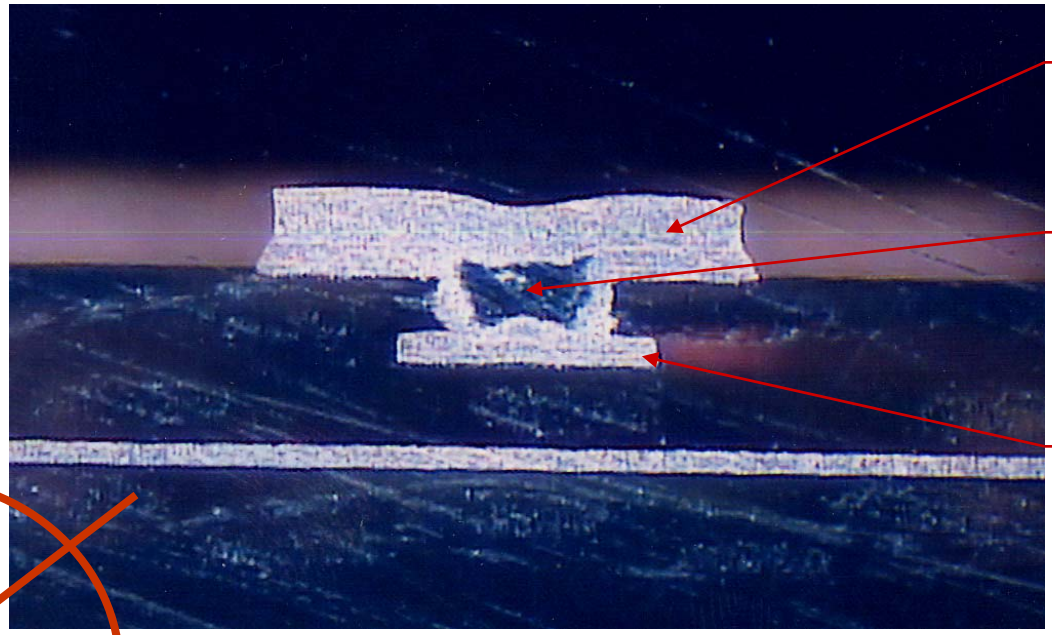
Microvia Technology

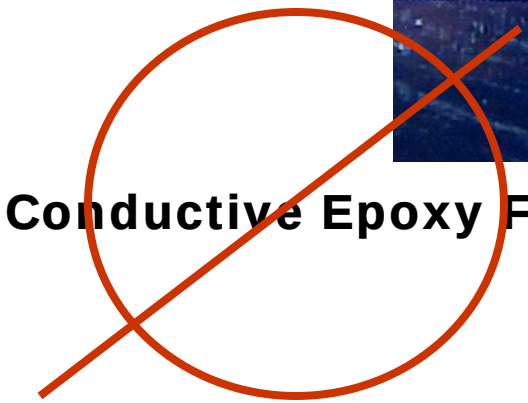
Conductive Epoxy Fill & Plate



Microvia Technology

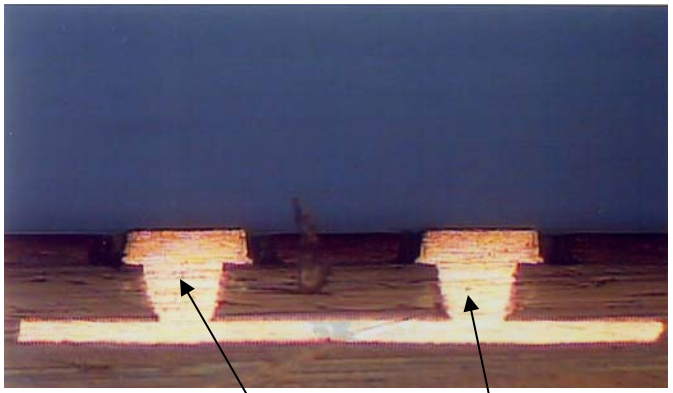
Conductive Epoxy Fill & Plate



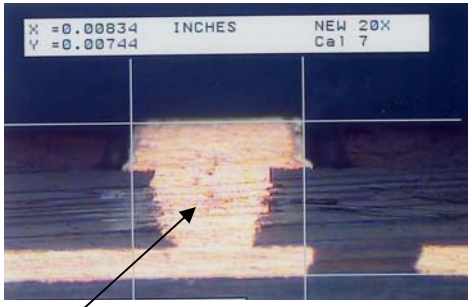


Stacked MicroVia (SMV™)

Single MicroVias



Maintain Planar Surface



.005” (125 μm) laser drilled & solid copper plate

.010” (250 μm) pad diameter

Stacked MicroVia (SMV™)

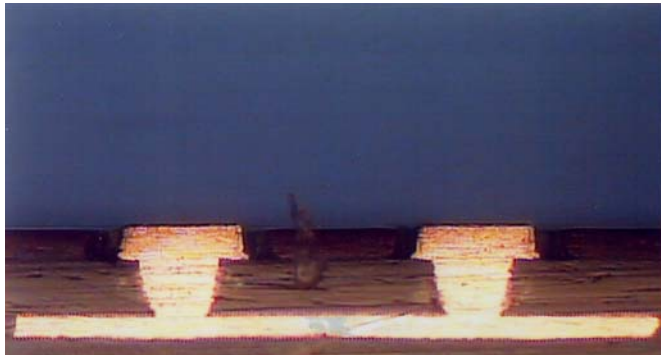
SMV™ Technology Provides Solutions for Next Generation Products

TD Technology
Stacked MicroVia (SMV™)

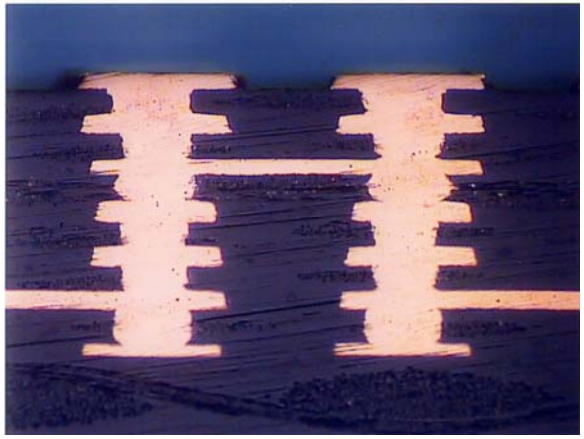
Definition:

.004” (100 μm) laser drilled MicroVia

(solid copper plate)



Single MicroVia



Stacked MicroVias

TD Technology
Stacked MicroVia (SMV™)

Design Guidelines:

- ***Standard***

➢ **.010” (250 *µ*m) Pad diameter & .005” (125 *µ*m) laser drill**

- ***Advanced***

➢ **.008” (200 *µ*m) Pad diameter & .004” (100 *µ*m) laser drill**

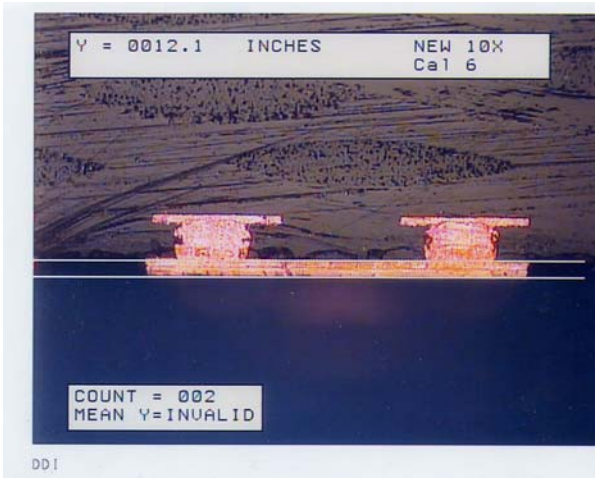
- ***Flip Chip Solution***

➢ **.007” (175 *µ*m) Pad diameter & .004” (100 *µ*m) laser drill**

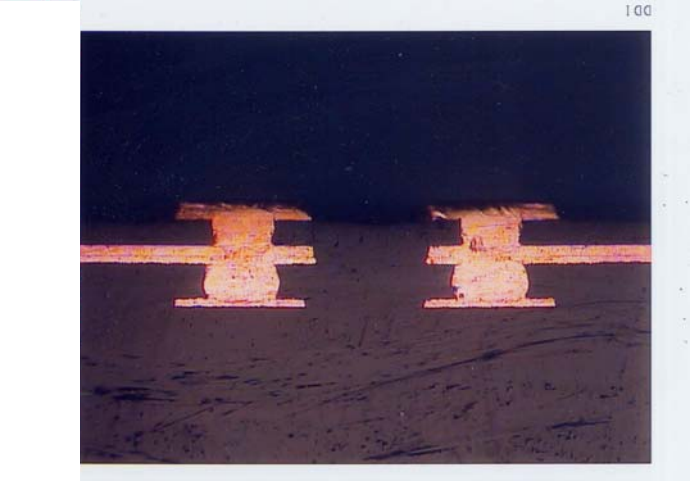
TD Technology
Stacked MicroVia (SMV™)

Definition: **.004” (100 *µ*m) laser drilled MicroVia**

solid copper plate



Planar Surface



Stacked MicroVias (SMV)

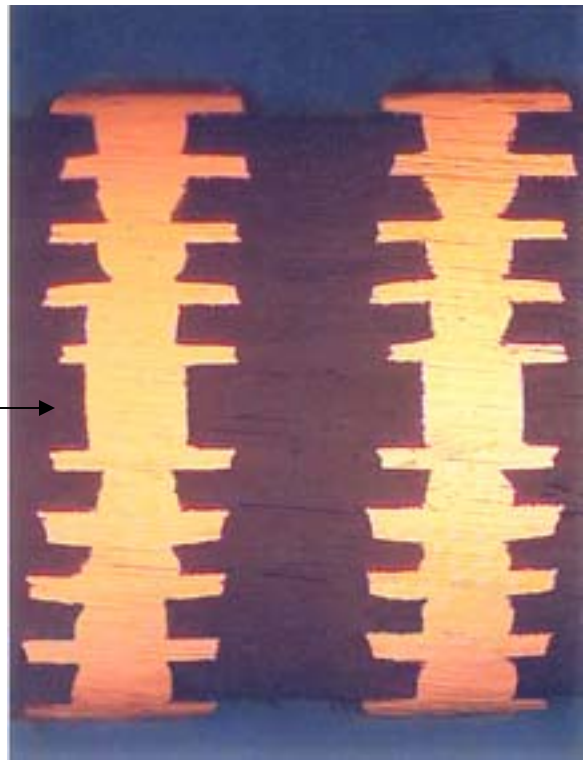
TD Technology
Stacked MicroVia (SMV™)

10 Layer SMV™ Technology

1:1 aspect ratio

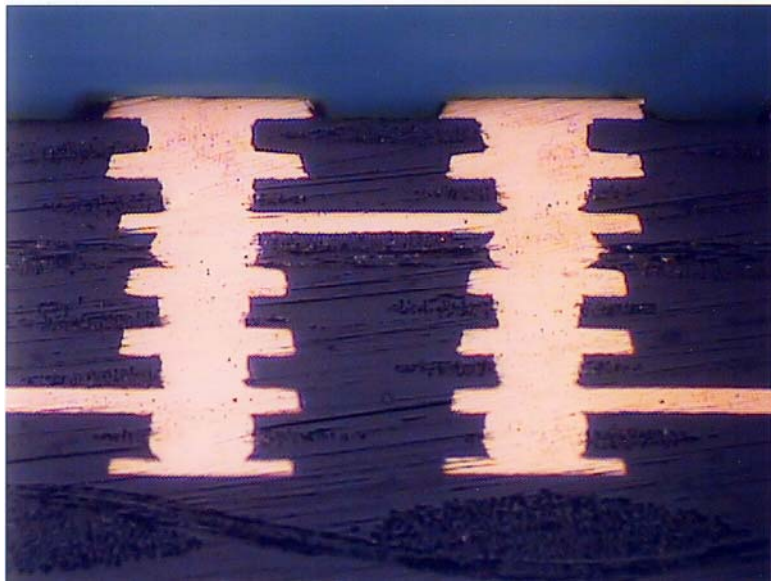
.004” (100 µM) dielectric

.004” (100 µM) laser drill



Core = Solid Copper Plate

TD Technology
Stacked MicroVia (SMV™)



Six Stacked MicroVias

Seven layers for fan-out of 0.65 mm, 0.5 mm & 0.4 mm BGAs

0.5 mm = .008" (200 μm) diameter pad using a .004" (100 μm) laser drill, .0039" (98 μm) trace & space

0.4 mm = .008" (200 μm) diameter pad, .004" (100 μm) laser drill, .0026" (65 μm) trace & space

Capable of creating a 14 Layer stacked configuration

TD Technology
Stacked MicroVia (SMV™)

Advantages:

- **Design flexibility (SMV post or buried SMV) single or stacked**
- **Provides a solid copper plate**
- **Improves Current Carrying Capability & Thermal Management**
- **Provides a Planar surface for BGA (Via-in-Pad)**
- **Increases routing density for Fine Pitch BGAs**
  (0.65 mm, 0.5 mm & 0.4 mm)
- **Allows Design Fan-out on multiple layers using**
  .010” (250 *μ*m) or .008” (200 *μ*m) pad diameters

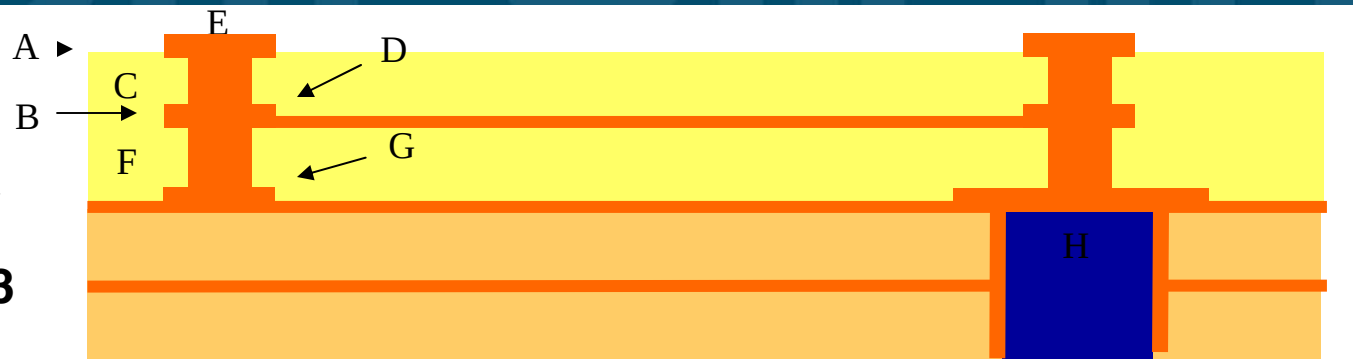
TD Technology
Stacked MicroVia (SMV™)

Applications:

- Mobile Phones (including Cell/PDA & camera phone)
- Hand Held products (PDAs, Cameras, GPS/Navigation)
- Telecom (Networks, Switches, Servers)
- Wireless LAN
- Medical Equipment
- Reference Designs
- Flip Chip BGA Interposer
- MCM BGA Interposer

TD Technology

Stacked MicroVia (SMV™)



Laser Drilled SMV

Layer 1 to 2 & 2 - 3

#	Description	Standard SMV		Advanced SMV	
		µm	+/-	µm	+/-
A	Minimum Layer 1 copper thickness	45	20%	45	10%
B	Minimum Layer 2 copper thickness	40	20%	40	10%
C	Layer 1 – 2 dielectric thickness	50	10%	75	10%
D	Minimum Layer 2 pad for Layer 1 to 2 Microvia	250	NA	200	NA
E	Minimum Layer 1 pad for Layer 1 to 2 Microvia	250	NA	200	NA
F	Minimum Layer 1 pad for Stacked Microvia	250	NA	200	NA
G	Minimum Layer 2 pad for Stacked Microvia	250	NA	200	NA
H	Minimum drill diameter for buried via	250	NA	2500	NA
I	Minimum Pad diameter for buried via	450		400	NA
J	Laser drilled Microvia diameter from layer 1 to 2 & 2 -3	100	NA	100	NA
K	Aspect ratio	0.5: 1	NA	0.75:1	NA

Standard Technology

1mm BGA

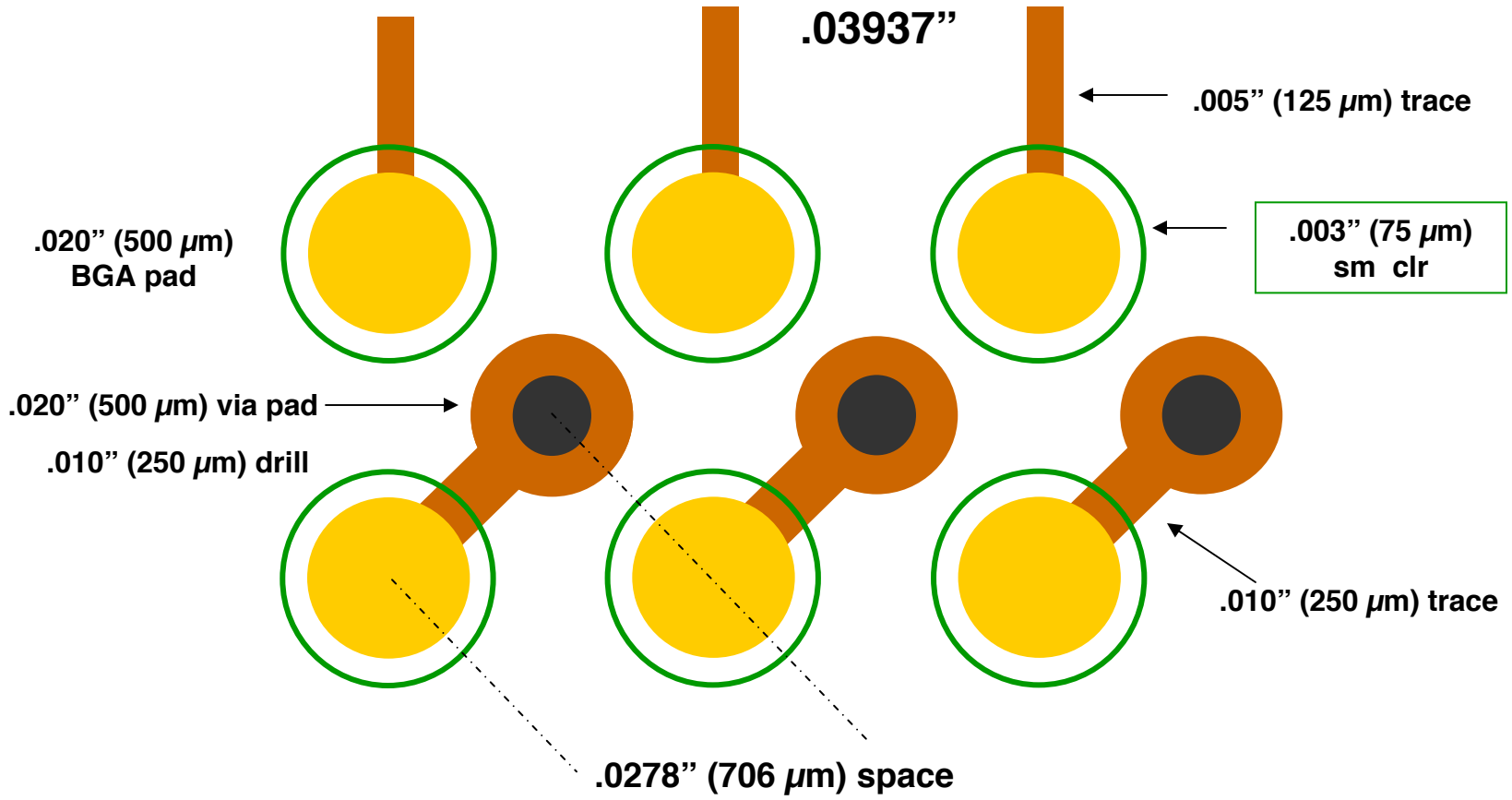
Design Guidelines

IPC 6011 / 6012

Class 2

Standard Technology

1 mm BGA



Thickness of .093”(2.362 mm)

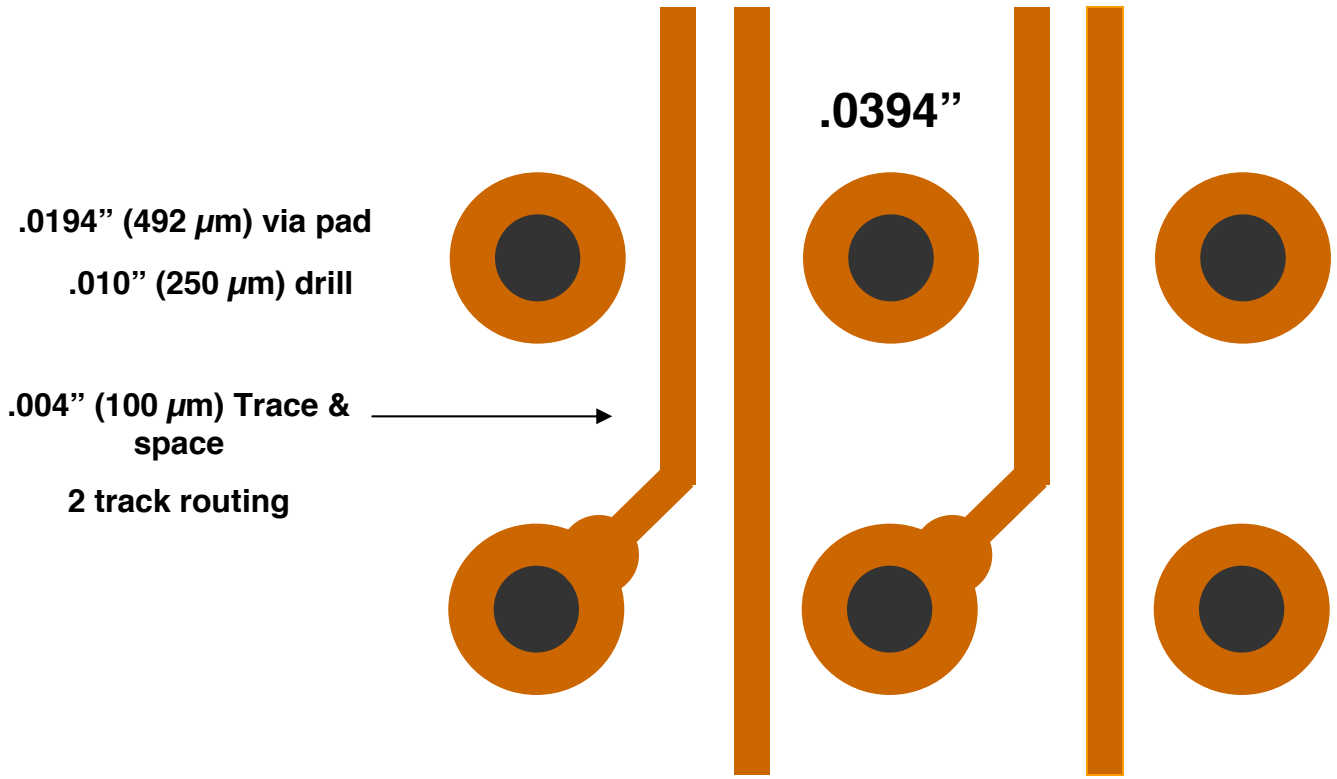
External

Aspect Ratio 10:1

Standard Technology

1 mm BGA

IPC 6011/6012 Class 2



Thickness of .093”(2.362 mm)

Internal

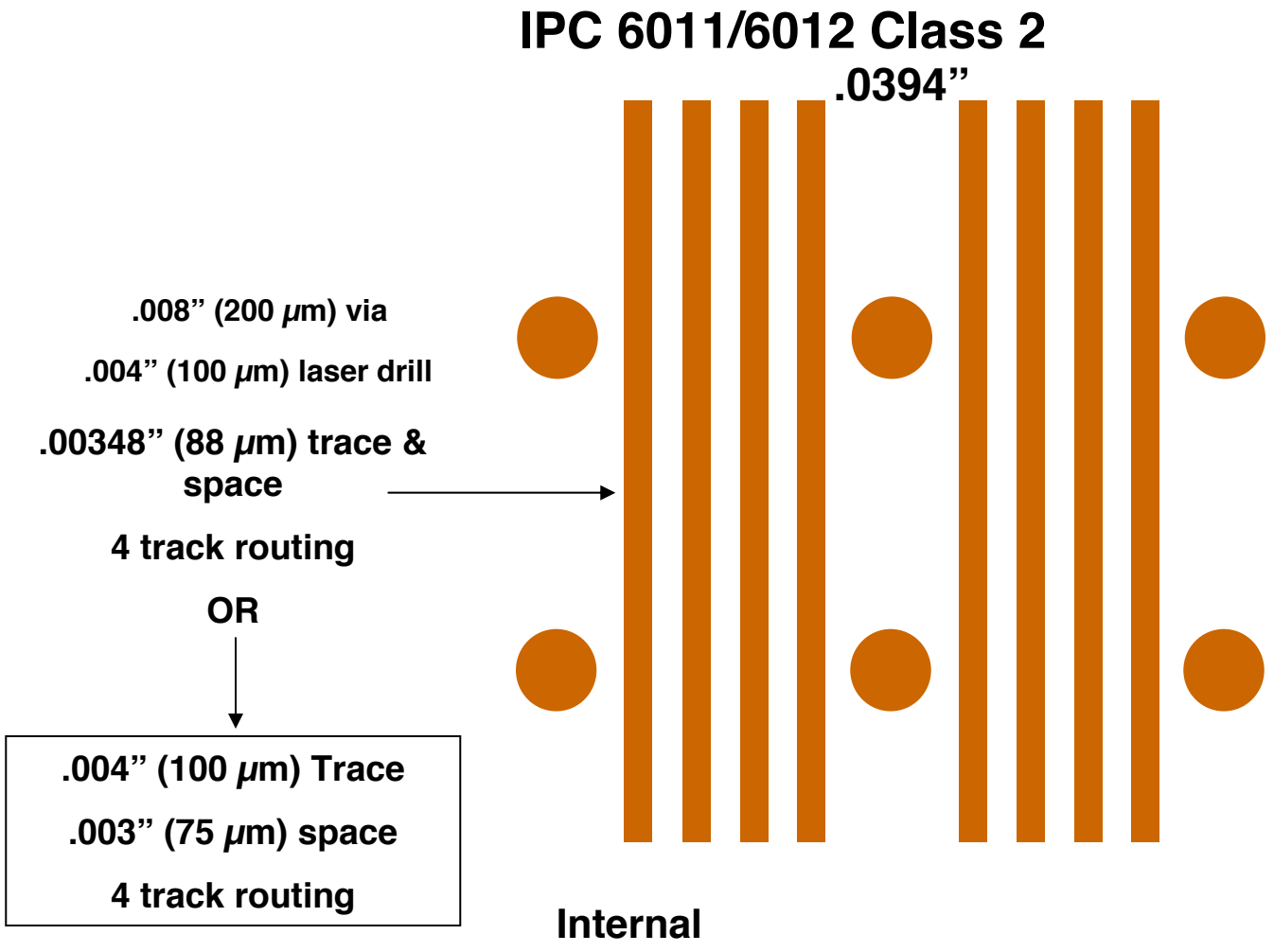
Aspect Ratio 10:1

TD Technology

Stacked MicroVia (SMV™)

1 mm BGA

IPC 6011/6012 Class 2

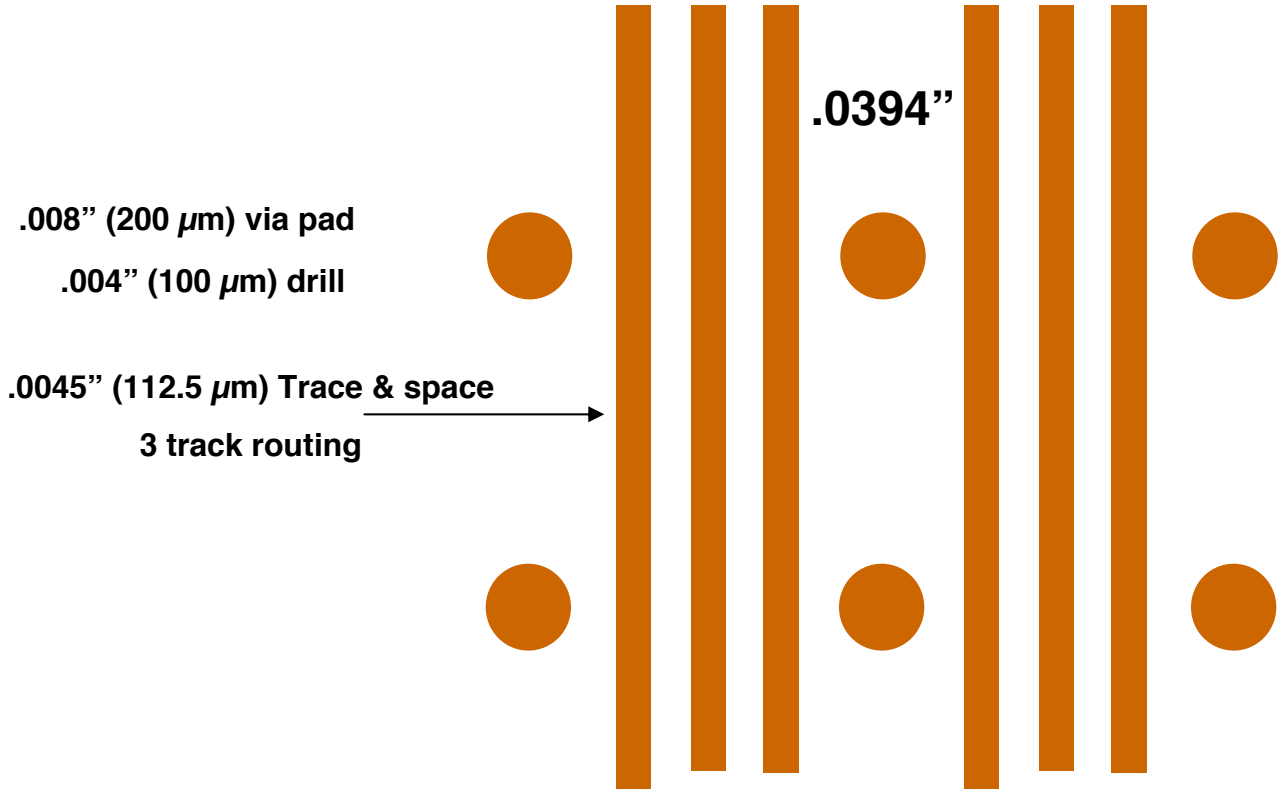


TD Technology

Stacked MicroVia (SMV™)

1 mm BGA

IPC 6011/6012 Class 2



Internal

Standard Technology

0.8 mm BGA

Design Guidelines

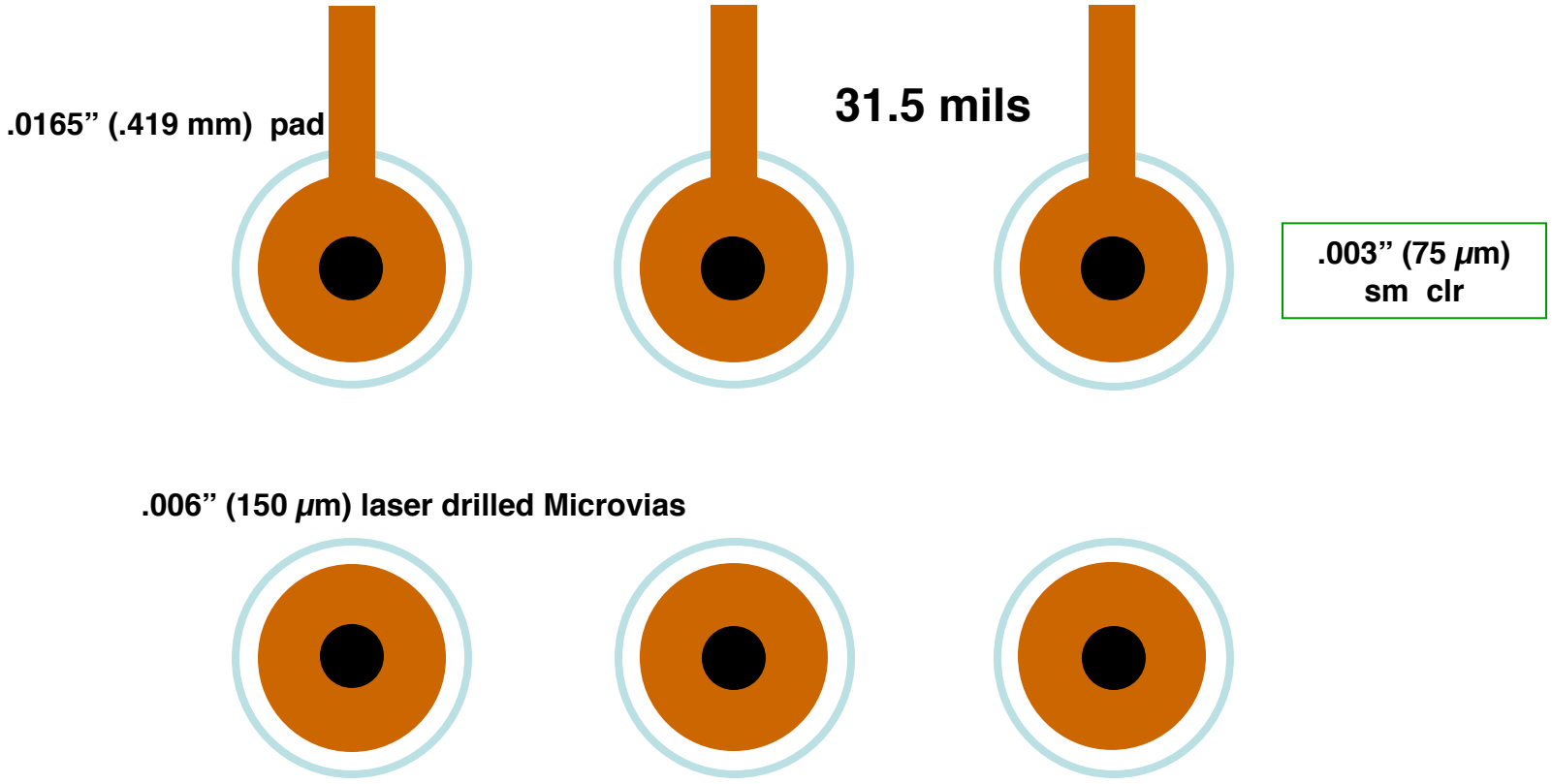
IPC 6011 / 6012

Class 2

Microvia Technology

0.8 mm BGA Design

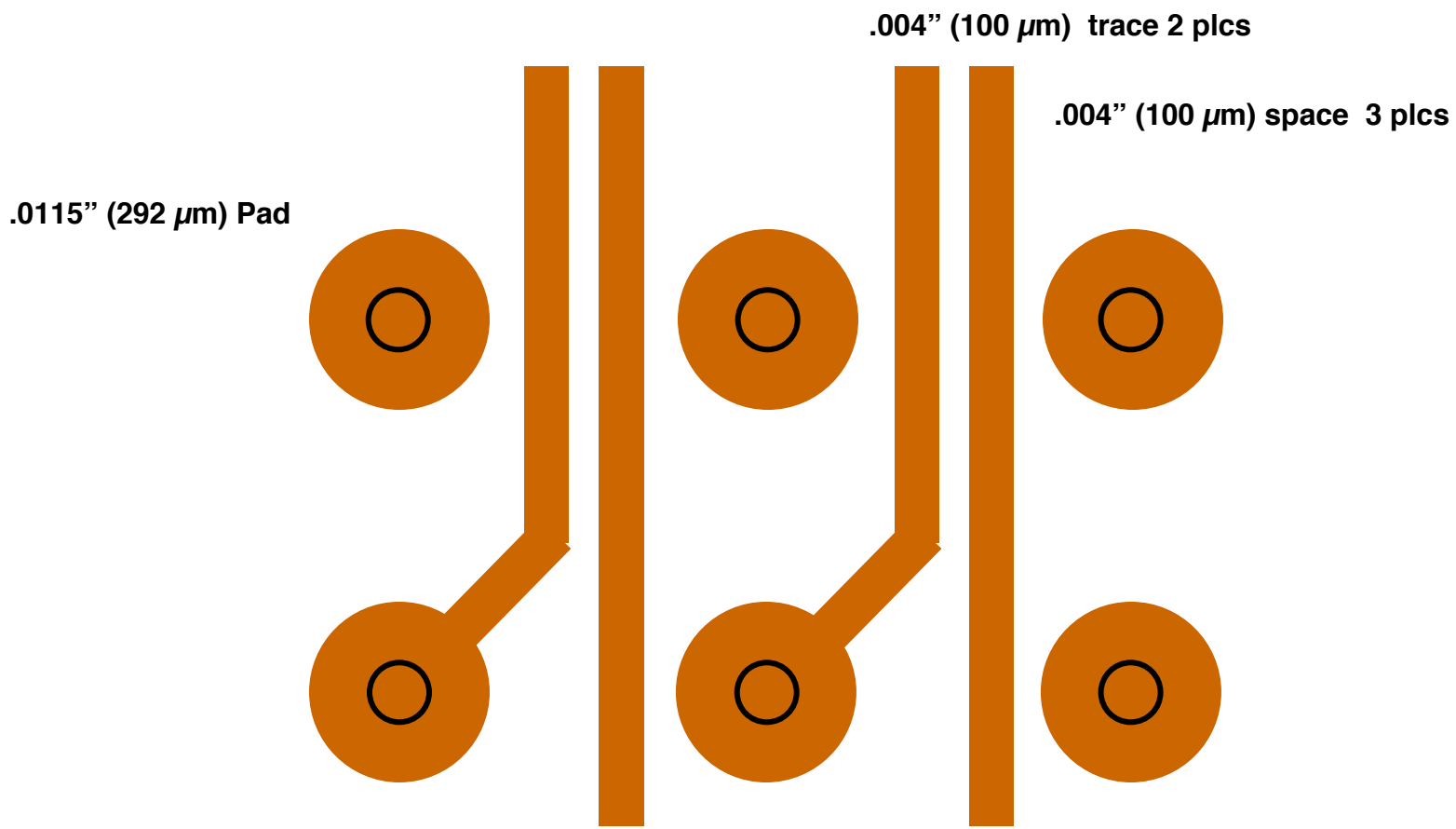
Layer 1



Microvia Technology

0.8 mm BGA

Layer 2

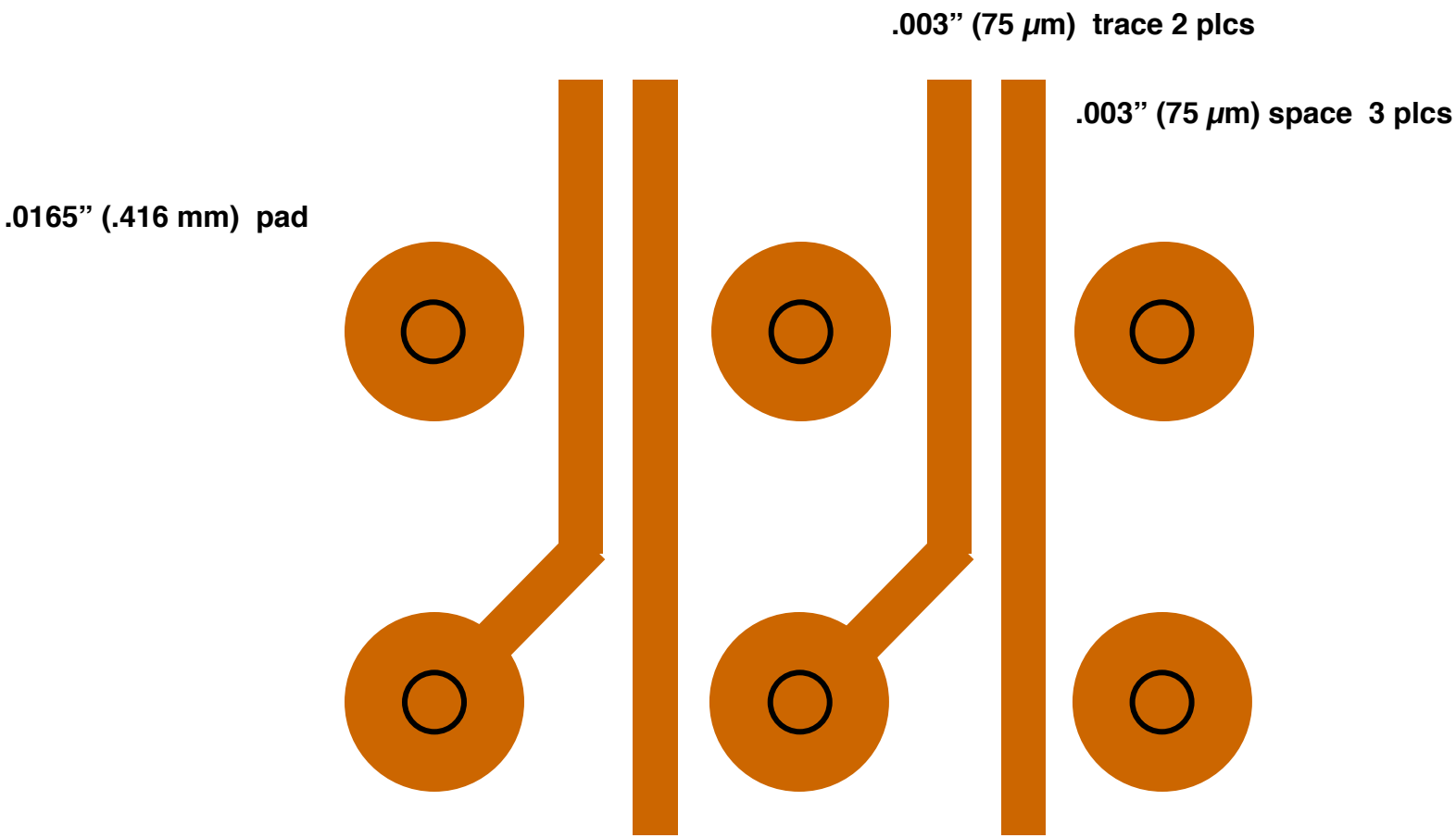


Standard Microvia Technology Layer 1 - 2

Microvia Technology

0.8 MM BGA Design

Layer 3



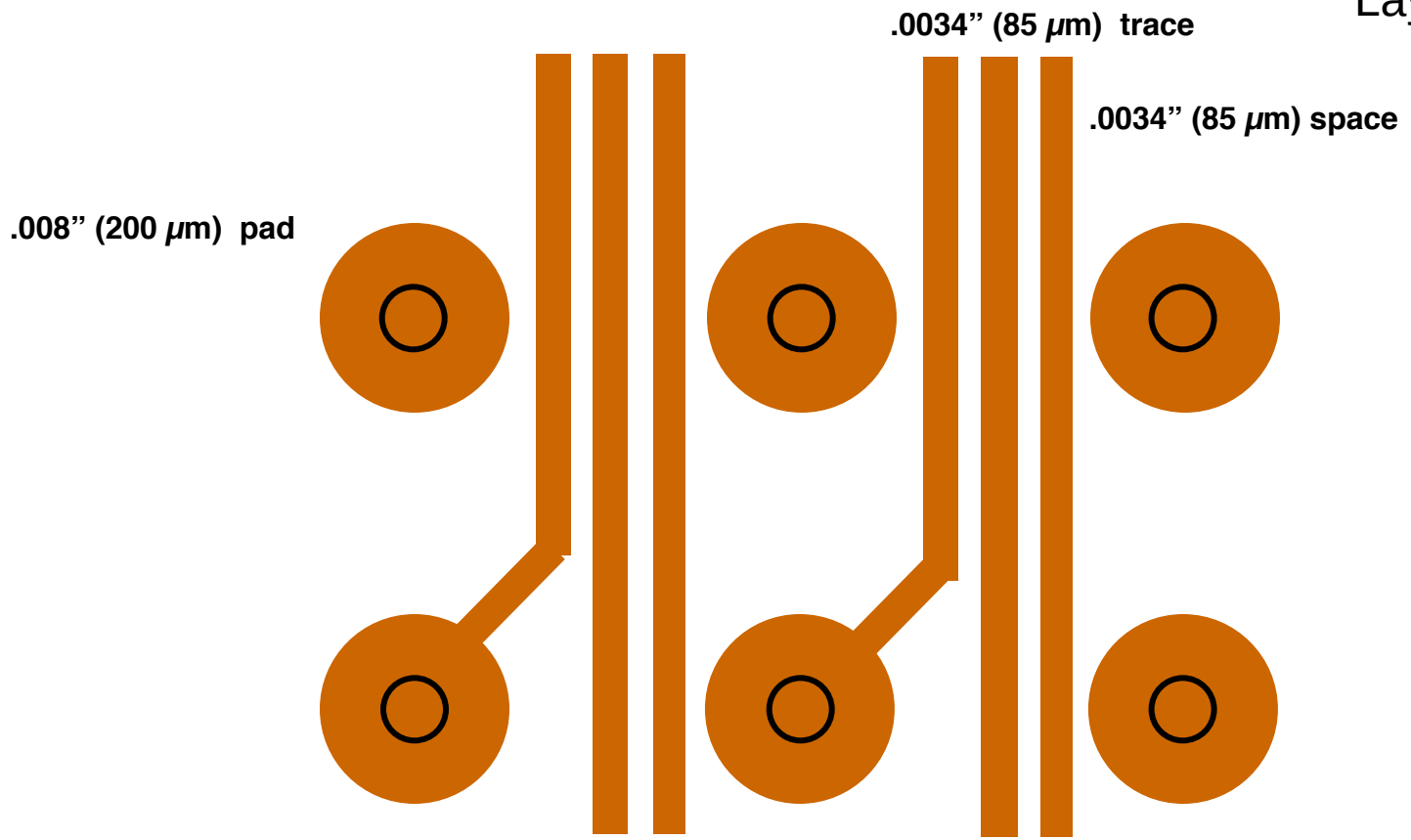
Standard Microvia Technology Layer 1 - 3

TD Technology

Stacked MicroVia (SMV™)

0.8 mm BGA Design

Layer 2 - 7



SMV™ Technology = Triple track on multiple layers

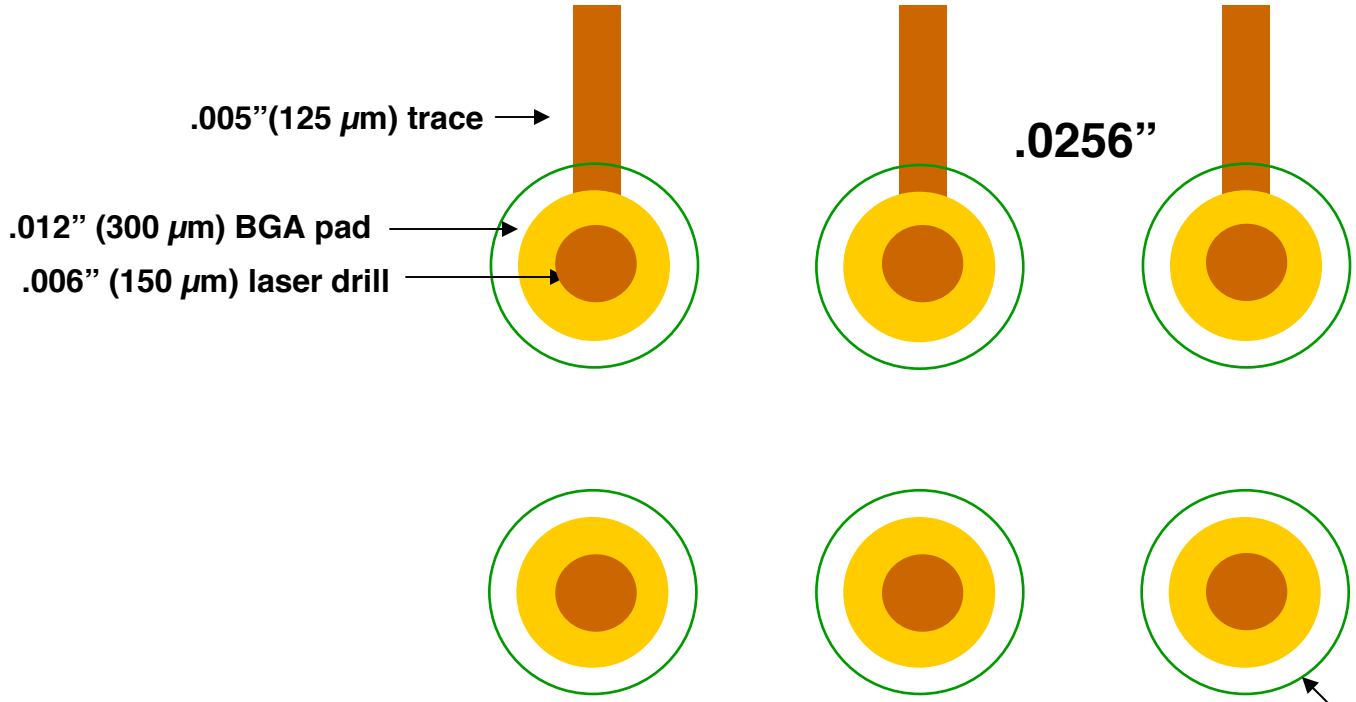
TD Technology

0.65 mm BGA

Design Guidelines

Microvia Technology

0.65 mm BGA

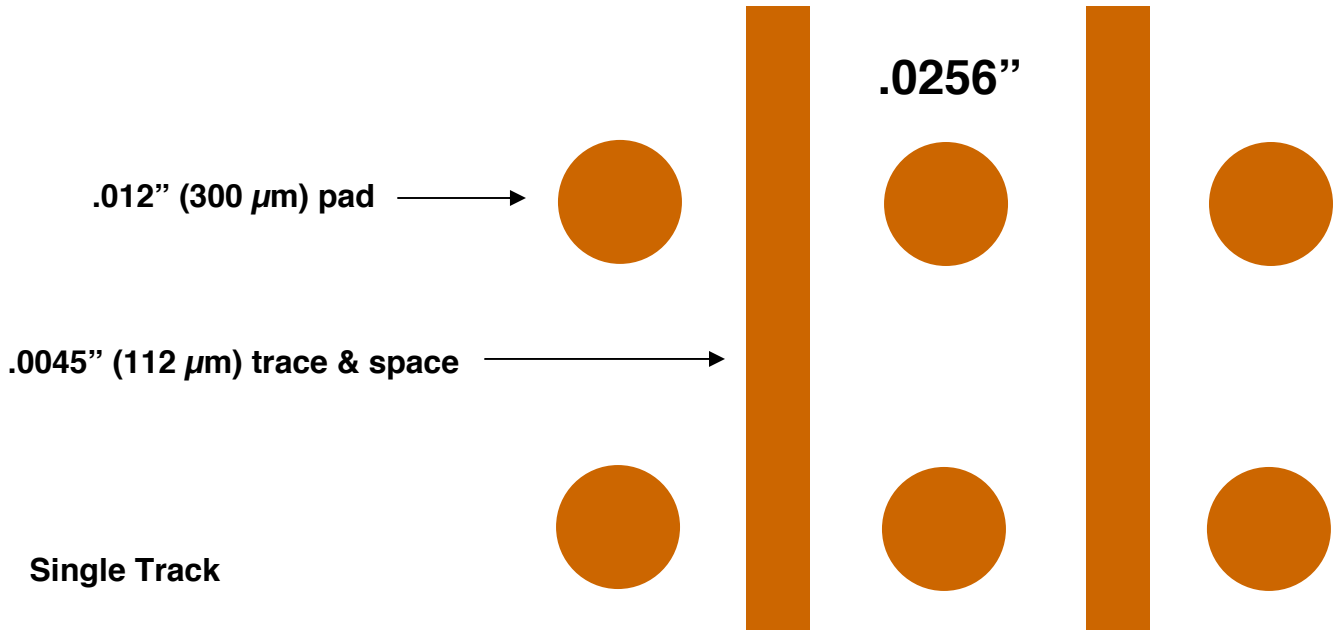


Soldermask dam = .0096” (240 µm)

External

Microvia Technology

0.65 mm BGA

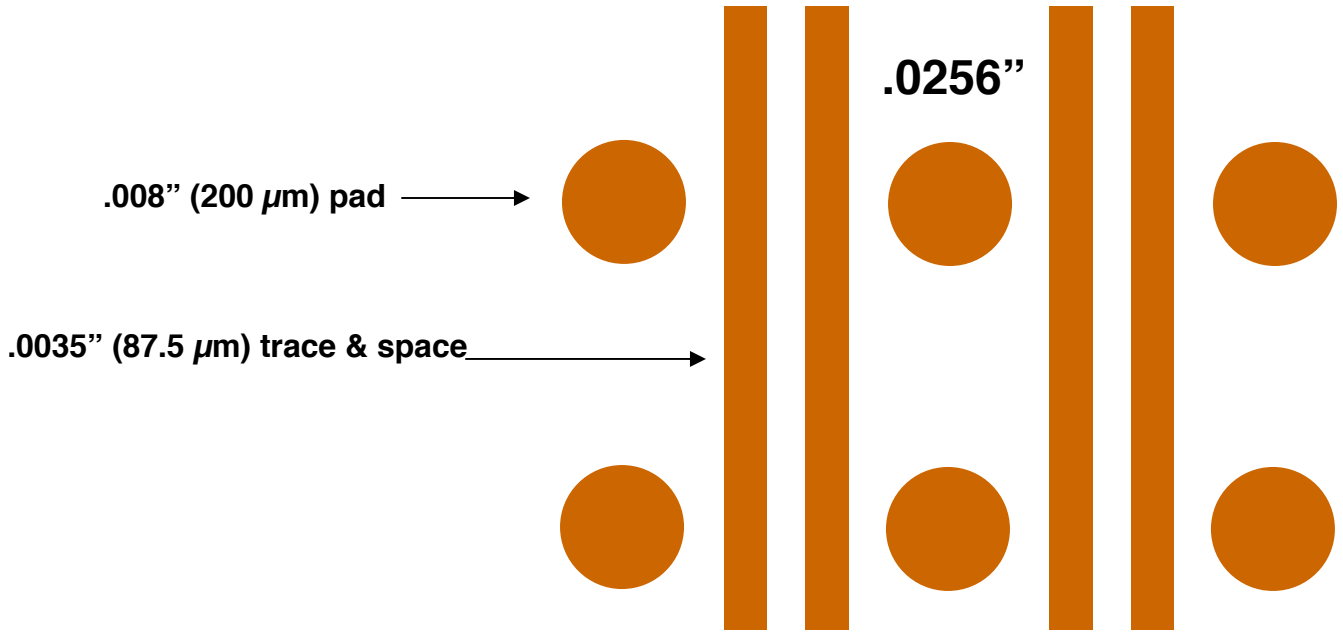


Internal

TD Technology

Stacked MicroVia (SMV™)

0.65 mm BGA



Double Track layers 2 - 7

TD Technology

0.5 mm BGA

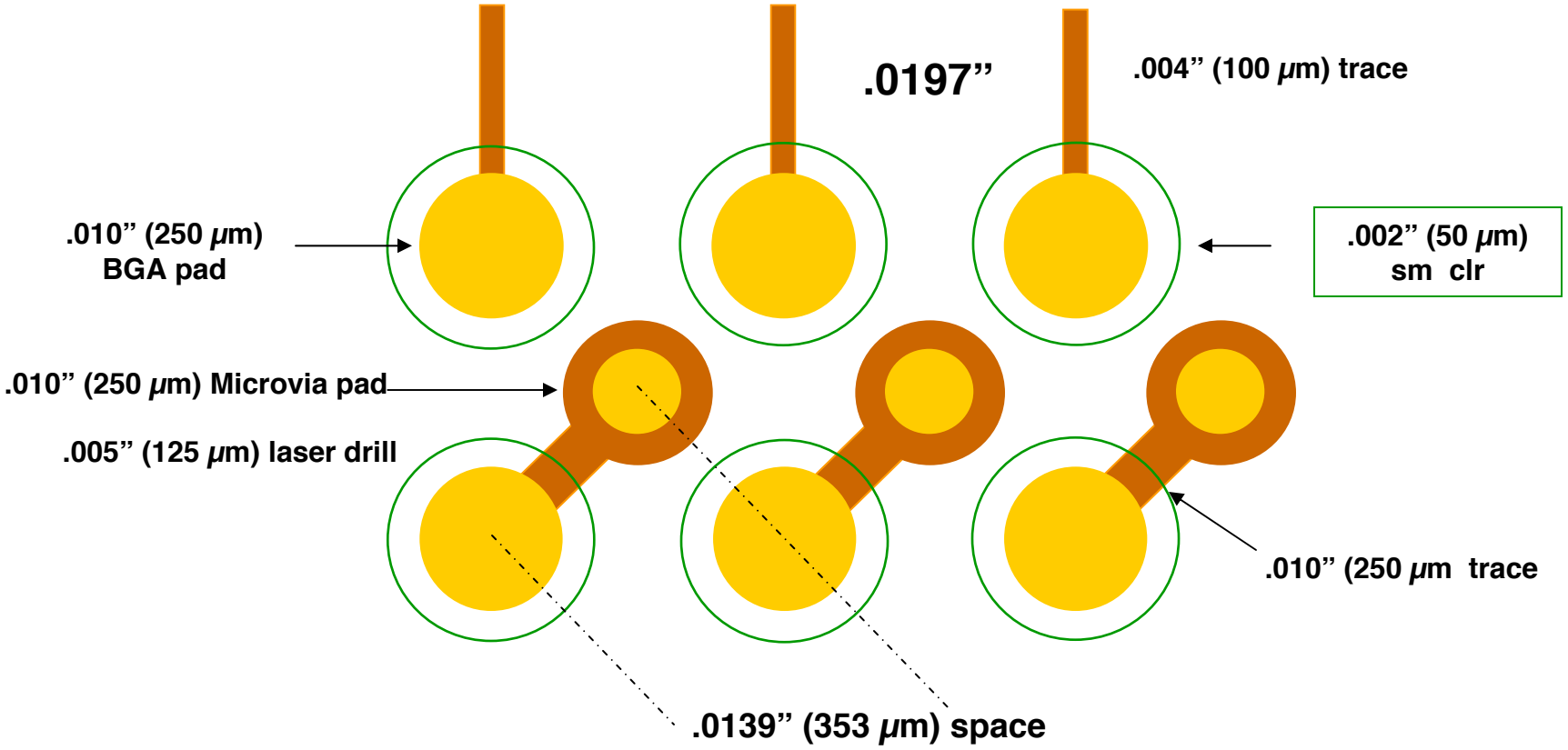
Design Guidelines

IPC 6011 / 6012

Class 2

off-set Microvia Technology

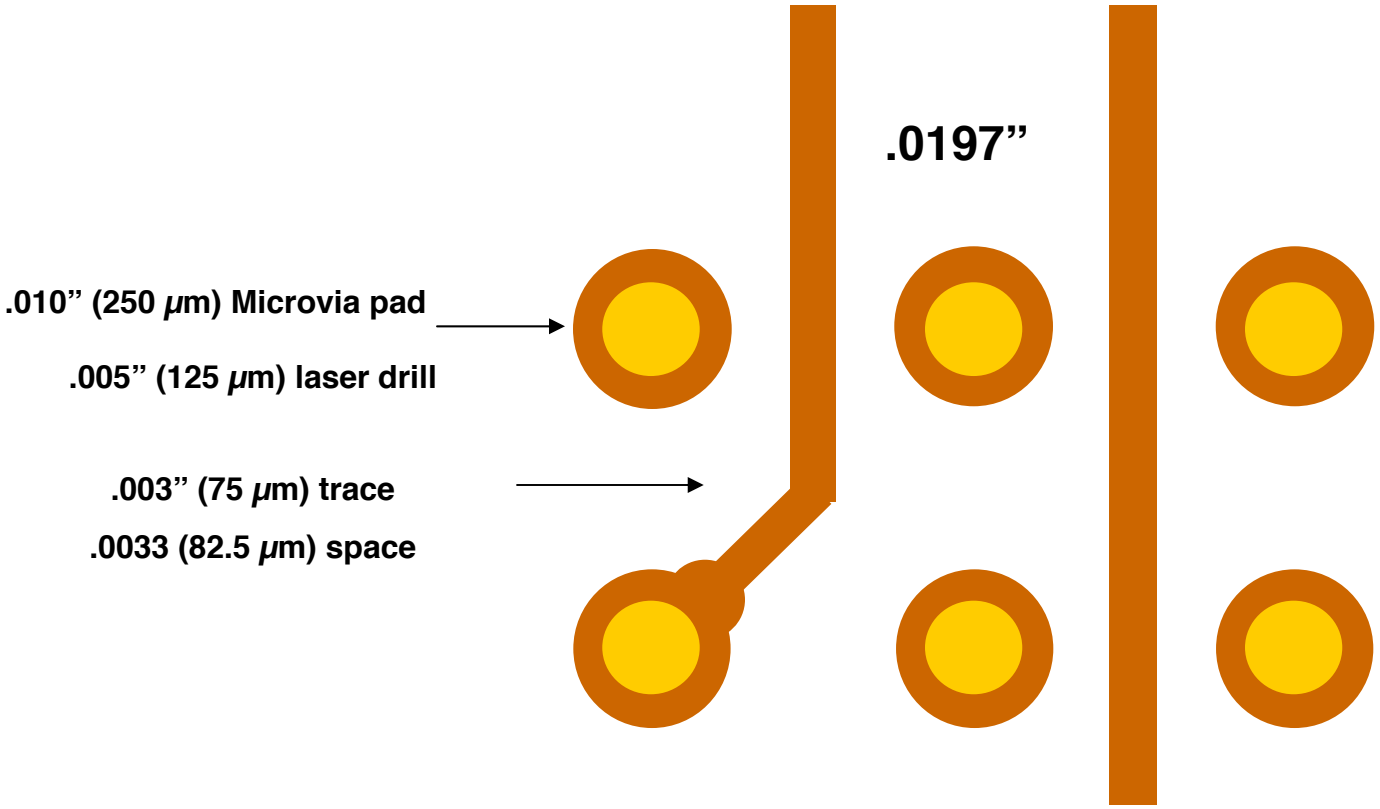
0.5 mm BGA



External

off-set Microvia Technology

0.5 mm BGA



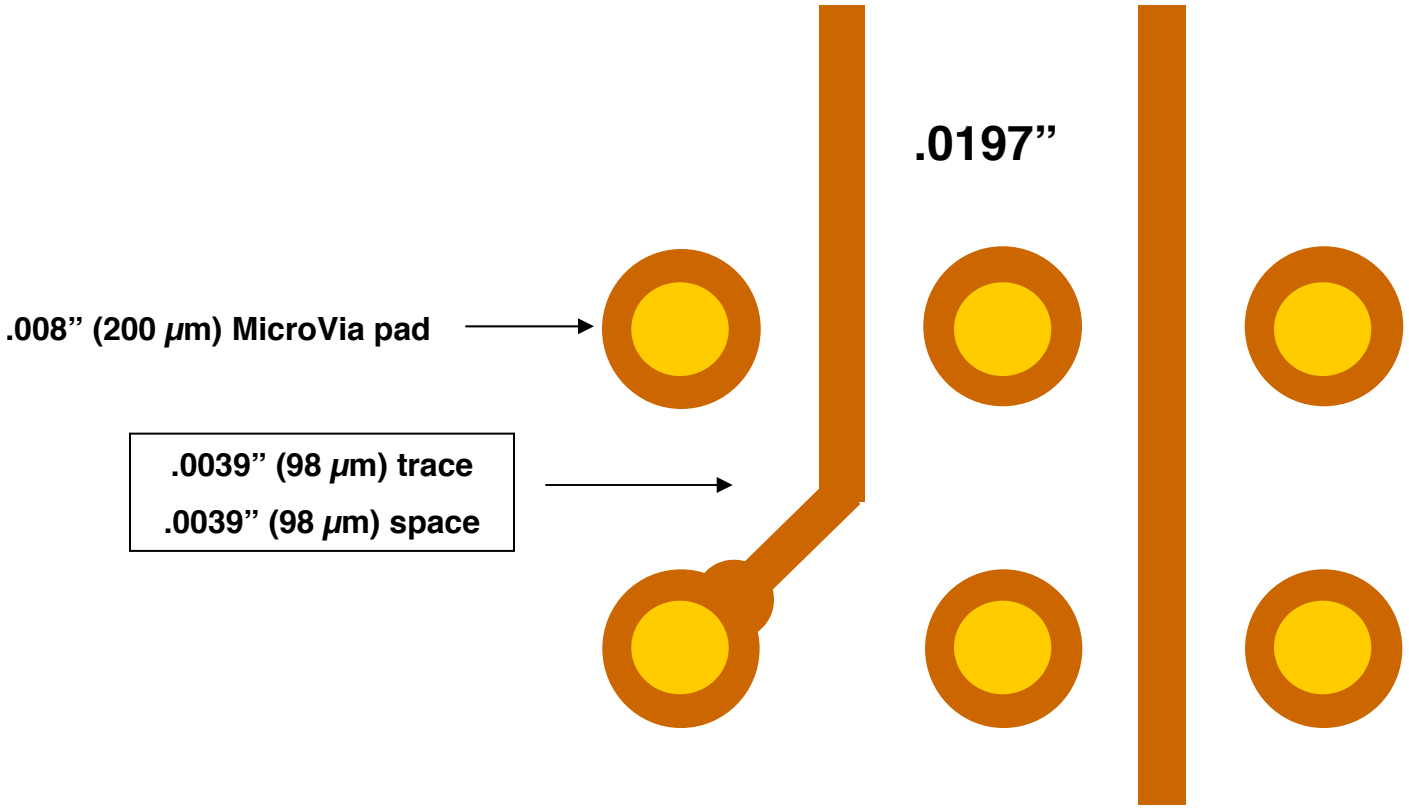
Single Track layer 2

Internal

TD Technology

Stacked MicroVia (SMV™)

0.5 mm BGA



Single Track layers 2 - 7

Internal

TD Technology

Stacked MicroVia (SMV™)

0.4 mm BGA

Design Guidelines

IPC 6011 / 6012

Class 2

SMV™ Technology

Standard Microvias provide fan-out Solutions from Layer 1 - 2

Stacked MicroVia SMV™ Technology Provides fan-out Solutions for Multiple Layers

SMV™ Technology

0.4 mm BGA

Design Guidelines:

- ***Standard***

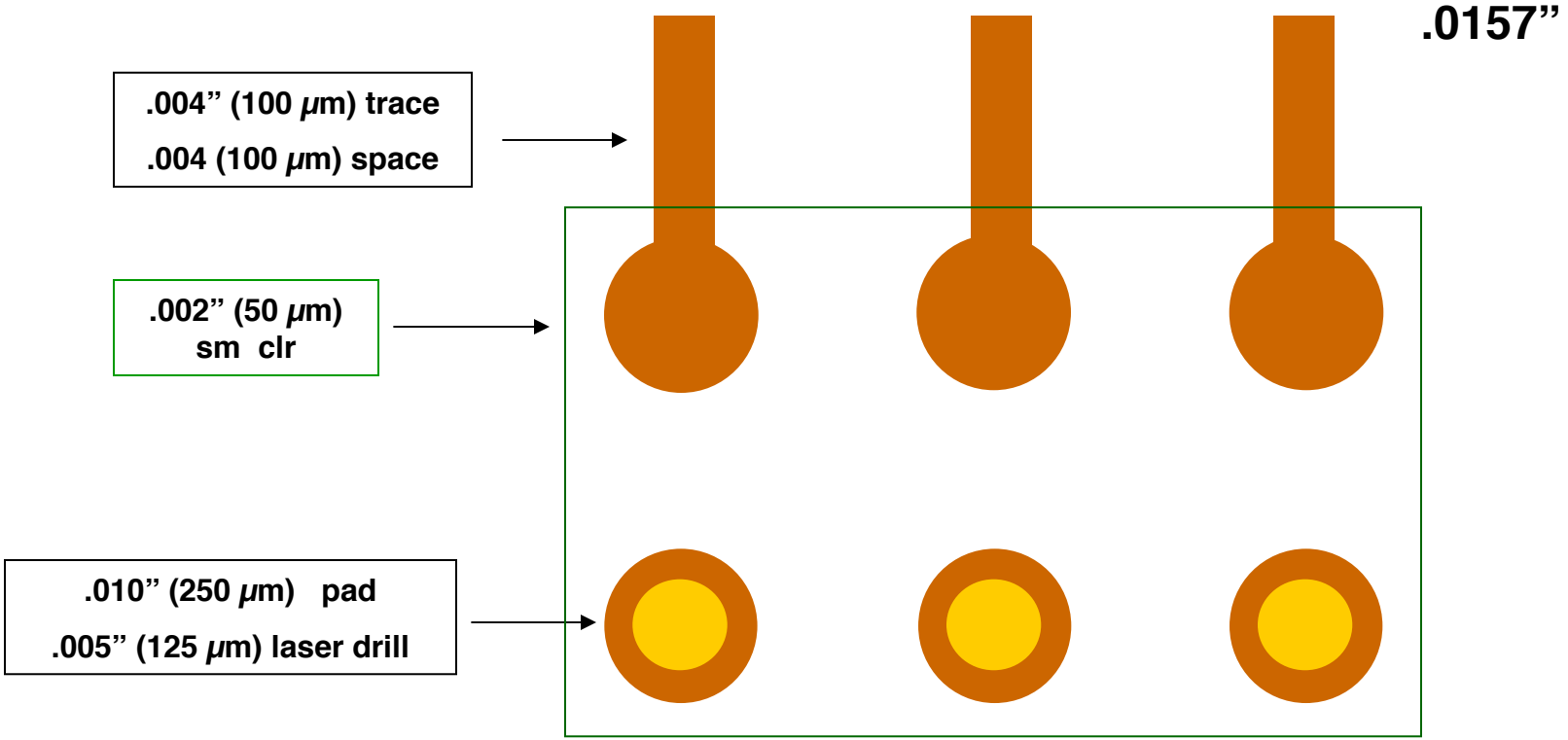
➢ **.010” (250 *µ*m) Pad diameter & .005” (125 *µ*m) laser drill**

- ***Advanced SMV™***

➢ **.008” (200 *µ*m) Pad diameter & .004” (100 *µ*m) laser drill**

Standard Microvia Technology Capable of layer 1 - 2

0.4 mm BGA

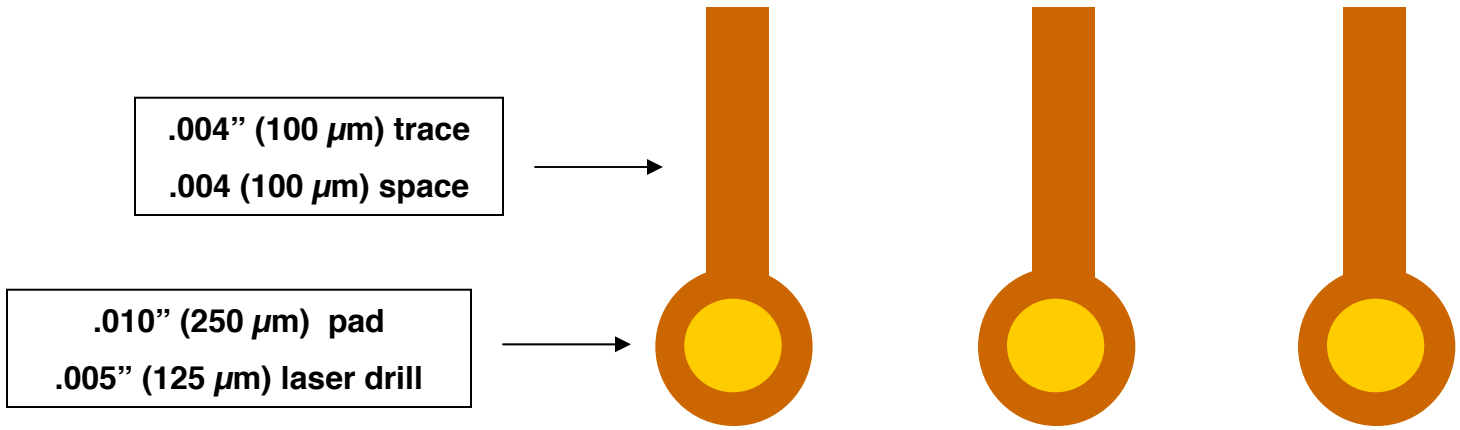


External Layer 1 = Window Solder Mask

Standard Microvia Technology Capable of layer 1 - 2

Standard 0.4 mm BGA

.0157”

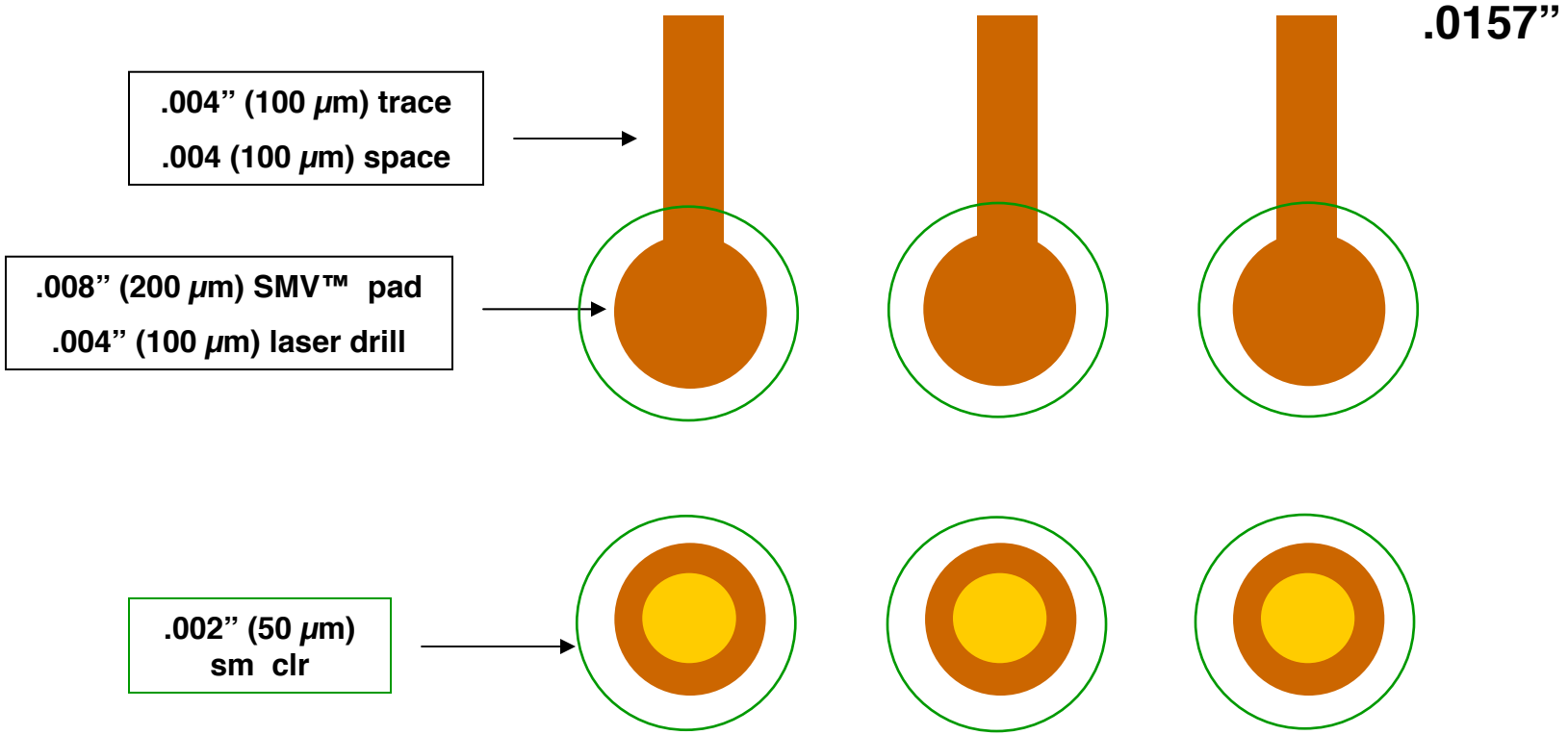


Internal Layer 2 – second row is outside row

Standard Microvias only capable of layer 1 - 2

SMV™ Technology
Capable of multiple layers

Advanced 0.4 mm BGA

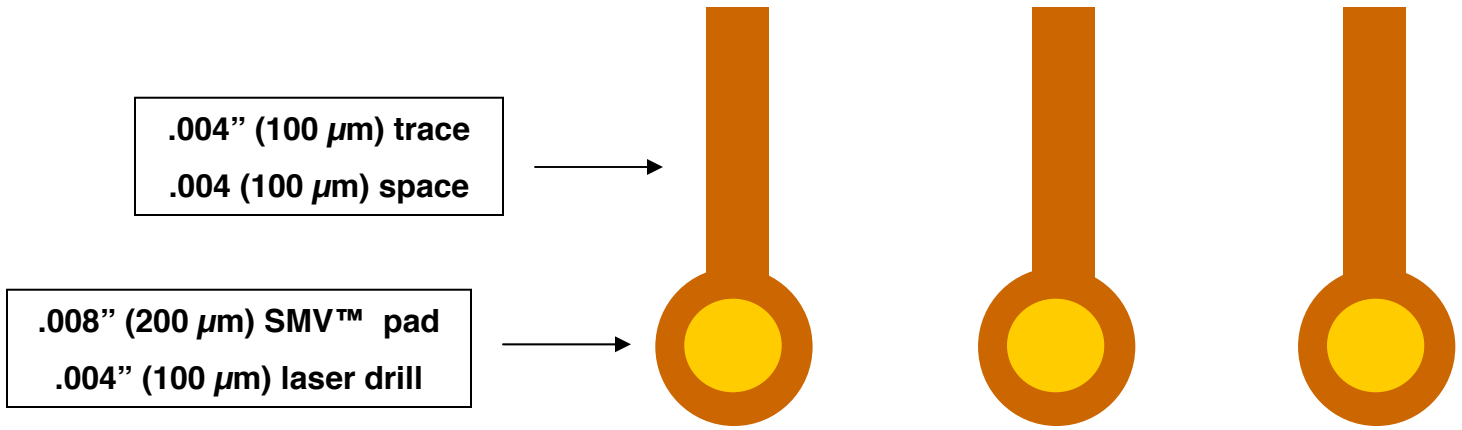


External Layer 1 .0037” Solder Dam

SMV™ Technology
Capable of multiple layers

Advanced 0.4 mm BGA

.0157”



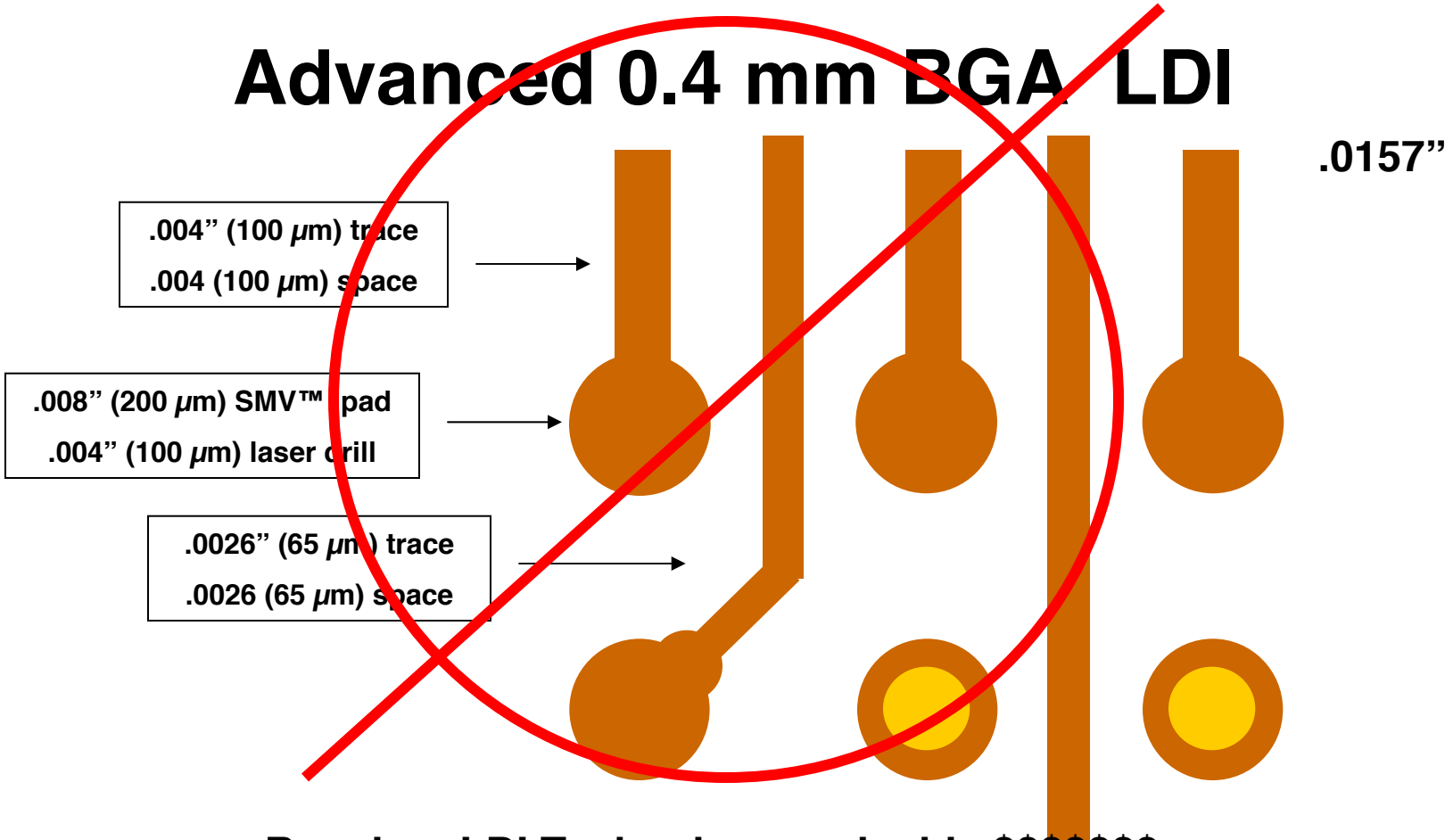
Internal Layer 2 – second row is outside row

Continue to fan out outside row and use Inverted Pyramid approach

Layer 3 - 4 - 5

SMV™ Technology

Advanced 0.4 mm BGA LDI



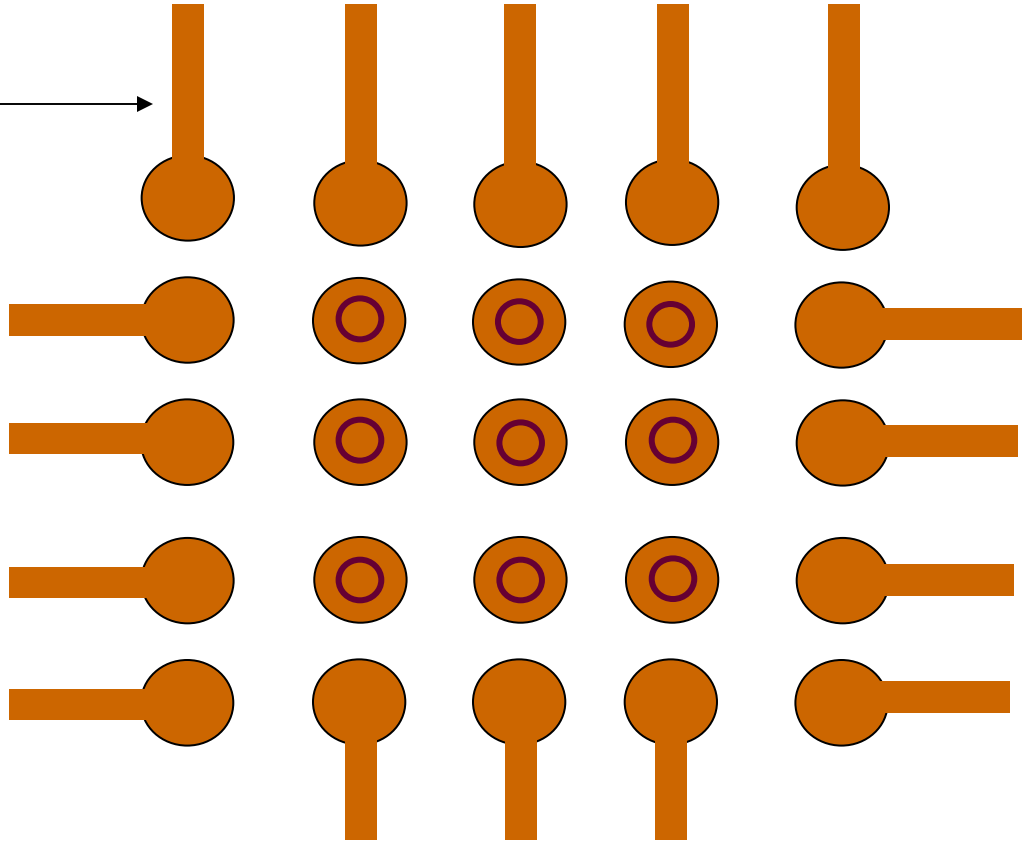
Requires LDI Technology and adds $$$$$$$

Recommend fan out on each layer using Inverted Pyramid approach

SMV™ Technology

Advanced 0.4 mm BGA 5 X 5

.004” (100 μm) trace
.004 (100 μm) space



.008” (200 μm) SMV™ pad
.004” (100 μm) laser drill

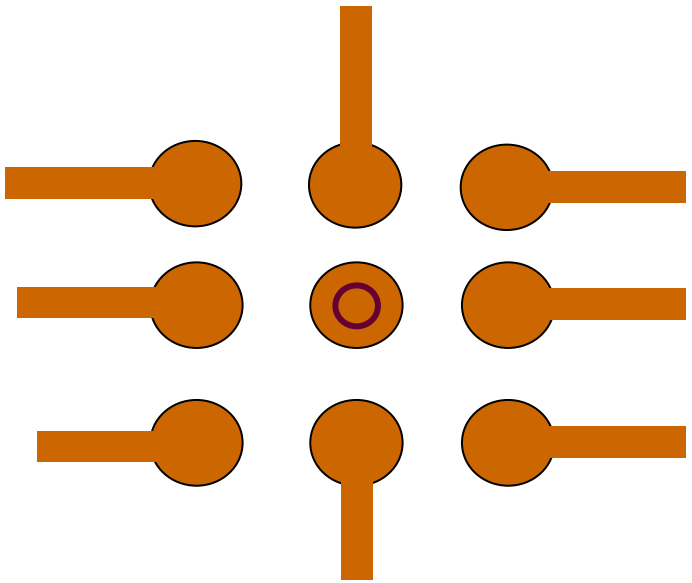
Layer 1

SMV™ Technology

Advanced 0.4 mm BGA

.004” (100 µm) trace
.004 (100 µm) space

.008” (200 µm) SMV™ pad
.004” (100 µm) laser drill



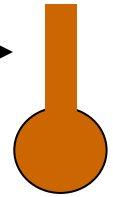
Layer 2

SMV™ Technology

Advanced 0.4 mm BGA

.004” (100 µm) trace

.004 (100 µm) space



.008” (200 µm) SMV™ pad

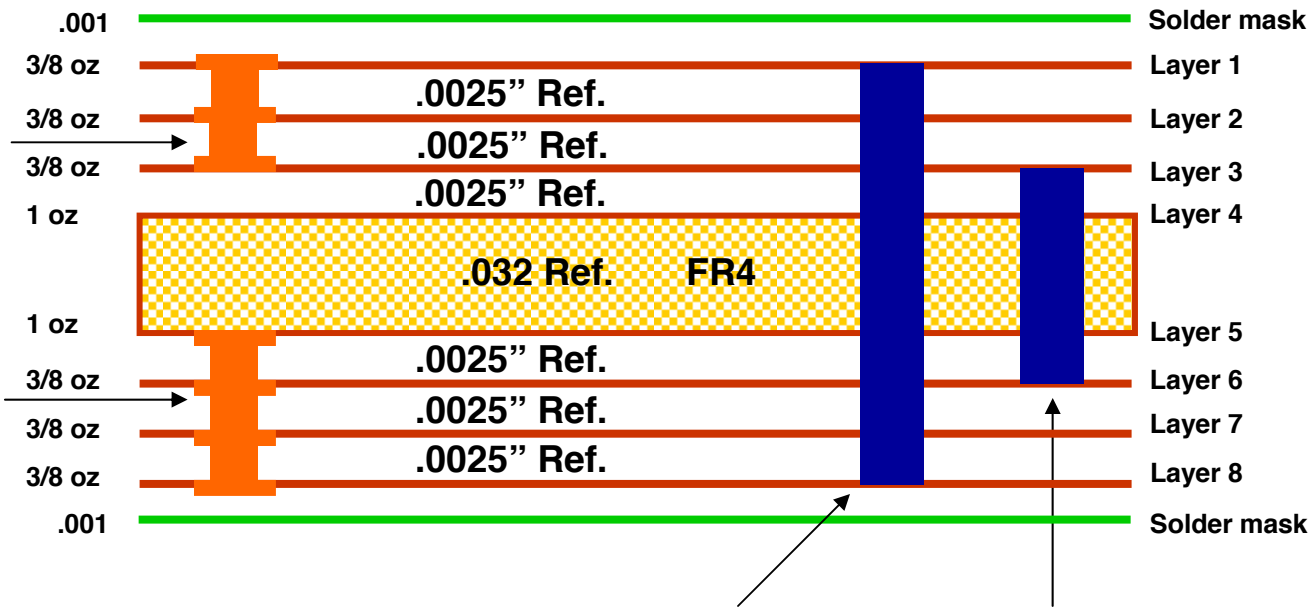
.004” (100 µm) laser drill

Layer 3

SMV™ Technology

Microvias
Layer 1 - 2
Layer 2 - 3
.010” pad
.005” laser drill

Microvias
Layer 8 - 7
Layer 7 - 6
Layer 6 - 5
.010” pad
.005” laser drill



Stacked MicroVias
Solid Cu Plate

Layer 1 - 8 = Through-hole
.022” pad & .012” drill

Layer 3 - 6 = Buried Vias
.020” pad & .010” drill

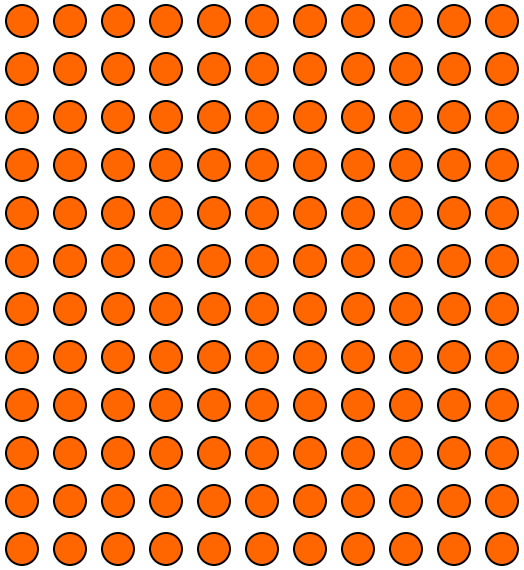
Buried via holes to be filled with non-conductive epoxy

Finish Thickness = .062 +/- .006
Material = High Temperature FR4 175° C Tg

TD Technology

SMV™ Technology

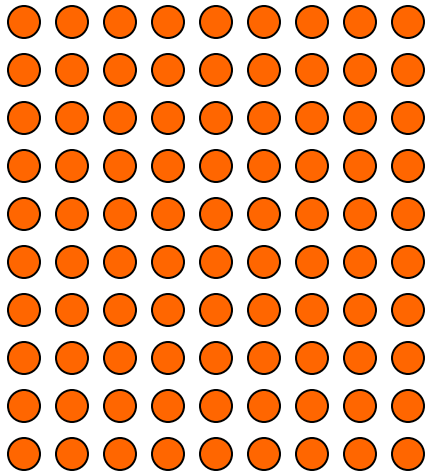
12 X 11 0.4 mm pitch



Rout outside row on Layer 1

TD Technology
SMV™ Technology

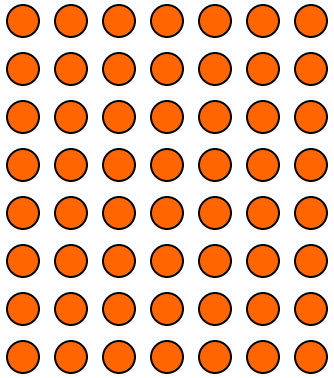
12 X 11 0.4 mm pitch



Rout outside row on Layer 2

TD Technology
SMV™ Technology

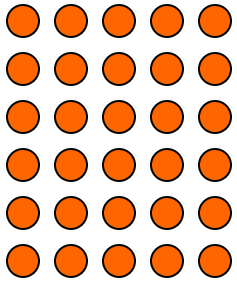
12 X 11 0.4 mm pitch



Rout outside row on Layer 3

TD Technology
SMV™ Technology

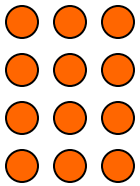
12 X 11 0.4 mm pitch



Rout outside row on Layer 4

TD Technology
SMV™ Technology

12 X 11 0.4 mm pitch



Rout outside row on Layer 5

TD Technology
SMV™ Technology

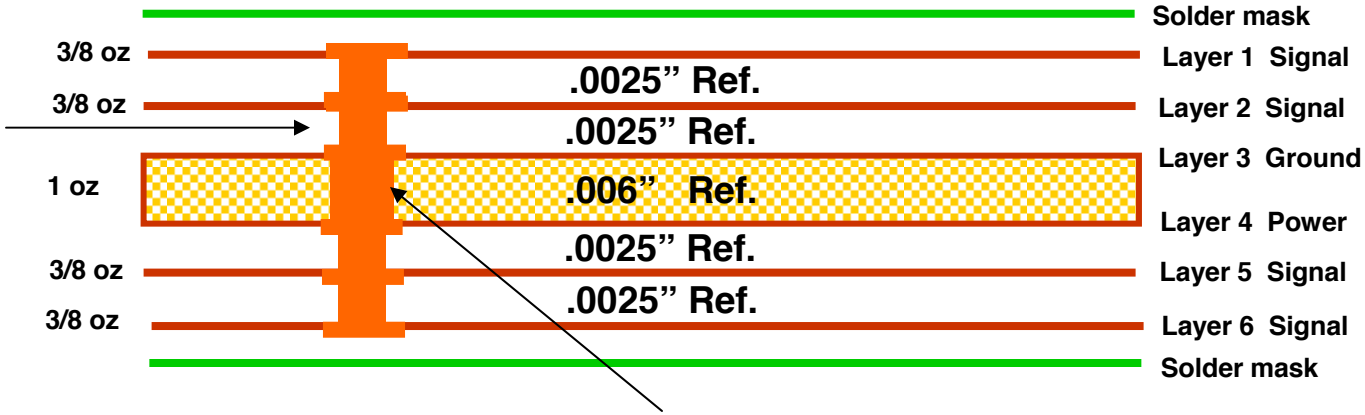
12 X 11 0.4 mm pitch

Rout outside row on Layer 6

TD Technology

Stacked MicroVias (SMV™)

Microvias
Layer 1 - 2
Layer 2 – 3
Layer 6 – 5
Layer 5 - 4
.010” pad
.005” laser drill
Solid Cu Plate



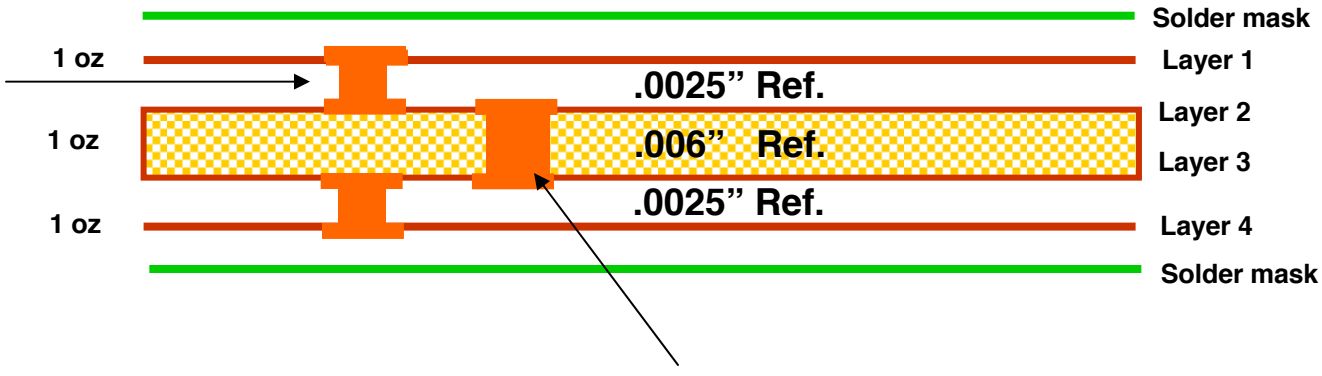
Buried Via
Layer 3 - 4
.012” pad
.006” mech drill
Solid cu plate
or laser drill
Solid cu plate

Finish Thickness = .030” +/- .003”
Material = High Temperature FR4

TD Technology

MicroVia Technology

Microvias
Layer 1 - 2
Layer 4 - 3
.012” pad
.006” laser drill
Solid Cu Plate



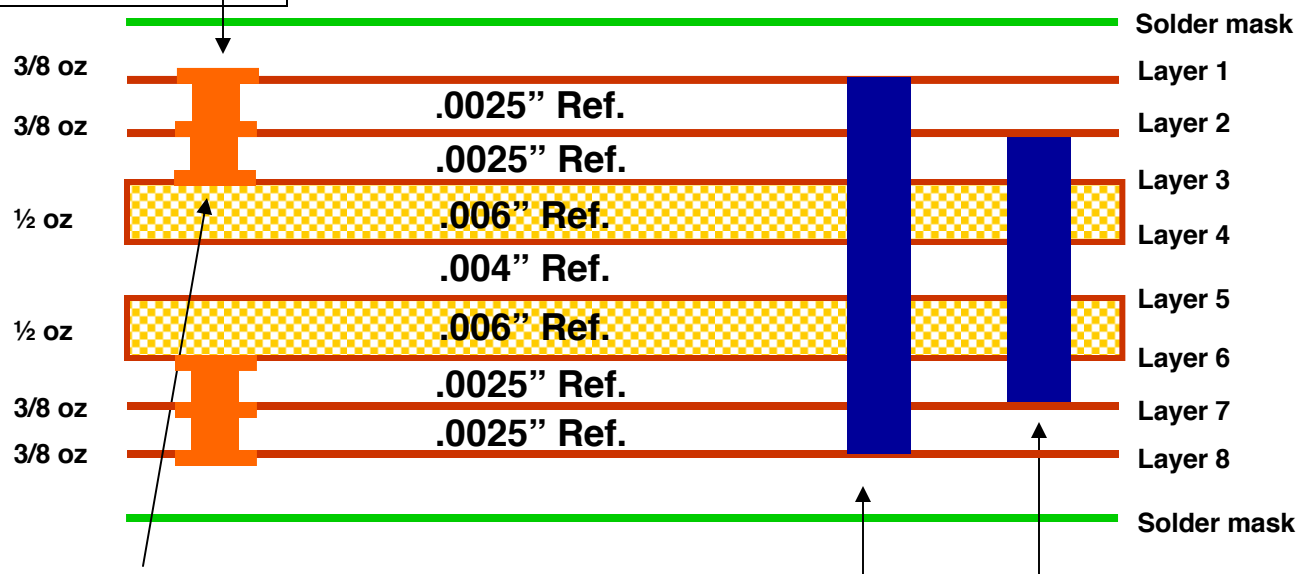
Buried Via
Layer 2 - 3
.012” pad
.006” laser drill

1 oz external layers plate up to 2 oz

Finish Thickness = .020” +/- .003”
Material = High Temperature FR4

TD SMV™ Technology

Layer 1 - 2 & 8-7 = SMV
L1 .010” pad & .005” laser drill



Layer 2 – 3 & 6 - 7 = SMV
.010” pad & .005” laser drill

Layer 1 - 8 = Through-hole
.020” pad & .010” drill

Layer 2 - 7 = Buried Vias
.018” pad & .008” drill

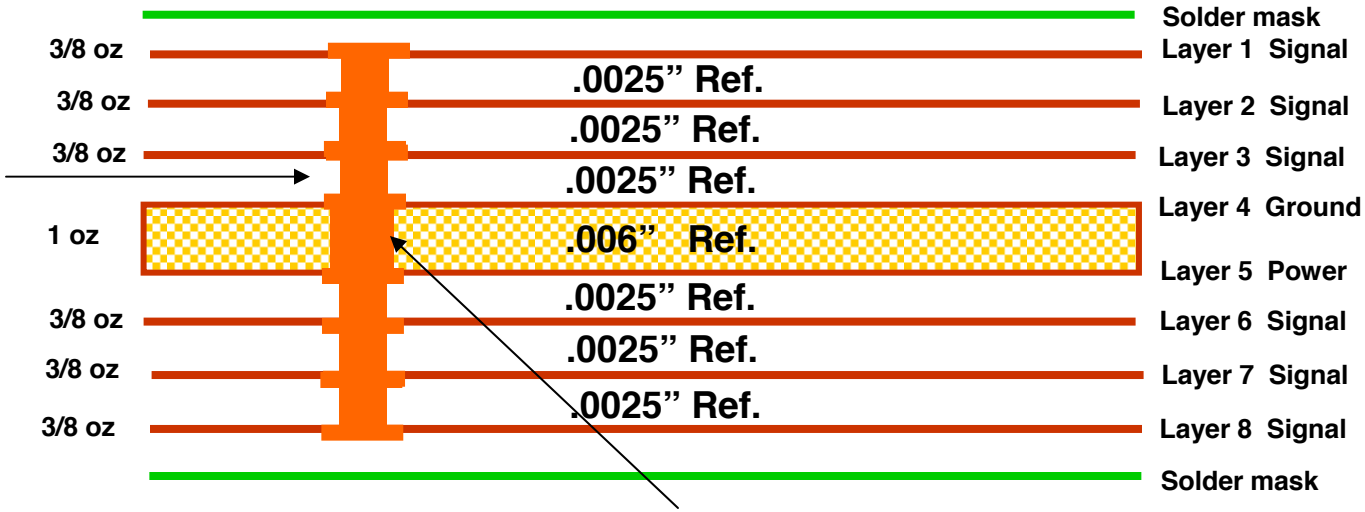
Stacked MicroVias
2-3 & 6-7
Solid Copper Plate

Finish Thickness = .038 +/- .004

TD Technology

Stacked MicroVias (SMV™)

Stacked MicroVias
Layer 1 - 2
Layer 2 – 3
Layer 3 – 4
Layer 8 - 7
Layer 7 – 6
Layer 6 - 5
.010” pad
.005” laser drill
Solid Cu Plate



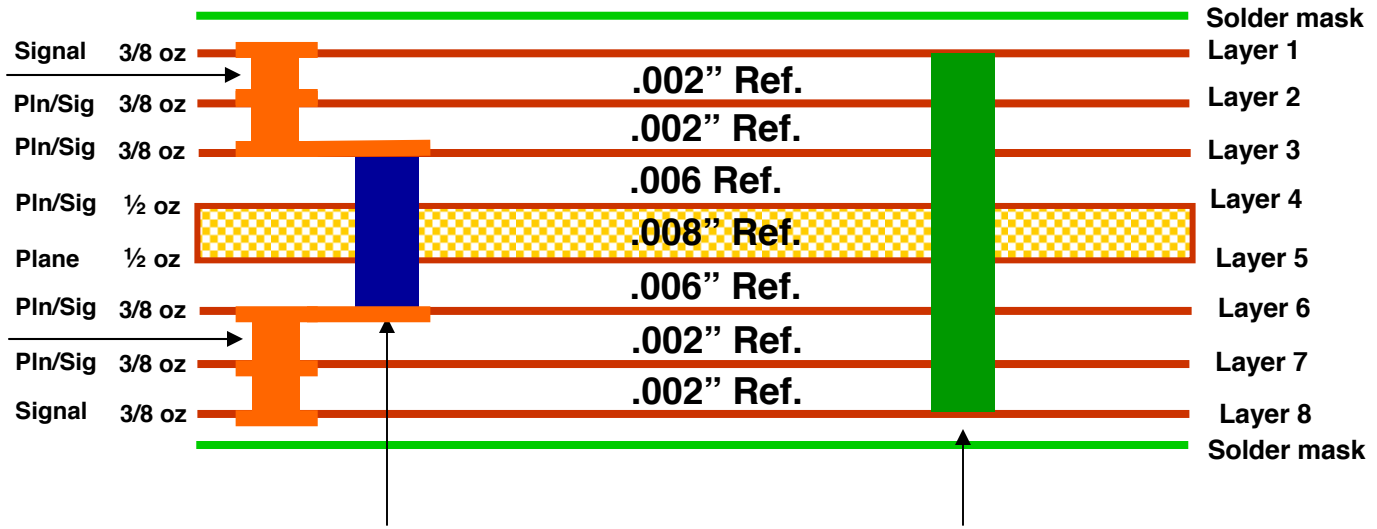
Buried Via
Layer 4 - 5
.012” pad
.006” mech drill
Solid cu plate
or laser drill
Solid cu plate

Finish Thickness = .038” +/- .004”
Material = High Temperature FR4

Stacked MicroVias (SMV™)

Stacked MicroVias
Layer 1 - 2
Layer 2 – 3
.010” pad
.005” laser drill

Stacked MicroVias
Layer 8 - 7
Layer 7 – 6
.010” pad
.005” laser drill



Layer 3 - 6 = Buried Vias
.018” pad & .008” drill

Layer 1 - 8 = through Vias
.020” pad & .010” drill

Stacked MicroVias
Solid Cu Plate

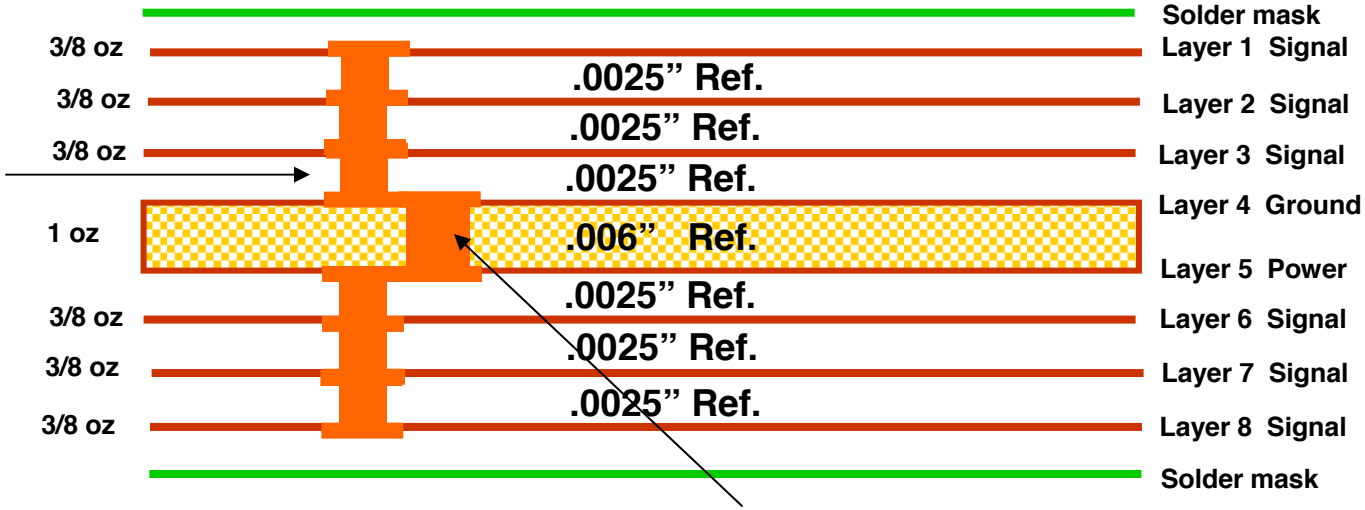
Copper Plating Thickness
Layers 1 & 8 plate to approx .002”
Layers 2, 3, & 6, 7 plate to approx .0016”
Layers 4 & 5 copper thickness = .0006”

Finish Thickness = .03937” +/- .004”
Material = High Temperature FR4

TD Technology

Stacked MicroVias (SMV™)

Stacked MicroVias
Layer 1 - 2
Layer 2 – 3
Layer 3 – 4
Layer 8 - 7
Layer 7 – 6
Layer 6 - 5
.010” pad
.005” laser drill
Solid Cu Plate



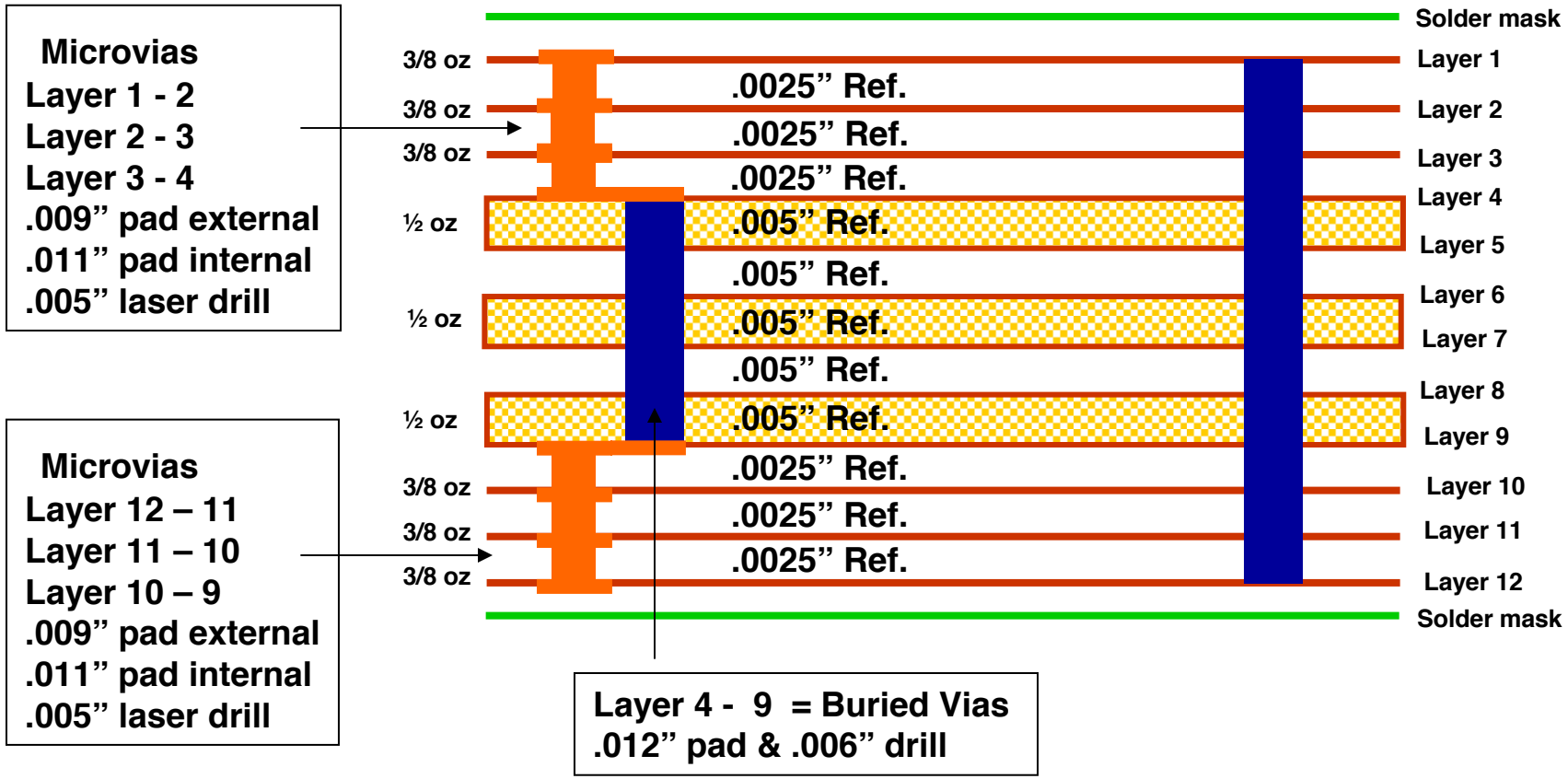
Buried Via
Layer 4 - 5
.012” pad
.006” mech drill
Solid cu plate
or laser drill
Solid cu plate

Finish Thickness = .038” +/- .004”
Material = High Temperature FR4

TD Technology

Stacked MicroVia (SMV™)

0.4 mm BGA 515 I/O



Finish Thickness = .062" +/- .006"
Material = High Temperature FR4 175° C Tg

TD Technology

Stacked MicroVia (SMV™)

0.3 mm BGA

Design Guidelines

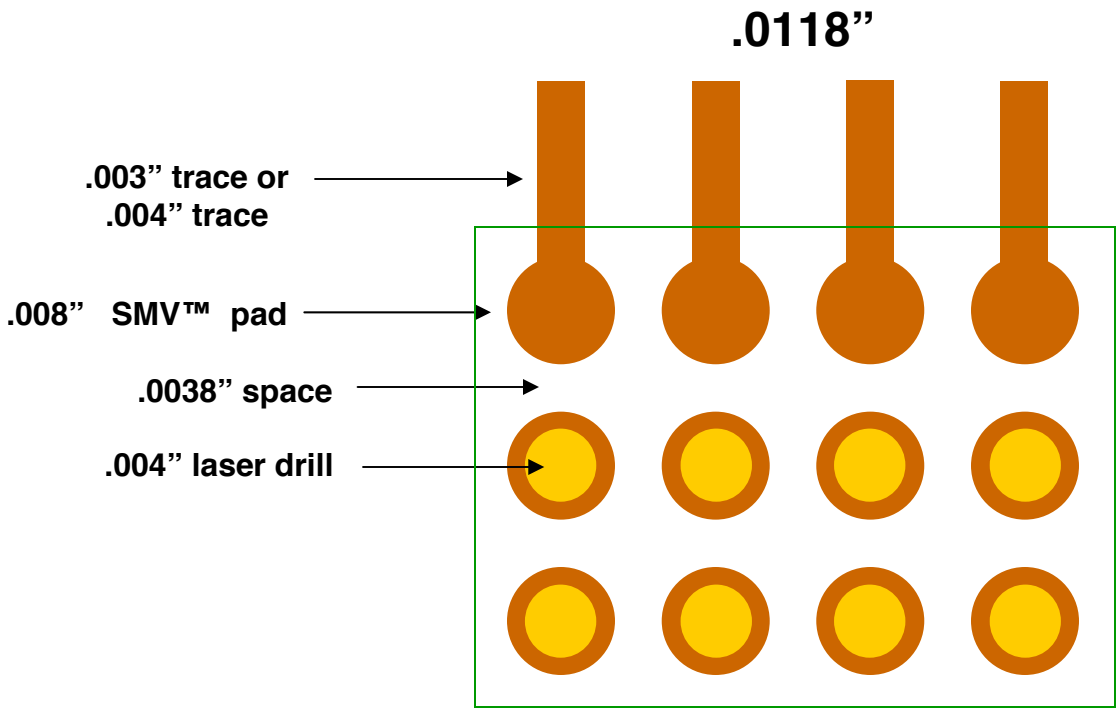
IPC 6011 / 6012

Class 2

TD Technology

Stacked MicroVia (SMV™)

0.3 mm Flip Chip

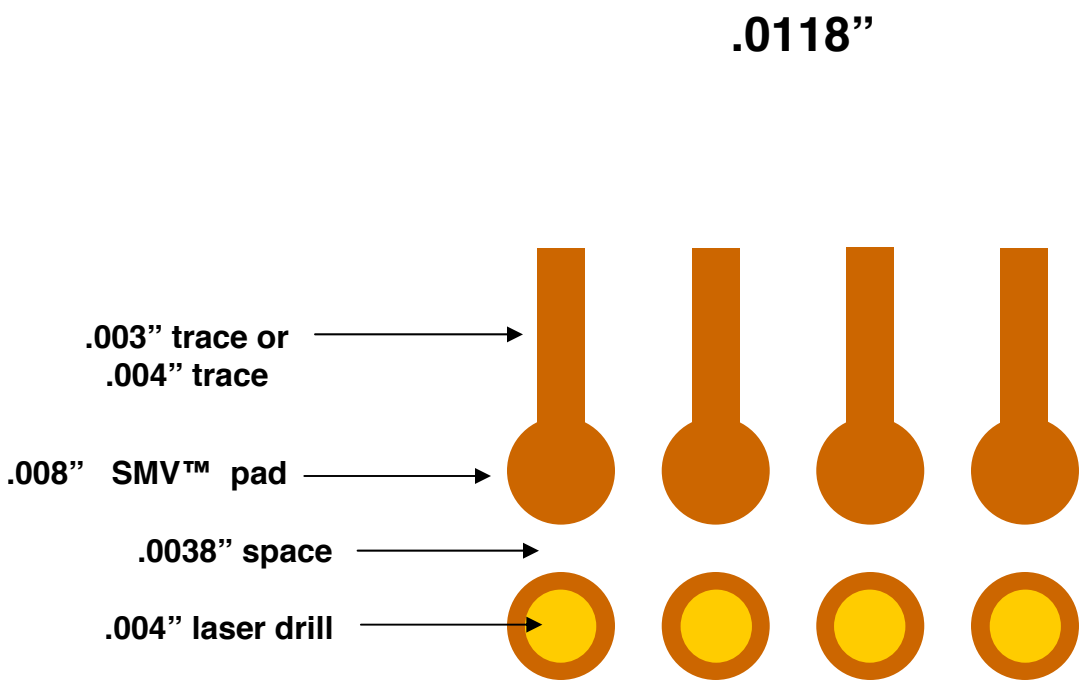


External Layer 1

TD Technology

Stacked MicroVia (SMV™)

0.3 mm Flip Chip



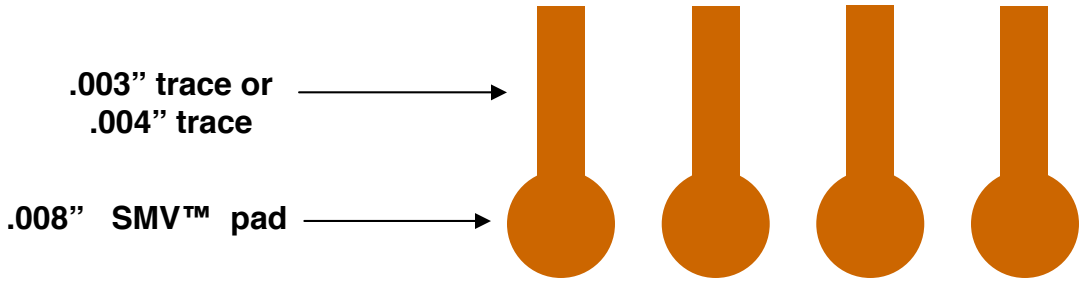
Internal Layer 2

TD Technology

Stacked MicroVia (SMV™)

0.3 mm Flip Chip

.0118”



Internal Layer 3

TD Technology

Stacked MicroVia (SMV™)

0.25 mm BGA

Design Guidelines

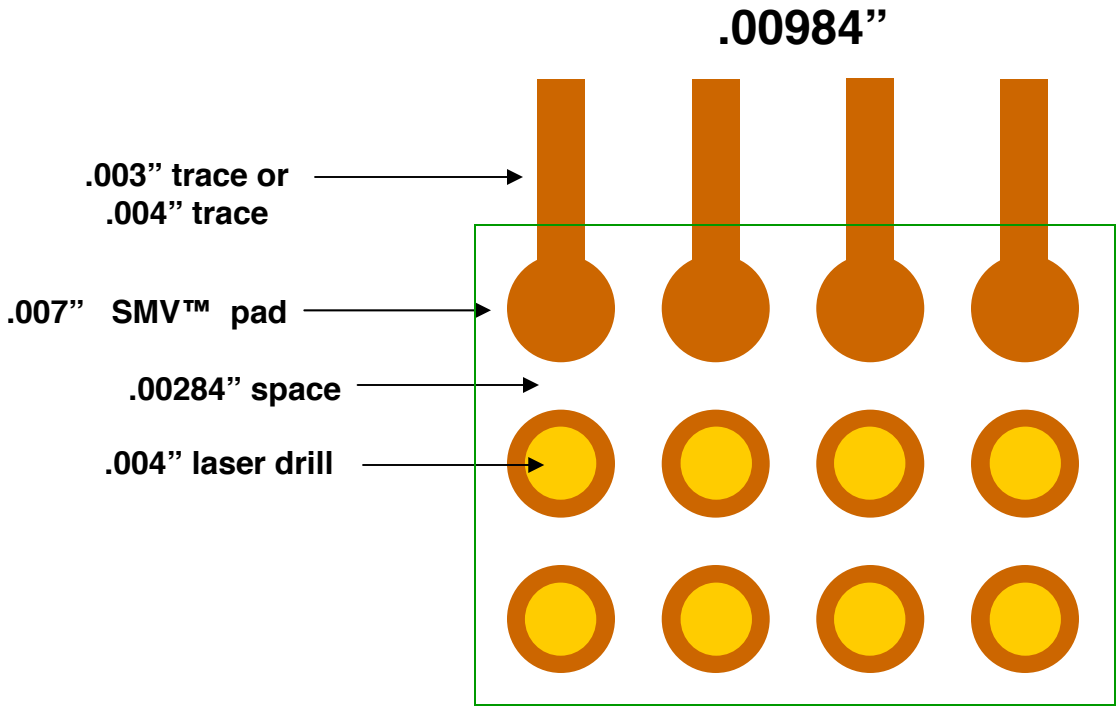
IPC 6011 / 6012

Class 2

TD Technology

Stacked MicroVia (SMV™)

0.25 mm Flip Chip

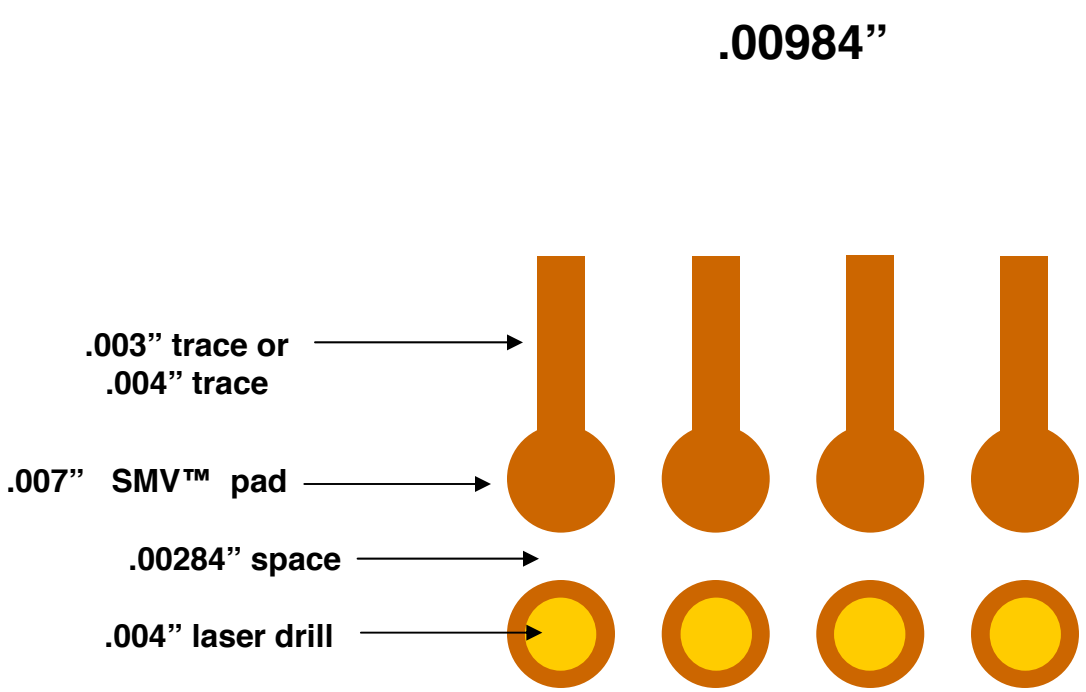


External Layer 1

TD Technology

Stacked MicroVia (SMV™)

0.25 mm Flip Chip



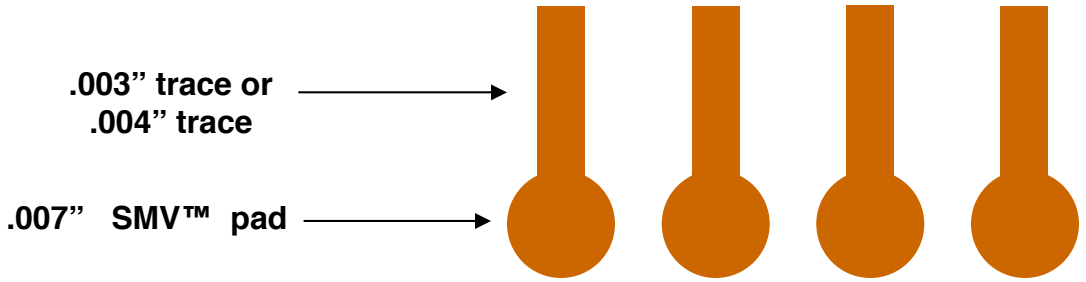
Internal Layer 2

TD Technology

Stacked MicroVia (SMV™)

0.25 mm Flip Chip

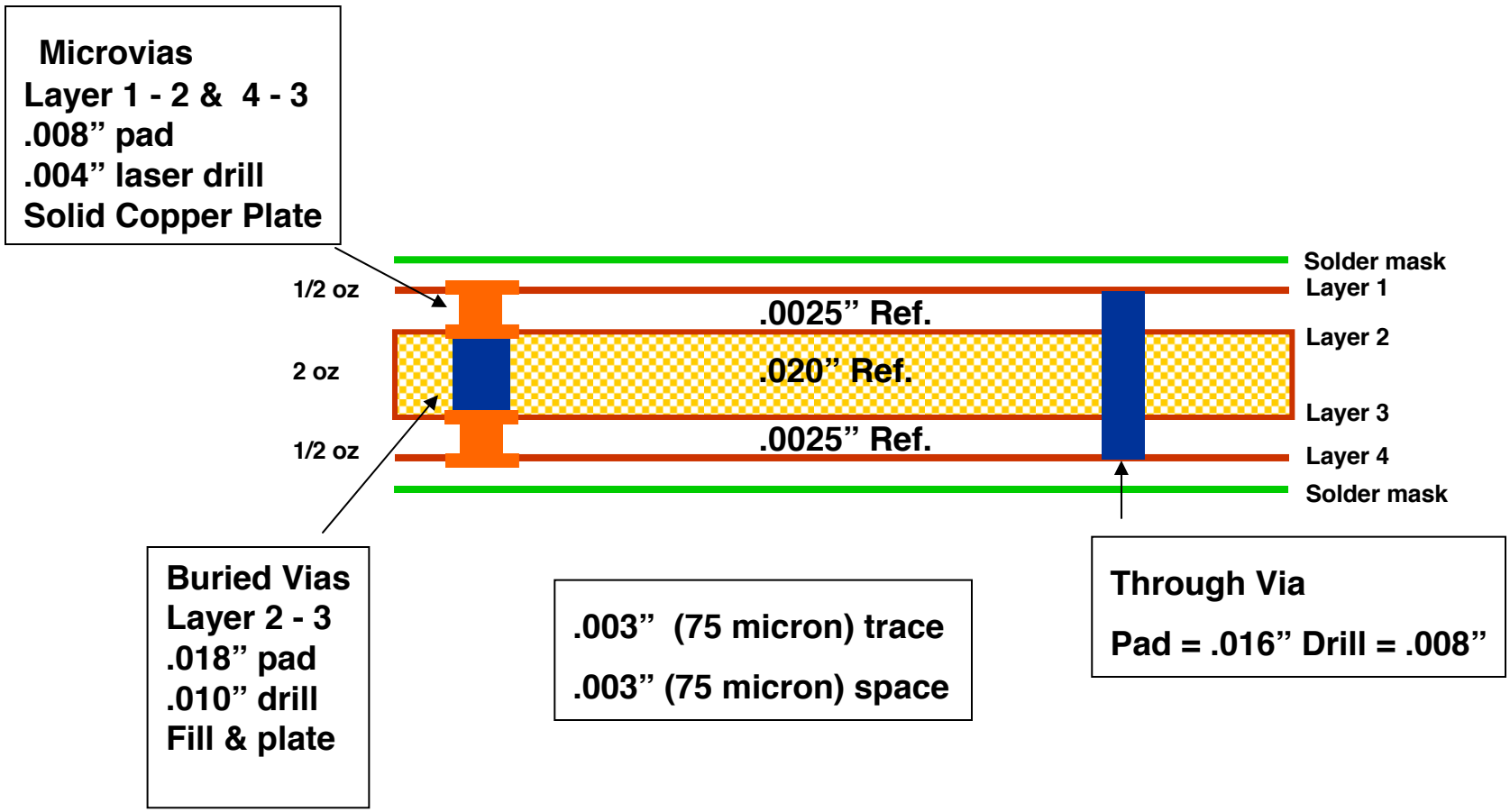
.00984”



Internal Layer 3

TD Technology

Stacked MicroVia (SMV™)



Finish Thickness = .022" +/- .002"
Material = High Performance FR4 210° C Tg

TD Technology

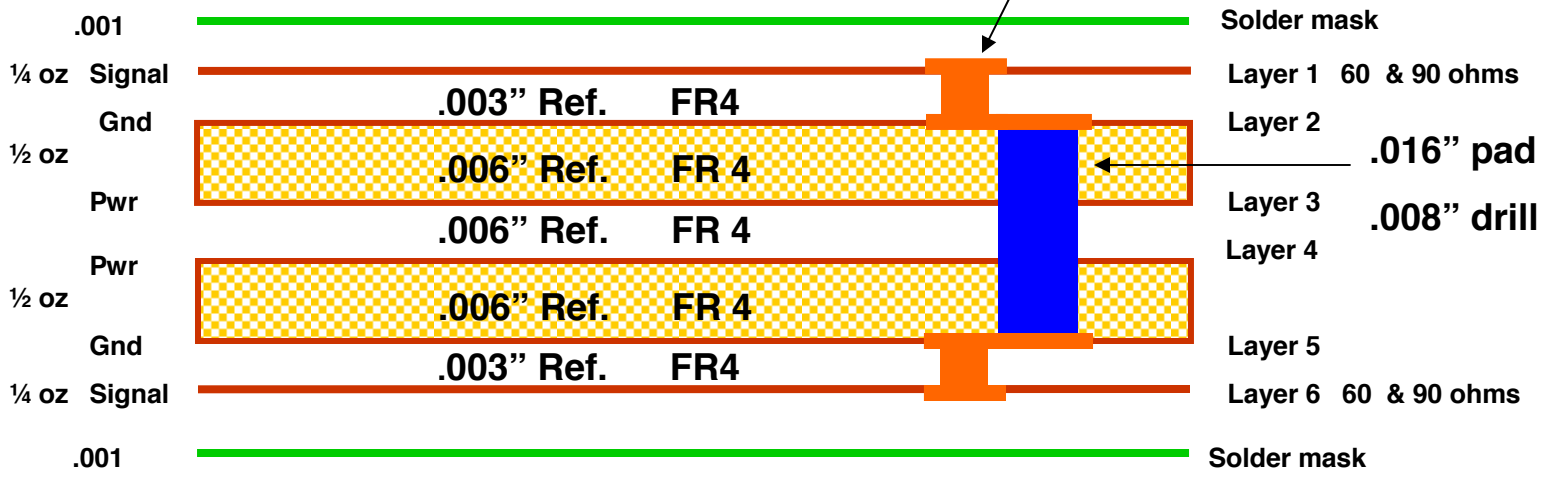
Stacked MicroVia (SMV™)

Finish Thickness = .032" +/- .003"

.004" Laser drilled Microvias

0.75:1 aspect ratio

.010" Pad, L2 & 5 .008" Pad



Coated Microstrip Impedance
3 mil Trace = 60 ohms
Layers 1 & 6
Coated Edge-Coupled Microstrip
3 mil trace & 3 mil space = 90 ohms

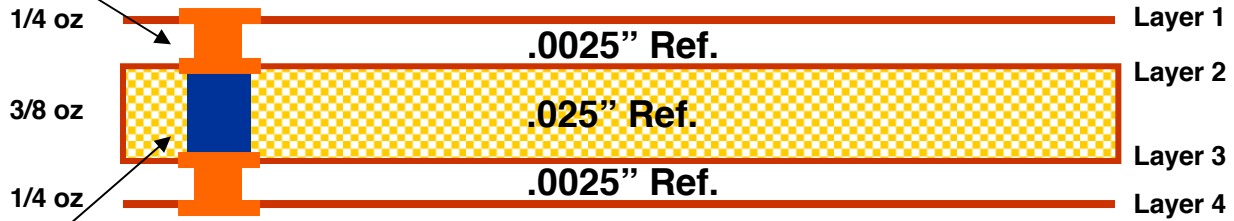
TD Technology

Stacked MicroVia (SMV™)

Microvias
Layer 1 - 2 & 4 - 3
.007" pad
.004" laser drill
Solid Copper Plate

.010" (250 micron) pitch

.007" (175 micron) pad & .003" (75 micron space)



Buried Vias
Layer 2 - 3
.018" pad
.010" drill
Fill & Plate

Electroless Nickel Immersion Gold (ENIG)

Layers 1 & 4 (Laser Direct Image LDI)

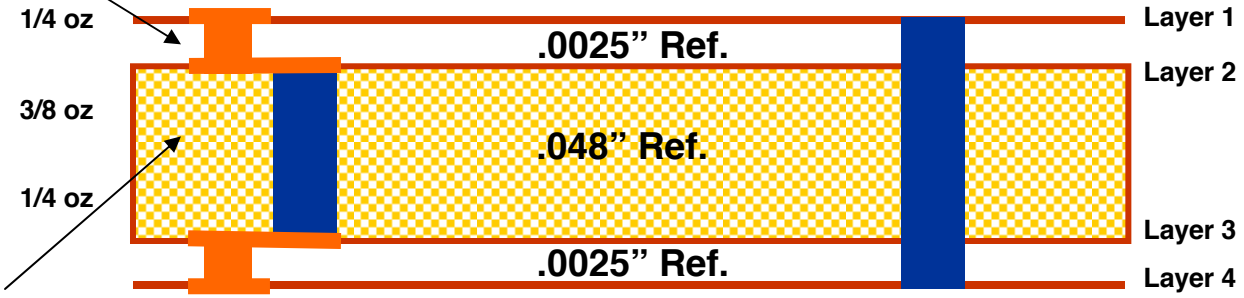
Layers 2 & 3 = .008" drill-to-copper

Finish Thickness = .039" +/- .002"
Material = High Performance FR4 210° C Tg

TD Technology

Stacked MicroVia (SMV™)

Microvias
Layer 1 - 2 & 4 - 3
.010” pad
.004” laser drill
Solid Copper Plate



Buried Vias
Layer 2 - 3
.016” pad
.008” drill

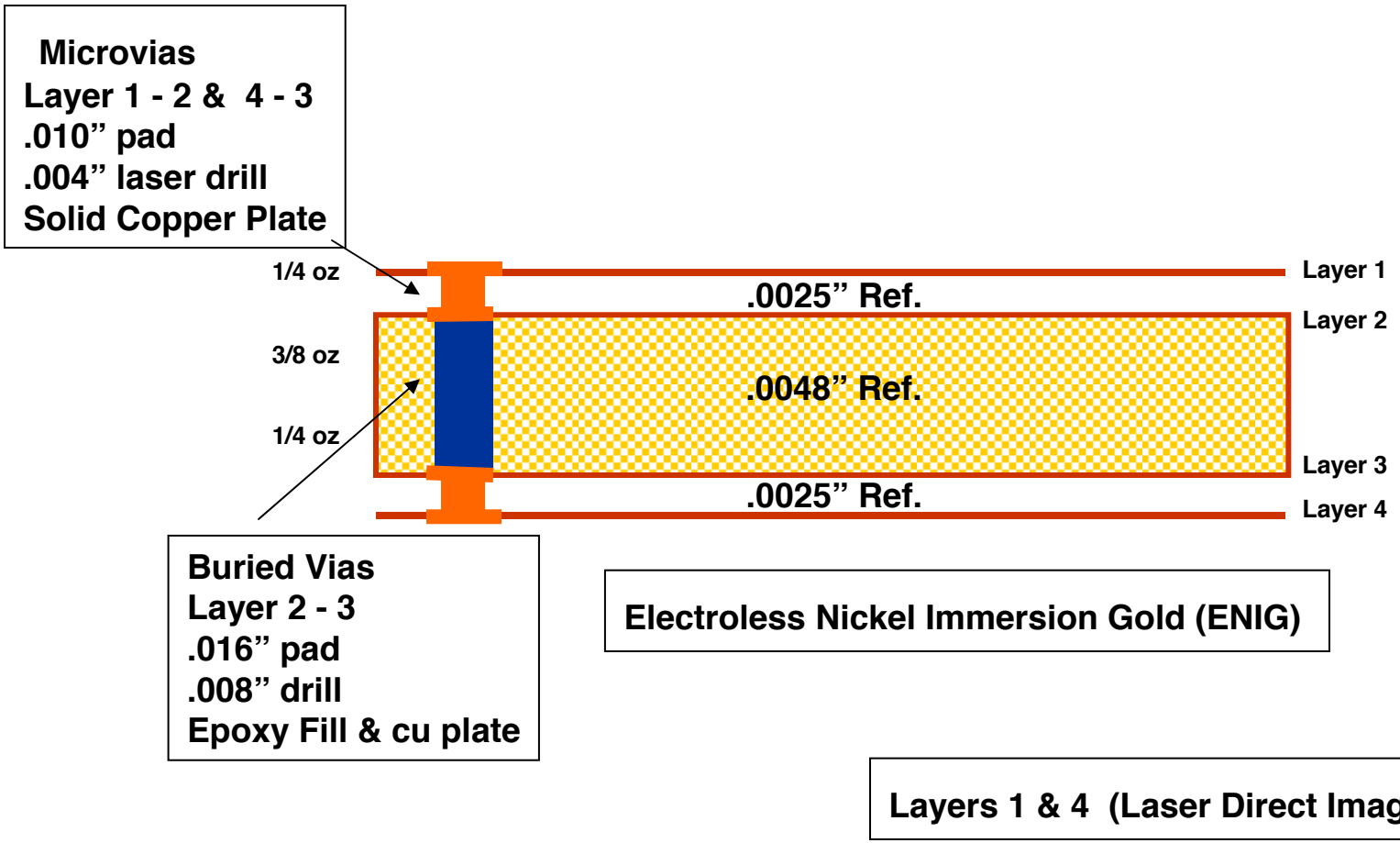
Electroless Nickel Immersion Gold (ENIG)

Layers 1 & 4 (Laser Direct Image LDI)

Finish Thickness = .062” +/- .006”
Material = High Performance FR4 210° C Tg

TD Technology

Stacked MicroVia (SMV™)

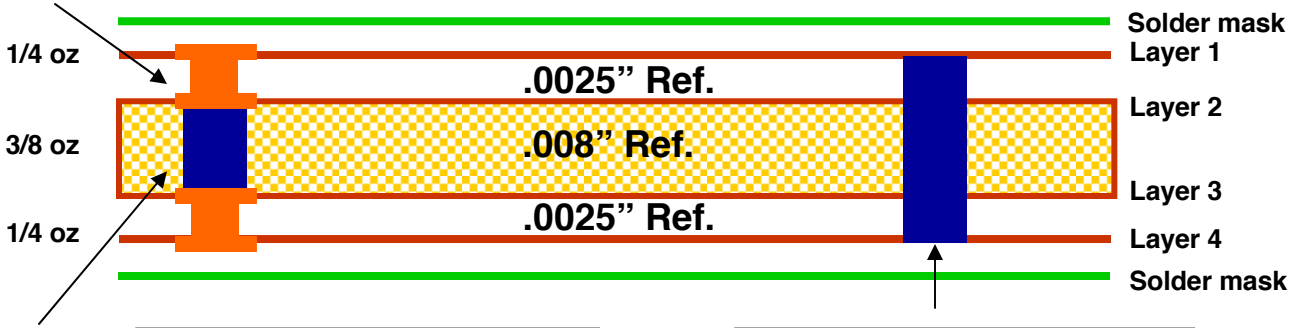


Finish Thickness = .062" +/- .006"
Material = High Performance FR4 210° C Tg

TD Technology

Stacked MicroVia (SMV™)

Microvias
Layer 1 - 2 & 4 - 3
.008" pad
.004" laser drill
Solid Copper Plate



Buried Vias
Layer 2 - 3
.018" pad
.010" drill
Fill & plate

.003" (75 micron) trace
.003" (75 micron) space

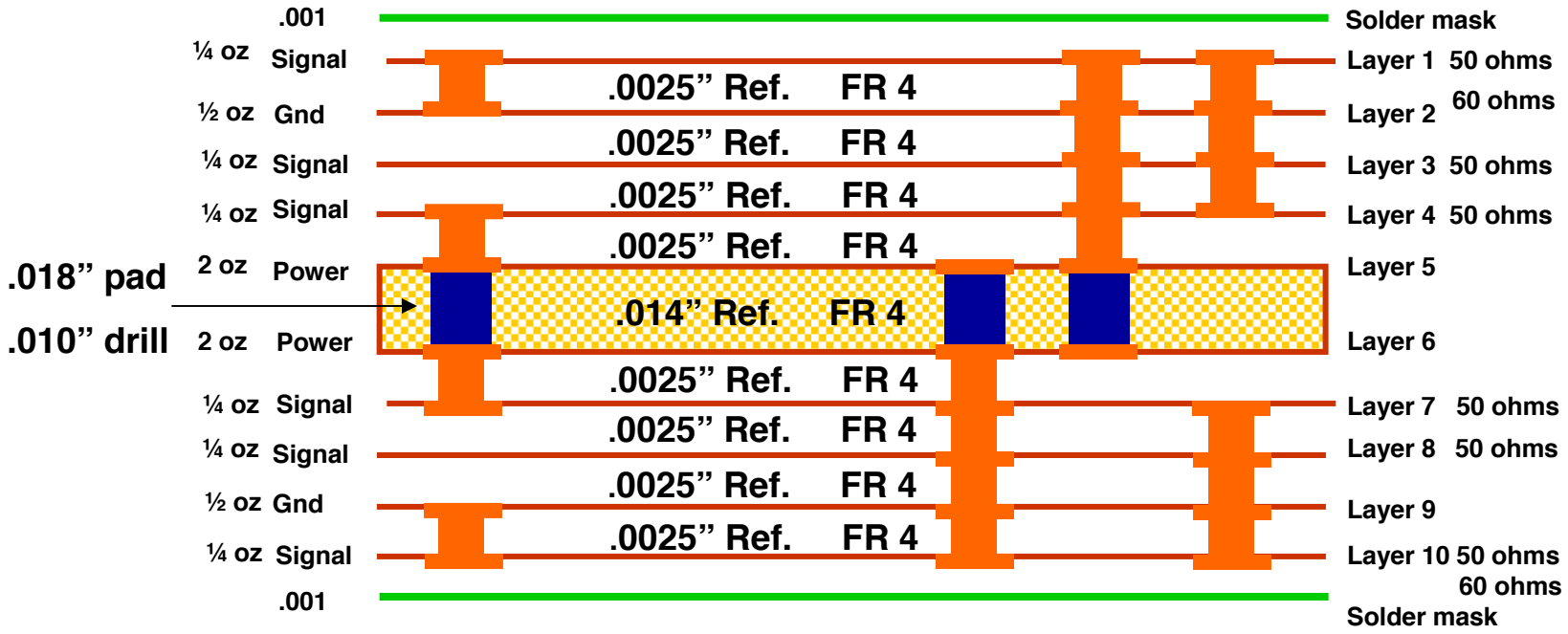
Through Via
Pad = .018" Drill = .008"

Finish Thickness = .022" +/- .002"
Material = High Performance FR4 210° C Tg

TD Technology

Stacked MicroVia (SMV™)

Stacked MicroVias
.008” Pad
.004” Laser Drill
0.625:1 Aspect Ratio
Solid Copper Plate



Dual Stripline .00275” trace = 50 ohms

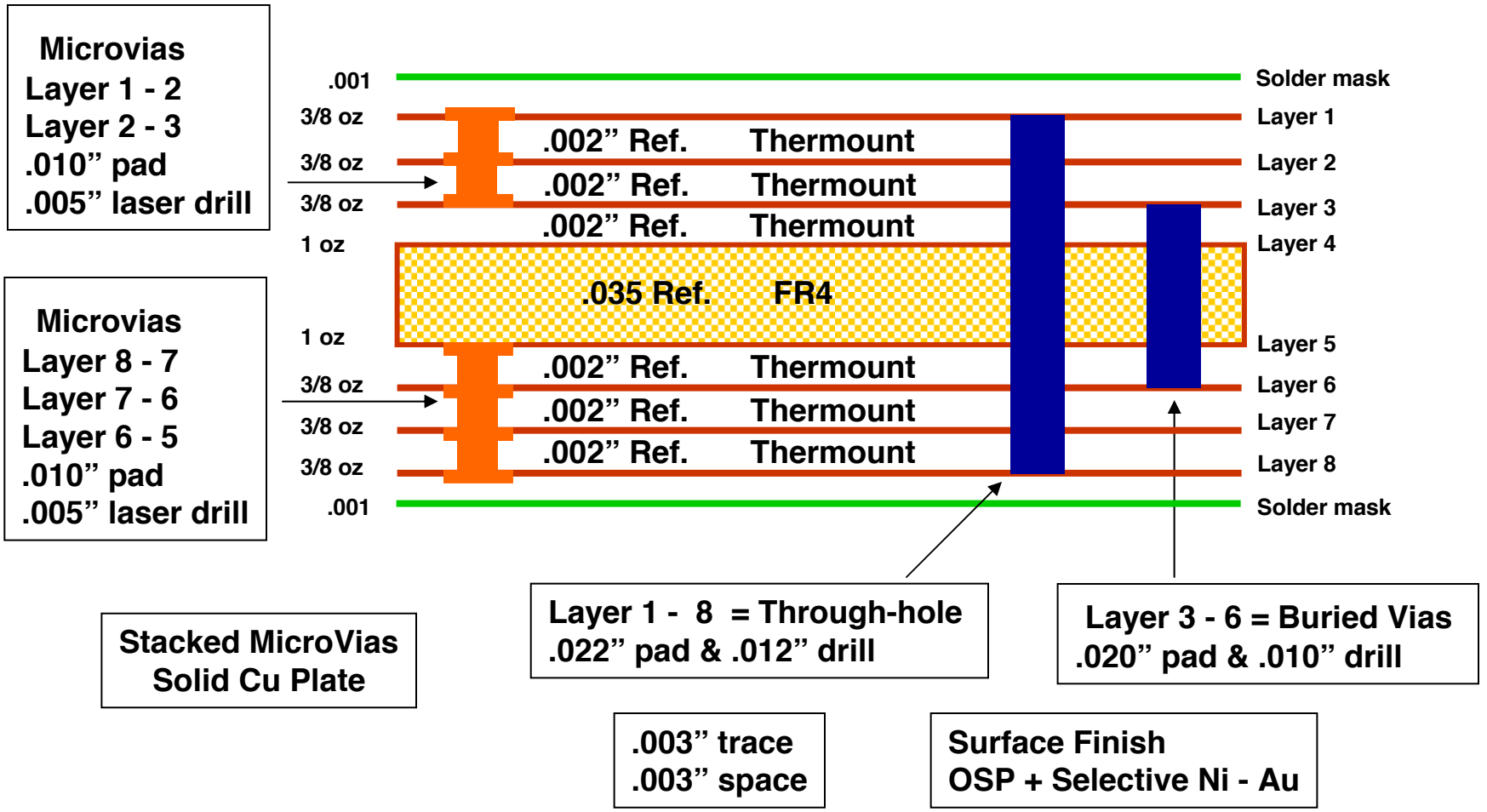
Coated Microstrip - .0025” trace = 60 ohms

.004” trace = 50 ohms

Finish Thickness = .050 +/- .005
Material = High Performance FR4 210° C Tg

TD Technology

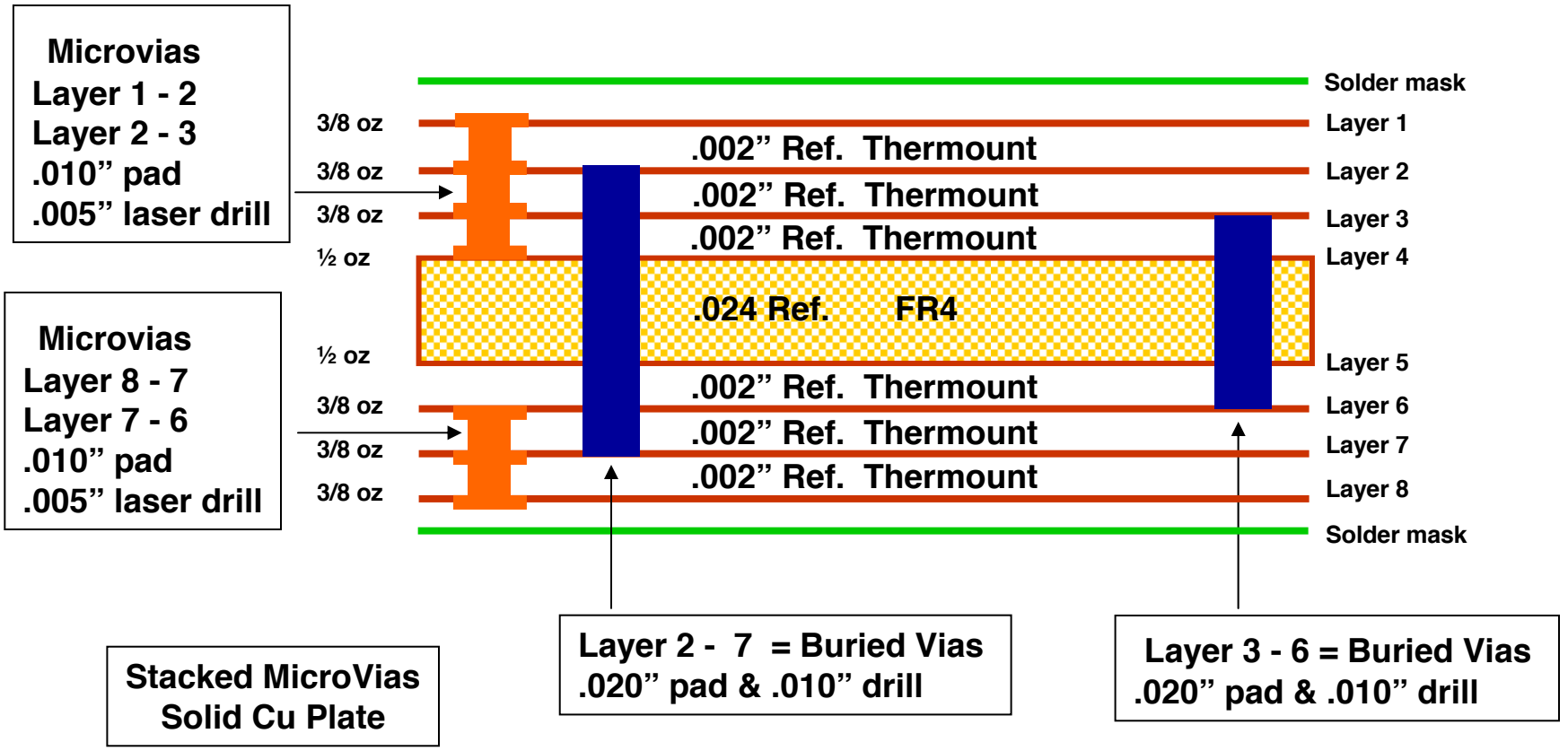
Stacked MicroVia (SMV™)



Finish Thickness = .062 +/- .006
Material = High Temperature FR4 175° C Tg

TD Technology

Stacked MicroVia (SMV™)

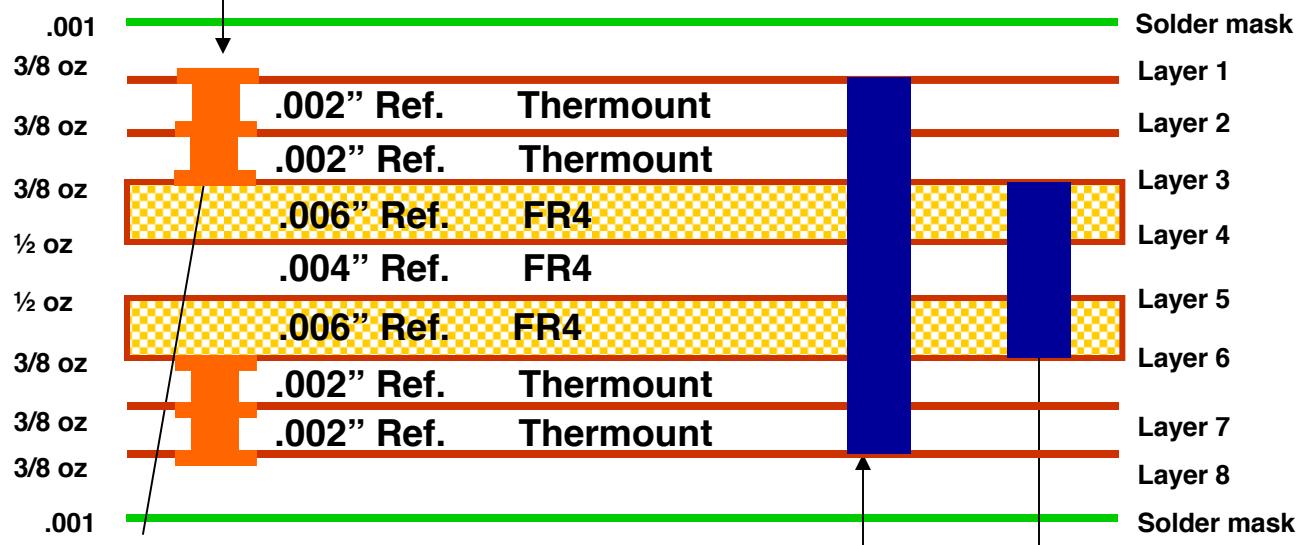


Finish Thickness = .048 +/- .004
Material = High Temperature FR4 175° C Tg
& Arlon 55ST Thermount

TD Technology

Stacked MicroVia (SMV™)

Layer 1 - 2 & 8-7 = SMV
L1 .010” pad & .004” laser drill



Layer 2 – 3 & 6 - 7 = SMV
.010” pad & .004” laser drill

Layer 1 - 8 = Through-hole
.022” pad & .012” drill

Layer 3 - 6 = Buried Vias
.022” pad & .010” drill

Stacked MicroVias
2-3 & 6-7
Solid Copper Plate

.003” trace
.003” space

Surface Finish
OSP + Selective Ni - Au

Finish Thickness = .038 +/- .004

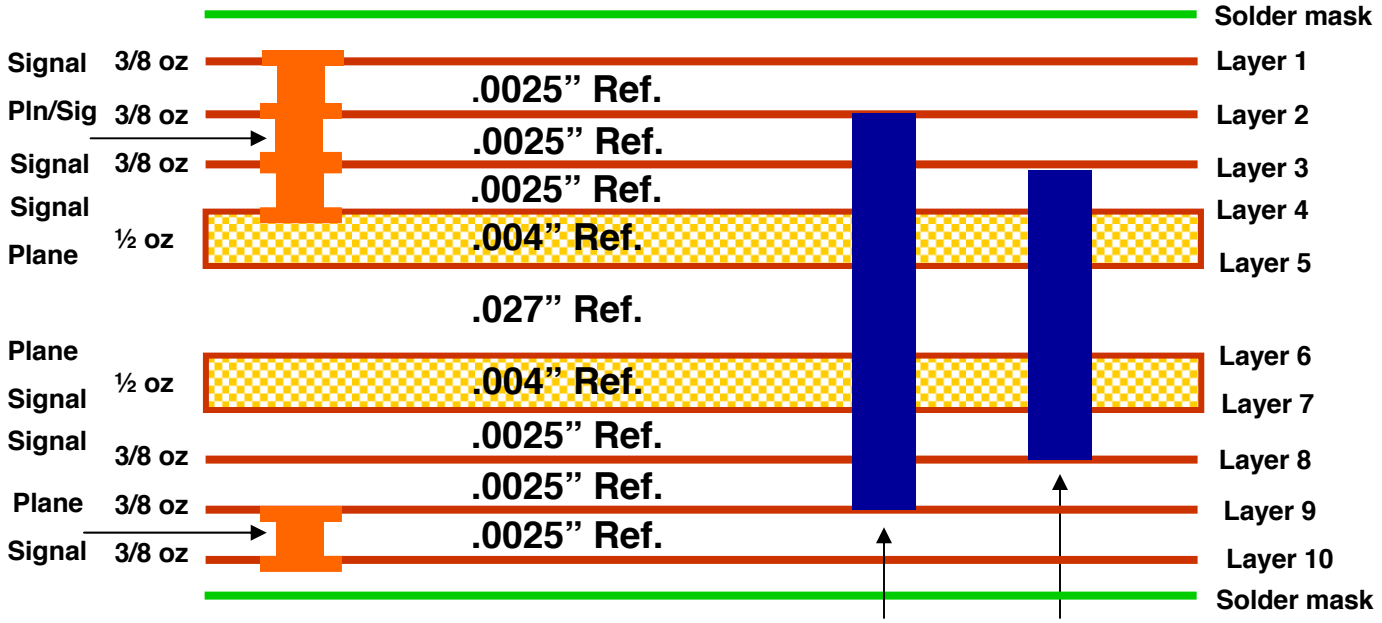
Buried via holes to be filled with non-conductive epoxy

TD Technology

Stacked MicroVia (SMV™)

Microvias
Layer 1 - 2
Layer 2 - 3
Layer 3 - 4
.010” pad
.004” laser drill

Microvias
Layer 10 - 9
.010” pad
.004” laser drill



Stacked MicroVias
Solid Cu Plate

Layer 2 - 9 = Buried Via
.018” pad & .008” drill

Layer 3 - 6 = Buried Vias
.018” pad & .008” drill

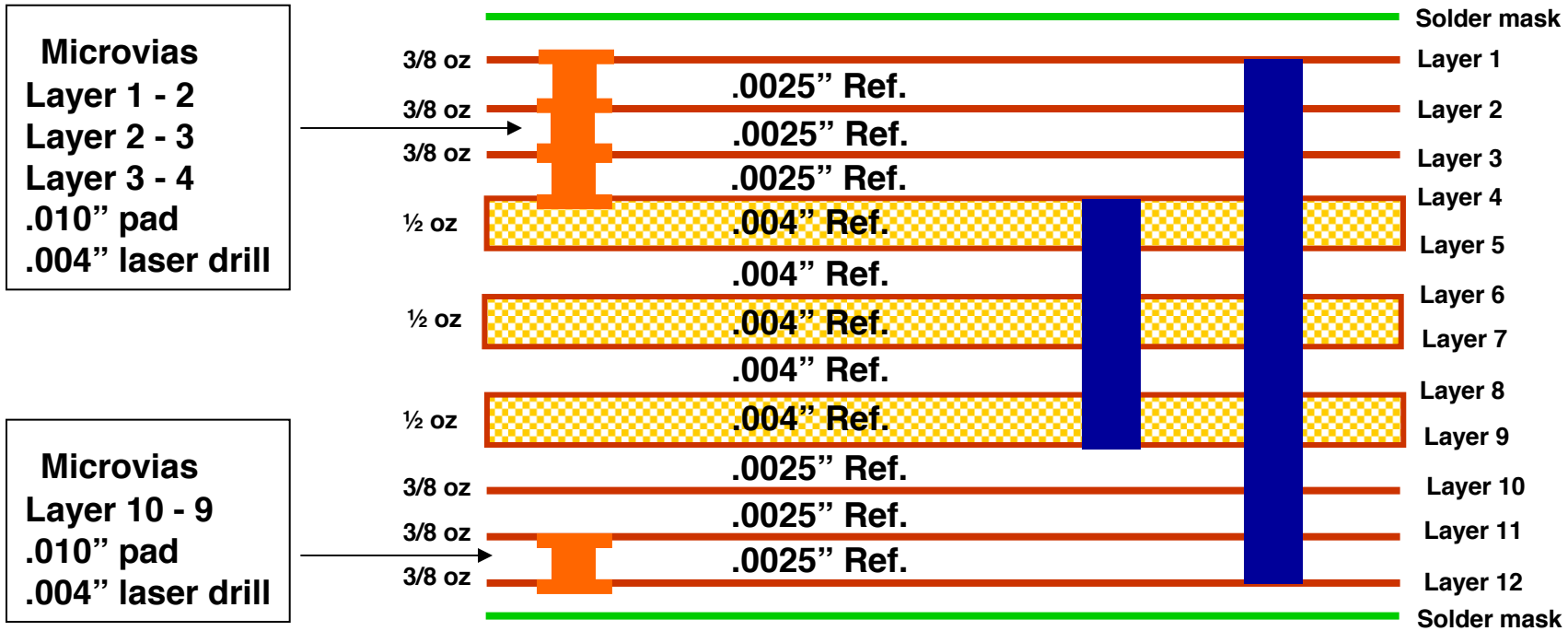
Coated Microstrip = .004” trace = 50 ohms
Coated Edge Coupled Microstrip = .0035” trace & .0045” space = 90 ohms

Single Stripline = .0045” trace = 50 ohms
Coated Edge Coupled Microstrip = .00425” trace & .00375” space = 90 ohms

Finish Thickness = .063 +/- .006
Material = High Temperature FR4 175° C Tg

TD Technology

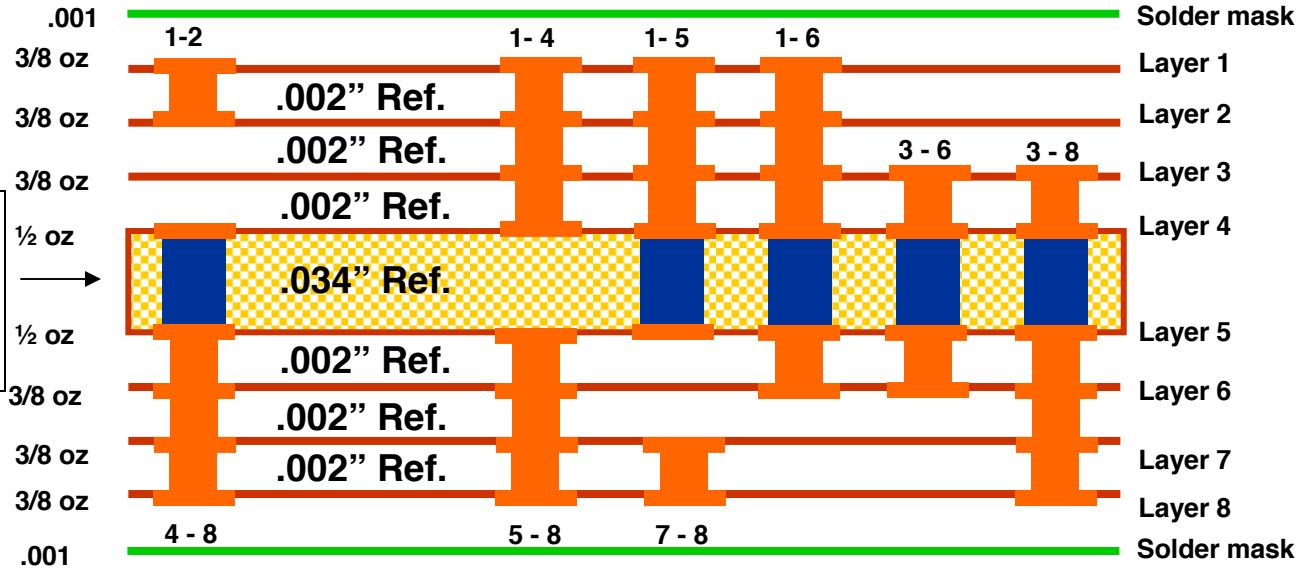
Stacked MicroVia (SMV™)



Finish Thickness = .063 +/- .006
Material = High Temperature FR4 175° C Tg

TD Technology

Stacked MicroVia (SMV™)



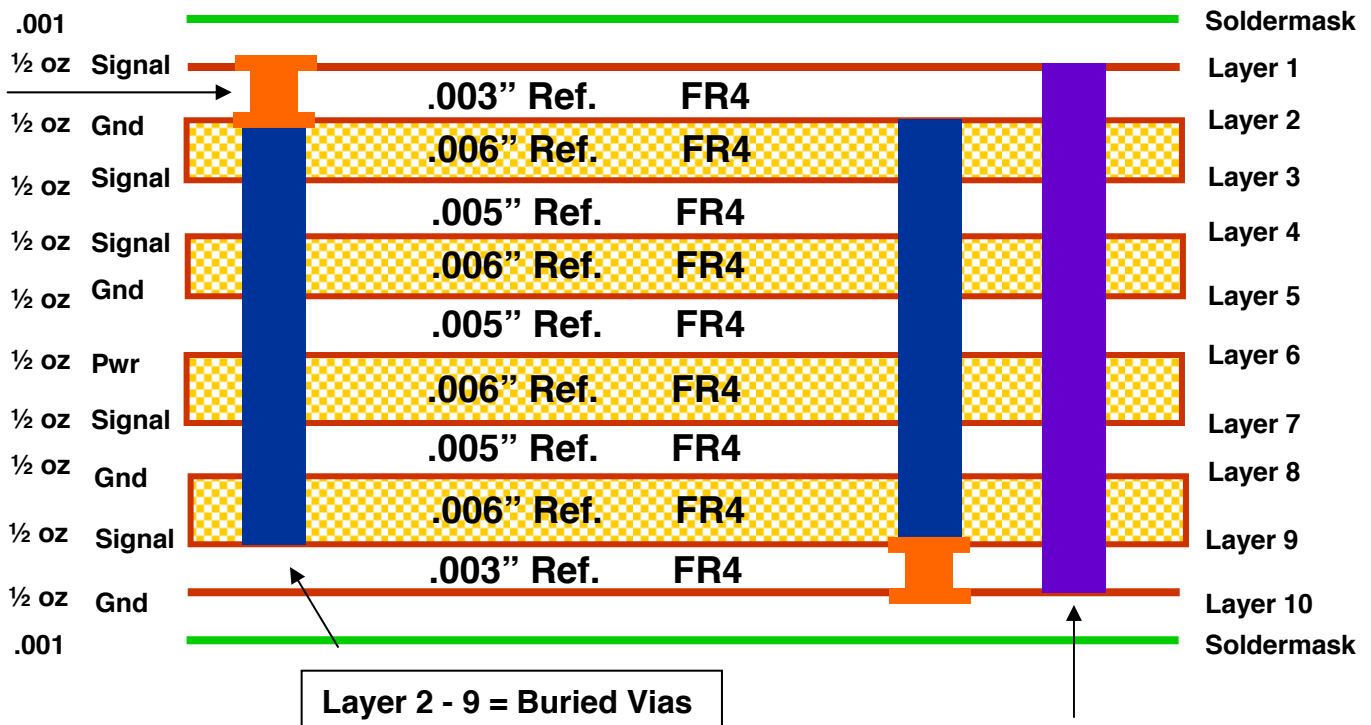
Layer 4 – 5 buried via
.016" pad & .008" drill
Conductive Fill
Planar & Plate

Stacked MicroVias
Laser drilled .004"
.008" pad
Solid Cu Plate

Finish Thickness = .062" +/- .005"
Material = High Temperature FR4 175° C Tg

TD Technology

Stacked MicroVia (SMV™)



Layer 1 - 2 & 9 – 10
Stacked MicroVias
L1 & 10 = .010" pad
.006" laser drill

Layer 2 - 9 = Buried Vias
.020" pad & .010" drill
Non-Conductive Via Fill

Layer 1 - 10 through Vias
.020" pad & .010" drill

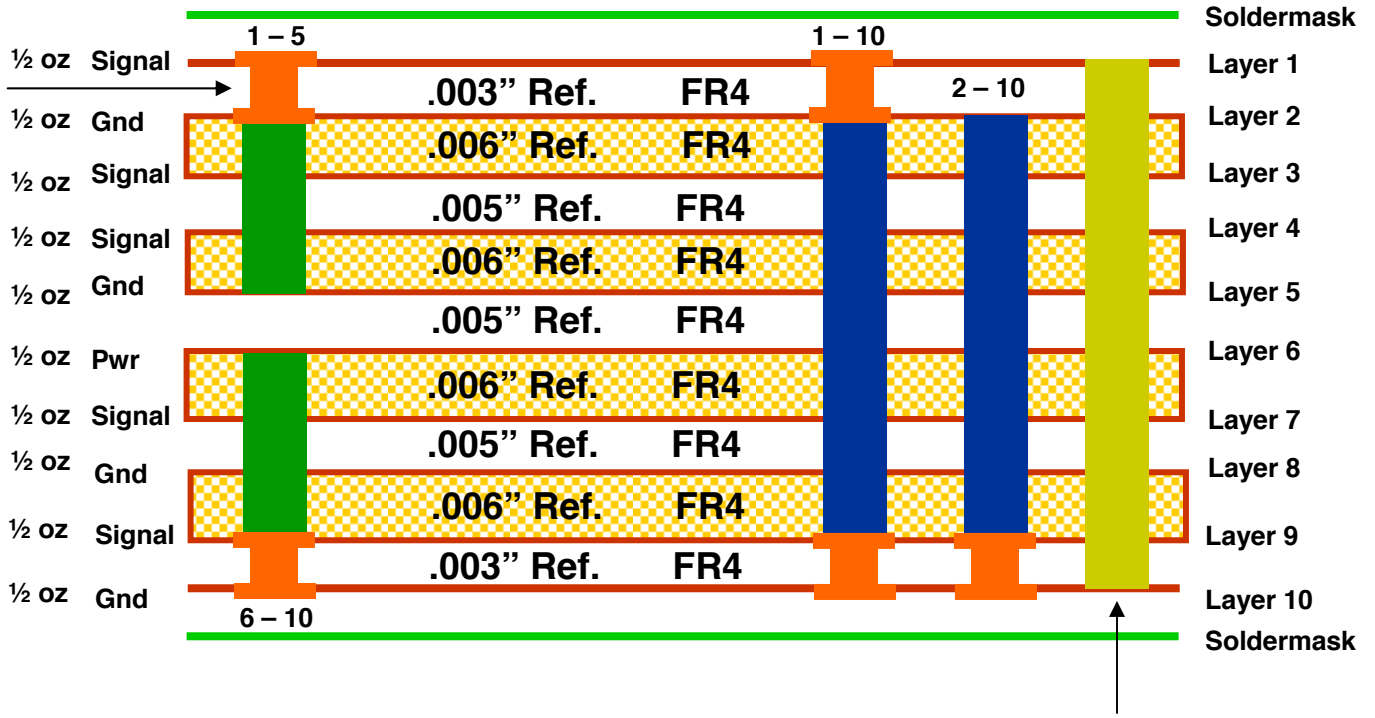
Layer 1 & 2 - 9 & 10
3/8 oz copper if trace and space <.004"

Finish Thickness = .060" +/- .006"
Material = Hi Performance FR4, 210° C Tg

TD Technology

Stacked MicroVia (SMV™)

Layer 1 - 2 & 9 – 10
SMV™
.010” pad
.004” laser drill
Solid Cu Plate



Layer 1 - 10 NPH

Layer 2 – 5 & 6 – 9
Buried Vias
.020” pad & .010” drill
Non-Conductive Via Fill

Layer 2 - 9 = Buried Vias
.020” pad & .010” drill
Non-Conductive Via Fill

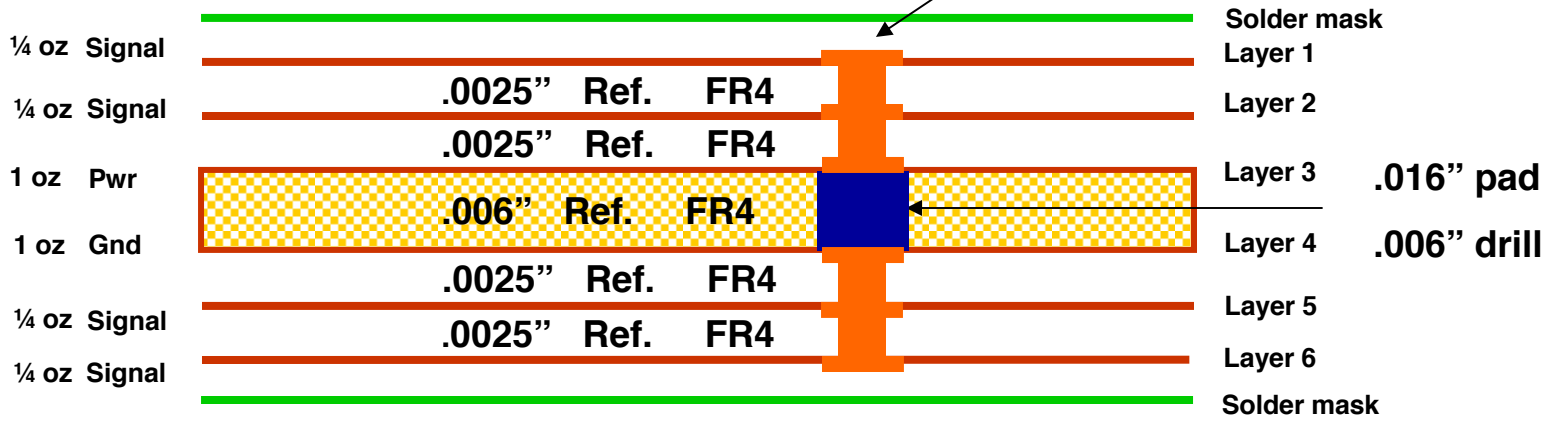
Finish Thickness = .060” +/- .006”
Material = Nelco N4000-13 210° C Tg

TD Technology

Stacked MicroVia (SMV™)

Stacked MicroVia Technology
Solid Cu Plate
.002” trace & space
Laser Direct Image (LDI)

.004” Laser drill
Solid Cu Plate
0.6:1 aspect ratio
L1 = .008” Pad
L2 & 5 = .010” Pad



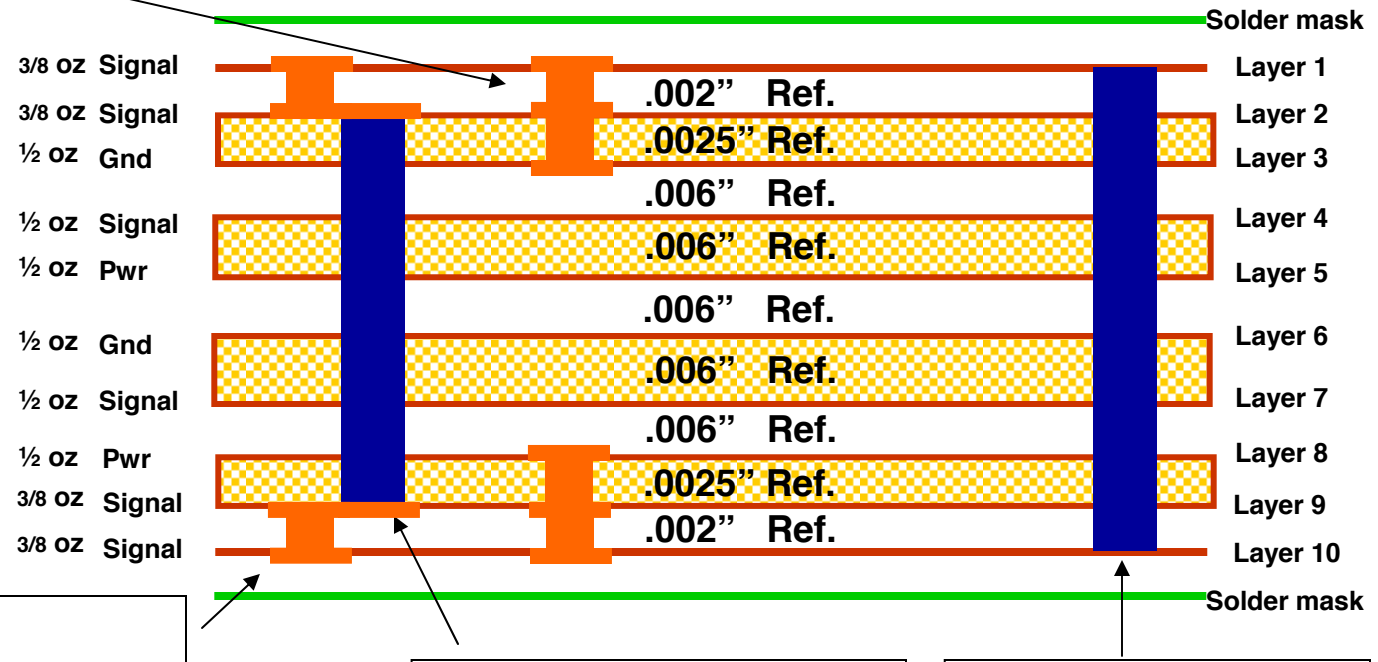
Solder mask clearance for Flip Chip Area .001”/side
Utilize Laser Direct Image (LDI) Solder mask

Finish Thickness = .032” +/- .003”
Material = High Performance FR4 Tg 210° C

TD Technology

Stacked MicroVia (SMV™)

Layer 1 – 2 – 3
Layer 10 – 9 - 8
Laser drill SMV
.008” pad
.004” laser drill
Solid Copper Plate



Layer 1 - 2 & 9 - 10
Laser drill SMV
Layer 1 & 10 .010” pad .004” drill
Solid Copper Plate

Layer 2 - 9 = Buried Vias
.018” pad & .008” drill

Layer 1 - 10
.018” pad & .008” drill

Layer 10 = Coated Microstrip
using Layer 6 reference planes
.038” trace = 50 ohms

Layer 4 = Stripline
.004” trace = 60 ohms

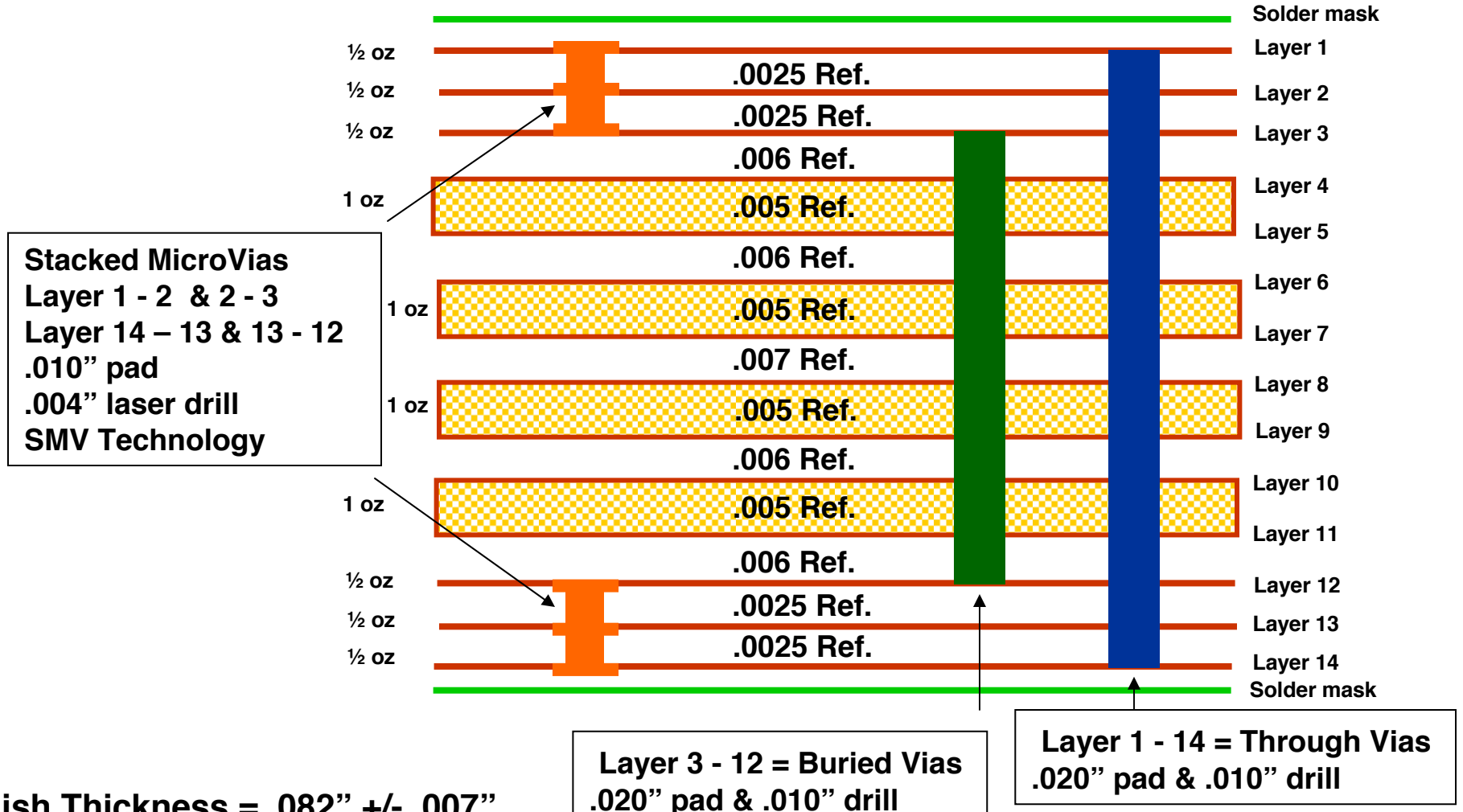
Layer 1 & 10 = Coated Microstrip
using Layer 3 & 8 reference planes
.0105” trace = 50 ohms

Finish Thickness = .050” +/- .005”
Material = High Performance FR4 210° C Tg

Layer 4 = Edge-Coupled Stripline
.0045” trace & .0055” space = 100 ohms

TD Technology

Stacked MicroVia (SMV™)



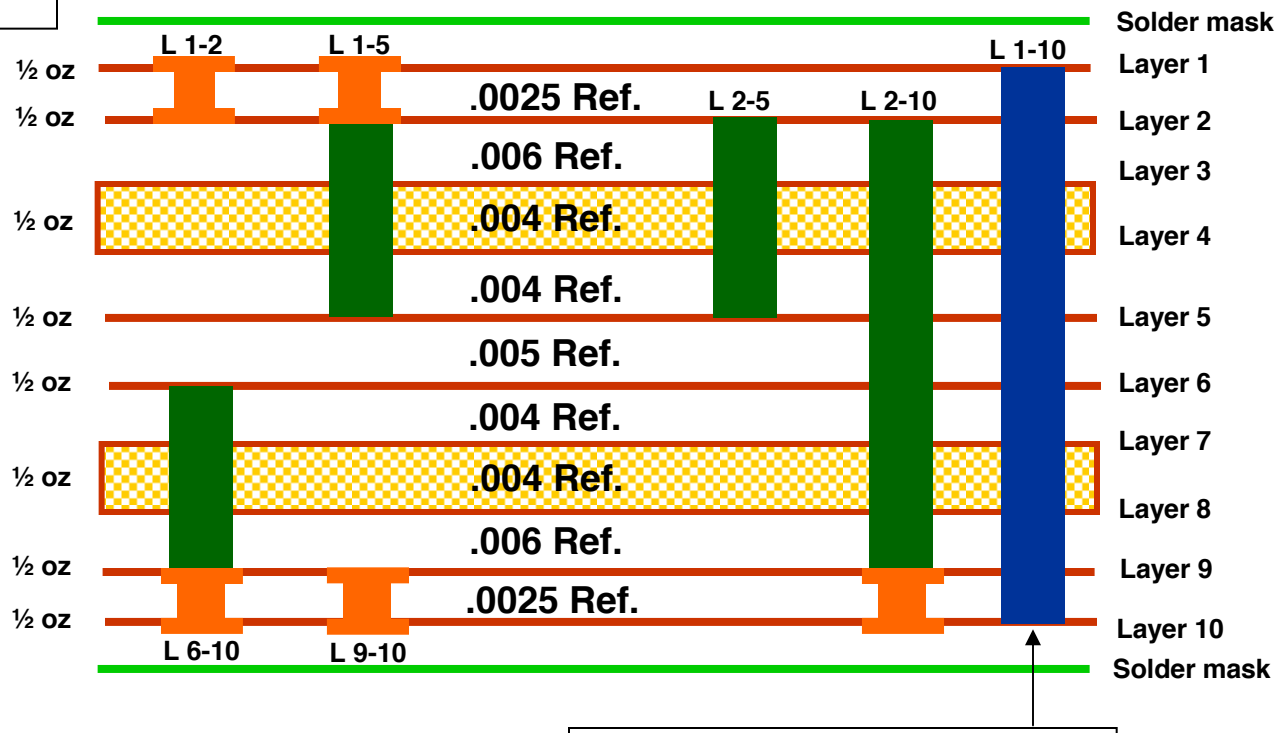
Finish Thickness = .082” +/- .007”
Material = High Temp FR4 175°C Tg

TD Technology

Stacked MicroVia (SMV™)

SMV Technology
Layer 1 - 2 & 9 - 10
.010” pad
.004” laser drill
Solid Copper Plate

Blind Vias
Layers 2 – 5
Layers 6 – 9
Layers 2 - 9
.020” pad & .010” drill
Non-Conductive Epoxy Fill



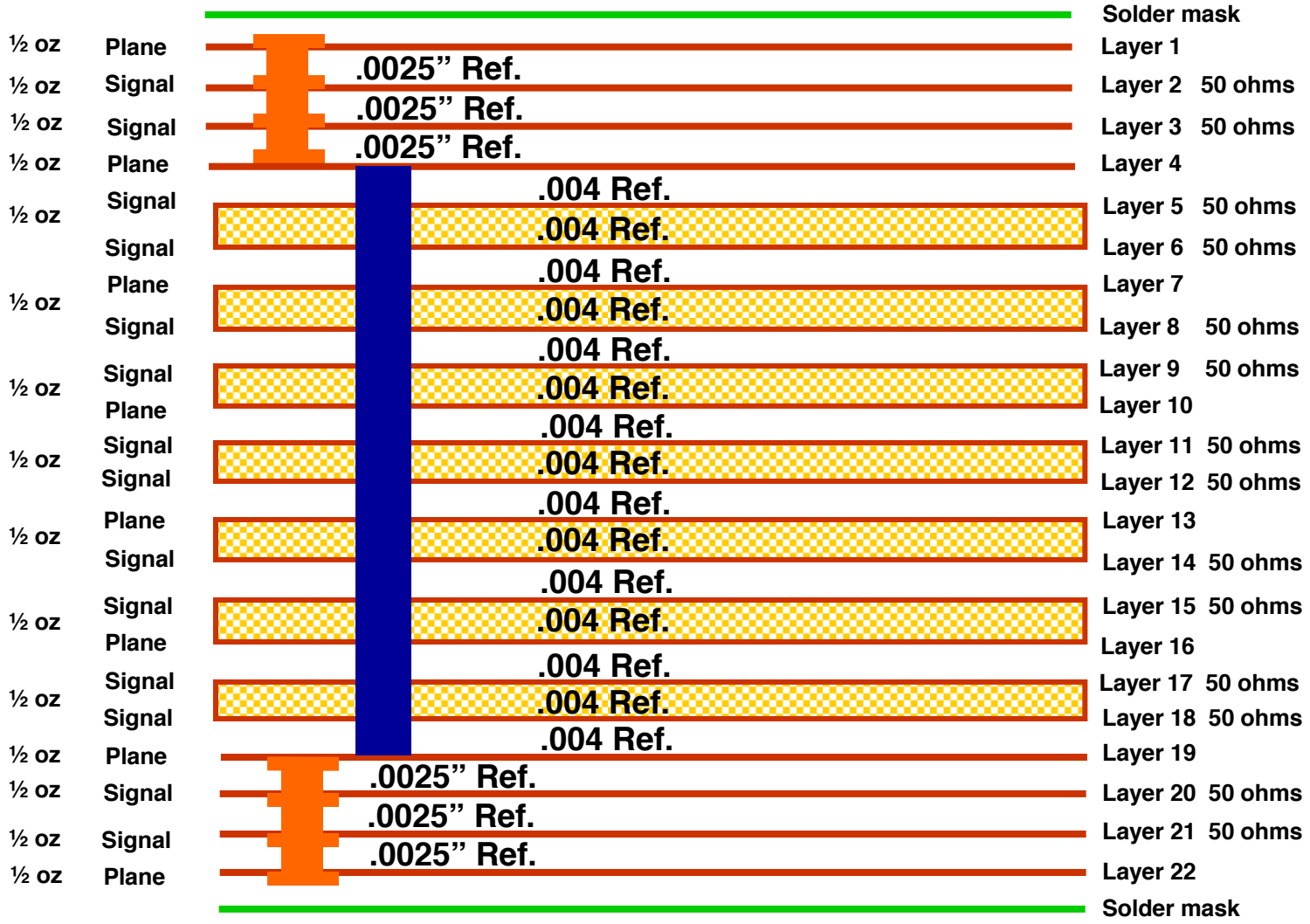
Layer 1 - 10 = Through Vias
.020” pad & .010” drill

Finish Thickness = .047” +/- .004”
Material = High Performance FR4 210°C Tg

TD Technology

Stacked MicroVia (SMV™)

3 + 16 + 3

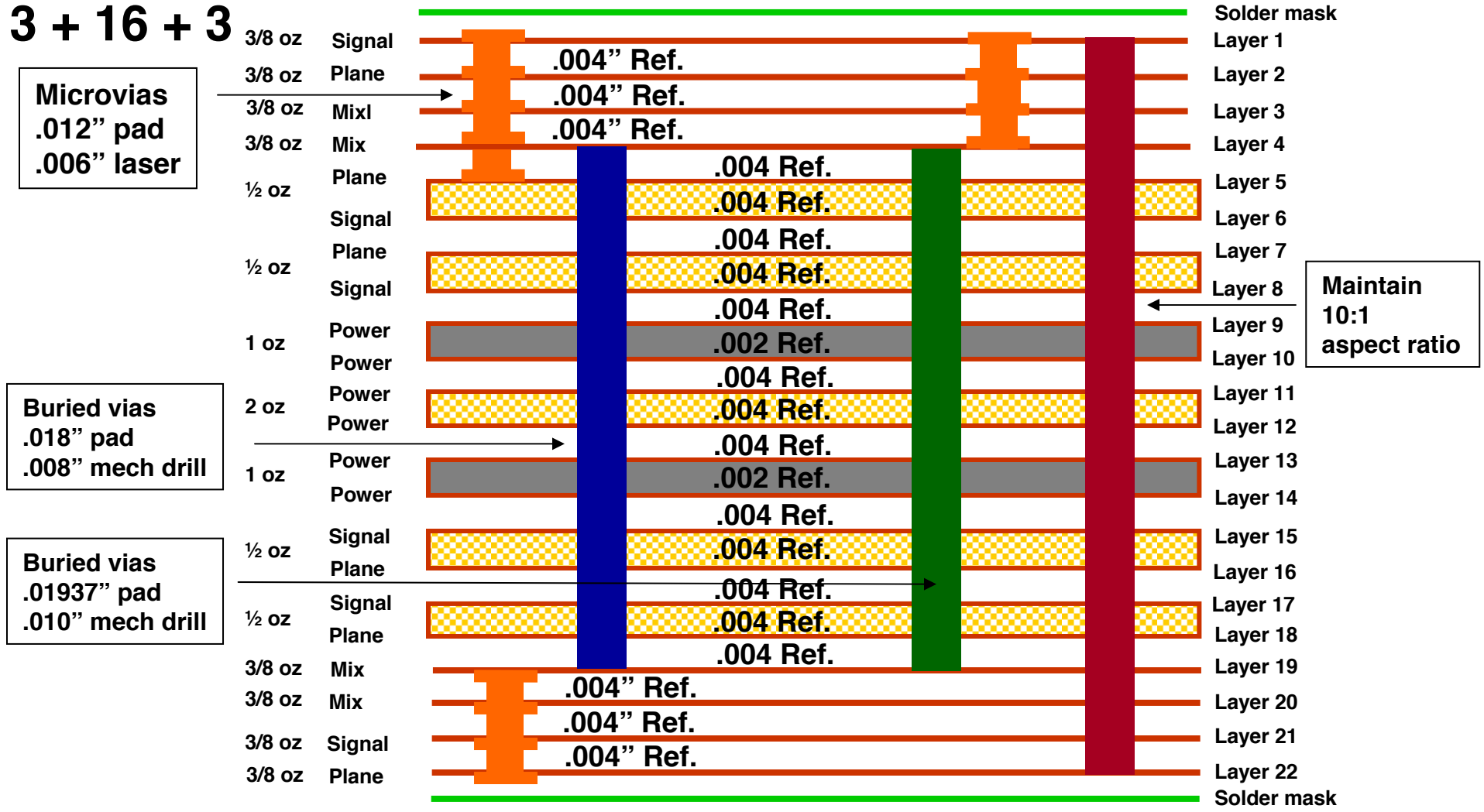


Finish Thickness = .105” +/- .010” Material = High Performance FR4 210° C Tg

TD Technology

Stacked MicroVia (SMV™)

3 + 16 + 3

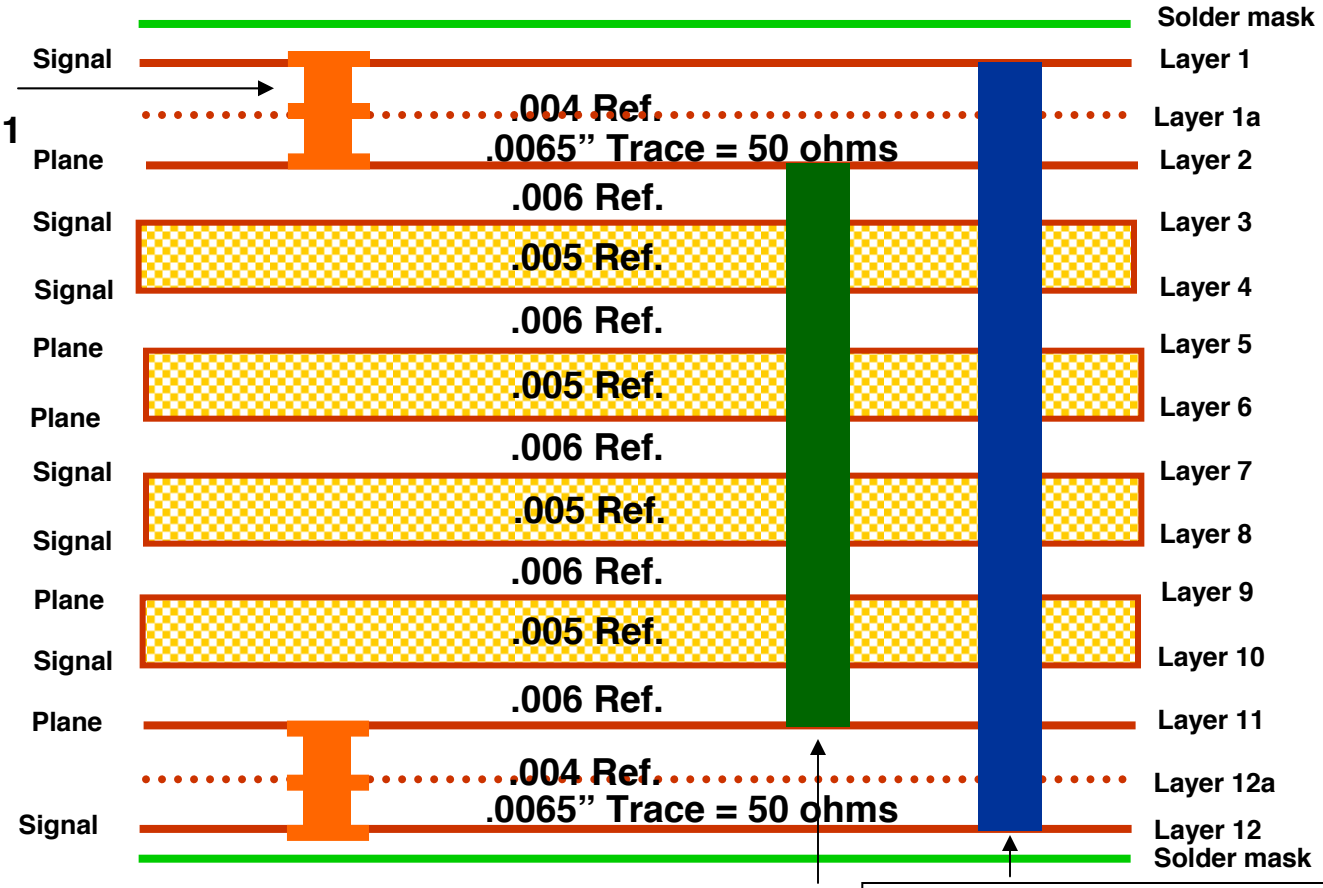


Finish Thickness = .000" +/- .000" Material = Nelco N4000-13i 210° Tg

TD Technology

Stacked MicroVia (SMV™)

SMV™
Layer 1 – 1a & 1a - 2
Layer 12 –12a ,12a - 11
.010” pad
.004” laser drill
SMV™ Technology



Layer 2 - 11 = Buried Vias
.020” pad & .010” drill

Layer 1 - 12 = Through Vias
.020” pad & .010” drill

Finish Thickness = .082” +/- .007”
Material = High Temp FR4 175°C Tg

TD SMV™ Technology

SMV™ Technology Provides Solutions for Next Generation Products

TD Technology

Microvia Technology Part II

- Review of Microvia Configurations or Types
- Discuss Advantages & Disadvantages
- Describe Evolution of Microvia Technology
- Introduce Next Generation Microvias

TD Technology

Microvia Types (IPC-2226 HDI Printed Boards)

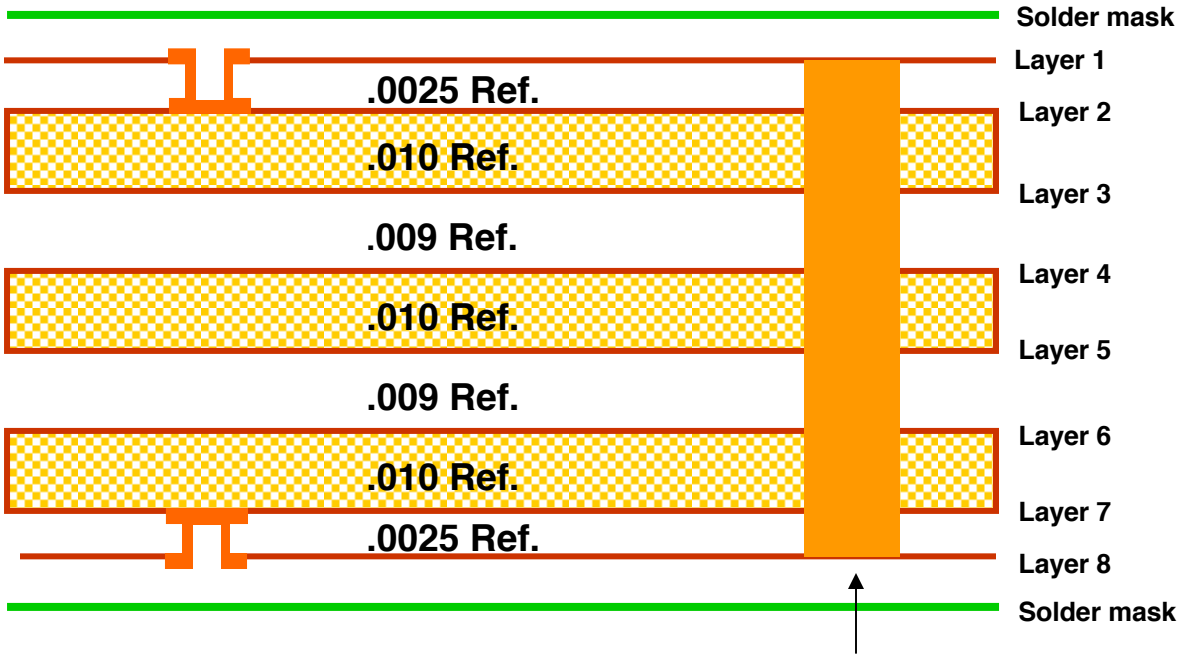
- ***Type I – standard microvias without buried vias***
- ***Type II – standard microvias with buried vias***
- ***Type III – staggered microvias***
- ***Type III stacked – stacked Microvias & stacked microvias on buried vias***

TD Technology

Lowest cost due to one lamination cycle

1 + 6 + 1

IPC Type I



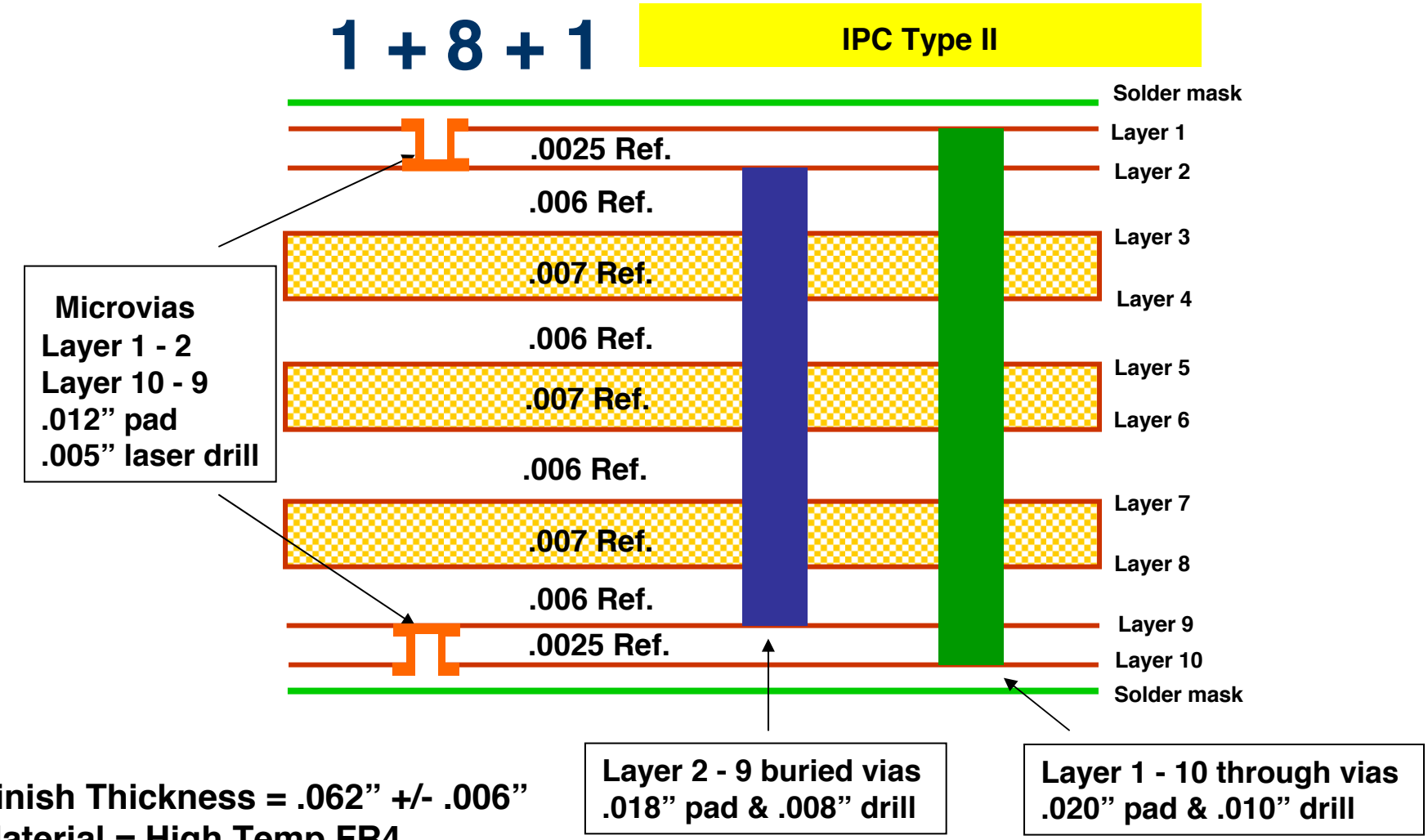
Microvias
Layer 1 - 2
Layer 8 - 7
.012” pad
.005” laser drill

Finish Thickness = .062 +/- .006
Material = High Temp FR4

Layer 1 – 8 through vias
.020” pad & .010” drill

TD Technology

Adds cost due to buried vias (two lamination cycles)



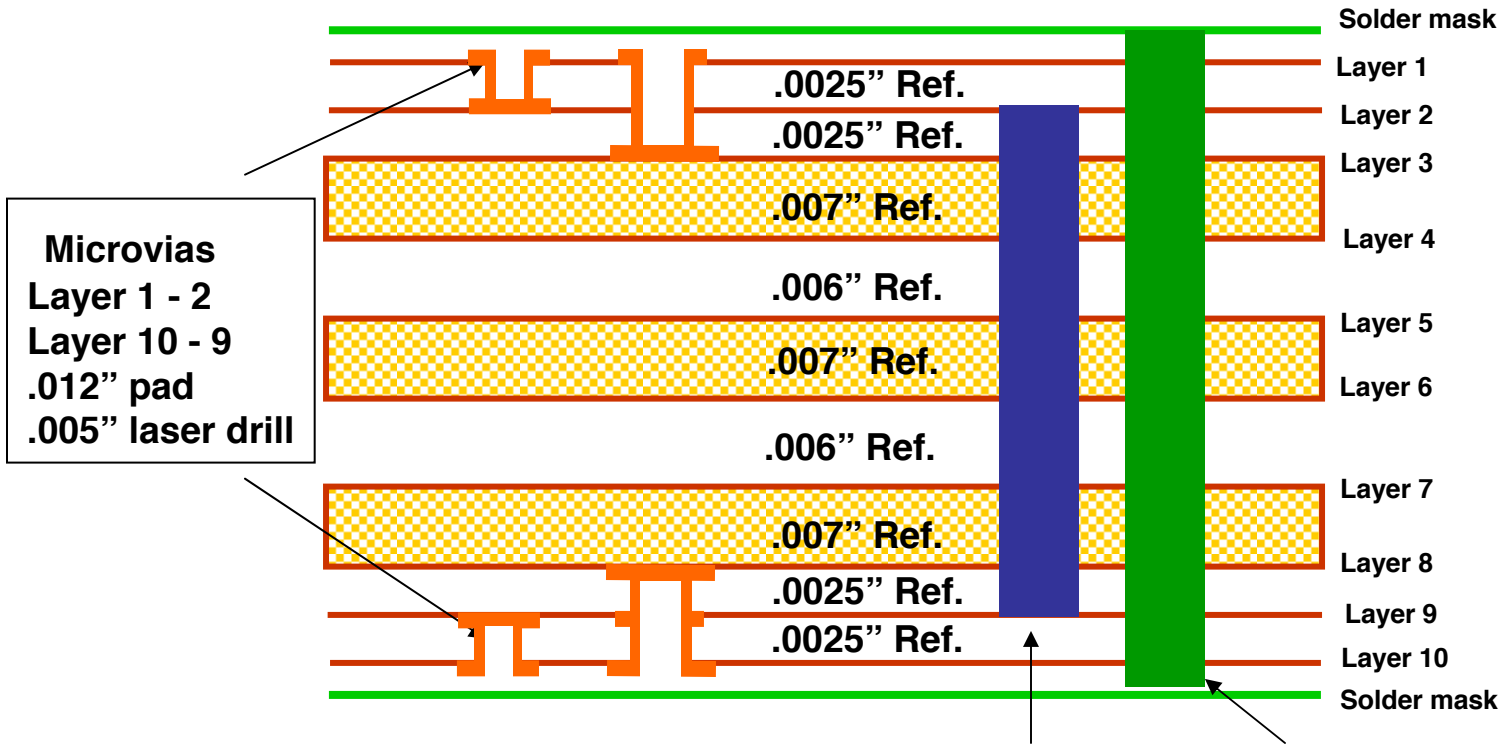
Finish Thickness = .062” +/- .006”
Material = High Temp FR4

TD Technology

Adds cost due to buried vias (two lamination cycles) & 1 – 3

2 + 6 + 2

IPC Type II – Variable depth



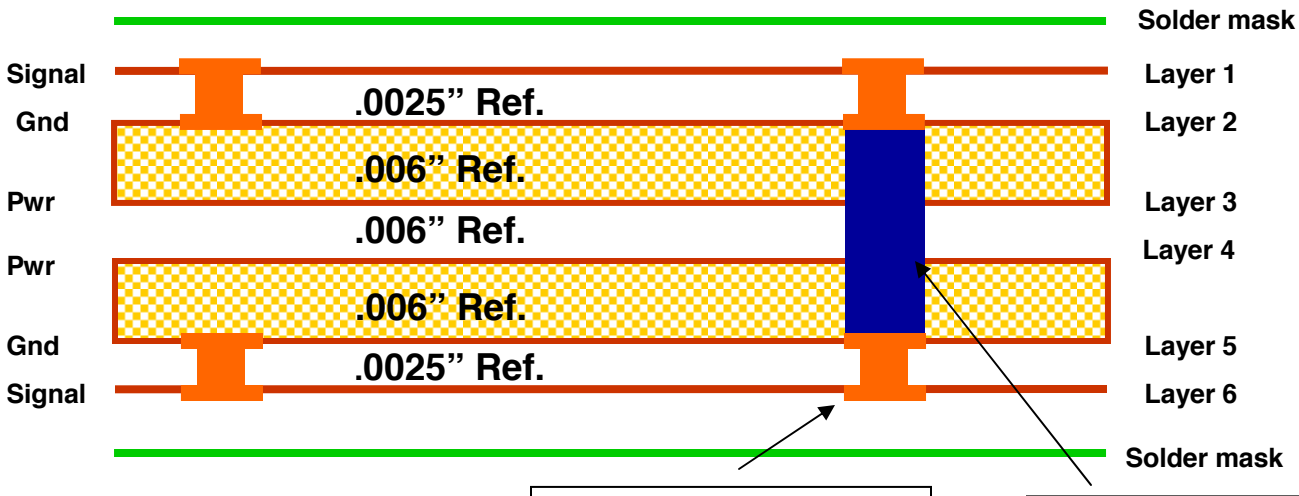
Finish Thickness = .062” +/- .006”
Material = High Temp FR4

TD Technology

Adds cost due to stacked microvia on a buried via & solid copper plate

1 + 4 + 1

IPC Type II – stacked vias



Stacked Microvias
Layer 1 - 2
Layer 6 - 5
.010” pad
.005” laser drill

Buried vias
Layer 2- 5
.010” drill
.020” pad
Fill with non-conductive
Plate-over

Finish Thickness = .032” +/- .003”

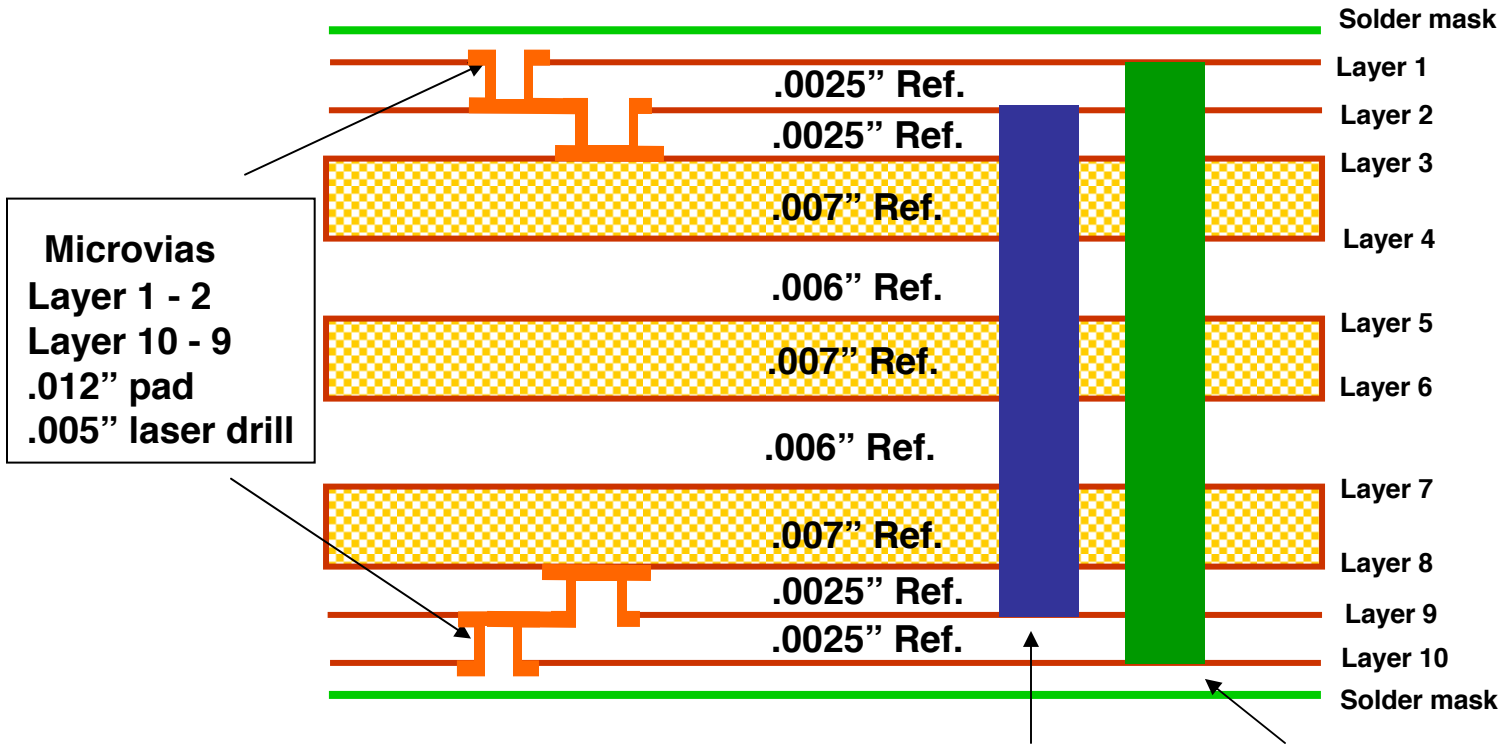
Requires wrap around plating

TD Technology

Reduces cost as compared to stacked microvias

2 + 6 + 2

IPC Type III



Finish Thickness = .062” +/- .006”
Material = High Temp FR4

TD Technology

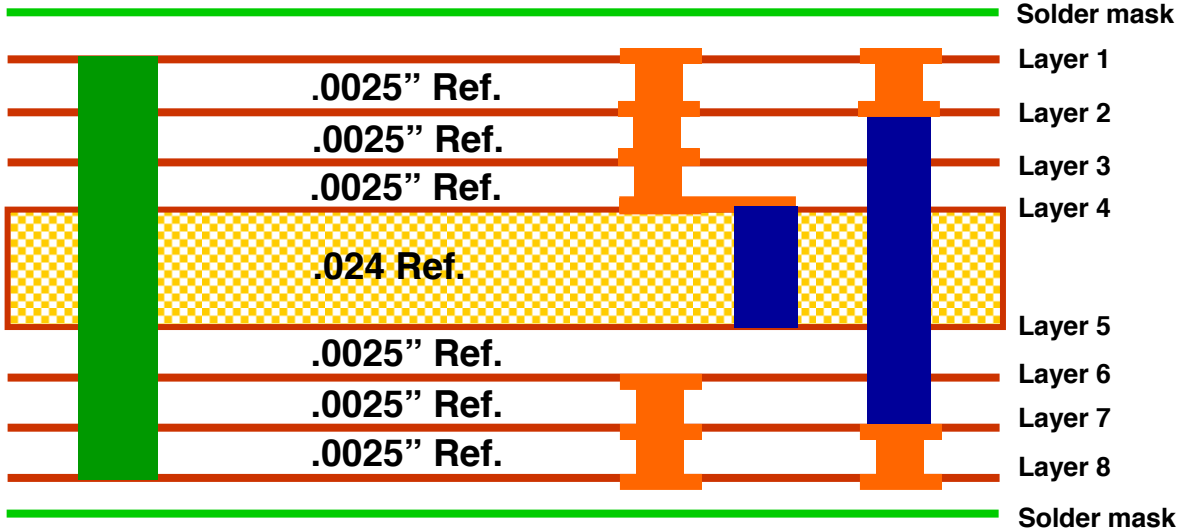
Adds cost due to stacked microvia on a buried via & solid copper plate

3 + 2 + 3

IPC Type III – stacked vias

Microvias
Layer 1 - 2
Layer 2 – 3
.010” pad
.005” laser drill

Microvias
Layer 8 - 7
Layer 7 – 6
.010” pad
.005” laser drill



Recommend using offset to buried via

Stacked MicroVias
Solid Cu Plate

Layer 2 - 7 = Buried Vias
.020” pad & .010” drill
Non-conductive fill & Plate

Finish Thickness = .048 +/- .004
Material = High Temperature FR4

Requires wrap around plating

TD Technology

- ***Standard Microvias provide fan-out Solutions from Layer 1 – 2 & 1 – 3***
- ***Stacked MicroVia SMV™ Provides fan-out Solutions for Multiple Layers***

Limitations are thin dielectrics between layers

0.5:1 aspect ratio = .0025” - .003”

TD Technology

Evolution of PCB Technology

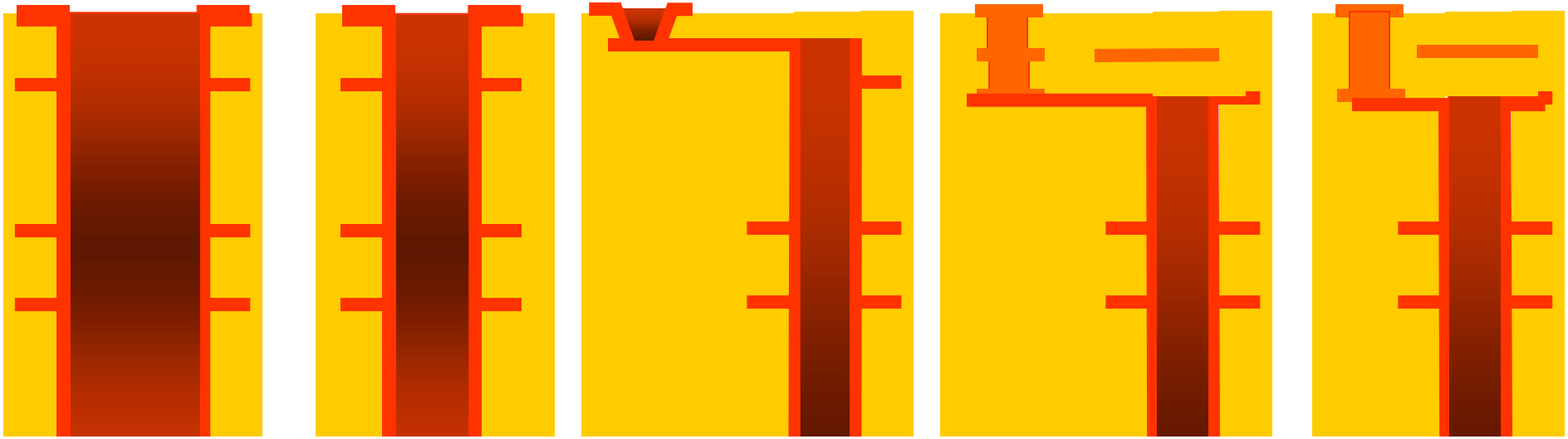
Through-hole Technology

Surface Mount Technology

Microvia Technology

Stacked Microvia Technology

Deep Microvia Technology



TD Technology

DDi Next Generation

Microvia Technology

Deep Microvias

TD Technology

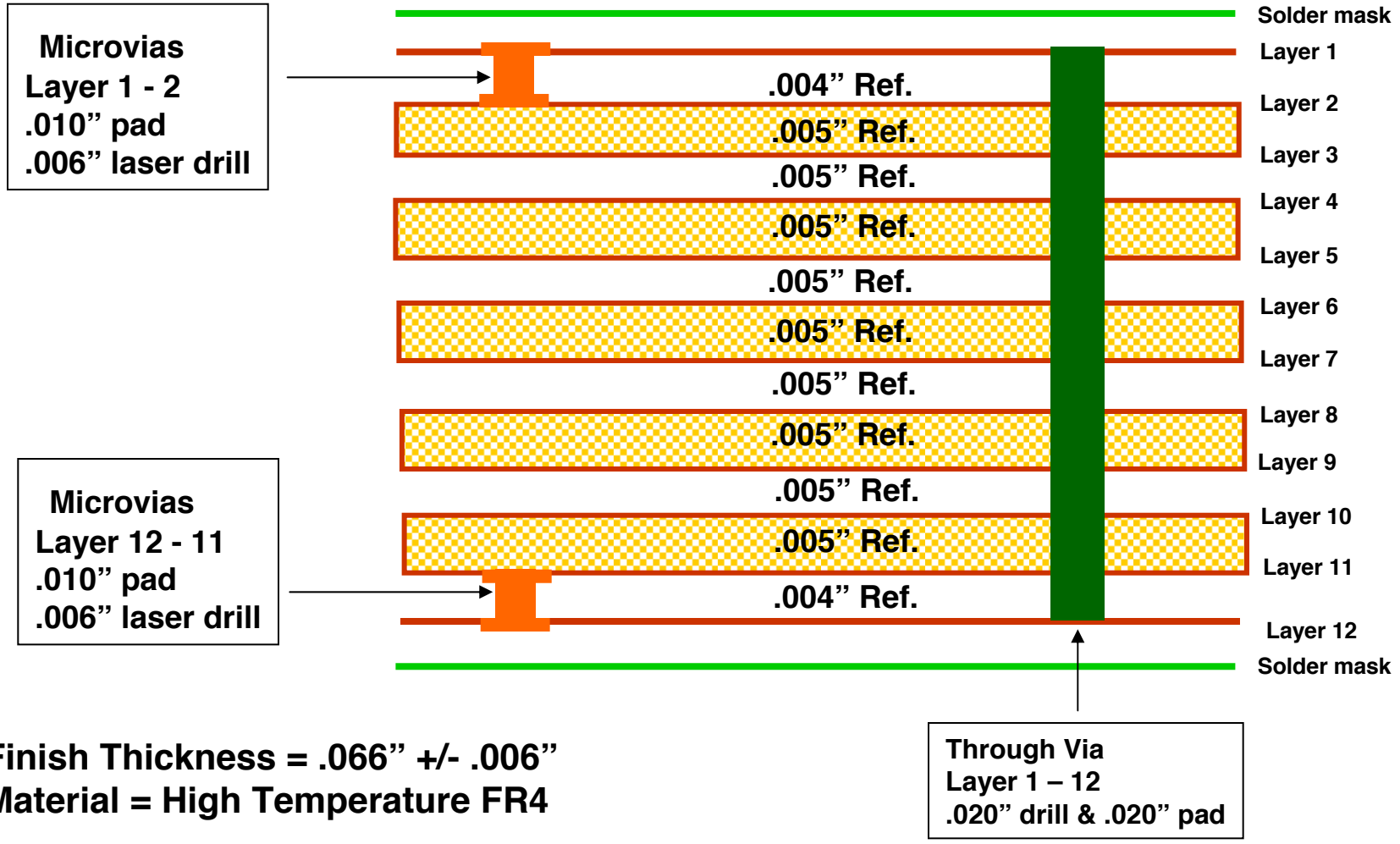
Deep Microvias:

- Provide additional dielectrics between layers
- Improved impedance performance
- Increased trace width external
- Provides a microvia RF solution
- Eliminates Lamination process in order to achieve dielectrics
- Provides Solid copper Plate (planar surface)
- Maintains small pad geometries (.010” pad)

TD Technology

Deep MicroVias

One Lamination Cycle

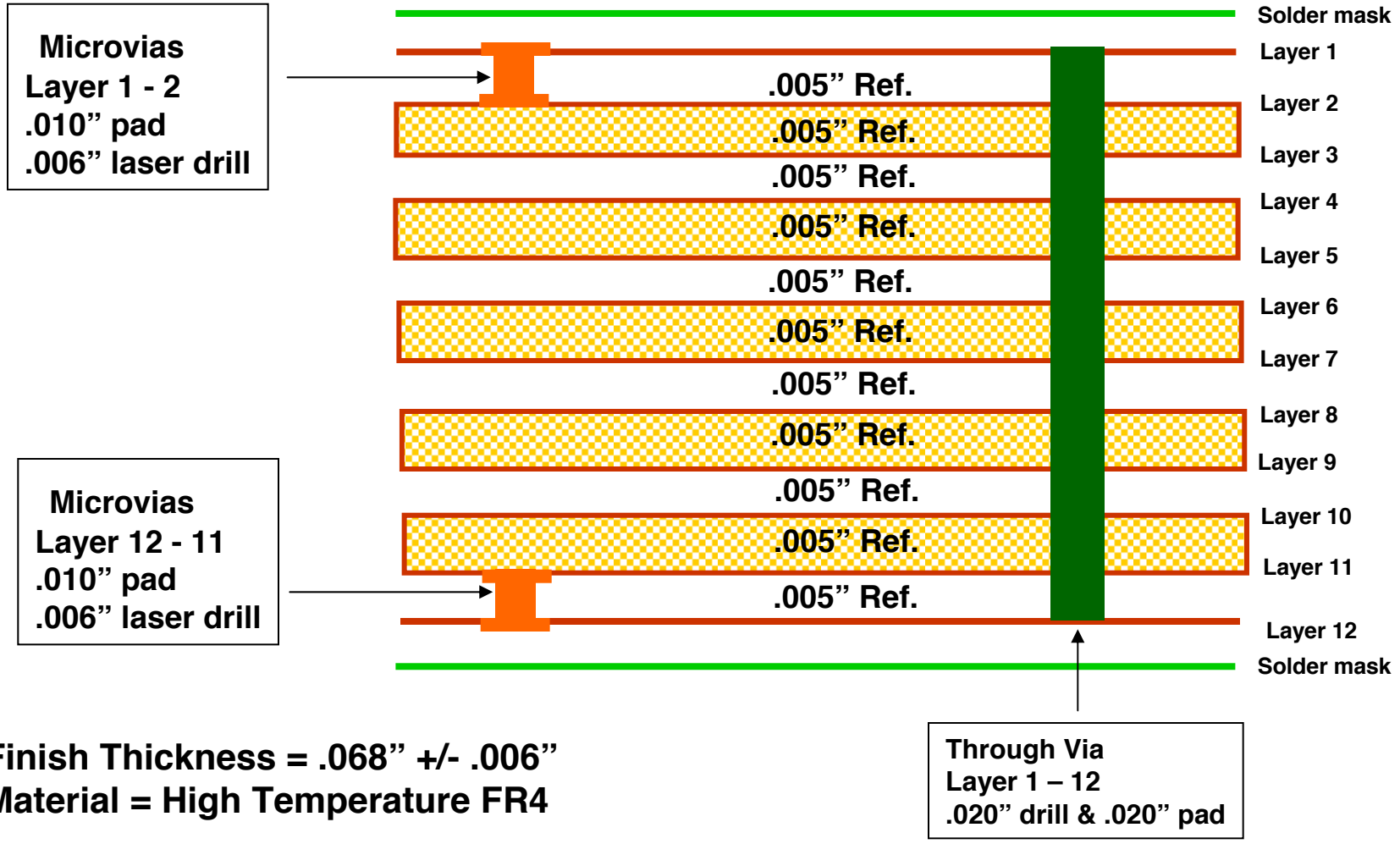


Finish Thickness = .066” +/- .006”
Material = High Temperature FR4

TD Technology

Deep MicroVias

One Lamination Cycle

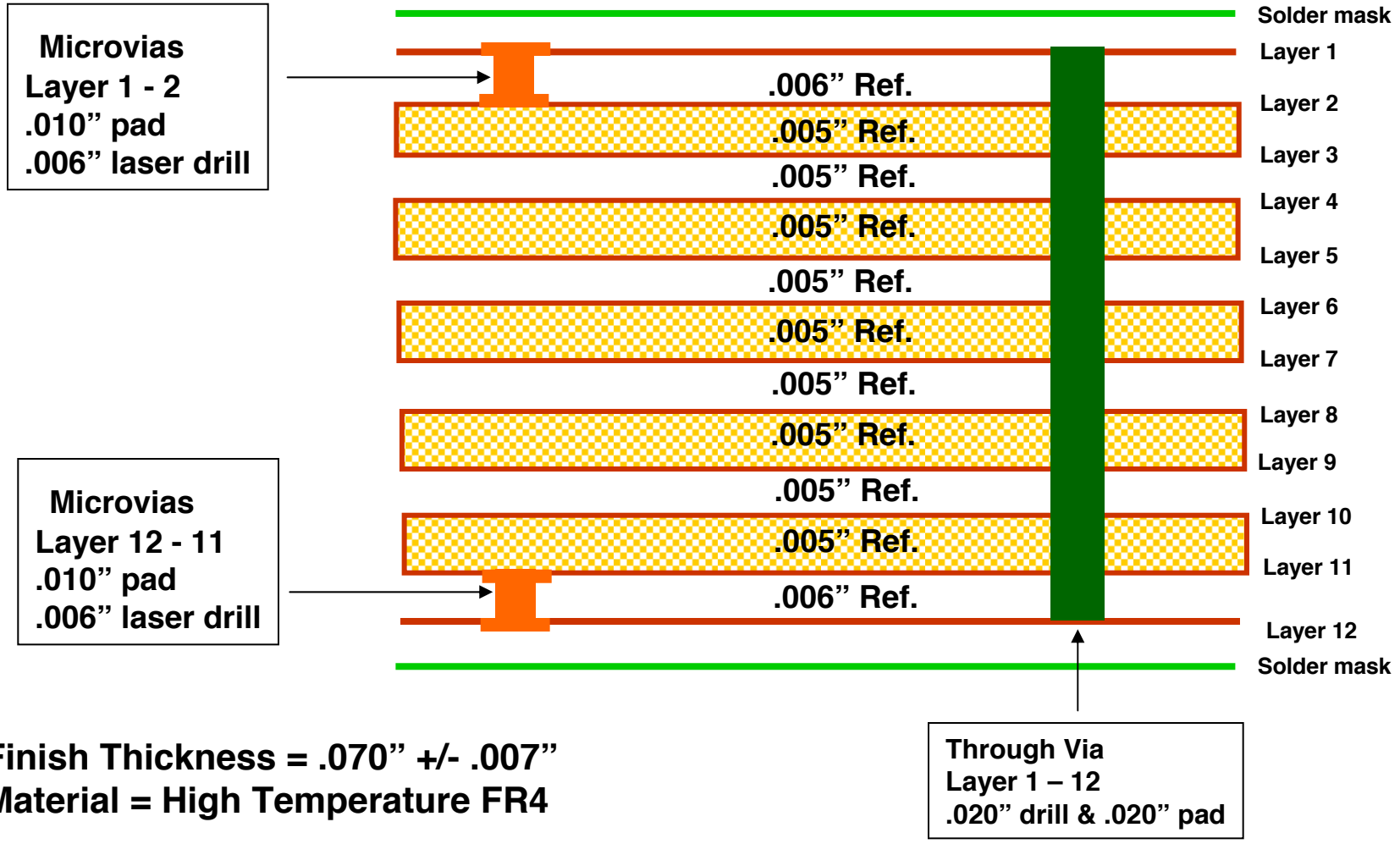


Finish Thickness = .068” +/- .006”
Material = High Temperature FR4

TD Technology

Deep MicroVias

One Lamination Cycle

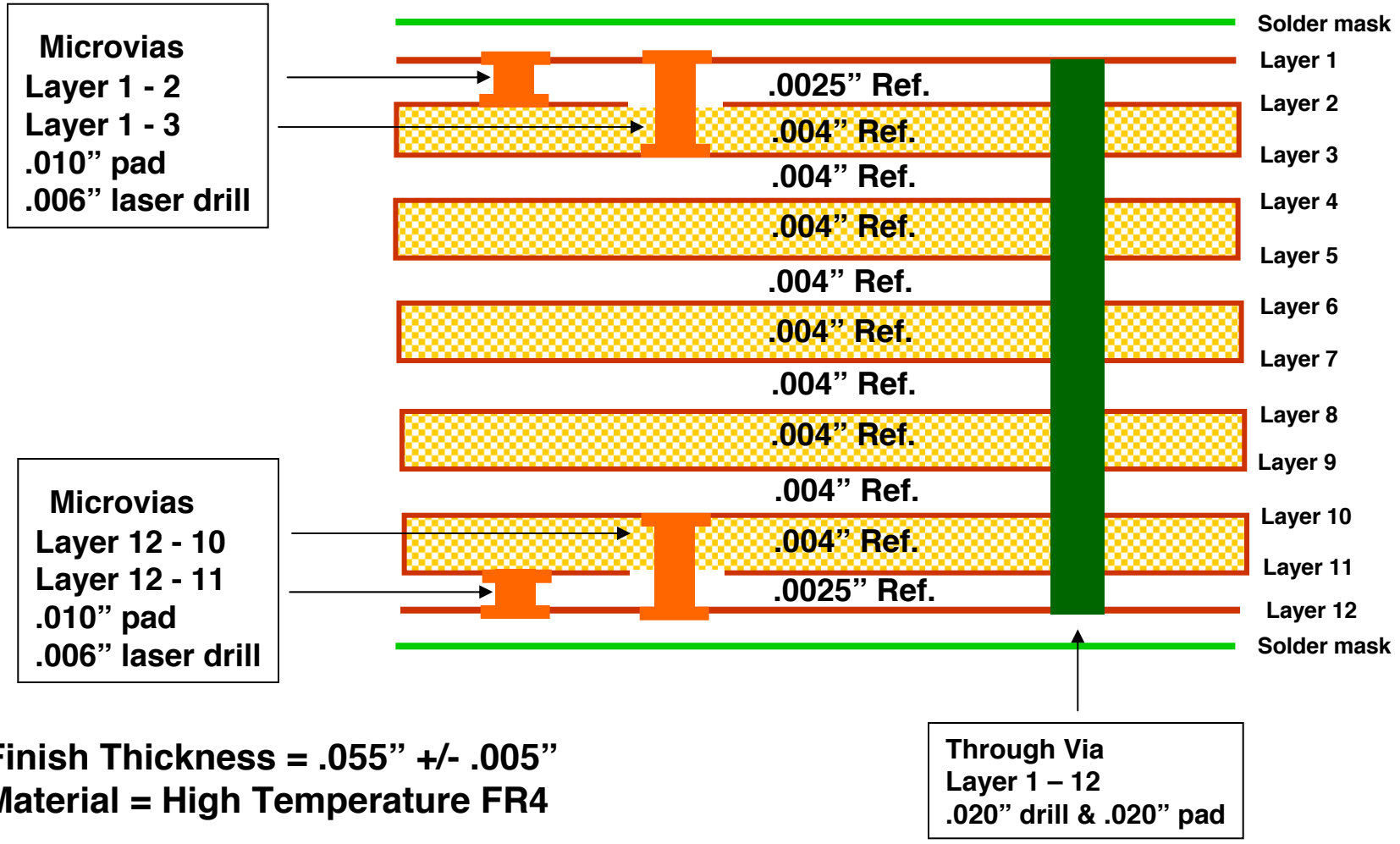


Finish Thickness = .070” +/- .007”
Material = High Temperature FR4

TD Technology

Deep MicroVias

One Lamination Cycle



Finish Thickness = .055” +/- .005”
Material = High Temperature FR4

TD Technology
Summary

- **Standard Microvias** create routing density (eliminate through vias)

  Reduce layer count

  Enhance electrical characteristics

  Standard Microvias limited to layers 1 – 2 & 1 - 3

- **Stacked Microvias** allows increased routing on multiple layers

  Provide Solutions for next generation applications

  1 mm – 0.8 mm – 0.65 mm - 0.5 mm – 0.4 mm – 0.3 mm & 0.25 mm

  SMV provides solid copper plate eliminating potential solder voiding

- **Deep Microvias** provide additional dielectric material & small geometry features

  Improved Impedance performance & provides RF microvia solutions

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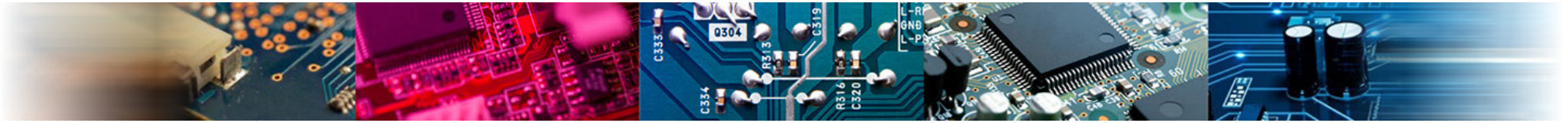

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