Note: Unless Specified, all ferrite beads are MPZ1608Y101BTA00
100R @ 100MHz / .04R DCR

Power

/RESET

File: power.kicad_sch

ESP32

fpga_cfg_data[0..7]
fpga_cfg_clk
fpga_cfg_csn
fpga_cfg_wrn
fpga_cfg_bsy
fpga_cfg_initn
fpga_cfg_done

File: esp32.kicad_sch

FPGA

fpga_cfg_data[0..7]
fpga_cfg_clk
fpga_cfg_csn
fpga_cfg_wrn
fpga_cfg_bsy
fpga_cfg_initn
fpga_cfg_done

USB

usb_data[0..15]
usb_clkout
usb_reset
usb_suspend
usb_db16_8
usb_opmode0
usb_opmode1
usb_linestate0
usb_linestate1
usb_xcvrsel
usb_termsel
usb_validh
usb_txready
usb_txvalid
usb_rxactive
usb_rxvalid
usb_rxerror

File: usb.kicad_sch

Ethernet

eth_reset
eth_tx_clk
eth_tx_ctrl
eth_txd[0..3]
eth_rx_clk
eth_rx_ctrl
eth_rxd[0..3]
eth_rx_er
eth_crs
eth_col
eth_mdc
eth_mdio

File: ethernet.kicad_sch

usb_data[0..15]
usb_clkout
usb_reset
usb_suspend
usb_db16_8
usb_opmode0
usb_opmode1
usb_linestate0
usb_linestate1
usb_xcvrsel
usb_termsel
usb_validh
usb_txready
usb_txvalid
usb_rxactive
usb_rxvalid
usb_rxerror
eth_reset
eth_tx_clk
eth_tx_ctrl
eth_txd[0..3]
eth_rx_clk
eth_rx_ctrl
eth_rxd[0..3]
eth_rx_er
eth_crs
eth_col
eth_mdc
eth_mdio
adc_q7_p
adc_q7_n
adc_q6_p
adc_q6_n
adc_q5_p
adc_q5_n
adc_q4_p
adc_q4_n
adc_q3_p
adc_q3_n
adc_q2_p
adc_q2_n
adc_q1_p
adc_q1_n
adc_q0_p
adc_q0_n
adc_dm_p
adc_dm_n
adc_wck_p
adc_wck_n
adc_dclk_p
adc_dclk_n
adc_cal
adc_sdio
adc_cs
adc_sclk
adc_reset

File: fpga.kicad_sch

ADC_Q7_P
ADC_Q7_N
ADC_Q6_P
ADC_Q6_N
ADC_Q5_P
ADC_Q5_N
ADC_Q4_P
ADC_Q4_N
ADC_Q3_P
ADC_Q3_N
ADC_Q2_P
ADC_Q2_N
ADC_Q1_P
ADC_Q1_N
ADC_Q0_P
ADC_Q0_N
ADC_DM_P
ADC_DM_N
ADC_WCK_P
ADC_WCK_N
ADC_DCLK_P
ADC_DCLK_N

RF_Receive

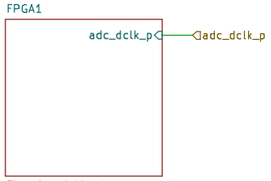
adc_q7_p
adc_q7_n
adc_q6_p
adc_q6_n
adc_q5_p
adc_q5_n
adc_q4_p
adc_q4_n
adc_q3_p
adc_q3_n
adc_q2_p
adc_q2_n
adc_q1_p
adc_q1_n
adc_q0_p
adc_q0_n
adc_dm_p
adc_dm_n
adc_wck_p
adc_wck_n
adc_dclk_p
adc_dclk_n
adc_cal
adc_sdio
adc_cs
adc_sclk
adc_reset
LO_HF
LO_LF

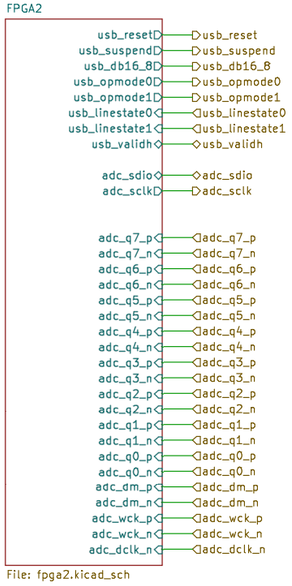
File: rf_receive.kicad_sch

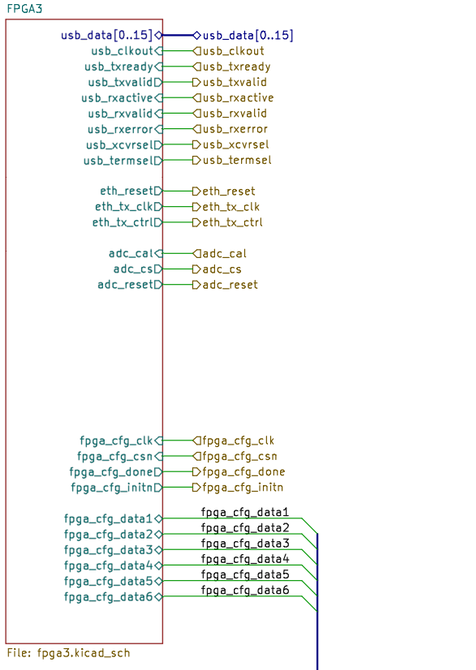
Sheet: /
File: VNA.kicad_sch

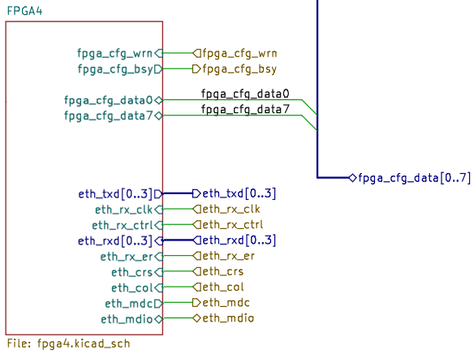
Title:

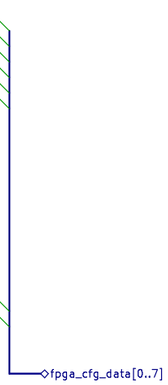
Size: A3 | Date: | Rev:
KiCad E.D.A. kicad 6.0.4-6f826c9f35~116~ubuntu20.04.1 | Id: 1/15







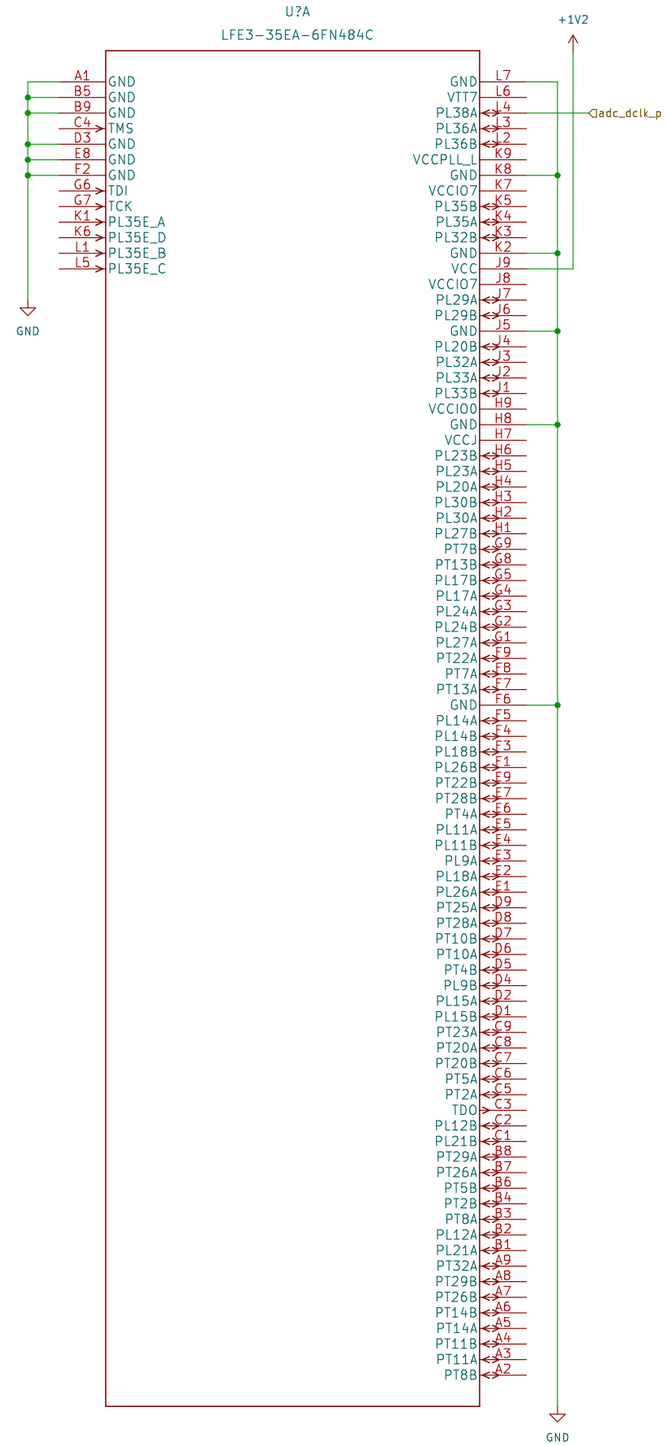




Sheet: /FPGA/
File: fpga.kicad_sch

Title:

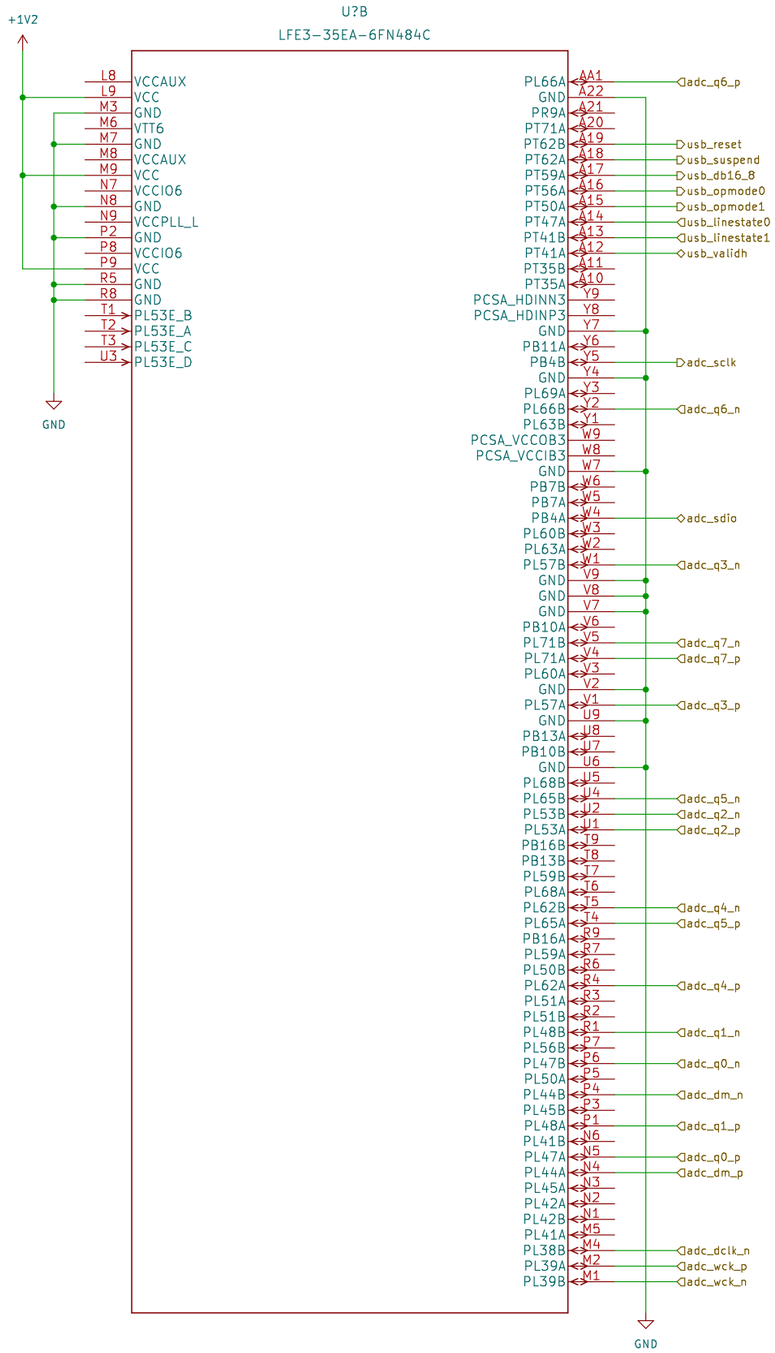
Size: A3	Date:	**Rev:**
KiCad E.D.A. kicad 6.0.4-6f826c9f35~116~ubuntu20.04.1		Id: 2/15



Sheet: /FPGA/FPGA1/
File: fpga1.kicad_sch

Title:

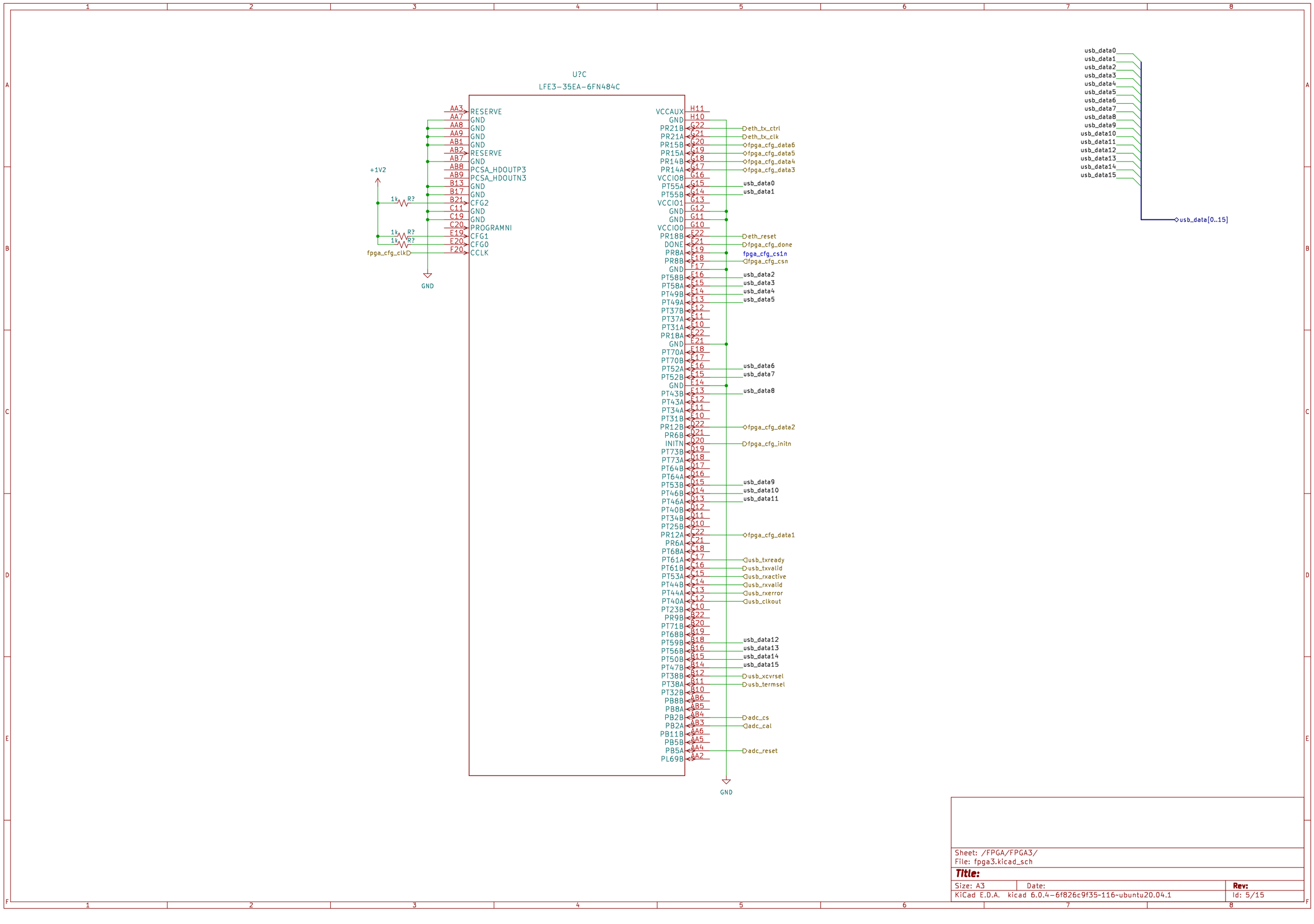
Size: A3	Date:	**Rev:**
KiCad E.D.A. kicad 6.0.4-6f826c9f35~116~ubuntu20.04.1		Id: 4/15

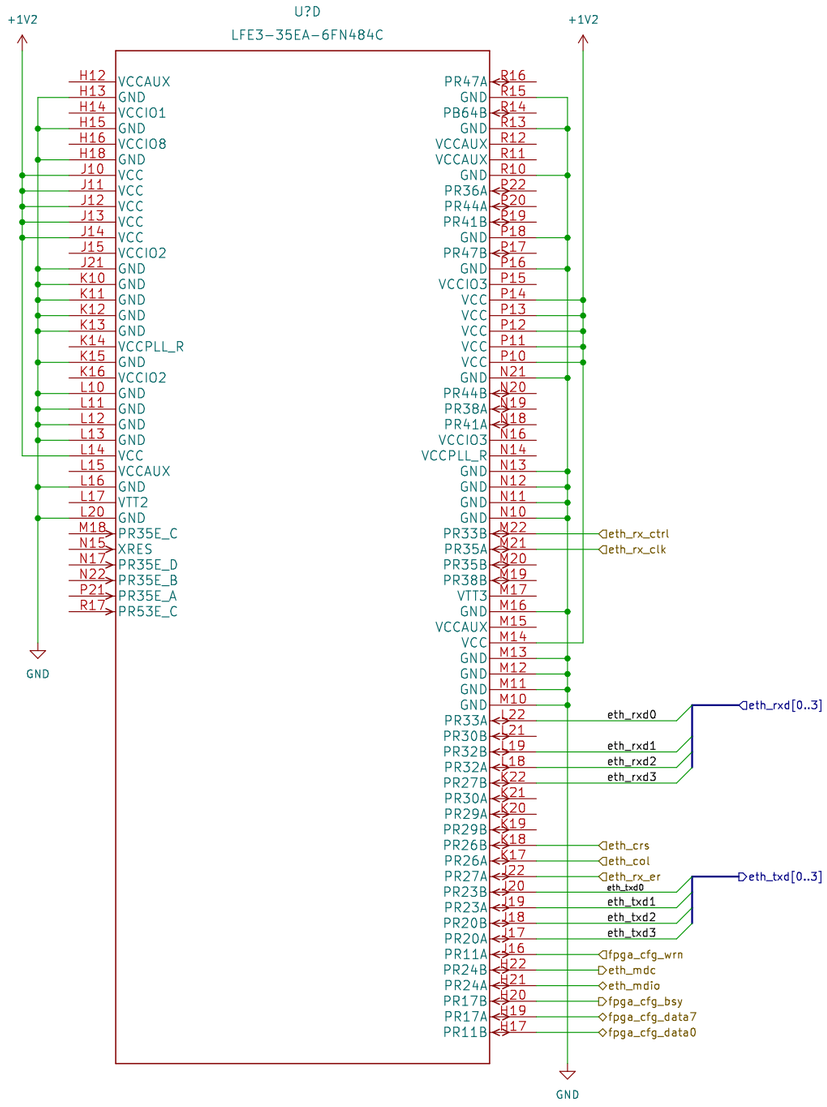


Sheet: /FPGA/FPGA2/
File: fpga2.kicad_sch

Title:

Size: A3	Date:	**Rev:**
KiCad E.D.A. kicad 6.0.4-6f826c9f35~116~ubuntu20.04.1		Id: 4/15

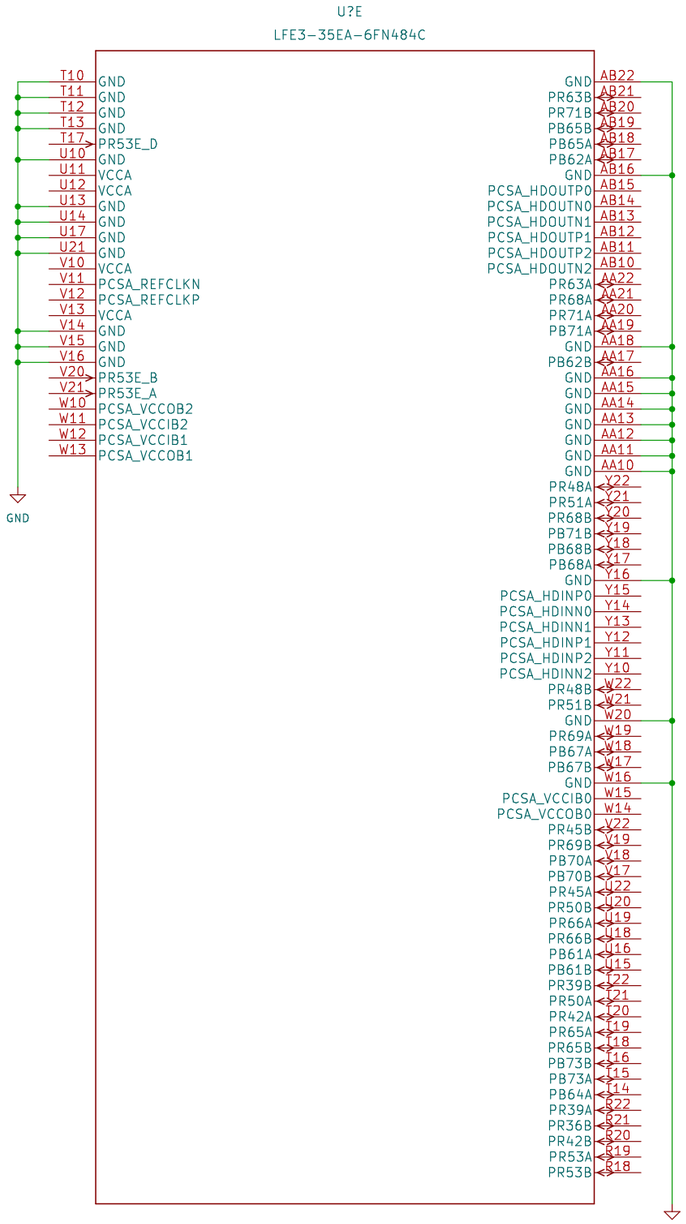

U?C
LFE3-35EA-6FN484C
AA3 RESERVE
AA7 GND
AA8 GND
AA9 GND
AB1 GND
AB2 RESERVE
AB7 GND
AB8 PCSA_HDOUTP3
AB9 PCSA_HDOUTN3
B13 GND
B17 GND
B21 CFG2
C11 GND
C19 GND
C20 PROGRAMNI
E19 CFG1
E20 CFG0
F20 CCLK
+1V2
1k R?
1k R?
1k R?
fpga_cfg_clk
GND
VCCAUX H11
GND H10
PR21B G22 eth_tx_ctrl
PR21A G21 eth_tx_clk
PR15B G20 fpga_cfg_data6
PR15A G19 fpga_cfg_data5
PR14B G18 fpga_cfg_data4
PR14A G17 fpga_cfg_data3
VCCIO8 G16
PT55A G15 usb_data0
PT55B G14 usb_data1
VCCIO1 G13
GND G12
GND G11
VCCIO0 G10
PR18B F22 eth_reset
DONE F21 fpga_cfg_done
PR8A F19 fpga_cfg_cs1n
PR8B F18 fpga_cfg_csn
GND F17
PT58B F16 usb_data2
PT58A F15 usb_data3
PT49B F14 usb_data4
PT49A F13 usb_data5
PT37B F12
PT37A F11
PT31A F10
PR18A E22
GND E21
PT70A E18
PT70B E17
PT52A E16 usb_data6
PT52B E15 usb_data7
GND E14
PT43B E13 usb_data8
PT43A E12
PT34A E11
PT31B E10
PR12B D22 fpga_cfg_data2
PR6B D21
INITN D20 fpga_cfg_initn
PT73B D19
PT73A D18
PT64B D17
PT64A D16
PT53B D15 usb_data9
PT46B D14 usb_data10
PT46A D13 usb_data11
PT40B D12
PT34B D11
PT25B D10
PR12A C22 fpga_cfg_data1
PR6A C21
PT68A C18
PT61A C17 usb_txready
PT61B C16 usb_txvalid
PT53A C15 usb_rxactive
PT44B C14 usb_rxvalid
PT44A C13 usb_rxerror
PT40A C12 usb_clkout
PT23B C10
PR9B B22
PT71B B20
PT68B B19
PT59B B18 usb_data12
PT56B B16 usb_data13
PT50B B15 usb_data14
PT47B B14 usb_data15
PT38B B12 usb_xcvrsel
PT38A B11 usb_termsel
PT32B B10
PB8B AB6
PB8A AB5
PB2B AB4 adc_cs
PB2A AB3 adc_cal
PB11B AA6
PB5B AA5
PB5A AA4 adc_reset
PL69B AA2
GND
usb_data0
usb_data1
usb_data2
usb_data3
usb_data4
usb_data5
usb_data6
usb_data7
usb_data8
usb_data9
usb_data10
usb_data11
usb_data12
usb_data13
usb_data14
usb_data15
usb_data[0..15]
Sheet: /FPGA/FPGA3/
File: fpga3.kicad_sch
Title:
Size: A3
Date:
Rev:
KiCad E.D.A. kicad 6.0.4-6f826c9f35~116~ubuntu20.04.1
Id: 5/15



Sheet: /FPGA/FPGA4/
File: fpga4.kicad_sch

Title:

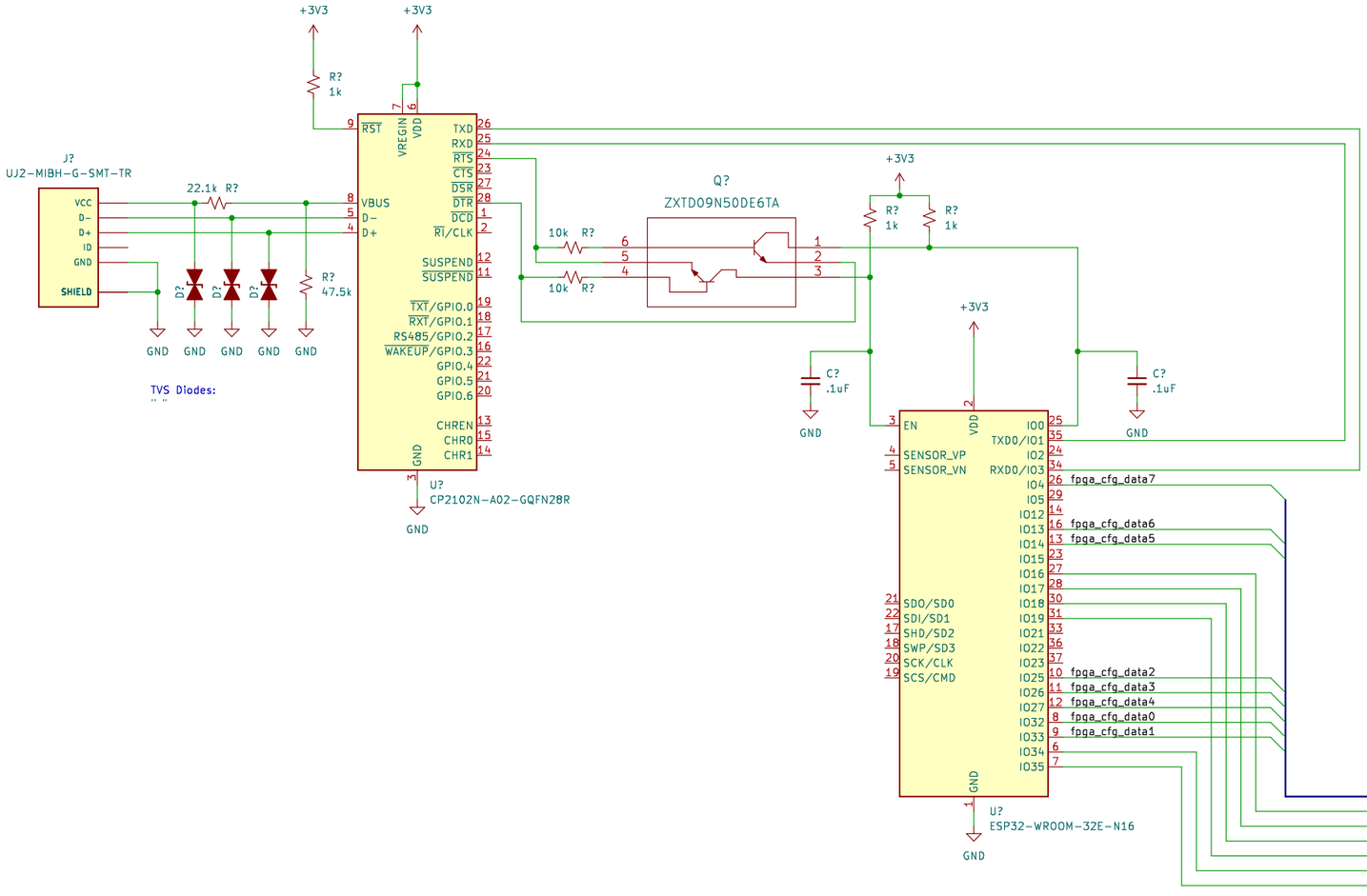
Size: A3	Date:	**Rev:**
KiCad E.D.A. kicad 6.0.4-6f826c9f35~116~ubuntu20.04.1		Id: 6/15



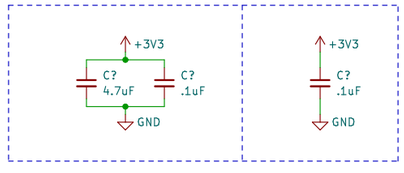
Sheet: /FPGA/FPGA5/
File: fpga5.kicad_sch

Title:

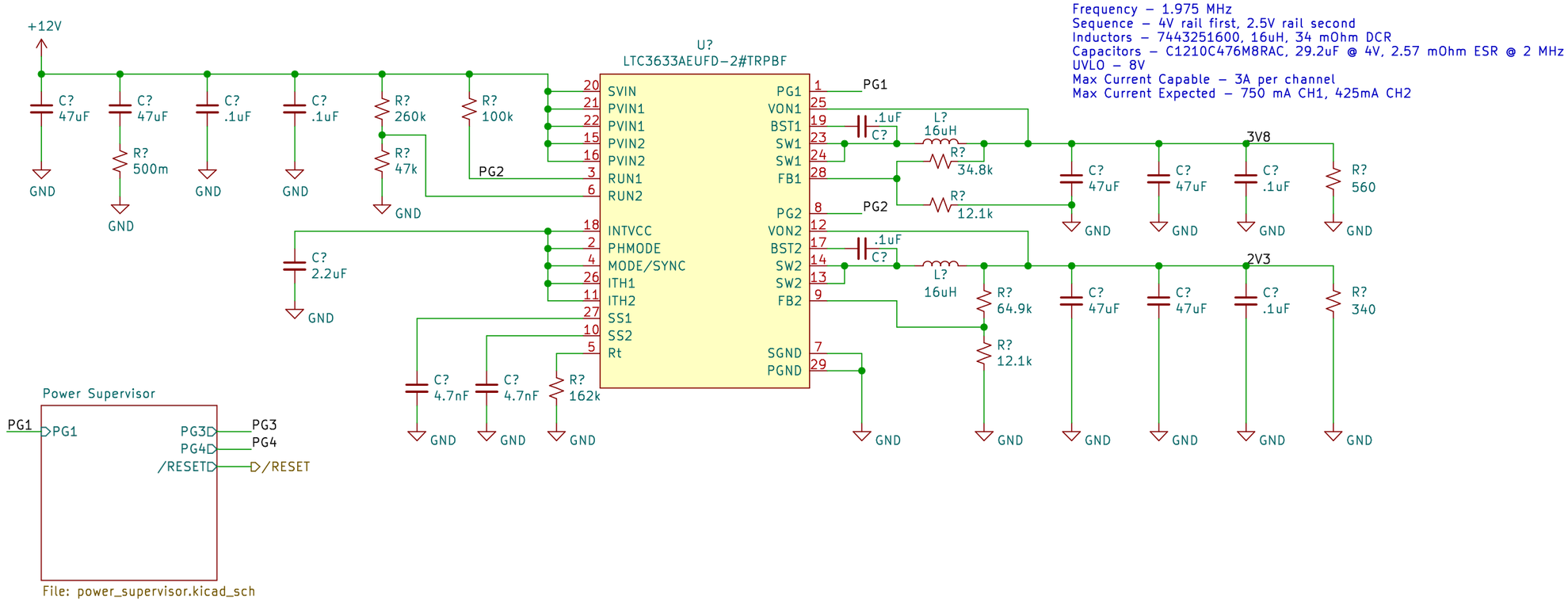
Size: A3	Date:	**Rev:**
KiCad E.D.A. kicad 6.0.4-6f826c9f35~116~ubuntu20.04.1		Id: 7/15



Bypass Capacitance:

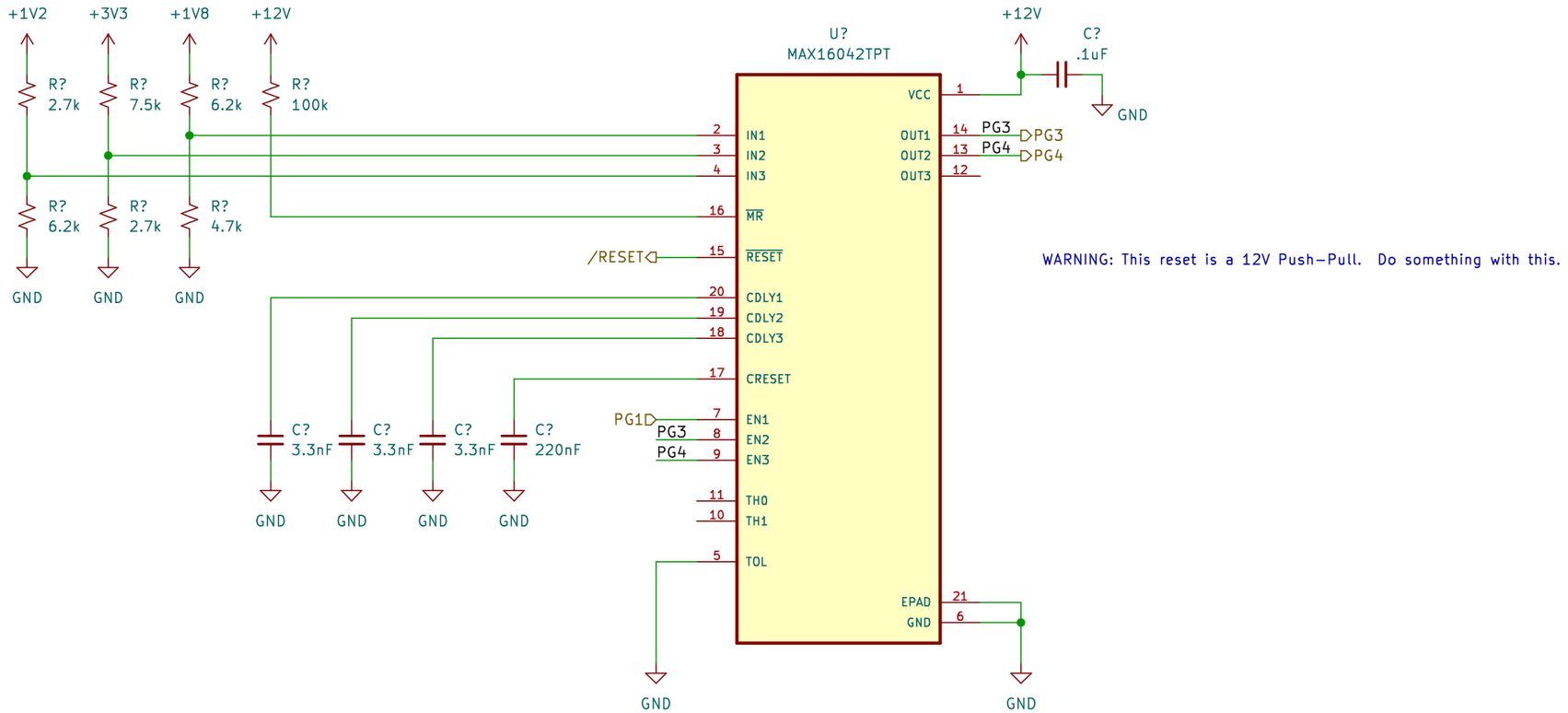


Sheet: /ESP32/	
File: esp32.kicad_sch	
Title:	
Size: A3	Date:
KiCad E.D.A. kicad 6.0.4-6f826c9f35~116~ubuntu20.04.1	Id: 8/15



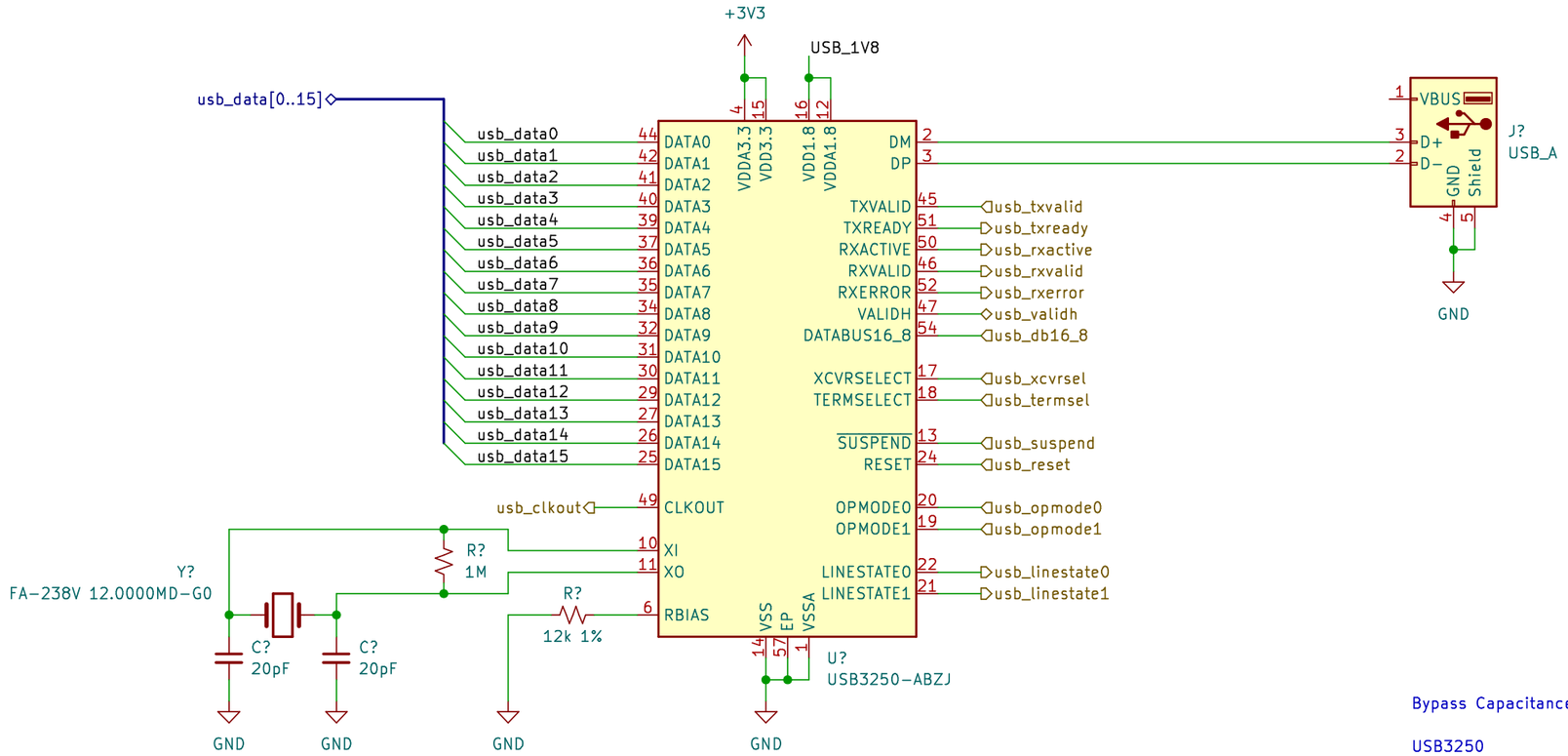
Sheet: /Power/		
File: power.kicad_sch		
Title:		
Size: A4	Date:	**Rev:**
KiCad E.D.A. kicad 6.0.4-6f826c9f35~116~ubuntu20.04.1		Id: 9/15

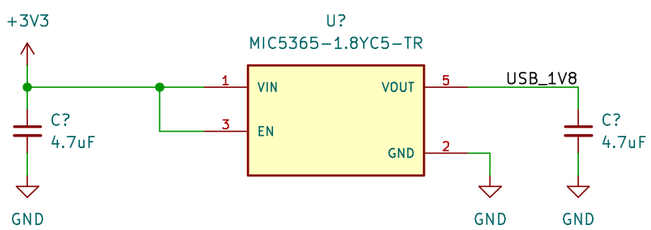
Note: Pull-up Resistors for PG3 and PG4 on parent schematic sheet
Note: Float TH0 and TH1 to operate in adjustable threshold mode
Note: 3.3nF of capacitance on CDLY_ provides 13 ms of delay between each rail going high
Note: 220nF of capacitance on CDLY_ provides 220 ms of delay between each rail going high



WARNING: This reset is a 12V Push-Pull. Do something with this.

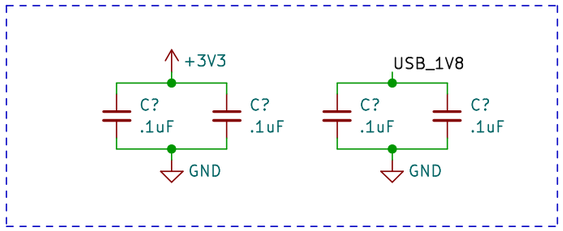
Sheet: /Power/Power Supervisor/		
File: power_supervisor.kicad_sch		
Title:		
Size: A4	Date:	**Rev:**
KiCad E.D.A. kicad 6.0.4-6f826c9f35-116~ubuntu20.04.1		Id: 10/15





Bypass Capacitance:

USB3250



Sheet: /USB/		
File: usb.kicad_sch		
Title:		
Size: A4	Date:	**Rev:**
KiCad E.D.A. kicad 6.0.4-6f826c9f35~116~ubuntu20.04.1		Id: 11/15

Note: Place DVDD bypass capacitance near pin 11

Configuration:
- Auto-Crossover Enabled
- PHYAD[4:0] = 00000
- Mode = 001 / Copper-RGMII, Receive clock transition when data stable

U?
88E3015-A2-NNP1C000

+3V3 +3V3 +3V3
FB? FB?
AVDDX AVDDC
29 AVDDC
14 AVDDX
6 VDDO
20 VDDO
36 VDDO
44 VDDOR
48 VDDOR
56 CFG0
1 CFG1
LED1 2 CFG2
LED0 3 CFG3
GND
eth_tx_clk 52 TX_CLK
eth_tx_ctrl 55 TX_CTRL
eth_txd0 50 TXD0
eth_txd1 51 TXD1
eth_txd2 53 TXD2
eth_txd3 54 TXD3
eth_txd[0..3]
eth_rx_clk 45 RX_CLK
eth_rx_ctrl 41 RX_CTRL
eth_rxd0 42 RXD0
eth_rxd1 43 RXD1
eth_rxd2 46 RXD2
eth_rxd3 47 RXD3
eth_rxd[0..3]
eth_rx_er 17 RX_ER
eth_crs 18 CRS
eth_col 19 COL
eth_mdc 38 MDC
MDIO 35 MDIO
eth_mdio
32 XTAL_IN
33 XTAL_OUT
eth_reset 9 RESETn

+3V3
R? 2.2k
MDIO

12 AVDDR
13 AVDDR
24 AVDD
C? 10uF
C? .1uF
C? .1uF
GND GND GND
4 DVDD
11 DVDD
34 DVDD
DVDD
Q? 2SAR533P5T100
FB?
+3V3
49 VREF
39 COMAn
16 SIGDET
15 CTRL25
10 DIS_REG12
GND
GND GND
C? .01uF
C? .01uF
R? 49.9 R? 49.9
R? 49.9 R? 49.9
26 MDIP0
25 MDIN0
23 MDIP1
22 MDIN1
5 LED0
7 LED1
8 LED2
28 RSET
27 TSTPT
30 HSDACN
31 HSDACP
21 NC
37 NC
40 NC
57 GND
R? 2k 1%
R? 422
GND GND GND

ENET_2V5 ENET_2V5
FB? FB?
C? .1uF C? .1uF
GND GND

J?
RJMG1BD3B8K1ANR
R1 TD+
R4 TCT
R2 TD-
R3 RD+
R5 RCT
R6 RD-
C1 C4 C5 C2 75 75
XMIT
C3 C7 C8 C6 75 75
RCV
1000pF
L4 LEDG_A GREEN
L3 LEDG_K
L1 LEDY_A YELLOW
L2 LEDY_K
GND
R8
SHIELD 13
GND1 GND1

R? 162 R? 162
GND GND

Bypass Capacitance:

88E3015

DVDD +3V3 +3V3 +3V3 +3V3 +3V3 AVDDX AVDDC
C? .1uF
GND

+3V3
C? .1uF
1 TRIS VDD 4
GND 2
OUT 3
X? ASCO-25.000MHZ-EK-T3
GND GND

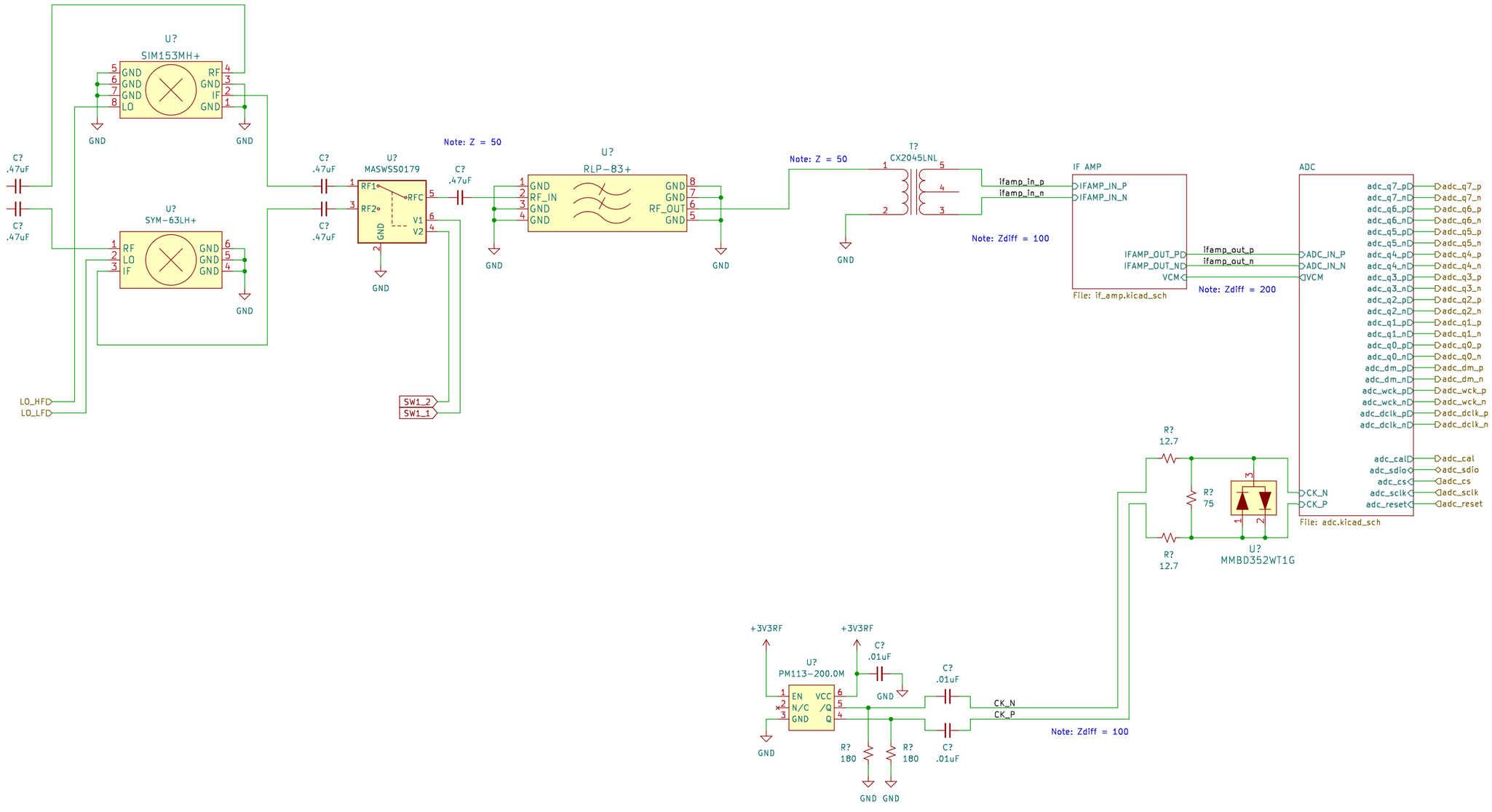
+3V3
C? 4.7uF
GND

U?
MIC5353-2.5YMT-TR
3 VIN VOUT 4
1 EN BYP 6
GND 2
C? .1uF
C? 4.7uF
GND GND GND
ENET_2V5

Sheet: /Ethernet/
File: ethernet.kicad_sch

Title:

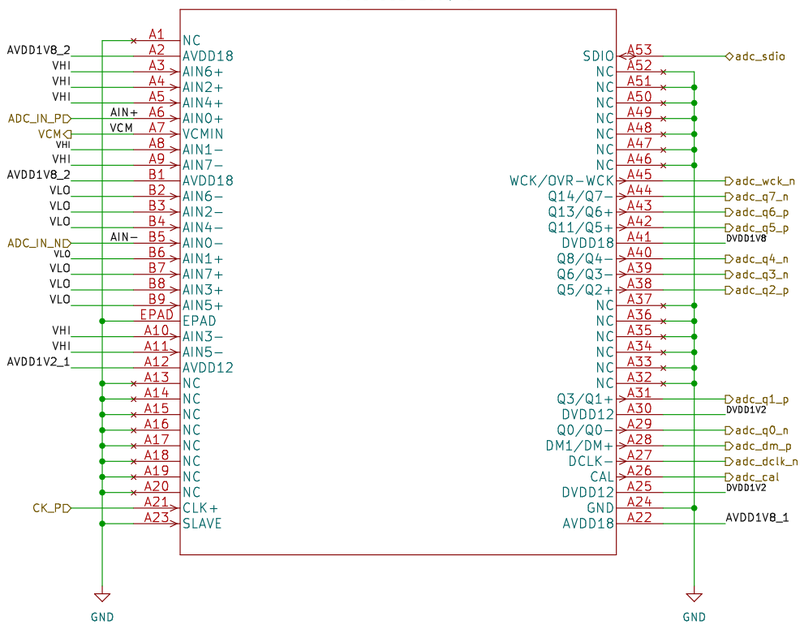
Size: A4 | Date: | Rev:
KiCad E.D.A. kicad 6.0.4-6f826c9f35-116~ubuntu20.04.1 | Id: 12/15



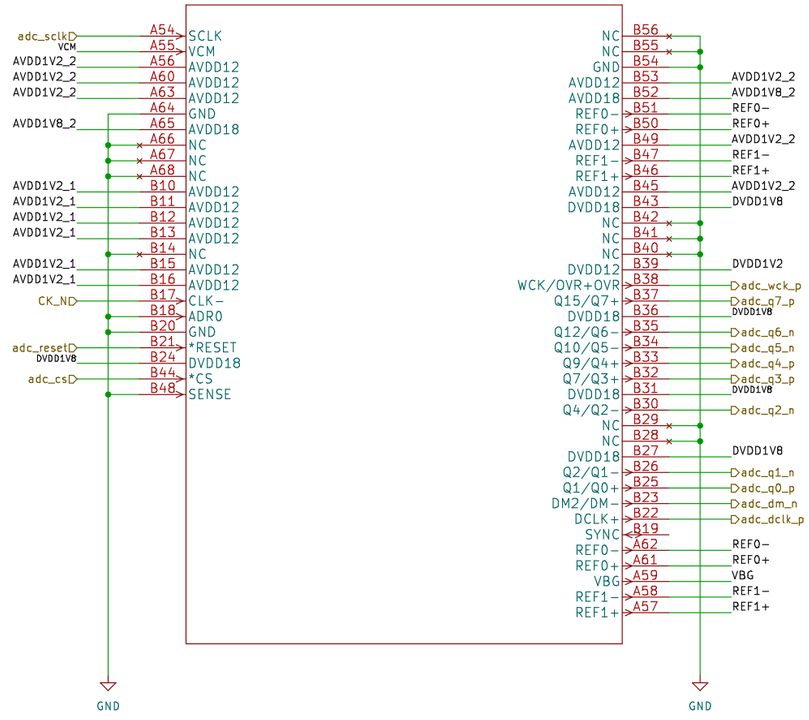
Sheet: /RF_Receive/		
File: rf_receive.kicad_sch		
Title:		
Size: A3	Date:	**Rev:**
KiCad E.D.A. kicad 6.0.4-6f826c9f35~116~ubuntu20.04.1		Id: 13/15

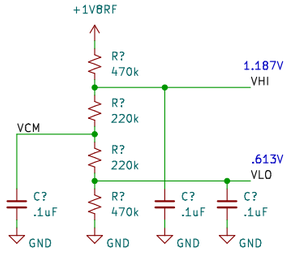
Note:
V_SENSE = GND
V_REF = 0.74 V
SLAVE = 0 (Not Used)
SYNC = FLOAT (Not Used)

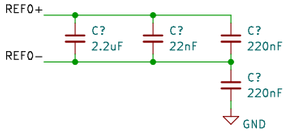
U?A
MCP37D31-200I/TL

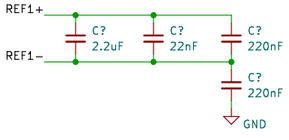


U?B
MCP37D31-200I/TL

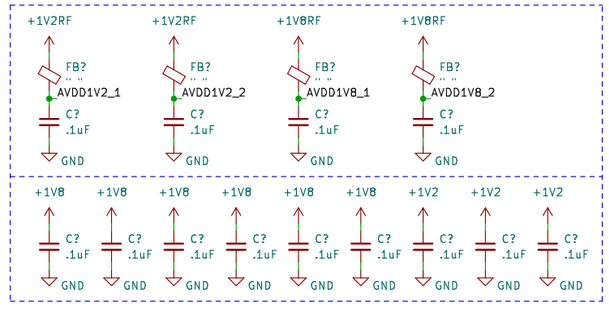




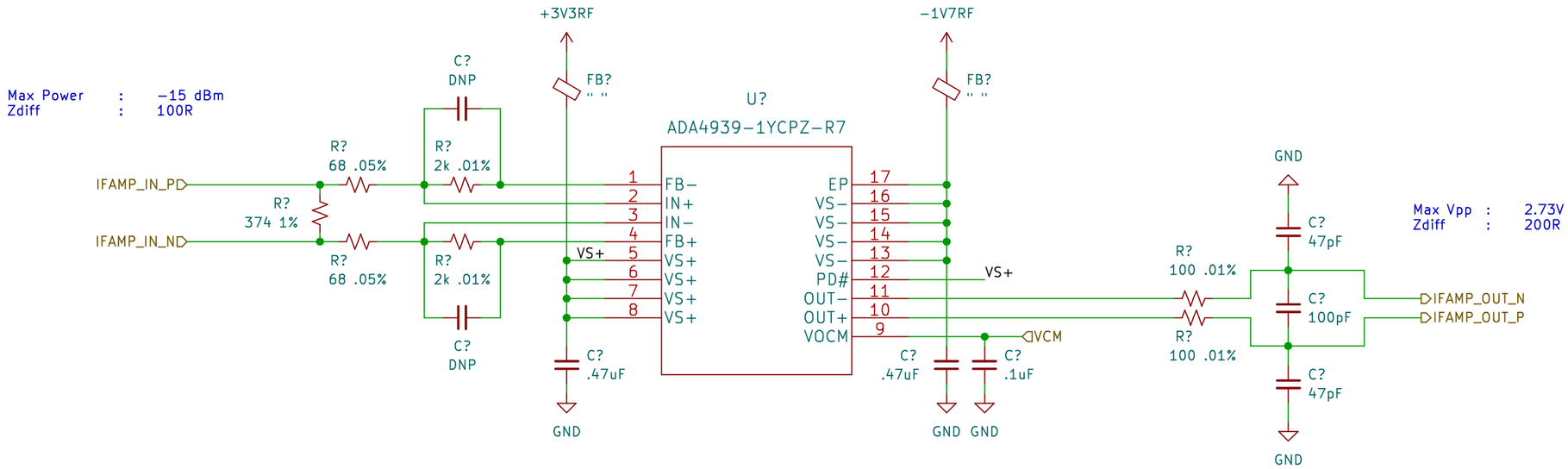




Bypass Capacitance:
MCP37D31



Sheet: /RF_Receive/ADC/		
File: adc.kicad_sch		
Title:		
Size: A3	Date:	**Rev:**
KiCad E.D.A. kicad 6.0.4-6f826c9f35~116~ubuntu20.04.1		Id: 14/15



Note: Reference has typographic error. LHS of equation should be VOUT/VIN.

In a terminated system, it is common practice to take the gain of the amplifier stage from the source to the load, or from $V_{IN\pm}$ to $V_{OUT\pm}$; so gain is given by

$$\frac{V_{IN\pm}}{V_{OUT\pm}} = \frac{R_L}{R_L + 2R_O} \times \frac{R_F}{R_G}. \qquad (1)$$

https://www.ti.com/lit/an/slyt326/slyt326.pdf?ts=1655353125313&ref_url=https%253A%252F%252Fwww.google.com%252F

Sheet: /RF_Receive/IF AMP/
File: if_amp.kicad_sch

Title:

Size: A4	Date:	**Rev:**
KiCad E.D.A. kicad 6.0.4−6f826c9f35~116~ubuntu20.04.1		Id: 15/15