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腾戈智慧半导体科技

Top provider of Web-native EDA for semiconductor yield improvement

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https://itanggo.com

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TANGO AI

Outline

About Tango AI

Reference

Why Tango AI

Product Capabilities

System Framework

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Tango AI At a Glance

Tango - AI, we are the leading information technology service company, provides data analytic solutions to improve yield management, quality enhancement and production control along the entire supply chain manufacturing for semiconductor and electronics companies since year 2000.

How We Help Customers

- Improve their profitability through manufacturing excellence.
- Lower their cost of product design and production control.
- Enhance their yield and quality management.
- Accelerate their production ramp with good traceability and transparency into manufacturing operations.
- Enable their manufacturing insights.

Our Customers: IC Design House

With over 70% of top 20 IC design customers in Taiwan and total 67 Fabless customers worldwide. We provide a full range of service for both frontend and backend customers in the semiconductor industry.

Taiwan

70% market share of top 20 IC design customers in Taiwan

Asia

China

Japan

Korea

Global

USA

Germany

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Taiwan

Customers rank on the top 20 list in Taiwan

MEDIATEK 联发科(1)
REALTEK 瑞昱(3)
HIMAX 奇景(4)
RICHTEK 立锜(5)
FOCALTECH 敦泰(7)
ESMT 晶豪(8)
SITRONIX 硅创(9)
SUNPLUS 凌阳(10)
GLOBALUNICHIP 创意(11)
RAYDIUM 瑞鼎(13)
FARADAY 智原(15)
PIXART 原相(17)
HOLTEK 盛群(18)
ALI 扬智(19)

Other Customers in Taiwan

AIROHA 络达
ALCHIP 世芯
ANAXIC 智安
APMEMORY 爱普
BROVOTEK 博发
CHAMPION 虹冠
ECMOS 飞虹
EGIS 神盾
FITIPOWER 天钰
GENERALPLUS 凌通
HTMobile 恒通
ICATCHTEK 芯鼎
ISSI 常忆
ICPLUS 九旸
INERGY 广闳
ISSC 创杰
JMICRON 智微
LEADTREND 通嘉
LITEON 敦南
MSTAR 晨星
NYQUEST 九齐
POWERFLASH 智旺
RALINK 雷凌
SIGMASTAR 星宸
SYNCMOS 新茂
SOCLE 虹晶
SOINC 晶相
SONIX 松翰
SUNPLUSIT 凌阳创新
UPI 力原
UBIQ 力祥
WELTREND 伟诠
ZENTEL 力积

Asia

China

ALLWINNER 珠海全志
AMLogic 上海晶晨
AUTOCHIPS 合肥杰发
AXERA 爱芯元智
BITMAIN 比特大陆
DJI 深圳大疆创新
HUAYA 上海华亚微
HDSC 上海华大半导体
LEADCORE 上海联芯
MEMSIC 美新半导体
MIRAMEMS 苏州明皜传感
MOORE ELITE 摩尔精英
NOVOSENSE 苏州纳芯微
QSTCORP 上海硅睿
RDA 上海锐迪科
ROCKCHIP 福州瑞芯微
SINOWEALTH 上海中颖微

China

SGMICRO 北京圣邦微
SOLOMON 香港晶门
SPREADTRUM 上海展讯
UNIC 西安紫光国芯
VERISILICON 上海芯原微
XHSC 小华半导体
YTM 苏州云途
TRUECORE 南京真芯润和微
MEGAHUNT 兆讯恒达
PHYTIUM 天津飞腾

Japan

Murata

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Global

USA

INVENSENSE 应美盛
MCUBE 硅立
MICRON 美光
ONSEMI 安森美
PIXELWORKS XMEMS 知微电子

Europe

BOSCH 博世

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Our Customers : Testing House

Taiwan

AGSTI 宏发半导体
ASIT 宏宇半导体
CHIPMOS 南茂科技
GIGA-Solution 全智科技
GREATEK 超丰电子
GT 寰邦科技
IST 飞信半导体
KYEC 京元电子
OSE 华泰电子
PANTHER 鸿谷科技
PTI 力成科技
SPIL 硅品精密
TESTAR 晶测电子
THAILIN 泰林科技
THEIL 同欣电子
UTAC 联测科技

Global

SANDISK(China)上海晟碟半导体
SANDISK(Malaysia)马来西亚
HSTS(China) 芯测半导体

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Why Tango AI ?

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Why Tango?

We help you "Bridge All the Big Data High Way"

To accelerate your production ramp, we help to bridge all the production metrics by collecting and aggregating data from multiple manufacturing sites into coherent information and enhance your production efficiency with advanced data science on our "***TANGO***"platform.

We help you "Relieve Your Data Hunting Nightmare"

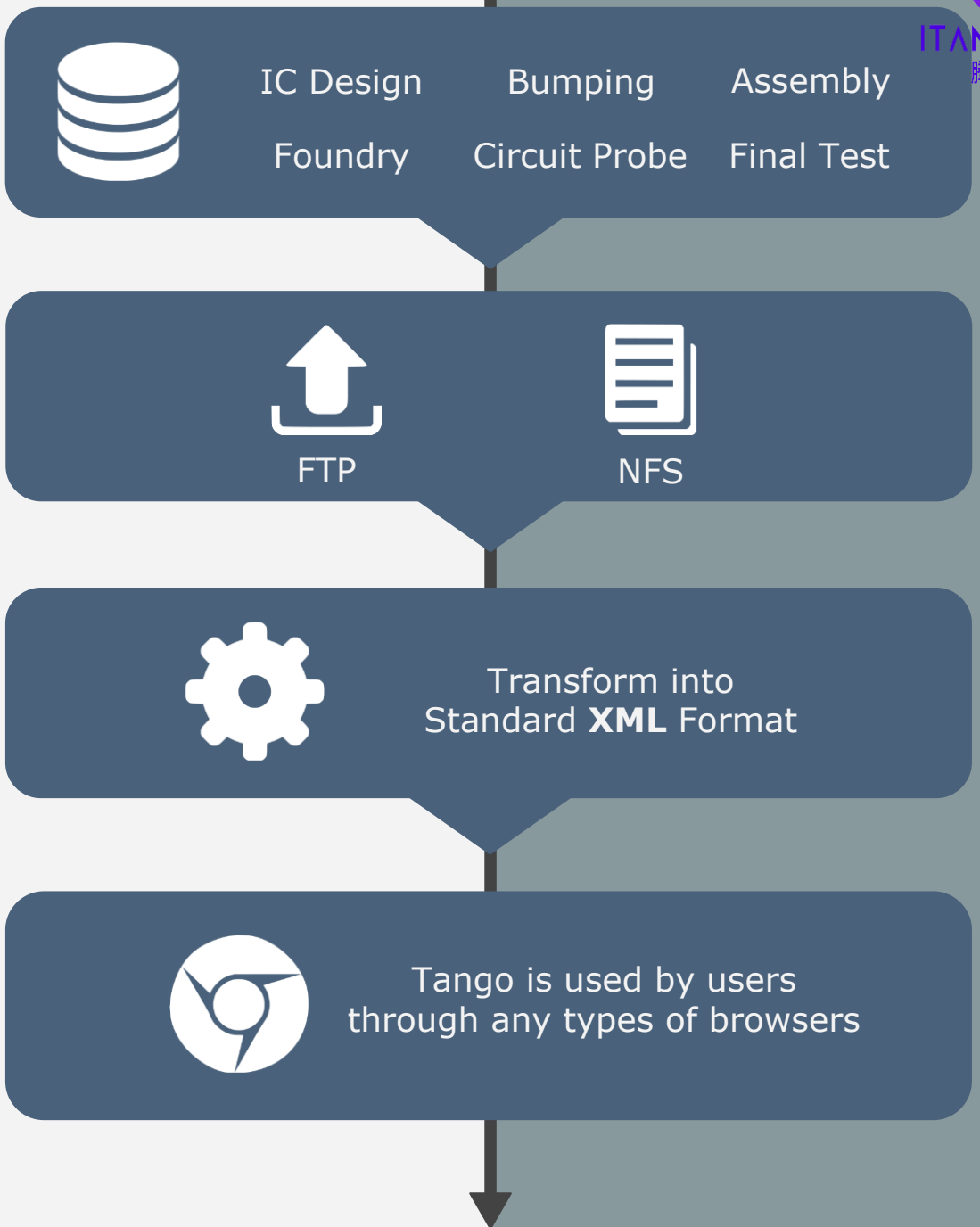
Tango solution helps you to alleviate fishing for a needle in the ocean nightmare and manage your production and yield ramp proactively.

We help you "Detect Your Process Excursion"

We provide an effective monitoring tool to help customers identify process excursion issues at early stage.

Bridge All the Data High Way

TANGO collect and aggregate data from multiple manufacturing sites and stages, then transform multiple data formats into the coherent format.



Bridge All the Data High Way

Data Integrity:
We extract, secure, clean and standardize the engineering data from multiple manufacturing sites and stages both internally or externally (subcontractors).

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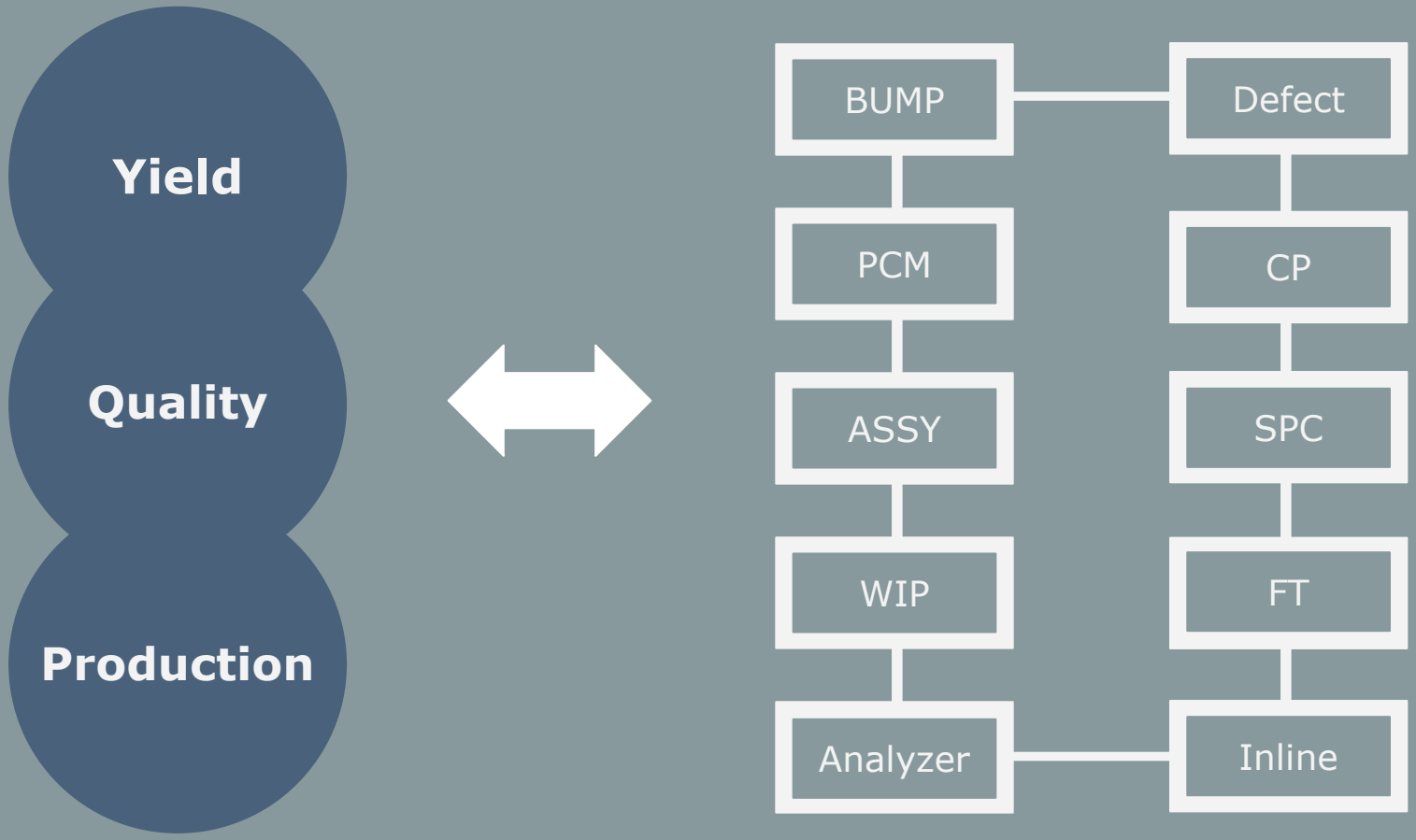

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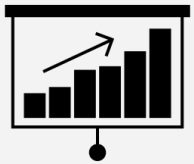
TANGO Solutions

We make “Big Data” transform into “Yield Enhancement”, “Quality Improvement” and “Production Efficiency”.

Early Excursion Detection
Yield Change Detection
Yield Trend Analysis
Recovery Bin Analysis

Yield Enhancement

Outlier Detection
Escape Prevention Rules
Statistical Process Control
Part Average Testing



Quality Improvement

Full SCM Visibility
Manufacturing Data Monitor
Wafer Map Gallery
Correlation Analysis
Product Sensitivity Analysis

Production Efficiency

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System Framework

Platform Framework

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Cloud Layer

Cloud Center

Oracle 10g/11g/12c/19c Database

Data Integration Layer

WIP Data
Machine Data
Defect DAta
Yield Data
Metrology Data

Data Integration and Exchange with Standard Data Format

Scheduling and Workflow Engine

Analytical Layer

Data Pre-process | Data Analysis | Core Algorithm

Analytical Engine | Visualization Engine | Adapter

Application Layer

Yield Management | Process Control Monitoring

Product Sensitivity Analysis | Outlier Detection

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Product Capabilities

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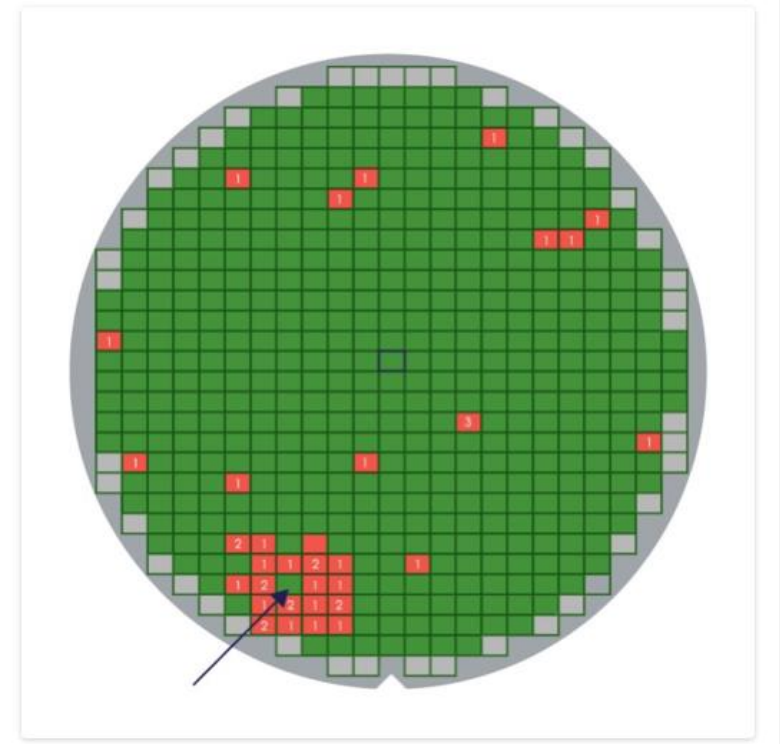
Data Hunting: Detect Suspect Area

We collect wafer maps and reconstruct and consolidate them to recognize failure patterns and remove the highly suspected area.



A good die in a bad neighborhood

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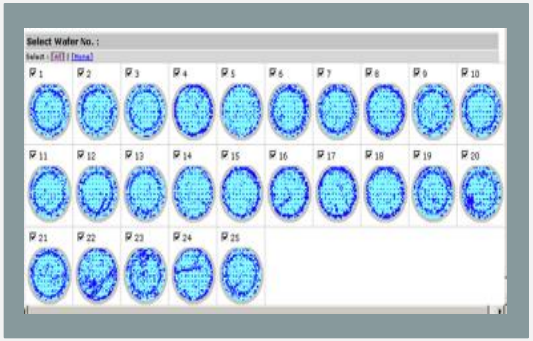
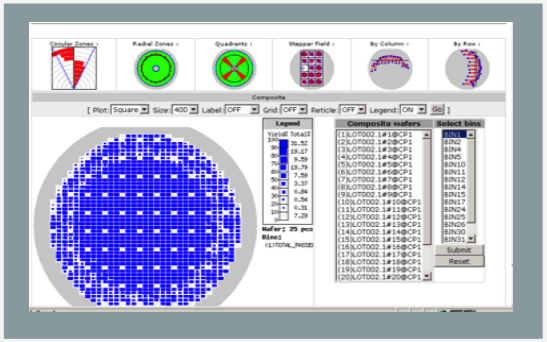
Data Hunting:
Detect Suspect Area

As the following steps

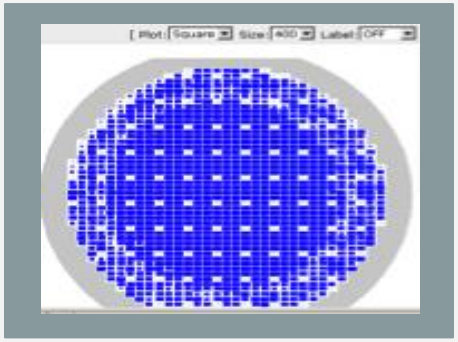
Select Wafer Map



Composite Wafer Map



Recognize Pattern



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Data Hunting:
Proactive Management

Automate outliner warming and data filtering is available to manage thousands of electronic characterized testing measures and parameters to improve operation efficiently and proactively.

Data Hunting:

As the following steps

Data Collecting and Monitoring

IC Design　Bumping　Assembly　Foundry　Circuit Probe　Final Test

Data Analysis

Outliners　Abnormal Parameters　Parts Issue　Failed Pattern　Abnormal Yield

Action and Improvement

Design Improvement　Parts Improvement　Process Improvement

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Data Hunting:
Supply Chain Traceability

In manufacturing process, systematic and parametric defects are buried throughout the entire supply chain process. Tracking down manufacturing issues is like looking for a needle in a haystack.

Tango solution helps to quickly identify highly correlated test pairs or parametric defects.

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Abnormal Yield

Defect

Customer Complain

RMA

IC Design

Foundry

Bumping

Circuit Probing

Assembly

Final Test

Process Issue

Design Issue

Parts Issue

Equipment Issue

Incident

Tango Solution

Insight

Data Hunting:

As the following steps

Data Hunting:
Supply Chain Traceability

We provide highly interactive data analyzer to accelerate the efficiency of correlation analysis.

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Parameter | Data Filter | Graph Setup

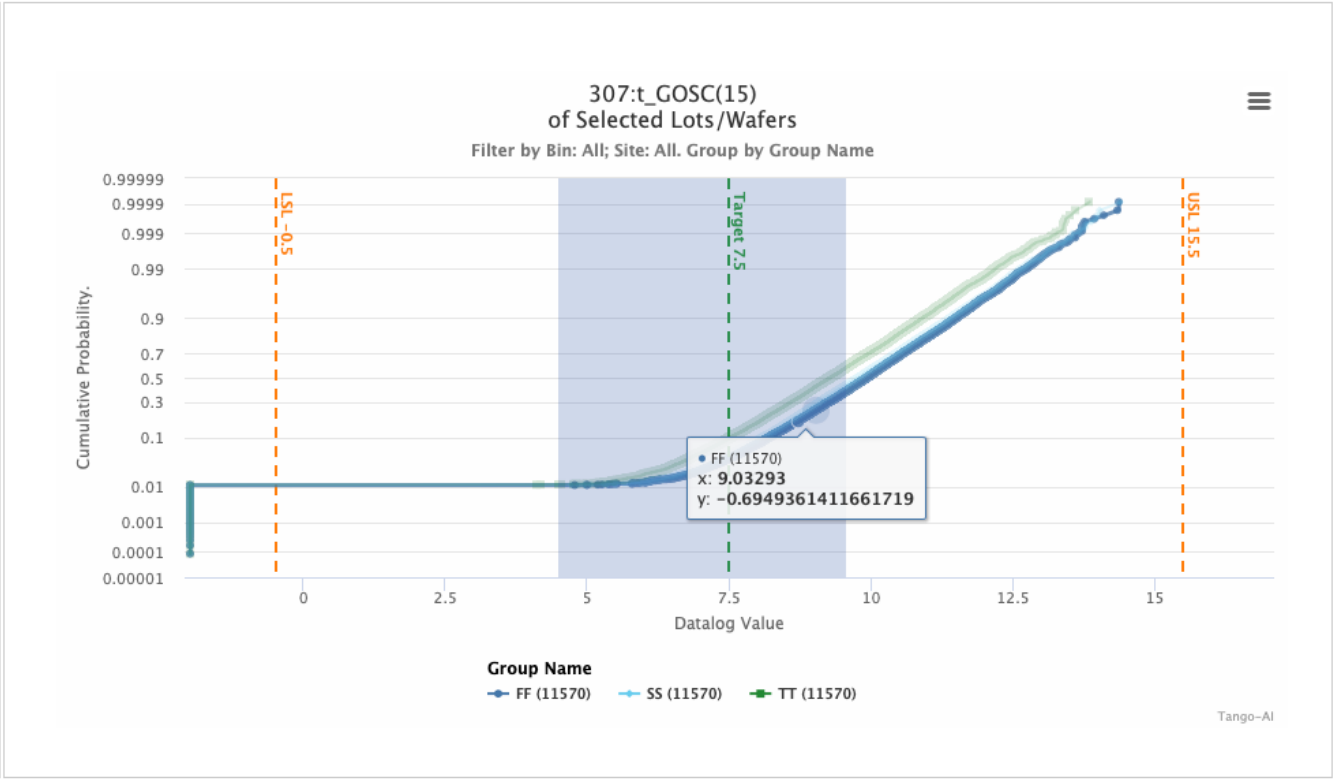
Graph Type: Probability Plot (P-Chart)

Group By: (3) Group Name

▸ **Grouping by Parameter will enable multiple selection of Parameter.**

Range: 1.2 * SPEC

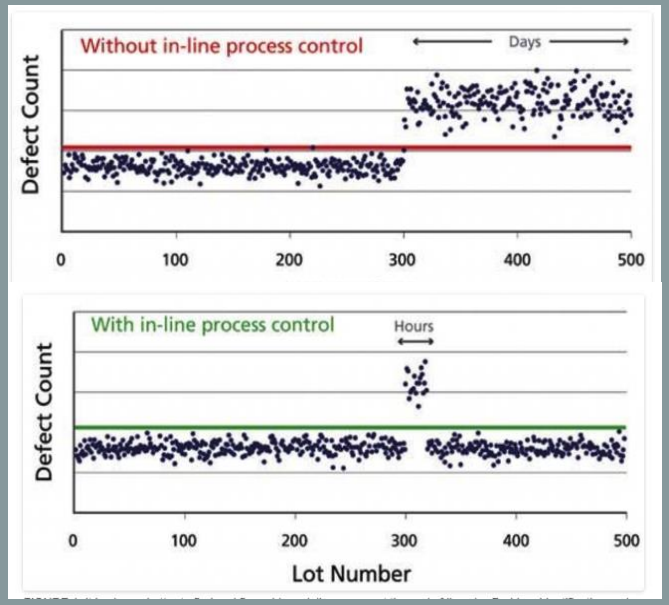
Color Preferences

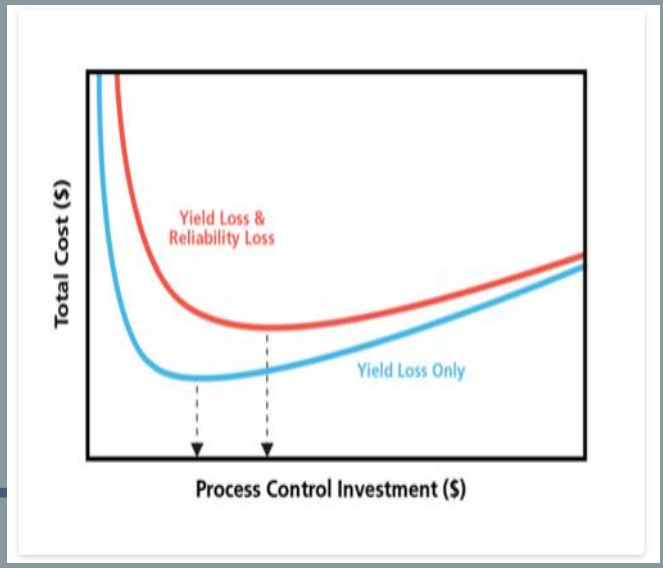


Detect Your Process Excursion:

Defect Is Expensive

The majority defect cost does not come from large excursions that cause significant yield loss which are usually identified and rectified very early on. Rather, the largest losses usually come from **small excursion that are difficult to detect**.



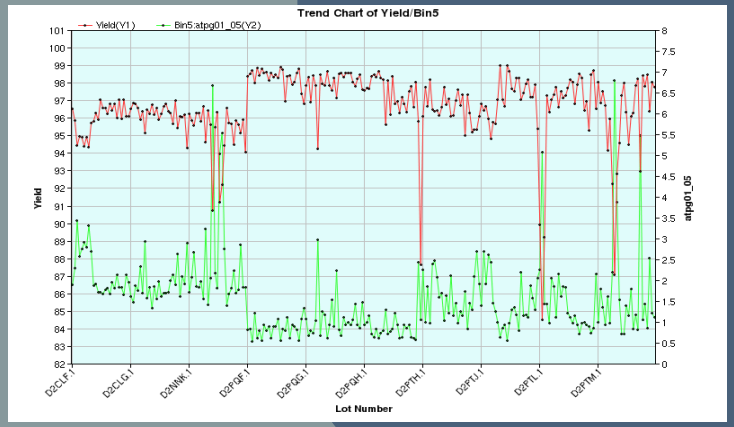


Source: Solid State Technology

Detect Your Process Excursion

✓ ✗	Rank #	r^2	Group1	Group2	Chart
☑	1	0.862032	CONTI_PP_D18	CP1 Bin4	
☑	2	0.847833	CONTI_NP_D18	CP1 Bin4	
☑	3	0.719595	BVDS_PAA33_10_D3	CP1 Bin4	
☑	4	0.584267	IDSAT_PAA33_10_D3	CP1 Bin4	
☑	5	0.513881	VTI_NAA18_10_D18	CP1 Bin4	
☐	6	0.435769	RSFV_PP_D18_556	CP1 Bin4	
☐	7	0.426996	SPAFI_M6_D46	CP1 Bin4	

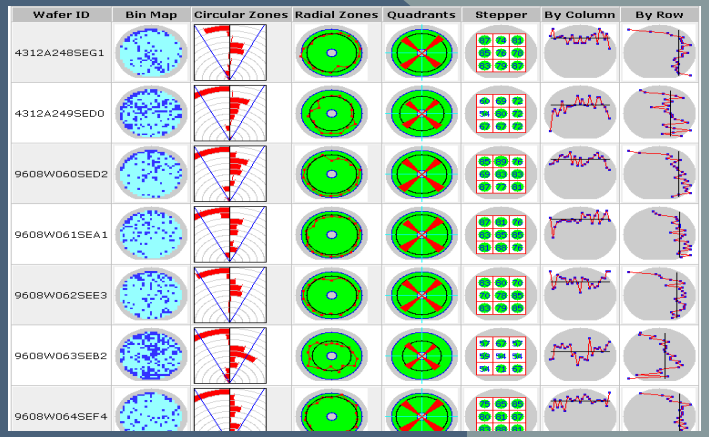
List R-Square Ranking
and Highlight the Top 5



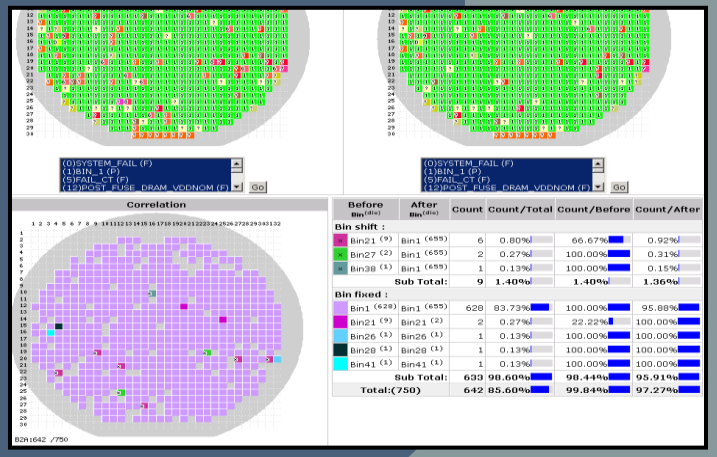
Provide Yield/
Bin Trend Chart

Detect Your Process Excursion

Exhibit Wafer Gallery



Conduct Correlation for wafer re-probing



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Test Time Reduction(TTR)

The main idea of TTR is to reduce test items without losing product quality，there are two general methods below：

1.By the large number of ICs，remove zero failure rate items

2.By the large number of ICs，remove low PPM failure rate items

But none of these methods considering the variation of product line，and most important of all，these cant’ alarm quality shift.

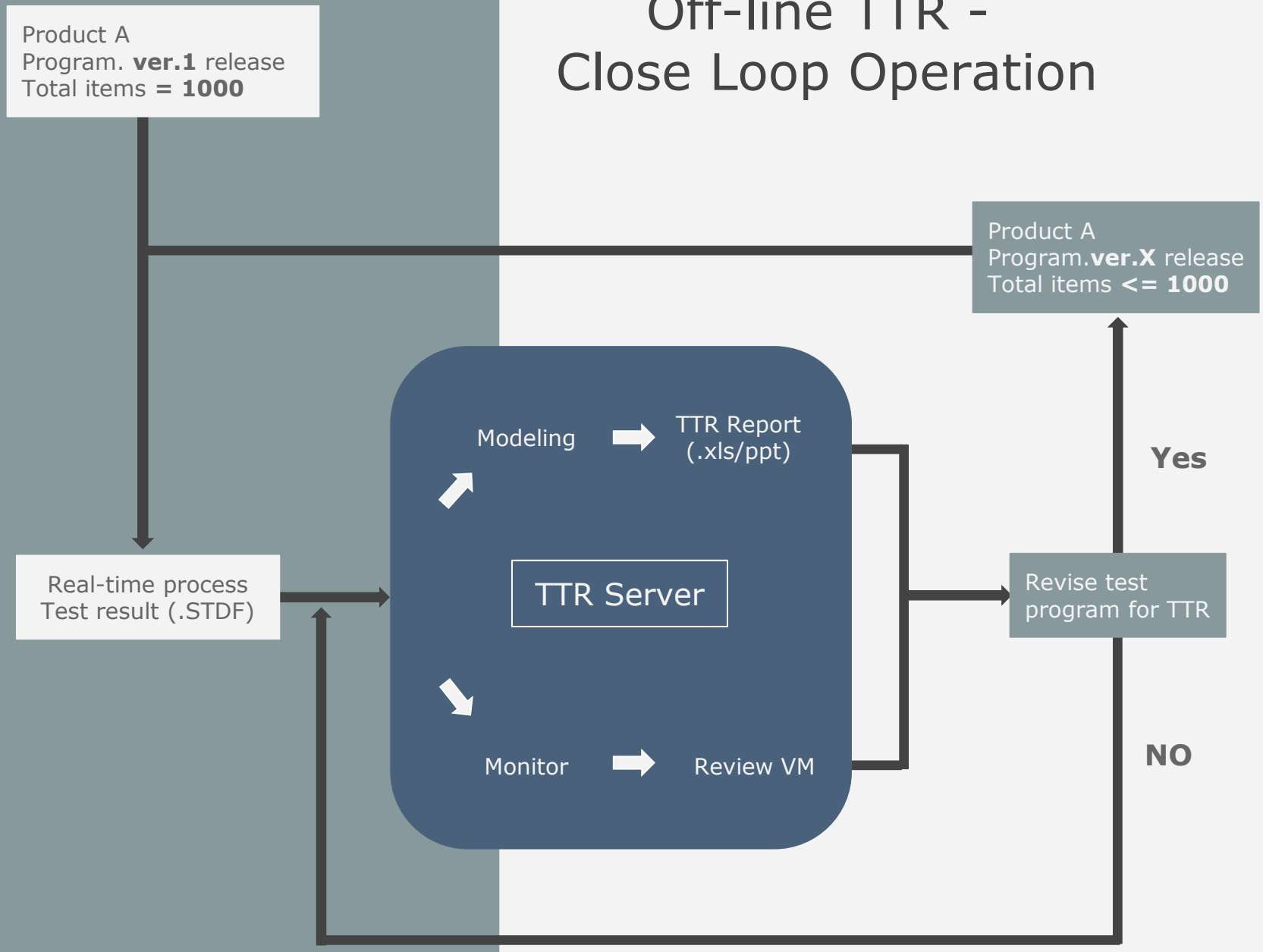
Strategy：Find the TTR items which can be replaced by other test items immediately, and monitoring them through Virtual Metrology(VM)

1.Item Filter:find the TTR items (Correlation/Explanation/Replacement)

2.User confirm TTR Summary、decide TTR List and generate Recipe File

3.Monitor prediction(VM) value of TTR items

Off-line TTR - Close Loop Operation



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AI Techniques for Wafer Map Classification

Take Edge and Line / Scratch Pattern as Example

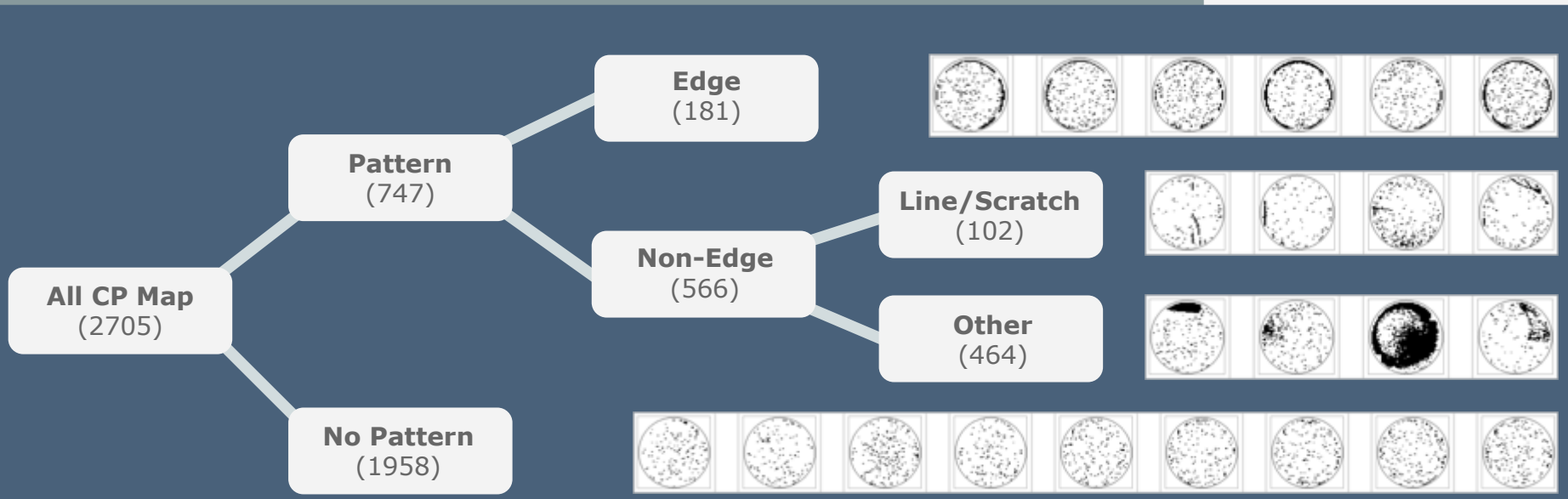
When the bin map exhibits specific patterns, it is usually a clue that equipment problems or process variations have occurred.

Visual inspection by engineers:

- Potential misjudgment due to human fatigue.
- The process can incur significant personnel costs.

Developed Methods Application

Customer A, 2020/03 all wafer



Step 1: Pattern Map Detection

Step 2: Edge Pattern Classification

Step 3: Line Pattern Detection

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PAT

GPAT - Spatial Correlation

1.GDBC (Good Die in a Bad Cluster)

- Type A(4) / Type B(8)
- By User Define
- Cut Wafer Edge N Rings

2.Stack / Reticle (by Wafer / Lot)

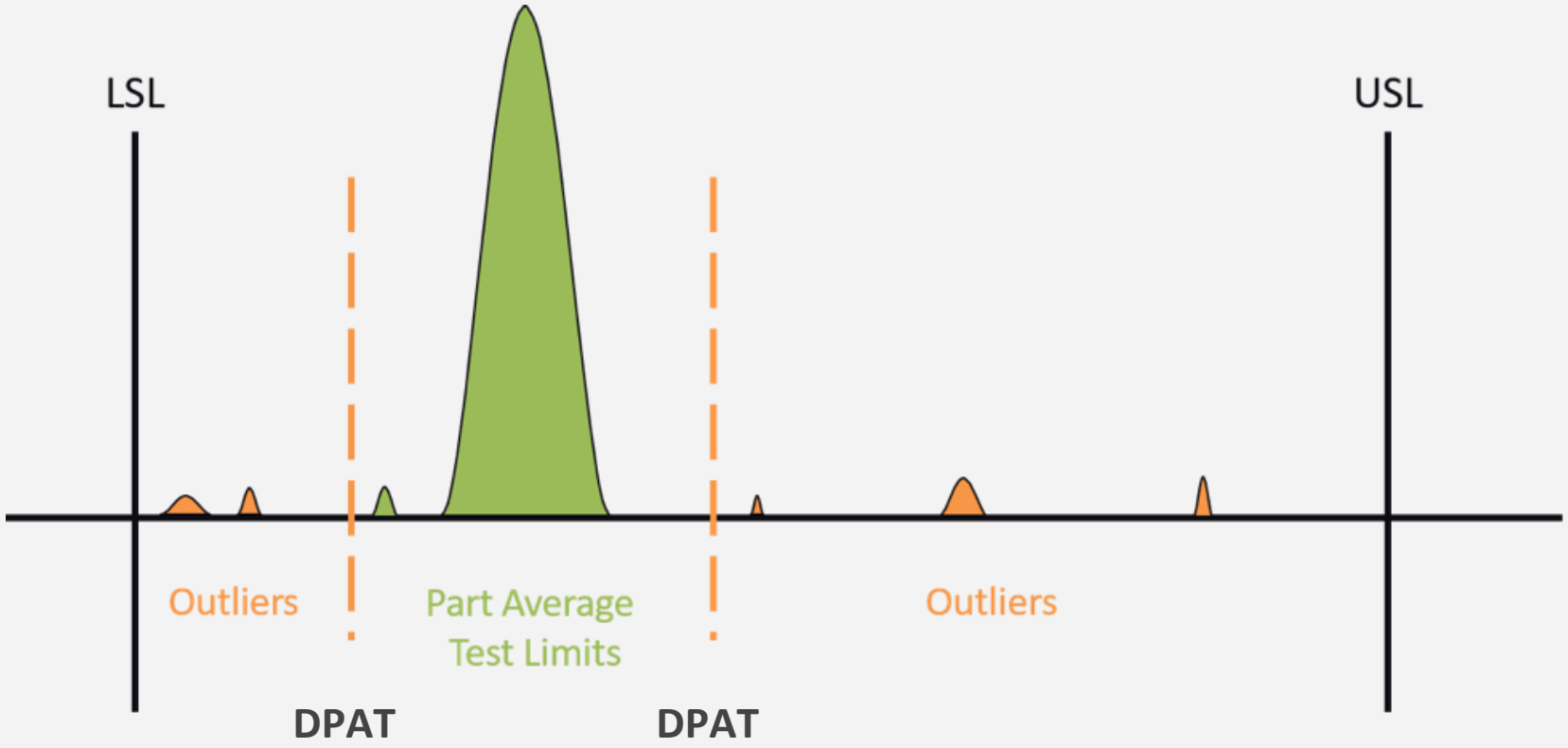
PPAT - Statistical Outliers

- AEC Standard
- User Define

PPAT

- According to AEC_Q001_Rev D
- Assumption on Gaussian distribution of the test parameters
- Static PAT limit (production, n>6) median+-6*[(Q3-Q1)/1.35]
- Dynamic PAT limit [passing Static PAT] median +- 6*IQR/1.35

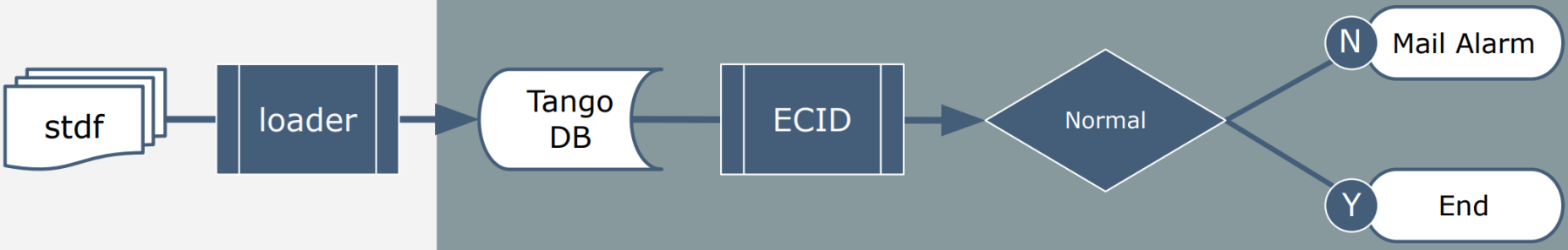
PAT Demonstration



2024 New Functions

ECID Check :

- Pre-define
  1. Test Numbers or Key word of test names (test program)
  2. Checking Rule
- Checking Flow



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Yield Simulation

A Flexible Approach to Simulating Yield
Based on Stop on Fail Strategy

Order by Test Sequence Displayed in 2 Types of Spec

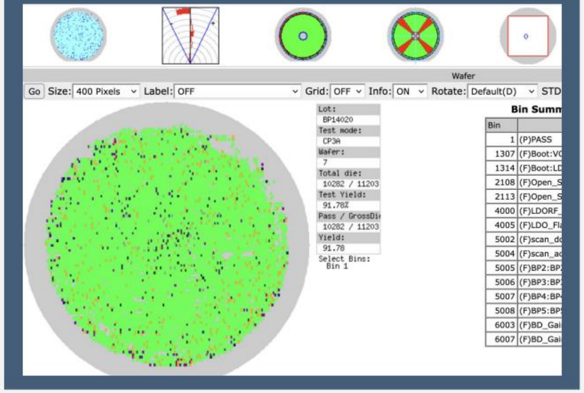
ExecCount_oos	FailCount_oos	FailRate_oos	ExecCount_nSig	FailCount_nSig	FailRate_nSig
243392	0	0.0	243392	69	0.028
243392	0	0.0	243323	175	0.072
243392	0	0.0	243148	16	0.007
243392	0	0.0	243132	49	0.02
243392	0	0.0	243083	23	0.009
243392	0	0.0	243060	26	0.011
243392	0	0.0	243034	23	0.009
243392	0	0.0	243011	25	0.01
243392	0	0.0	242986	75	0.031
243392	0	0.0	242911	16	0.007
243392	0	0.0	242895	25	0.01
243392	0	0.0	242870	24	0.01
243392	0	0.0	242846	5	0.002
243392	0	0.0	242841	9	0.004
243392	0	0.0	242832	0	0.0
243392	0	0.0	242832	618	0.254
243392	39	0.016	242214	244	0.101
243353	11	0.005	241970	111	0.046

Define Spec, Bin and Limits Criteria

LSL	Target	USL	SBin	HBin
0.25	0.725	1.2	2001	2
0.25	0.725	1.2	2013	2
0.25	0.725	1.2	2014	2
0.25	0.725	1.2	2015	2
0.25	0.725	1.2	2016	2
0.25	0.725	1.2	2017	2

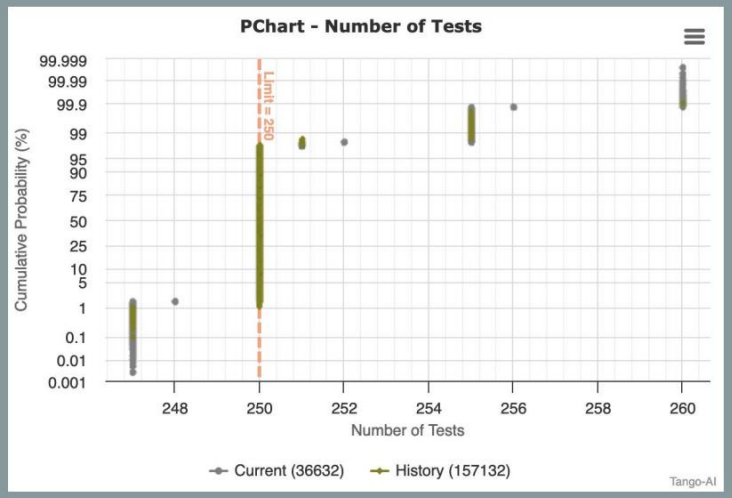
LSL	Target	USL	Center	Variation	nLower	nUpper
0.25	0.725	1.2	○ Mean ◉ Median	○ Std ◉ RStd	6	6
0.25	0.725	1.2	○ Mean ◉ Median	○ Std ◉ RStd	6	6
0.25	0.725	1.2	○ Mean ◉ Median	○ Std ◉ RStd	6	6
0.25	0.725	1.2	○ Mean ◉ Median	○ Std ◉ RStd	6	6
0.25	0.725	1.2	○ Mean ◉ Median	○ Std ◉ RStd	6	6
0.25	0.725	1.2	○ Mean ◉ Median	○ Std ◉ RStd	6	6

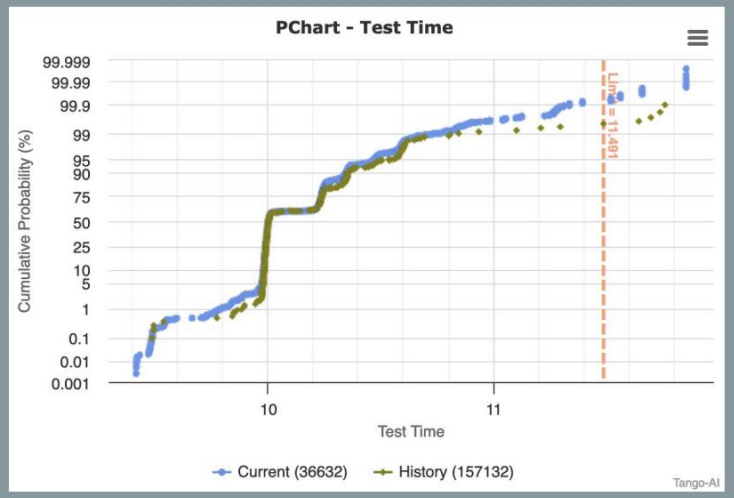
Generate New CP Map

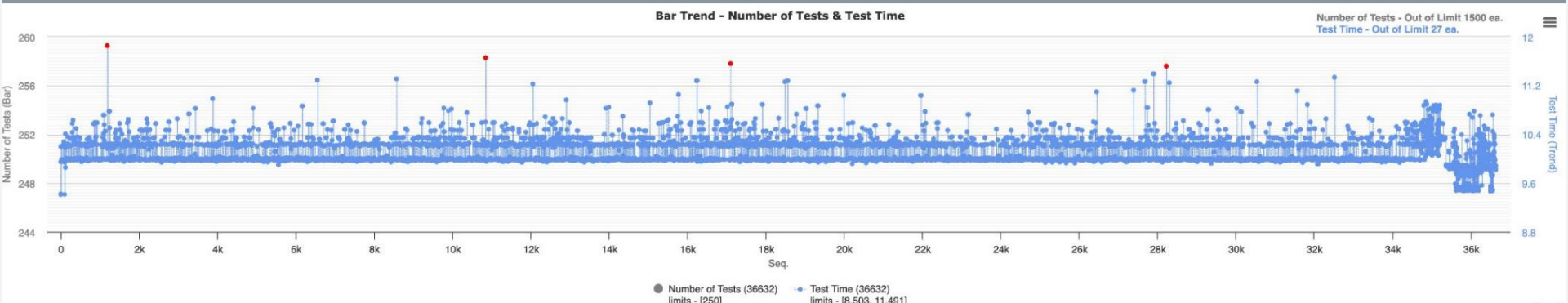


FT Anomaly Detection

Efficiently detect outliers from pass die based on number of tests and test time for quality improvement.







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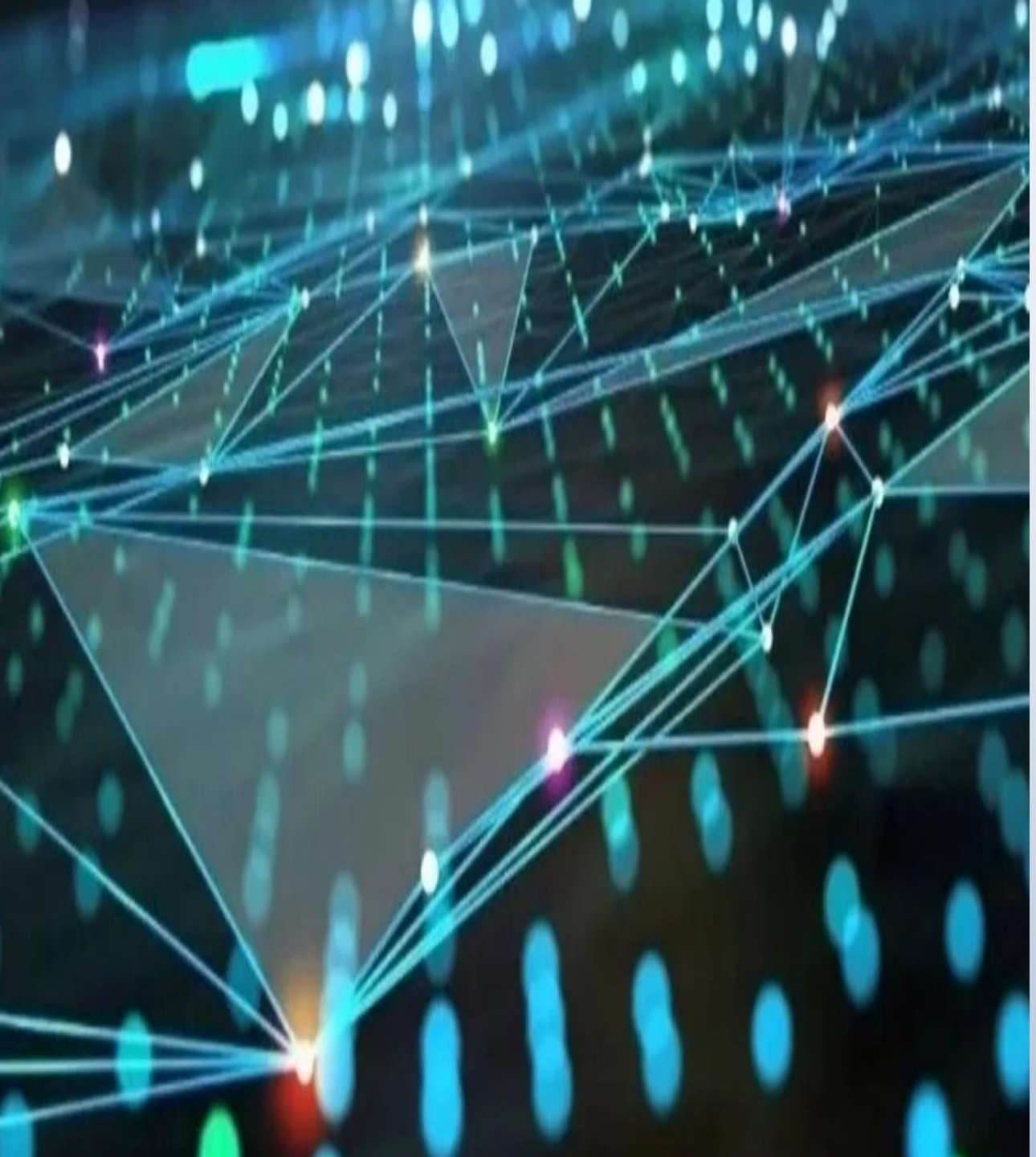
Thank You



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