APPENDIX C

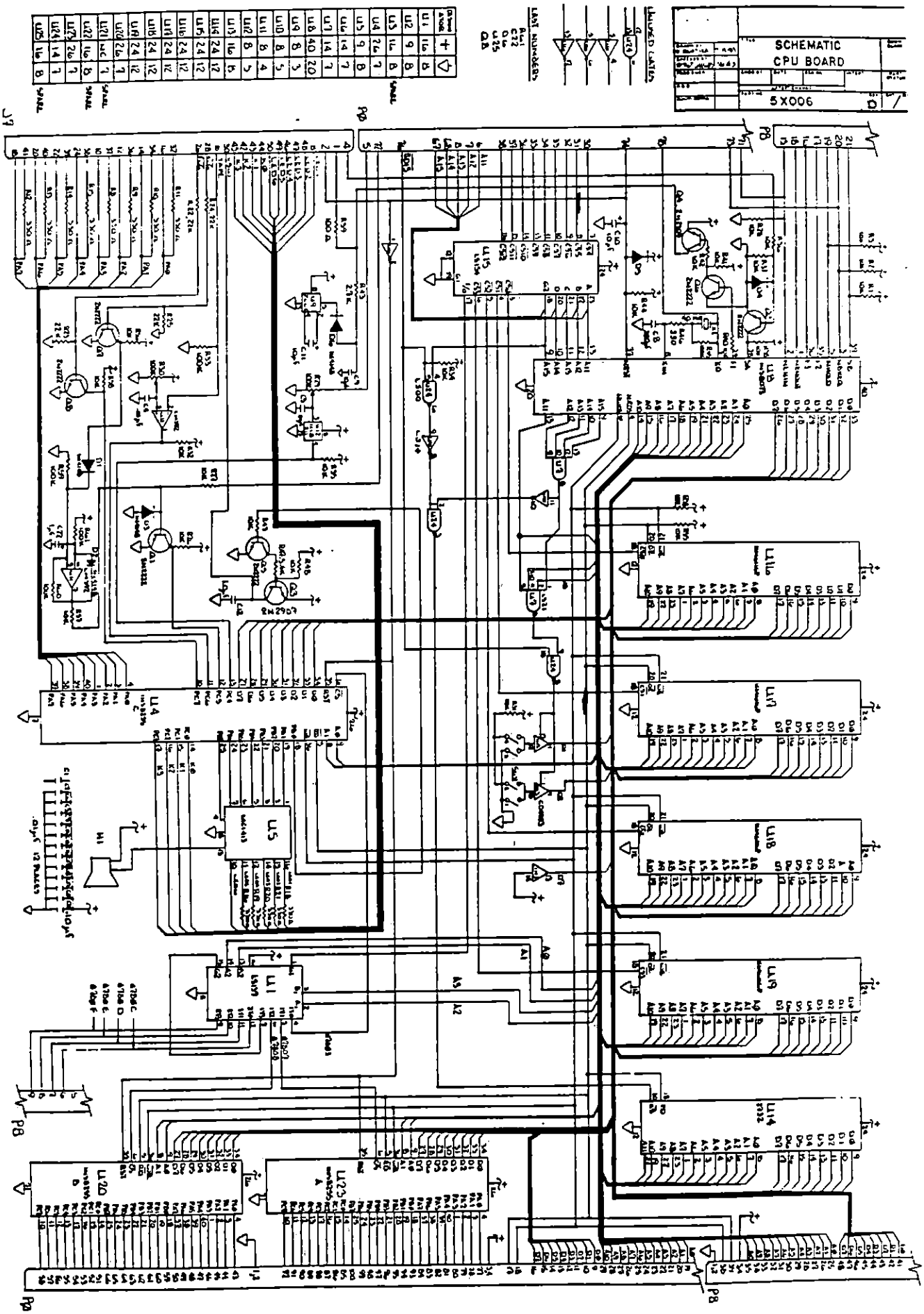
MOTHER BOARD INTERCONNECT LIST

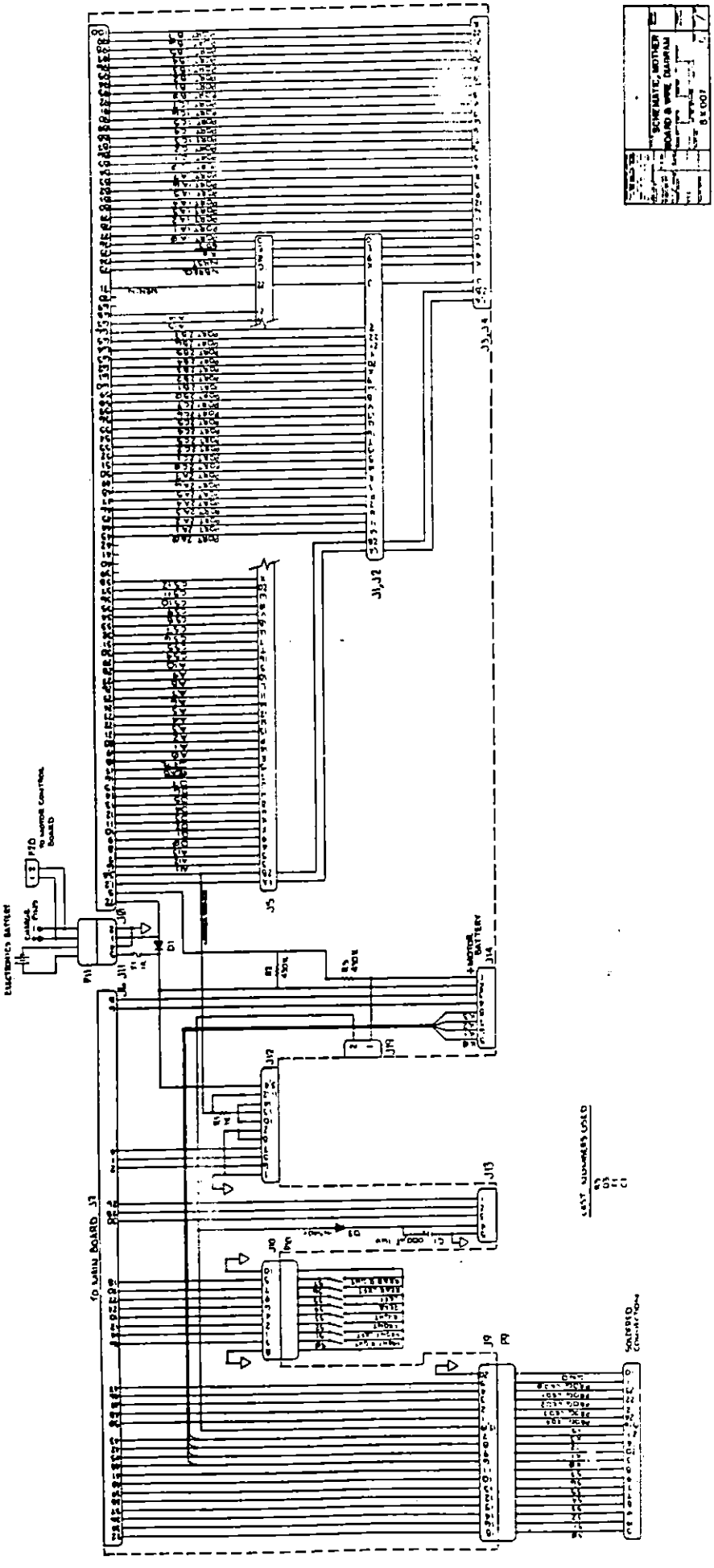
Figure 4.
Mother Board Interconnect List

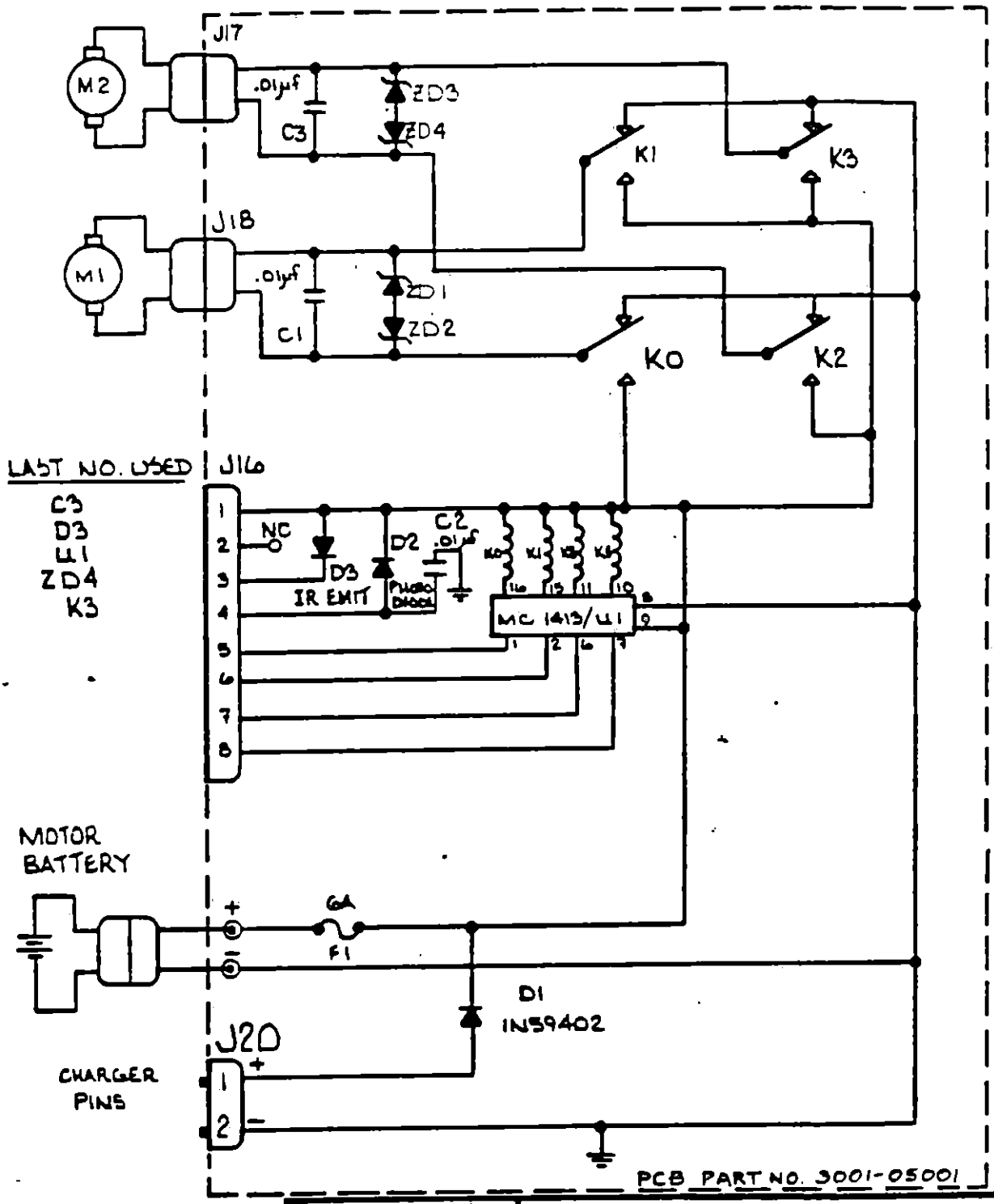
Connector	Configuration	Pin Centers	Intended Use
J0	2x50 pin	.125 centers	CPU board
J5	2x22 pin	.156 centers	Memory option
J1 & J2	2x22 pin	.156 centers	I/O boards (parallel from INS8255 A)
J3 & J4	2x22 pin	.156 centers	I/O boards (parallel from INS8255 B)
J6	50 pin	.100 centers	Mother board to CPU board
J9	20 pin	.100 centers	LED card
J10	10 pin	.100 centers	Bumper switches
J11	4 pin	.156 centers	Main battery and recharge lines
J12	14 pin	DIP socket	Interface panel
J13	5 pin	.100 centers	Sonar cable
J14	8 pin	.100 centers	Motor control board
J19	2 pin	.156 centers	Sonar/LED switch cable

APPENDIX D

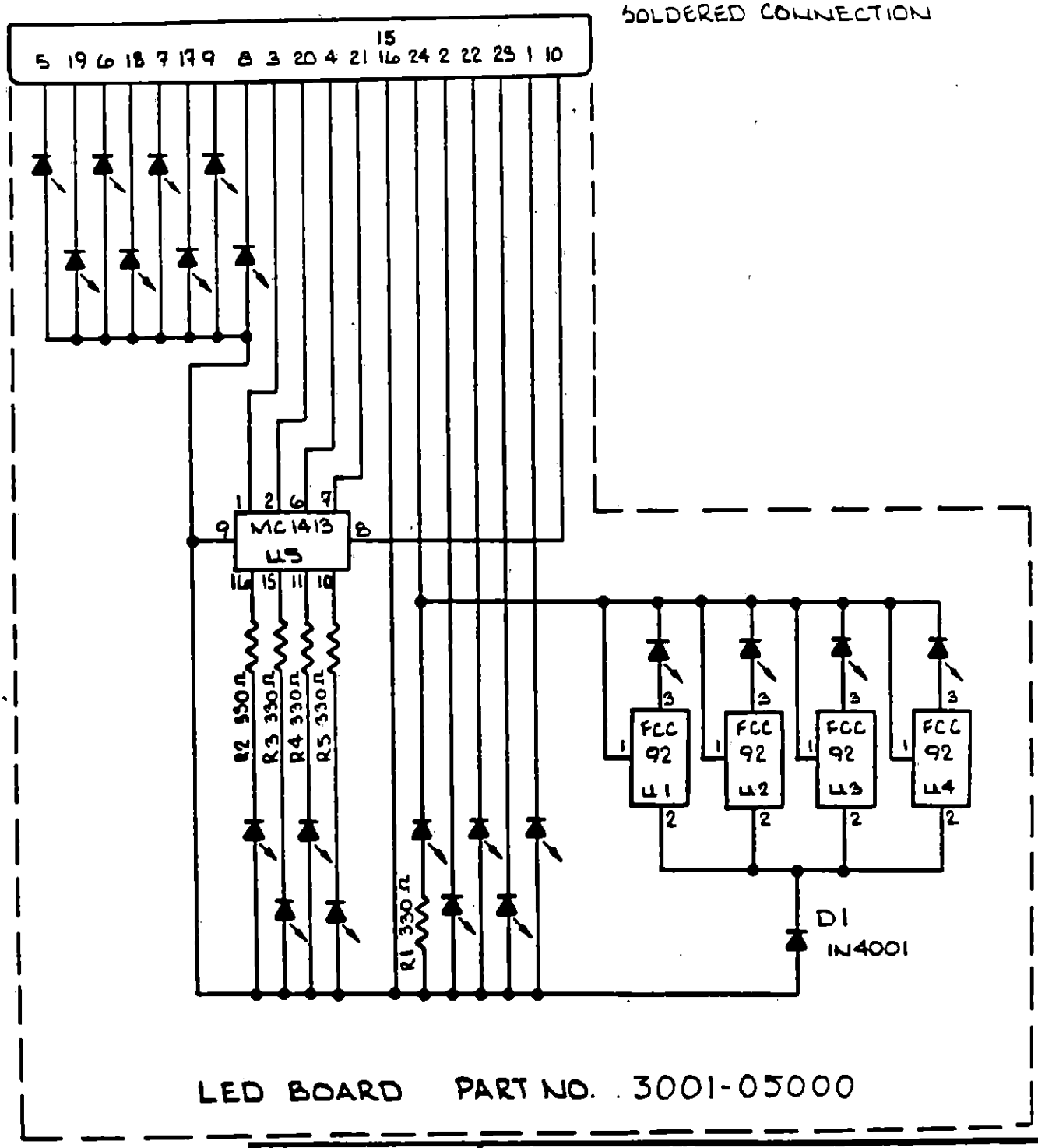
RB5X SCHEMATICS


SCHEMATIC
CPU BOARD
5X006

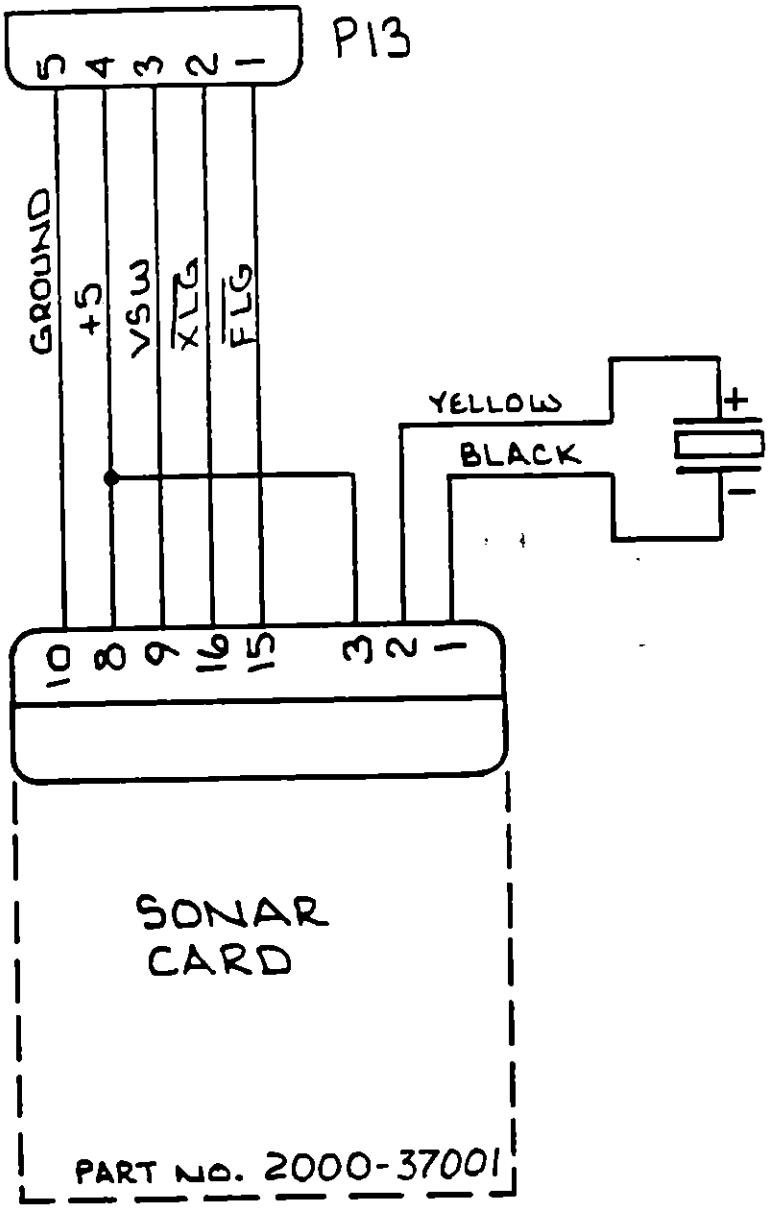




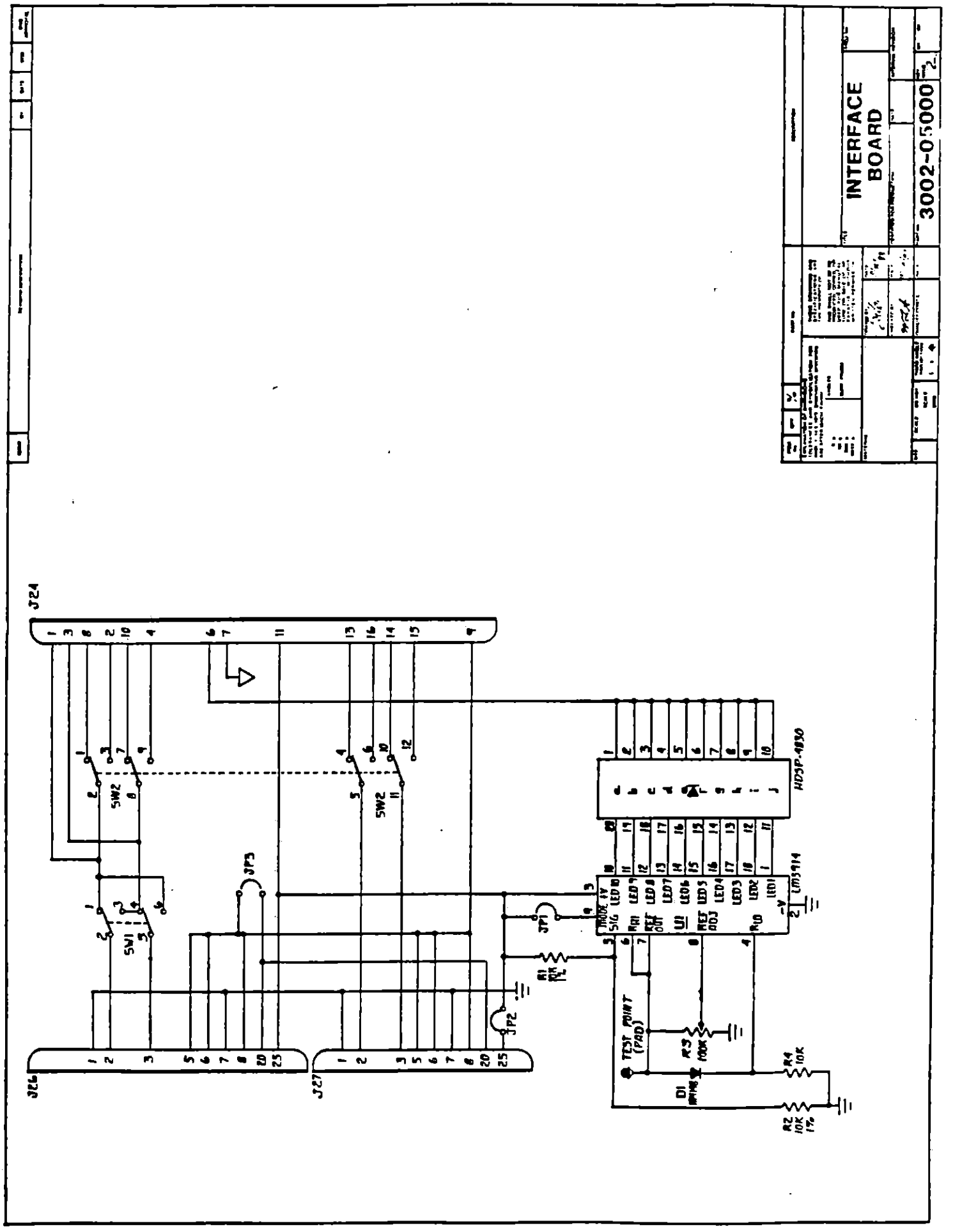
DRAWN BY D. QUATIER	9-12-93	TITLE SCHEMATIC MOTOR CONTROL BD.			COMM CLASS
CHECKED BY	7/20/92	CHGD BY	DATE	ECO NO.	INTENT
PROD ENGR		LATEST CHANGE			PART STATUS
R & D		PART NO. 3001-02007		REV B	SHT 1 OF
QUALITY CONTROL					

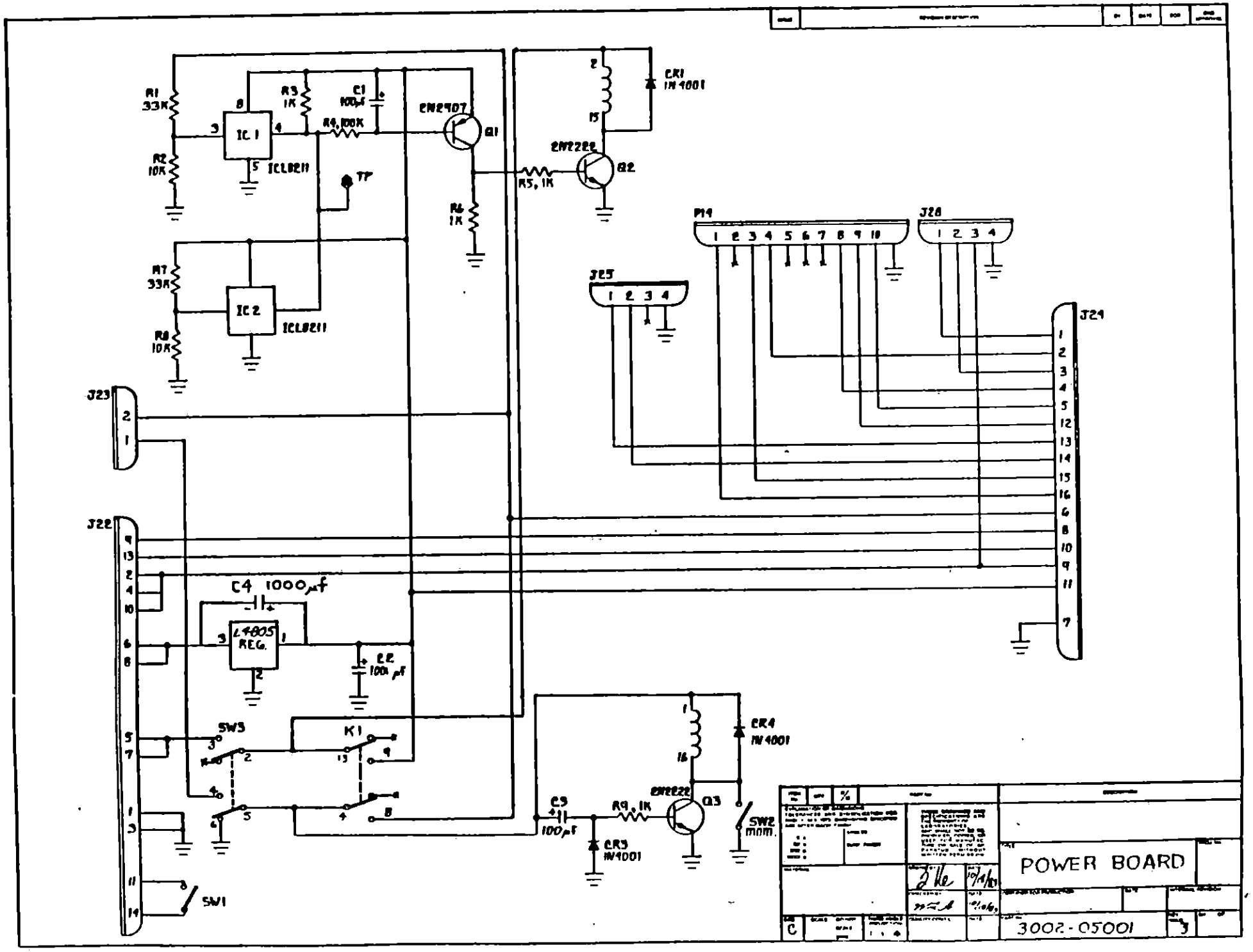


DRAWN BY D. Quattier	7-12-83	TITLE SCHEMATIC, LED BOARD					COMM CLASS
CHECKED BY [illegible]	7/19/83						
PROD ENGR		CHGD BY	DATE	ECO NO.	INTENT		PART STATUS
R & D		LATEST CHANGE					
QUALITY CONTROL		PART NO. 5001-02002				REV A	SHT 1 OF 1



DRAWN BY D.GRATIER 7-12-83	TITLE SONAR CARD, CONNECTION					COMM CLASS
CHECKED BY [illegible] 7/19/83						
PROD ENGR	CHGD BY	DATE	ECO NO.	INTENT		PART STATUS
R & D	LATEST CHANGE					
QUALITY CONTROL	PART NO.				REV	SHT 1 OF


INTERFACE BOARD
3002-05000
J24
J26
J27
SW1
SW2
JP1
JP2
JP3
R1
R2
R3
R4
D1
TEST POINT (PAD)
LM3914
HDSP-4830


R1 33K
R2 10K
R3 1K
C1 100µf
R4, 100K
IC 1
ICL8211
TP
2N2907
Q1
R6 1K
R7 33K
R8 10K
IC 2
ICL8211
2
15
CR1 IN4001
2N2222
Q2
R5, 1K
P14
J28
J25
J24
J23
J22
C4 1000µf
LM340S REG.
C2 100µf
SW3
K1
SW1
CR4 IN4001
C3 100µf
R9, 1K
2N2222
Q3
CR3 IN4001
SW2 mom.
POWER BOARD
3002-05001

APPENDIX E

UTILITY SOFTWARE MODULE ROUTINE LISTINGS

UTILITY SOFTWARE MODULE SUBROUTINES

The standard utility software module that comes with each RB5X contains several assembly-language subroutines. We introduced you to three of these -- the self-diagnostic routine, Beta with Sonar, and Tiny BASIC command mode -- in Section B, "Getting Started."

There are several other subroutines in the software on this module that you can include in your Tiny BASIC programs using the LINK command. Complete listings of these assembly-language subroutines are contained in Appendix 3, "Utility Module Subroutine Listings."

Speech

If you have the optional RB5X voice/sound synthesis package, you can include this subroutine in your Tiny BASIC program to run the speech synthesizer. It can be accessed at the entry point LINK #82CE.

Before running this assembly-language subroutine, you should do the following:

a. Read the instructions that come with your voice/sound synthesis package.

b. Prepare the LED I/O port by entering the Tiny BASIC statement "@#7803=#98."

c. Prepare the sound I/O ports by entering the Tiny BASIC statement "@#780B=#A7."

d. Load a list of phonemes into the robot's memory, making sure that the last one is the "STOP" phoneme.

e. Load the Tiny BASIC variable S with the starting address of the list of phonemes.

While RB5X is running this subroutine, all of its LEDs are on; they remain lit until the robot has completed its speech.

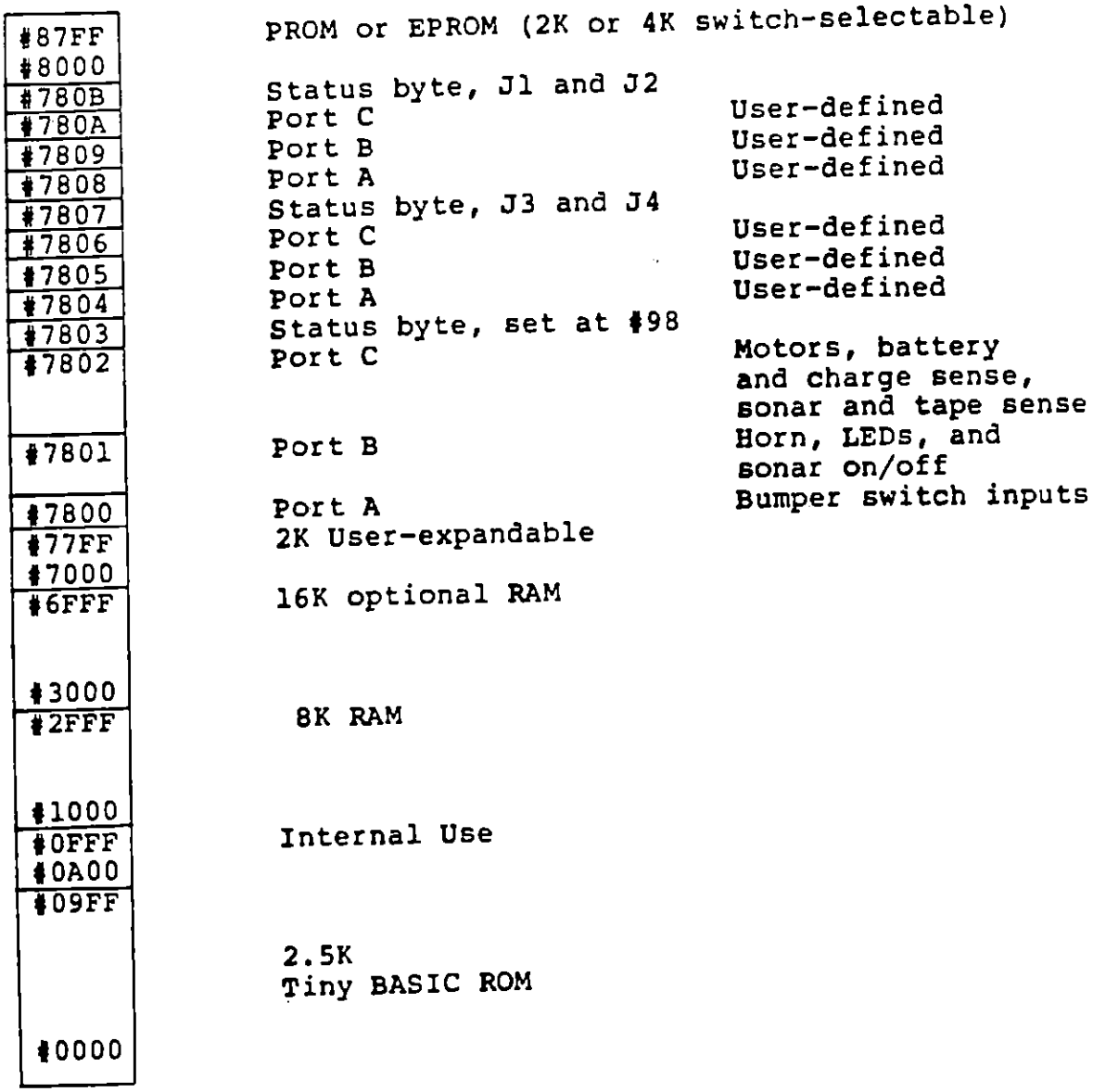
Sonar Ranging

This routine returns a number in Tiny BASIC variable D that is proportional to the distance the sonar sensor is from an object.

APPENDIX F

MEMORY MAP

Figure 6.
Memory Map



APPENDIX G

FUNCTIONS

Figure 11.
Functions

Function	Address	Data Bit	Active	Turn-On	Mask
Horn	$7801	D7	High	$80	---
Relay K0	$7802	D0	High	$01	---
Relay K1	$7802	D1	High	$02	---
Relay K2	$7802	D2	High	$04	---
Relay K3	$7802	D3	High	$08	---
Battery Sense	$7802	D4	Low	---	$10
Sonar On/Off	$7801	D0	High	$01	---
Sonar Transmit	$7802	D5	Low	---	$20
Sonar Echo	$7802	D7	High	---	$80
Charge Sense	$7802	D5	Low	---	$20
Tape Sense	$7802	D6	Low	---	$40
LED 1 (infrared LED for tape sense)	$7801	D1	High	$02	---
LED 2	$7801	D2	High	$04	---
LED 3	$7801	D3	High	$08	---
LED 4	$7801	D4	High	$10	---
LED 5	$7801	D5	High	$20	---
LED 6 (and all flashing LEDs)	$7801	D6	High	$40	---

APPENDIX H

MOTOR CODES AND RELAY/MOTION ASSIGNMENT

Figure 12.
Motor Codes

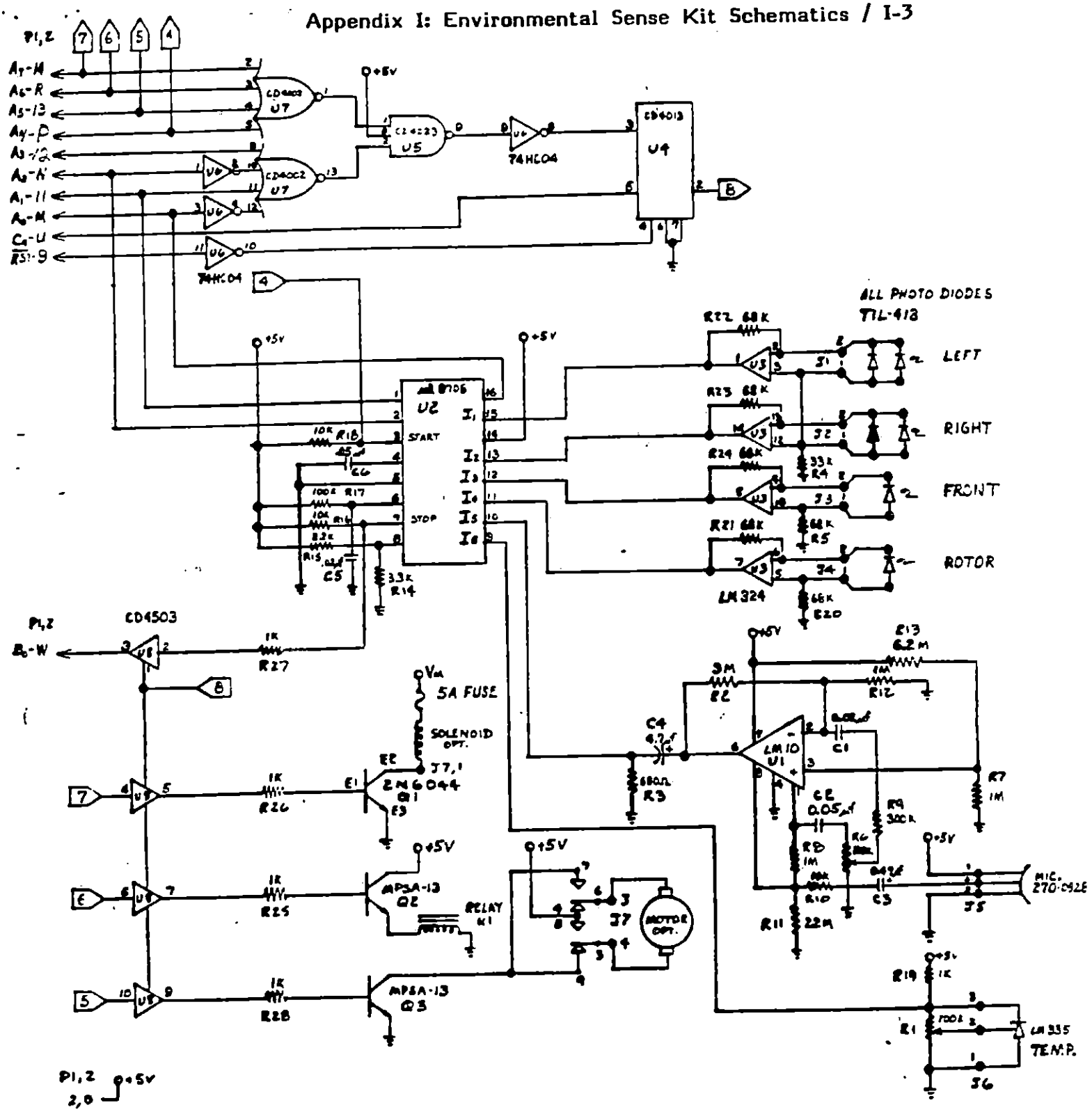
Functions	Data Byte	Decimal
Off	00	0
Left Forward	01	1
Left Reverse	02	2
Off	03	3
Right Reverse	04	4
Clockwise Spin	05	5
Reverse	06	6
Right Reverse	07	7
Right Forward	08	8
Forward	09	9
Counterclockwise Spin	0A	10
Right Forward	0B	11
Off	0C	12
Left Forward	0D	13
Left Reverse	0E	14
Off	0F	15

Relay/Motion Assignments

Relay On	Motion
K0	Left Forward
K1	Left Reverse
K2	Right Reverse
K3	Right Forward

APPENDIX I

ENVIRONMENTAL SENSE KIT SCHEMATICS



P1,2 +5V
2,B
1,A

NOTE: ALL RESISTORS ¼ W, 5%
● REMOTE CONNECTION
GATES NOT USED:
74HC04 - 2
CD4503 - 2
CD4023 - 2
CD4013 - 1

RB ROBOT CORP.
CRT: FIREMAN/ENVIRONMENTAL SENSE DATE: 5-7-84 CHECKED: 9-19-84 [illegible]

APPENDIX J

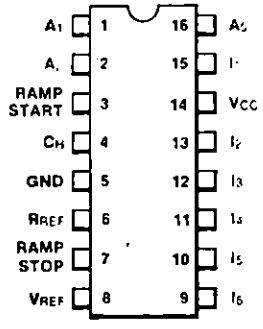
ESK CHIP DATA SHEETS

GENERAL DESCRIPTION — The μA9708 is a single slope 8-bit, 6-channel ADC subsystem that provides all of the necessary analog functions for a microprocessor-based data control system. The device uses a microprocessor system like the F3870 or F6800 to provide the necessary addressing, timing and counting functions and includes a 1 of 8 decoder, 8-channel analog multiplexer, sample and hold, ramp integrator, precision ramp reference, and a comparator on a single monolithic chip.

- MPU COMPATIBLE
- EXCELLENT LINEARITY OVER FULL TEMP RANGE - ±0.2% MAX
- TYPICAL 300 μs CONVERSION TIME PER CHANNEL
- WIDE DYNAMIC RANGE INCLUDES GROUND
- AUTO-ZERO AND FULL-SCALE CORRECTION CAPABILITY
- RATIOMETRIC CONVERSION — NO PRECISION REFERENCE REQUIRED
- SINGLE-SUPPLY OPERATION
- TTL COMPATIBLE
- DOES NOT REQUIRE ACCESS TO DATA BUS OR ADDRESS BUS

CONNECTION DIAGRAM
16-PIN DUAL IN-LINE

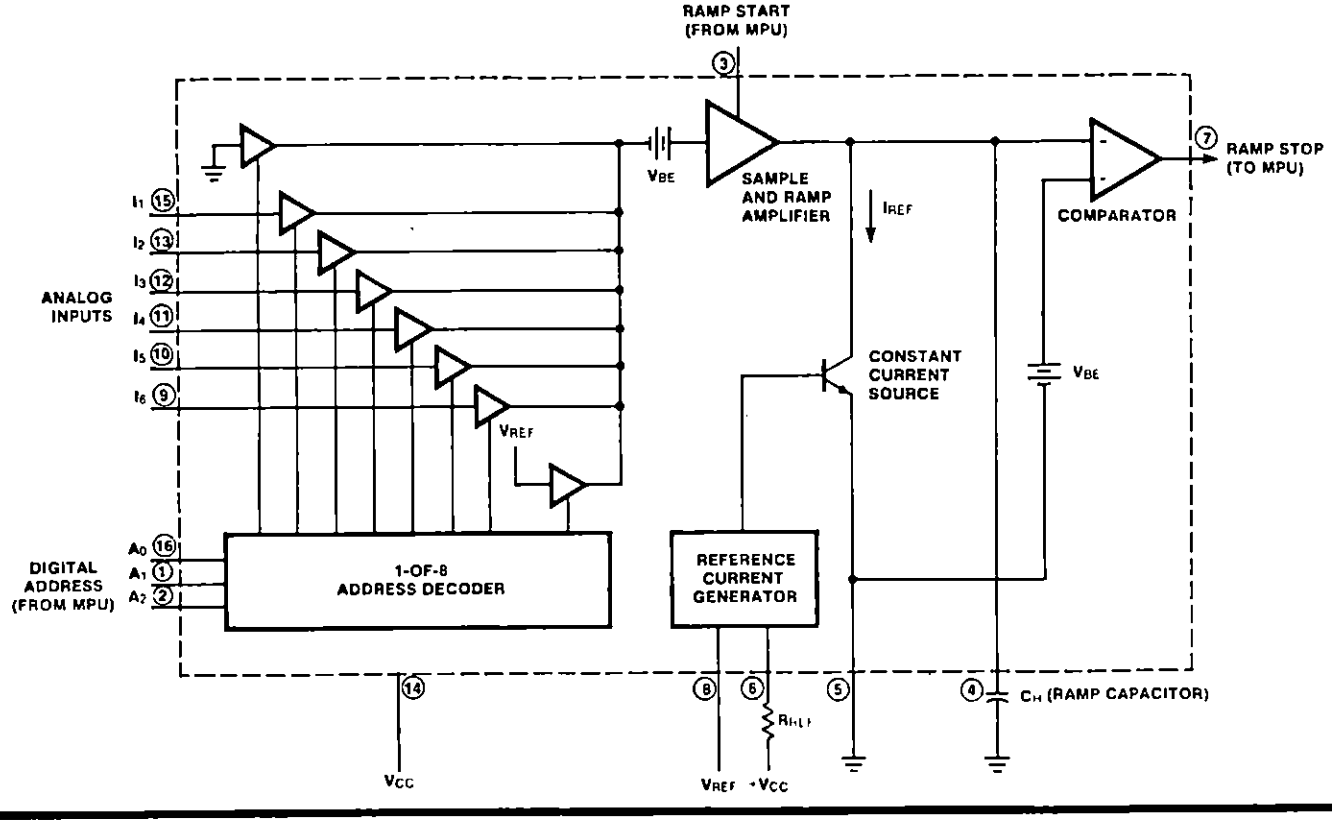
(TOP VIEW)
PACKAGE OUTLINES 7B 9B
PACKAGE CODES D P



ORDER INFORMATION

TYPE	PART NO.
μA9708	μA9708DM
μA9708	μA9708DC
μA9708	μA9708PC

BLOCK DIAGRAM



FAIRCHILD

ABSOLUTE MAXIMUM RATINGS

Supply Voltage (V_{CC})	18 V
Comparator Output (Ramp Stop)	-0.3 V to +18 V
Analog Input Range	-0.3 V to 30 V
Digital Input Range	-0.3 V to 30 V
Output Sink Current	10 mA
Operating Temperature Range	
μA9708PC, μA9708DC	0° C to 70° C
μA9708DM	-55° C to 125° C
Storage Temperature Range	-65° C to +150° C
Continuous Total Dissipation	
Ceramic DIP Package	900 mW
Plastic DIP Package	1000 mW
Pin Temperature, Ceramic DIP (Soldering, 60 s)	300° C
Plastic DIP (Soldering, 10 s)	260° C

RECOMMENDED OPERATING CONDITIONS

CHARACTERISTICS	MIN	TYP	MAX	UNITS
Supply Voltage (V_{CC})	4.75	5.0	15	V
Reference Voltage (V_{REF})*	2.8		5.25	V
Ramp Capacitor (C_H)	300			pF
Reference Current (I_R)	12		50	μA
Analog Input Range	0		V_{REF}	V
Ramp Stop Output Current			1.6	mA

*2 V ≤ V_{REF} ≤ (V_{CC} -2 V)

CHANNEL SELECTION

INPUT ADDRESS LINE			SELECTED ANALOG INPUT
A_2	A_1	A_0	
0	0	0	Ground
0	0	1	I_1
0	1	0	I_2
0	1	1	I_3
1	0	0	I_4
1	0	1	I_5
1	1	0	I_6
1	1	1	V_{REF}

ELECTRICAL CHARACTERISTICS: Over recommended operating conditions, -55°C ≤ T_A ≤ +125°C, for μA9708DM and 0°C ≤ T_A ≤ +70°C for μA9708DC or μA9708PC; unless otherwise specified.

CHARACTERISTICS	SYMBOL	CONDITIONS	LIMITS			UNITS
			MIN	TYP	MAX	
Conversion Accuracy	E_A	Over entire temperature range (Note 1)		±0.2	±0.3	%
Linearity	E_R	Applies to any one channel (Note 2)		±0.08	±0.2	%
Multiplexer Input Offset Voltage	V_{OSM}	Channel ON		2.0	4.0	mV
Conversion Time Per Channel	t_C	Analog Input = 0v to V_{REF} C_H = 300 pF, I_{REF} = 50 μA		296	350	μs
Acquisition Time	t_A	C_H = 1000 pF		20	40	μs
Acquistion Current	I_A		150			μA
Ramp Start Delay Time	t_D			100		ns
Multiplexer Address Time	t_M			1.0		μs
Digital Input HIGH Voltage	V_{IH}	A_0, A_1, A_2, ramp start	2.0			V
Digital Input LOW Voltage	V_{IL}	A_0, A_1, A_2, ramp start			0.8	V
Analog Input Current	I_B	Channel ON or OFF	-3.0	-1.0		μA
Input LOW Current	I_{IL}	A_0, A_1, A_2, ramp start = 0.4 V	-15	-5		μA
Input HIGH Current	I_{IH}	A_0, A_1, A_2, ramp start = 5.5 V			1.0	μA
Input Offset Current	I_{OS}			1.0	3.0	μA
Comparator Logic "1" Output Leakage Current	I_{OH}	V_{OH} = 15 V			10	μA
Comparator Logic "0" Output Voltage	V_{OL}	I_{OL} = 1.6 mA			0.4	V
Power Supply Rejection Ratio	PSRR	(Note 3)	40			dB
Crosstalk Between Any Two Channels		(Note 4)	60			dB
Power Supply Current	I_{CC}	V_{CC} = 5 V to 15 V, I_0 = 0		7.5	15	mA
Input Capacitance	C_{IN}			3.0		pF
Comparator Output Capacitance	C_{OUT}			5.0		pF

NOTES:
1. Conversion accuracy is defined as the deviations from a straight line drawn between the points defined by channel address 000 (0 scale) and channel address 111 (full scale) for all channels.
2. Linearity is defined as the deviation from a straight line drawn between the 0 and full scale points for each channel.
3. Power supply rejection ratio is defined as the conversion error contributed by power supply voltage variations while resolving mid scale on any channel.
4. Crosstalk between channels = 20 log $\frac{\Delta V_{CH}}{\Delta V_I}$

FUNCTIONAL DESCRIPTION

This Analog to Digital Converter is a single-slope 8-bit, 6-channel A/D converter that provides all of the necessary analog functions for a microprocessor-based data/control system. The device uses the processor system to provide the necessary addressing, timing and counting functions and includes a 1 of 8 decoder, 8-channel analog multiplexer, sample and hold, precision current reference, ramp integrator and comparator on a single monolithic chip.

For applications that require auto-zero or autc-calibration, *(See Figures 2-5)* line select address 0, 0, 0 and 1, 1, 1 may be used in conjunction with the arithmetic capability of the microprocessor to provide ground and scaling factors. Address 0, 0, 0 internally connects the input of the ramp generator to ground and may be used for zero offset correction in subsequent conversions. Address 1, 1, 1 internally connects the input of the ramp generator, to the voltage reference, V_{REF}, and may be used for scale factor correction in subsequent conversions. For the following, refer to the Functional Block Diagram.

Six separate external analog voltage inputs may come into terminals I_1-I_6 and the specific analog input to be converted is selected via address terminals A_0-A_2. The analog input voltage level is transferred to the external ramp capacitor connected to pin 4 when the input to the ramp start terminal (pin 3) is at a logic 0 *(See Figure 1)*. The time to charge the capacitor is the acquisition time

which is a function of the output impedance of an amplifier internal to the A/D and the value of the capacitor. After charging the external capacitor the ramp start terminal is switched to a logic 1 which introduces a high impedance between the analog input voltage and the external capacitor.

The capacitor begins to discharge at a controlled rate. The controlled rate of discharge (ramp) is established by the external reference voltage, the external reference resistor, the value of the external capacitor and the internal leakage of the A/D. Connected to the capacitor terminal is a comparator internal to the A/D with its output going to the ramp stop terminal (pin 7). The comparator output is a logical one when the capacitor is charged and switches to a logic 0 when the capacitor is in a discharged state. The ramp time is the time from when ramp start goes high (logic "1") to when ramp stop goes low (logic "0"). The microprocessor must be programmed to determine this conversion time. The ideal (no undesirable internal source impedances, leakage paths, errors on levels where comparator switches or delay time) conversion time is calculated as follows.

$$\text{Ramp Time} = V_1 \frac{C_H}{I_R}$$

Where V_1 = Analog Input Voltage being measured

C_H = External Ramp Capacitor

$$I_R = \frac{V_{CC} - V_{REF}}{R_{REF}}$$

Where V_{CC} = Power Supply Voltage

V_{REF} = Reference Voltage

R_{REF} = Reference Resistor

In actual use the errors due to a nonideal A/D can be minimized by using a microprocessor to make the calculations. *(See Figures 2 through 5)*

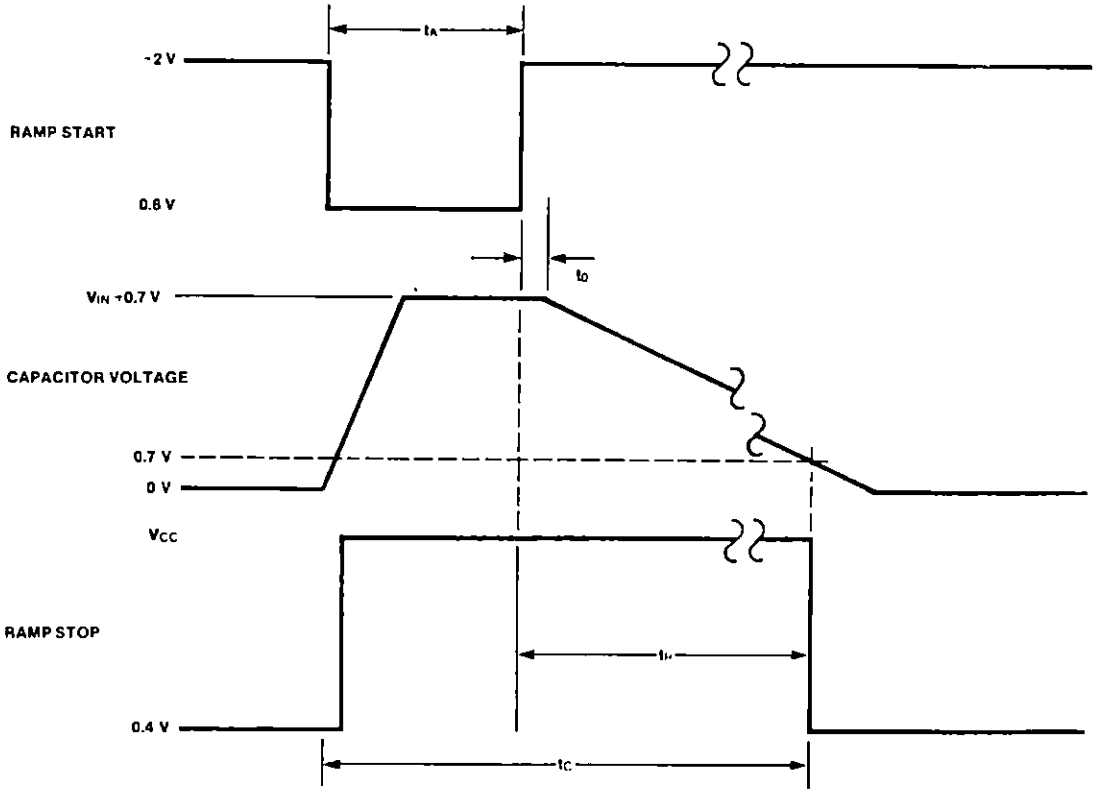
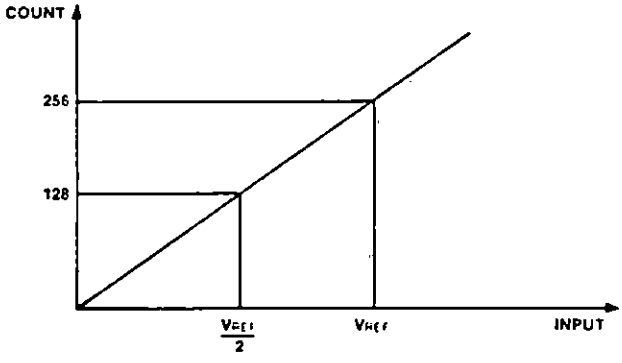


Fig. 1 Equivalent Timing Waveform for Test Circuits and Applications

APPLICATION HINTS AND FORMULAS

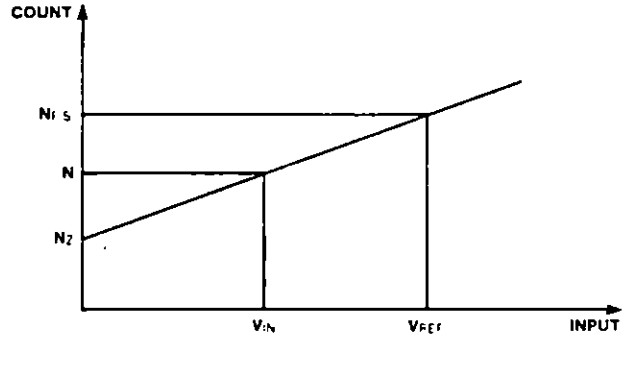
1. The capacitor node impedance is approximately 30 $\mu\Omega$ and should have no parallel resistance for proper operation.
2. t_R when V_{IN} = 0 V will be finite (i.e., the comparator will always toggle for $V_{IN} \geq 0$ V.)
3. The ramp stop output is open collector, and an external pull up resistor is required.
4. All digital inputs and outputs are TTL compatible.
5. For proper operation timing commences on the 0 to 1 transition of ramp start and terminates on the 1 to 0 transition of ramp stop.
6. $t_A \geq \frac{C_H}{150\ \mu A - I_R} \times V_{REF}$
7. t_R (ramp time) $= \frac{C_H}{I_R} \times V_{IN}$, $t_R|_{max} = \frac{C_H}{I_R} \times V_{REF}$
8. $I_R = \frac{V_{CC} - V_{REF}}{R_{REF}}$
9. $2\ V \leq V_{REF} \leq (V_{CC} - 2\ V)$
10. Address lines A_0, A_1, A_2 must be stable throughout the sampling interval, t_A.

AUTO-ZERO AND FULL-SCALE FEATURES



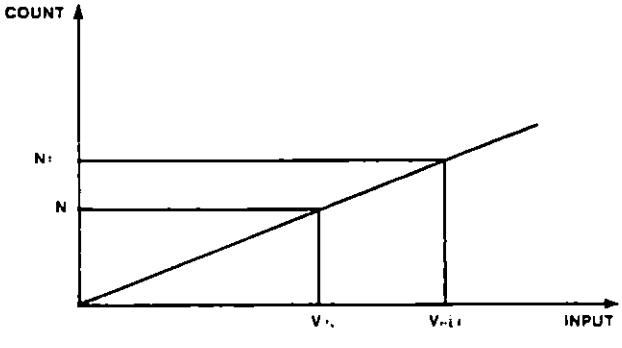
- NO ZERO OFFSET
- NO FULL-SCALE ERROR
- COUNT (N) = $\frac{V_{IN}}{V_{REF}}$ = 256

Fig. 2 Ideal Transfer Function



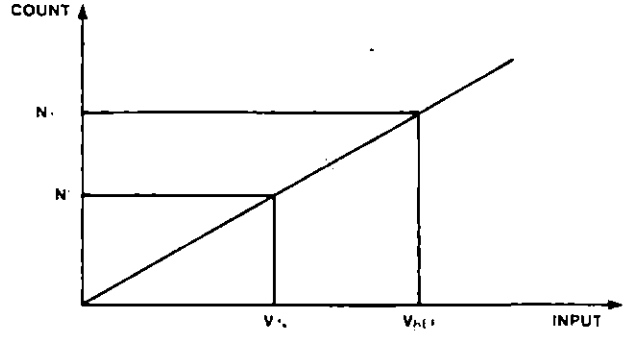
- $N_{FS} \neq 256$
- $N_Z \neq 0$
- (N) HAS BOTH FULL-SCALE AND ZERO ERRORS

Fig. 3 Transfer Function with Zero and Full-Scale Error



- $N' = N - N_Z$
- N' HAS FULL-SCALE ERROR

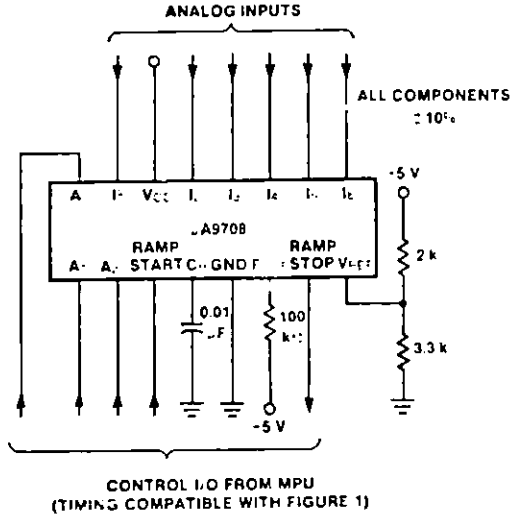
Fig. 4 Zero-Correction Added



- $N'' = (N - N_Z) \times \frac{256}{(N_{FS} - N_Z)}$

Fig. 5 Both Zero and Full-Scale Correction Added

TEST CIRCUITS



INPUT TIMING.

$t_A > 400\ \mu s$

$$V_{REF} = \left(\frac{3.3\ k\Omega}{2\ k\Omega + 3.3\ k\Omega}\right) 5\ V = 3.1\ V$$

$$I_R = \frac{5 - 3.1}{100\ k\Omega} = 19\ \mu A$$

$$t_R\Big|_{max} = \text{full scale ramp time} = \frac{0.01 \times 10^{-6}}{19 \times 10^{-6}} \times 3.1 = 1.6\ ms$$

NOTE
For evaluation purposes, the ramp start timing generation can be implemented with a µA555 timer (astable operation) or MPU evaluation kit, and a time interval meter for ramp time measurement. The TIM meter will measure the time between the 0 to 1 transition of the ramp start and the 1 to 0 transition of the ramp stop. The ramp stop is open collector, and must have an external pull up resistor to Vcc.

Fig. 6 Slow Speed Evaluation Circuit for Ratiometric Operation

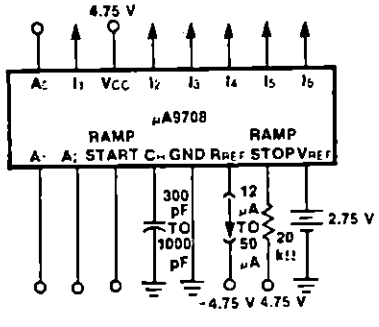


Fig. 7 Linearity/Acquisition Time/Conversion Time Test Circuit

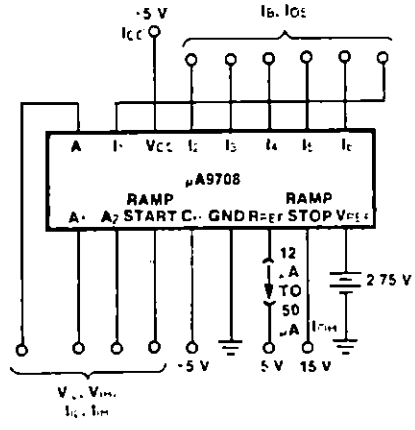
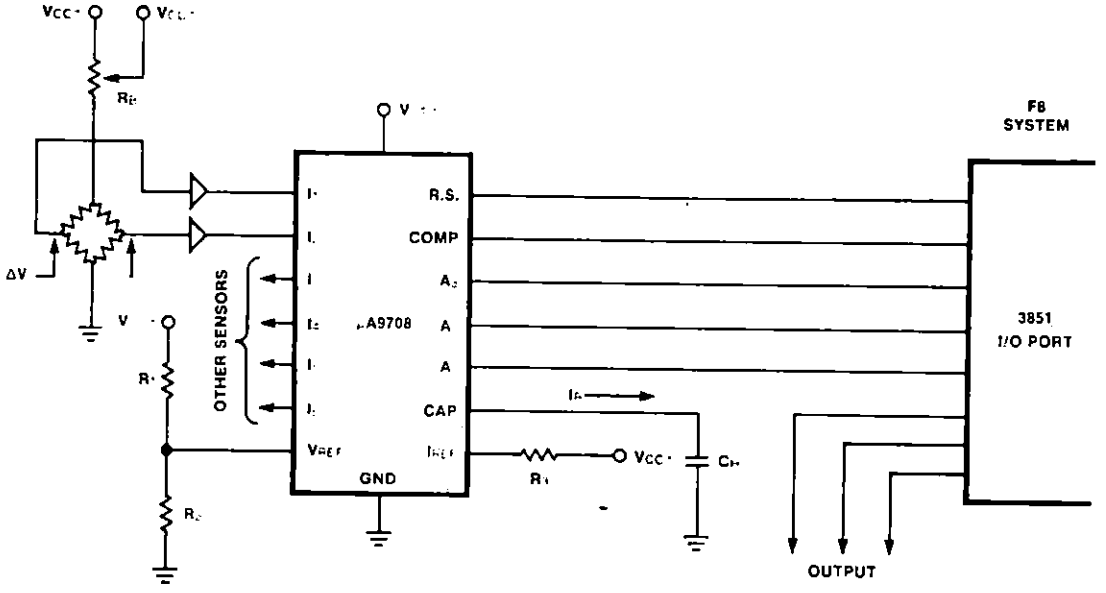


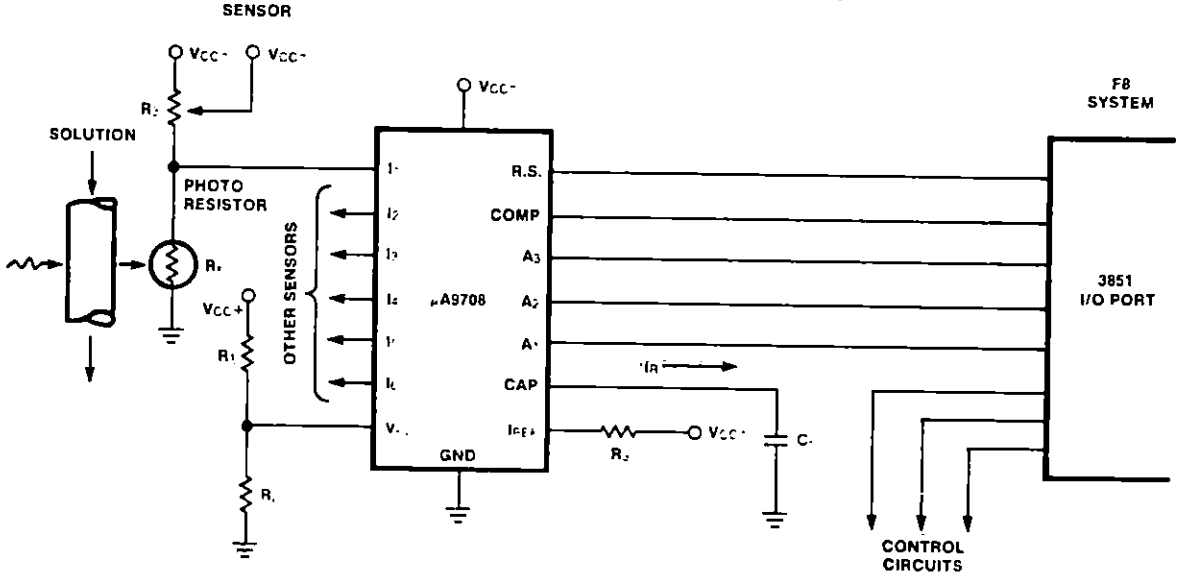
Fig. 8 Static Measurements

TYPICAL APPLICATIONS



ΔV_I = (Applied Force) and can be Linearized (if necessary) in F8 Software.

Ratiometric Strain Gage Sensor/Controller



APPLICATIONS:

- BEVERAGE BREWERS/DISPENSERS
- CHEMICAL SOLUTION CONTROL
- AUTOMATIC LIQUID MIXING CONTROL

$$\text{RAMP CURRENT} = I_R = V_{CC}\left(\frac{R_1}{R_1 + R_2}\right)\left(\frac{1}{R_3}\right)$$

$$V_I = \left(\frac{R_X}{R_X + R_B}\right) V_{CC+}$$

$$\text{RAMP TIME} = V_I \frac{C_H}{I_R} = \left(\frac{R_X}{R_X + R_B}\right)\left(1 + \frac{R_2}{R_1}\right)\left(C_H R_3\right)$$

Opaque Solution Controller

SYSTEM HINTS:

Several alternatives exist from a hardware/software standpoint in microprocessor based systems using the μA9708.

1. The ramp time measurement may be implemented in software using a register increment, followed by a branch back depending on the status of the ramp stop.

2. Alternately, the ramp stop may be tied into the interrupt structure in systems containing a programmable binary timer. This scheme has the following advantages:

   A. The CPU is not committed during the ramp time interval.
   B. It requires only 4 bits of an I/O port for control signals.

3. The auto-zero/auto-full-scale (see *Figures 2-5*) should use double precision, rounded (as opposed to truncated) arithmatics. Several points are worth noting:

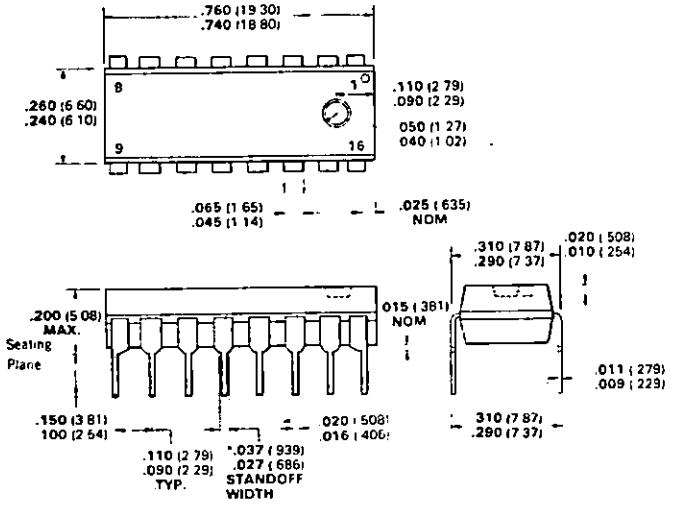
   A. The subtractions are single op code instructions.
   B. The full scale correction uses a multiply by 256 and can be accomplished by a shift left 8 bits (usually one instruction) or placing (N-Nz) in the MSB register and setting the LSB register to zero, for the double precision divide.
   C. The divisor ($N_{F.S.}$ - Nz) MSB's register will always be zero.

These schemes have the following advantages:

A. No access to the data buss or address buss is required, by the A/D system.
B. 4 I/O bits completely support the A/D system.
C. Since auto full scale/auto zero are implemented in software and long term drift (aging) effects are eliminated.
D. Software overhead is minimal (typically 30 bytes).
E. Where ratiometric operation is permissible, the 4 external components may be ±5% tolerance, including the power supply.

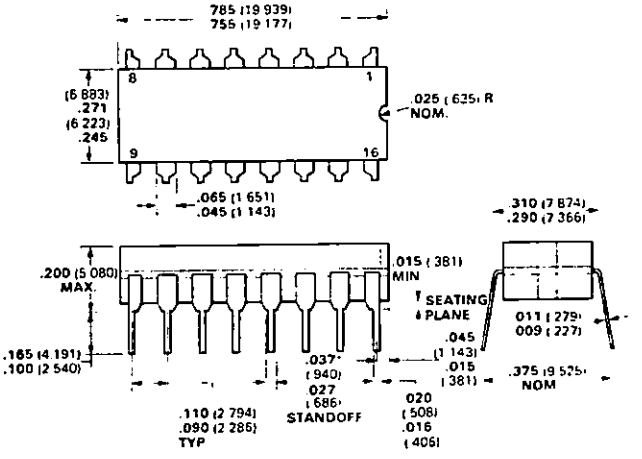
PACKAGE OUTLINES

(P)9B 16-PIN MOLDED DUAL IN-LINE



NOTES:
All dimensions in inches (bold) and millimeters (parentheses)
Pins are intended for insertion in hole rows on .300" (7.62) centers
Board-drilling dimensions should equal your practice for .020" (0.508) diameter pin
*The .037/.027 dimension does not apply to the corner pins
Package weight is 0.9 gram

(D) 7B 16-PIN HERMETIC DIP



NOTES:
All dimensions in inches
Pins are tin-plated 42 alloy
Pins are intended for insertion in hole rows on .300" (7.62) centers
They are purposely shipped with "positive" misalignment to facilitate insertion
Board-drilling dimensions should equal your practice for .020 (0.51) inch diameter pin
Hermetically sealed alumina package
*The .037-.027 (0.94-0.69) dimension does not apply to the corner pins
Package weight is 2.2 grams

National Semiconductor

CD4002M/CD4002C Dual 4-Input NOR Gate
CD4012M/CD4012C Dual 4-Input NAND Gate

General Description

These NOR and NAND gates are monolithic complementary MOS (CMOS) integrated circuits. The N- and P-channel enhancement mode transistors provide a symmetrical circuit with output swings essentially equal to the supply voltage. This results in high noise immunity over a wide supply voltage range. No DC power other than that caused by leakage current is consumed during static conditions. All inputs are protected against static discharge and latching conditions.

Features

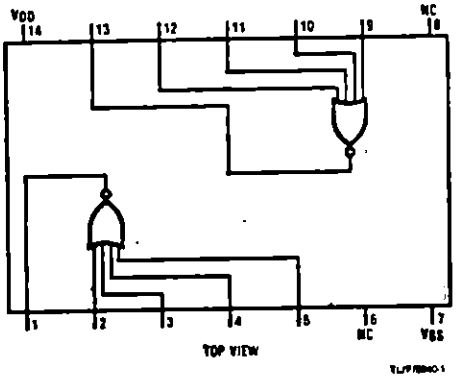
■ Wide supply voltage range	3.0 V to 15 V
■ Low power	10 nW (typ.)
■ High noise immunity	0.45 V_{DD} (typ.)

Applications

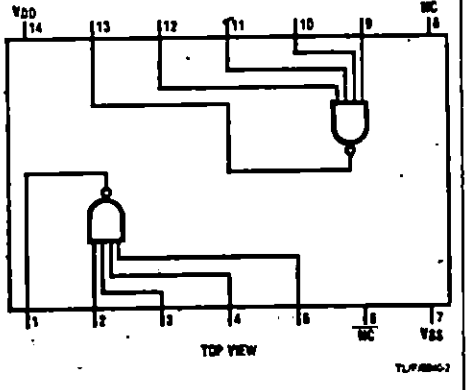
- Automotive
- Data terminals
- Instrumentation
- Medical Electronics
- Alarm system
- Industrial controls
- Remote metering
- Computers

Connection Diagrams Dual-In-Line Packages

CD4002



CD4012



Absolute Maximum Ratings (Note 1)

Voltage an Any Pin V_{SS} − 0.3 V to V_{DD} + 0.3 V
Operating Temperature Range
CD4002M, CD4012M −55°C to +125°C
CD4002C, CD4012C −40°C to +85°C

Storage Temperature Range −65°C to +150°C
Package Dissipation 500 mW
Operating V_{DD} Range V_{SS} + 3.0 V to V_{SS} + 15 V
Lead Temperature (Soldering, 10 seconds) 260°C

DC Electrical Characteristics — CD4002M, CD4012M

Sym	Parameter	Conditions	Limits							Units
			−55°C		25°C			125°C		
			Min	Max	Min	Typ	Max	Min	Max	
I_L	Quiescent Device Current	V_{DD} = 5.0V V_{DD} = 10V		0.05 0.1		0.001 0.001	0.05 0.1		3.0 6.0	μA μA
P_D	Quiescent Device Dissipation/Package	V_{DD} = 5.0V V_{DD} = 10V		0.25 1.0		0.005 0.01	0.25 1.0		15 60	μW μW
V_{OL}	Output Voltage Low Level	V_{DD} = 5.0V, V_I = V_{DD}, I_O = 0A V_{DD} = 10V, V_I = V_{DD}, I_O = 0A		0.05 0.05		0 0	0.05 0.05		0.05 0.05	V V
V_{OH}	Output Voltage High Level	V_{DD} = 5.0V, V_I = V_{SS}, I_O = 0A V_{DD} = 10V, V_I = V_{SS}, I_O = 0A	4.95 9.95		4.95 9.95	5.0 10		4.95 9.95		V V
V_{NL}	Noise Immunity (All Inputs)	V_{DD} = 5.0V, V_O = 3.6V, I_O = 0A V_{DD} = 10V, V_O = 7.2V, I_O = 0A	1.5 3.0		1.5 3.0	2.25 4.5		1.4 2.9		V V
V_{NH}	Noise Immunity (All Inputs)	V_{DD} = 5.0V, V_O = 0.95V, I_O = 0A V_{DD} = 10V, V_O = 2.9V, I_O = 0A	1.4 2.9		1.5 3.0	2.25 4.5		1.5 3.0		V V
I_DN	Output Drive Current N-Channel (4002) (Note 2)	V_{DD} = 5.0V, V_O = 0.4V, V_I = V_{DD} V_{DD} = 10V, V_O = 0.5V, V_I = V_{DD}	0.5 1.1		0.40 0.9	1.0 2.5		0.28 0.65		mA mA
I_DP	Output Drive Current P-Channel (4002) (Note 2)	V_{DD} = 5.0V, V_O = 2.5V, V_I = V_{SS} V_{DD} = 10V, V_O = 9.5V, V_I = V_{SS}	−0.62 −0.62		−0.5 −0.5	−2.0 −1.0		−0.35 −0.35		mA mA
I_DN	Output Drive Current N-Channel (4012) (Note 2)	V_{DD} = 5.0V, V_O = 0.4V, V_I = V_{DD} V_{DD} = 10V, V_O = 0.5V, V_I = V_{DD}	0.31 0.63		0.25 0.5	0.5 0.6		0.175 0.35		mA mA
I_DP	Output Drive Current P-Channel (4012) (Note 2)	V_{DD} = 5.0V, V_O = 2.5V, V_I = V_{SS} V_{DD} = 10V, V_O = 9.5V, V_I = V_{SS}	−0.31 −0.75		−0.25 −0.6	−0.5 −1.2		−0.175 −0.4		mA mA
I_I	Input Current					10				pA

DC Electrical Characteristics — CD4002C, CD4012C

Sym	Parameter	Conditions	Limits							Units
			−40°C		25°C			85°C		
			Min	Max	Min	Typ	Max	Min	Max	
I_L	Quiescent Device Current	$V_{DD} = 5.0V$ $V_{DD} = 10V$		0.5 5.0		0.005 0.005	0.5 5.0		15 30	μA μA
P_D	Quiescent Device Dissipation/Package	$V_{DD} = 5.0V$ $V_{DD} = 10V$		2.5 50		0.025 0.05	2.5 50		75 300	μW μW
V_{OL}	Output Voltage Low Level	$V_{DD} = 5.0V$, $V_I = V_{DD}$, $I_O = 0A$ $V_{DD} = 10V$, $V_I = V_{DD}$, $I_O = 0A$		0.05 0.05		0 0	0.05 0.05		0.05 0.05	V V
V_{OH}	Output Voltage High Level	$V_{DD} = 5.0V$, $V_I = V_{SS}$, $I_O = 0A$ $V_{DD} = 10V$, $V_I = V_{SS}$, $I_O = 0A$	4.95 9.95		4.95 9.95	5.0 10		4.95 9.95		V V
V_{NL}	Noise Immunity (All Inputs)	$V_{DD} = 5.0V$, $V_O \geq 3.5V$, $I_O = 0A$ $V_{DD} = 10V$, $V_O \geq 7.2V$, $I_O = 0A$	1.5 3.0		1.5 3.0	2.25 4.5		1.4 2.8		V V
V_{NH}	Noise Immunity (All Inputs)	$V_{DD} = 5.0V$, $V_O \leq 1.5V$, $I_O = 0A$ $V_{DD} = 10V$, $V_O \leq 3.5V$, $I_O = 0A$	1.4 2.8		1.5 3.0	2.25 4.5		1.5 3.0		V V
I_{DN}	Output Drive Current N-Channel (4002) (Note 2)	$V_{DD} = 5.0V$, $V_O = 0.4V$, $V_I = V_{DD}$ $V_{DD} = 10V$, $V_O = 0.5V$, $V_I = V_{DD}$	0.35 0.72		0.3 0.6	1.0 2.5		0.24 0.48		mA mA
I_{DN}	Output Drive Current N-Channel (4012) (Note 2)	$V_{DD} = 5.0V$, $V_O = 0.4V$, $V_I = V_{DD}$ $V_{DD} = 10V$, $V_O = 0.5V$, $V_I = V_{DD}$	0.145 0.3		0.12 0.25	0.5 0.8		0.095 0.2		mA mA
I_{DP}	Output Drive Current P-Channel (4002) (Note 2)	$V_{DD} = 5.0V$, $V_O = 2.5V$, $V_I = V_{SS}$ $V_{DD} = 10V$, $V_O = 9.5V$, $V_I = V_{SS}$	−0.35 −0.3		−0.3 −0.25	−2.0 −1.0		−0.24 −0.2		mA mA
I_{DP}	Output Drive Current P-Channel (4012) (Note 2)	$V_{DD} = 5.0V$, $V_O = 2.5V$, $V_I = V_{SS}$ $V_{DD} = 10V$, $V_O = 9.5V$, $V_I = V_{SS}$	−0.145 −0.35		−0.12 −0.3	−0.5 −1.2		−0.095 −0.24		mA mA
I_I	Input Current					10				pA

AC Electrical Characteristics $T_A = 25°C$, $C_L = 15pF$, and input rise and fall times = 20ns.

Typical temperature coefficient for all values of $V_{DD} = 0.3\%/°C$

Sym	Parameter	Conditions	Min	Typ	Max	Units
CD4002M						
t_{PHL}	Propagation Delay Time High to Low Level	$V_{DD} = 5.0V$ $V_{DD} = 10V$		35 25	50 40	ns ns
t_{PLH}	Propagation Delay Time Low to High Level	$V_{DD} = 5.0V$ $V_{DD} = 10V$		35 25	50 40	ns ns
t_{THL}	Transition Time High to Low Level	$V_{DD} = 5.0V$ $V_{DD} = 10V$		65 35	175 75	ns ns
t_{TLH}	Transition Time Low to High Level	$V_{DD} = 5.0V$ $V_{DD} = 10V$		65 35	125 70	ns ns
C_{IN}	Input Capacitance	Any Input		5.0		pF
CD4002C						
t_{PHL}	Propagation Delay Time High to Low Level	$V_{DD} = 5.0V$ $V_{DD} = 10V$		35 25	120 65	ns ns
t_{PLH}	Propagation Delay Time Low to High Level	$V_{DD} = 5.0V$ $V_{DD} = 10V$		35 25	80 55	ns ns
t_{THL}	Transition Time High to Low Level	$V_{DD} = 5.0V$ $V_{DD} = 10V$		65 35	300 125	ns ns
t_{TLH}	Transition Time Low to High Level	$V_{DD} = 5.0V$ $V_{DD} = 10V$		65 35	200 115	ns ns
C_{IN}	Input Capacitance	Any Input		5.0		pF

AC Electrical Characteristics $T_A = 25°C$, $C_L = 15pF$, and input rise and fall times = 20ns.

Typical temperature coefficient for all values of $V_{DD} = 0.3\%/°C$

Sym	Parameter	Conditions	Min	Typ	Max	Units
CD4012M						
t_{PHL}	Propagation Delay Time High to Low Level	$V_{DD} = 5.0V$ $V_{DD} = 10V$		50 25	75 40	ns ns
t_{PLH}	Propagation Delay Time Low to High Level	$V_{DD} = 5.0V$ $V_{DD} = 10V$		50 25	75 40	ns ns
t_{THL}	Transition Time High to Low Level	$V_{DD} = 5.0V$ $V_{DD} = 10V$		75 50	125 75	ns ns
t_{TLH}	Transition Time Low to High Level	$V_{DD} = 5.0V$ $V_{DD} = 10V$		75 40	100 60	ns ns
C_{IN}	Input Capacitance	Any Input		5.0		pF
CD4012C						
t_{PHL}	Propagation Delay Time High to Low Level	$V_{DD} = 5.0V$ $V_{DD} = 10V$		50 25	100 50	ns ns
t_{PLH}	Propagation Delay Time Low to High Level	$V_{DD} = 5.0V$ $V_{DD} = 10V$		50 25	100 50	ns ns
t_{THL}	Transition Time High to Low Level	$V_{DD} = 5.0V$ $V_{DD} = 10V$		75 50	150 100	ns ns
t_{TLH}	Transition Time Low to High Level	$V_{DD} = 5.0V$ $V_{DD} = 10V$		75 40	125 75	ns ns
C_{IN}	Input Capacitance	Any Input		5.0		pF

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: I_DN and I_DP are tested one output at a time.

National Semiconductor

MM54C00/MM74C00 Quad 2-Input NAND Gate
MM54C02/MM74C02 Quad 2-Input NOR Gate
MM54C04/MM74C04 Hex Inverter
MM54C10/MM74C10 Triple 3-Input NAND Gate
MM54C20/MM74C20 Dual 4-Input NAND Gate

General Description

These logic gates employ complementary MOS (CMOS) to achieve wide power supply operating range, low power consumption, high noise immunity and symmetric controlled rise and fall times. With features such as this the 54C/74C logic family is close to ideal for use in digital systems. Function and pin out compatibility with series 54/74 devices minimizes design time for those designers already familiar with the standard 54/74 logic family.

All inputs are protected from damage due to static discharge by diode clamps to V_{CC} and GND.

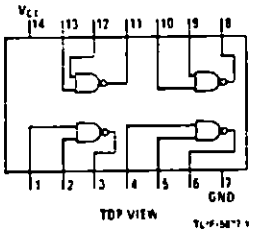
Features

■ Wide supply voltage range	3.0V to 15V
■ Guaranteed noise margin	1.0V
■ High noise immunity	0.45 V_{CC} (typ.)
■ Low power consumption	10 nW/package (typ.)
■ Low power TTL compatibility	fan out of 2 driving 74L

Connection Diagrams

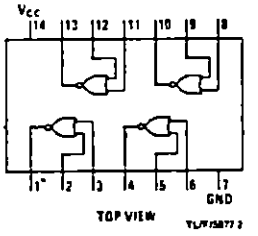
Dual-In-Line Packages

MM54C00/MM74C00



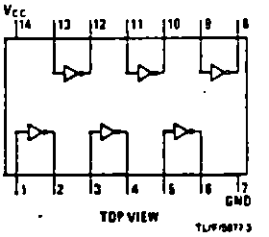
Order Number MM54C00J, MM74C00J, MM54C00N or MM74C00N
See NS Package J14A or N14A

MM54C02/MM74C02



Order Number MM54C02J, MM74C02J, MM54C02N or MM74C02N
See NS Package J14A or N14A

MM54C04/MM74C04



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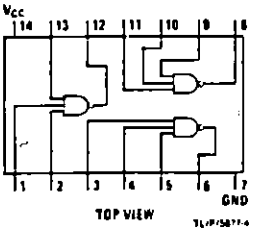
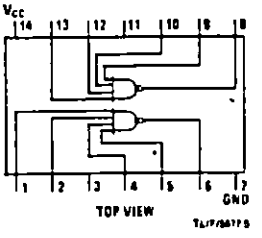
See NS Package J14A or N14A

MM54C10/MM74C10



MM54C20/MM74C20



Absolute Maximum Ratings

Voltage at Any Pin	−0.3V to V_{CC} + 0.3V	Operating V_{CC} Range	3.0V to 15V
Operating Temperature Range		Maximum V_{CC} Voltage	18V
54C	−55°C to +125°C	Package Dissipation	500 mW
74C	−40°C to +85°C	Lead Temperature (Soldering, 10 seconds)	300°C
Storage Temperature Range	−65°C to +150°C		

DC Electrical Characteristics

Min/max limits apply across the guaranteed temperature range unless otherwise noted.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
CMOS to CMOS						
$V_{IN(1)}$	Logical "1" Input Voltage	V_{CC} = 5.0V V_{CC} = 10V	3.5 8.0			V V
$V_{IN(0)}$	Logical "0" Input Voltage	V_{CC} = 5.0V V_{CC} = 10V			1.5 2.0	V V
$V_{OUT(1)}$	Logical "1" Output Voltage	V_{CC} = 5.0V, I_O = −10μA V_{CC} = 10V, I_O = −10μA	4.5 9.0			V V
$V_{OUT(0)}$	Logical "0" Output Voltage	V_{CC} = 5.0V, I_O = +10μA V_{CC} = 10V, I_O = +10μA			0.5 1.0	V V
$I_{IN(1)}$	Logical "1" Input Current	V_{CC} = 15V, V_{IN} = 15V		0.005	1.0	μA
$I_{IN(0)}$	Logical "0" Input Current	V_{CC} = 15V, V_{IN} = 0V	−1.0	−0.005		μA
I_{CC}	Supply Current	V_{CC} = 15V		0.01	15	μA
Low Power to CMOS						
$V_{IN(1)}$	Logical "1" Input Voltage	54C, V_{CC} = 4.5V 74C, V_{CC} = 4.75V	V_{CC} − 1.5 V_{CC} − 1.5			V V
$V_{IN(0)}$	Logical "0" Input Voltage	54C, V_{CC} = 4.5V 74C, V_{CC} = 4.75V			0.8 0.8	V V
$V_{OUT(1)}$	Logical "1" Output Voltage	54C, V_{CC} = 4.5V, I_O = −10μA 74C, V_{CC} = 4.75V, I_O = −10μA	4.4 4.4			V V
$V_{OUT(0)}$	Logical "0" Output Voltage	54C, V_{CC} = 4.5V, I_O = +10μA 74C, V_{CC} = 4.75V, I_O = +10μA			0.4 0.4	V V
CMOS to Low Power						
$V_{IN(1)}$	Logical "1" Input Voltage	54C, V_{CC} = 4.5V 74C, V_{CC} = 4.75V	4.0 4.0			V V
$V_{IN(0)}$	Logical "0" Input Voltage	54C, V_{CC} = 4.5V 74C, V_{CC} = 4.75V			1.0 1.0	V V
$V_{OUT(1)}$	Logical "1" Output Voltage	54C, V_{CC} = 4.5V, I_O = −360μA 74C, V_{CC} = 4.75V, I_O = −360μA	2.4 2.4			V V
$V_{OUT(0)}$	Logical "0" Output Voltage	54C, V_{CC} = 4.5V, I_O = 360μA 74C, V_{CC} = 4.75V, I_O = 360μA			0.4 0.4	V V
Output Drive (See 54C/74C Family Characteristics Data Sheet) (short circuit current)						
I_{SOURCE}	Output Source Current	V_{CC} = 5.0V, $V_{IN(0)}$ = 0V T_A = 25°C, V_{OUT} = 0V	−1.75			mA
I_{SOURCE}	Output Source Current	V_{CC} = 10V, $V_{IN(0)}$ = 0V T_A = 25°C, V_{OUT} = 0V	−8.0			mA
I_{SINK}	Output Sink Current	V_{CC} = 5.0V, $V_{IN(1)}$ = 5.0V T_A = 25°C, V_{OUT} = V_{CC}	1.75			mA
I_{SINK}	Output Sink Current	V_{CC} = 10V, $V_{IN(1)}$ = 10V T_A = 25°C, V_{OUT} = V_{CC}	8.0			mA

AC Electrical Characteristics

$T_A = 25°C$, $C_L = 50\,pF$, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
MM54C00/MM74C00, MM54C02/MM74C02, MM54C04/MM74C04						
t_{pd0}, t_{pd1}	Propagation Delay Time to Logical "1" or "0"	$V_{CC} = 5.0V$		50	80	ns
		$V_{CC} = 10V$		30	60	ns
C_{IN}	Input Capacitance	(Note 2)		6.0		pF
C_{PD}	Power Dissipation Capacitance	(Note 3) Per Gate or Inverter		12		pF
MM54C10/MM74C10						
t_{pd0}, t_{pd1}	Propagation Delay Time to Logical "1" or "0"	$V_{CC} = 5.0V$		60	100	ns
		$V_{CC} = 10V$		35	70	ns
C_{IN}	Input Capacitance	(Note 2)		7.0		pF
C_{PD}	Power Dissipation Capacitance	(Note 3) Per Gate		18		pF
MM54C20/MM74C20						
t_{pd0}, t_{pd1}	Propagation Delay Time to Logical "1" or "0"	$V_{CC} = 5.0V$		70	115	ns
		$V_{CC} = 10V$		40	80	ns
C_{IN}	Input Capacitance	(Note 2)		9		pF
C_{PD}	Power Dissipation Capacitance	(Note 3) Per Gate		30		pF

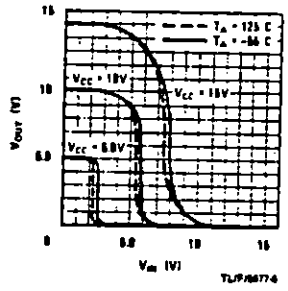
Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Capacitance is guaranteed by periodic testing.

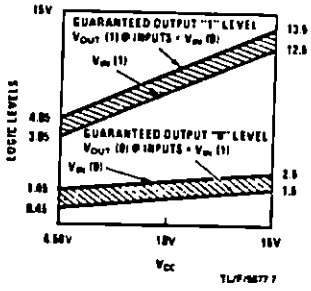
Note 3: C_{PD} determines the no load ac power consumption of any CMOS device. For complete explanation see 54C/74C Family Characteristics application note — AN-90.

Typical Performance Characteristics

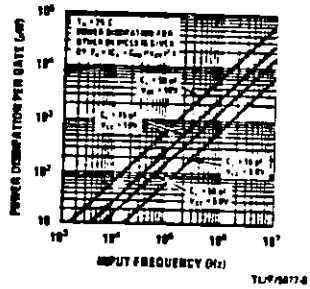
Gate Transfer Characteristics



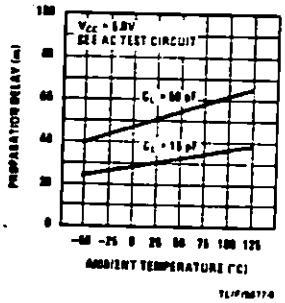
Guaranteed Noise Margin Over Temperature vs V_{CC}



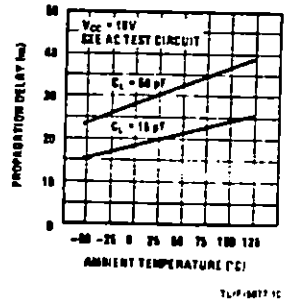
Power Dissipation vs Frequency MM54C00/MM74C00, MM54C02/MM74C02, MM54C04/MM74C04



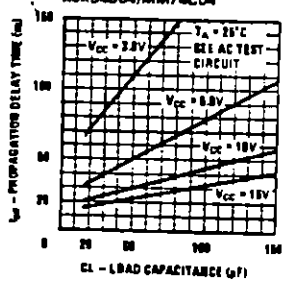
Propagation Delay vs Ambient Temperature MM54C00/MM74C00, MM54C02/MM74C02, MM54C04/MM74C04



Propagation Delay vs Ambient Temperature MM54C00/MM74C00, MM54C02/MM74C02, MM54C04/MM74C04

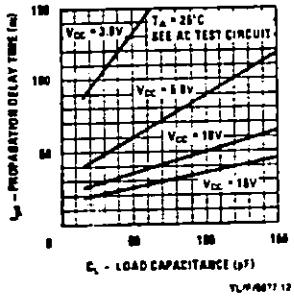


Propagation Delay Time vs Load Capacitance MM54C00/MM74C00, MM54C02/MM74C02, MM54C04/MM74C04

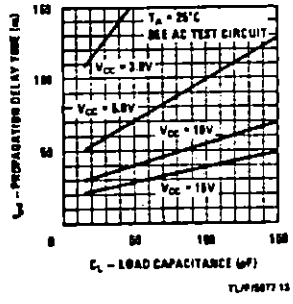


Typical Performance Characteristics (Cont'd)

Propagation Delay Time vs
Load Capacitance
MM54C10/MM74C10

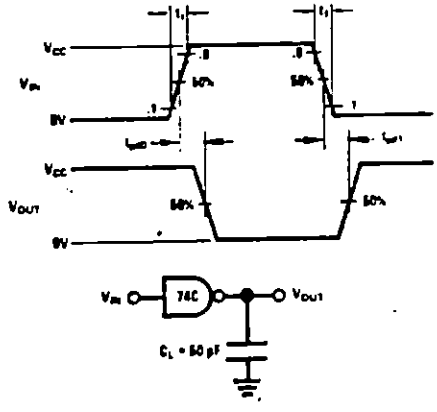


Propagation Delay Time vs
Load Capacitance
MM54C20/MM74C20



Switching Time Waveforms and AC Test Circuit

CMOS to CMOS



NOTE: DELAYS MEASURED WITH INPUT $t_r, t_f \leq 20$ ns.

MOTOROLA

MC14503B

HEX NON-INVERTING 3-STATE BUFFER

The MC14503B is a hex non-inverting buffer with 3-state outputs, and a high current source and sink capability. The 3-state outputs make it useful in common bussing applications. Two disable controls are provided. A high level on the Disable A input causes the outputs of buffers 1 through 4 to go into a high impedance state and a high level on the Disable B input causes the outputs of buffers 5 and 6 to go into a high impedance state.

- 3-State Outputs
- TTL Compatible – Will Drive One TTL Load Over Full Temperature Range
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Symmetrical Turn-On and Turn-off Delays
- Symmetrical Output Rise and Fall Times
- Two Disable Controls for Added Versatility
- Pin for Pin Replacement for MM80C97 and 340097

CMOS SSI

(LOW-POWER COMPLEMENTARY MOS)

HEX 3-STATE BUFFER



L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648

ORDERING INFORMATION

MC14XXXB — Suffix — Denotes

- L — Ceramic Package
- P — Plastic Package
- A — Extended Operating Temperature Range
- C — Limited Operating Temperature Range

MAXIMUM RATINGS (Voltages referenced to V_{SS}, Pin 8)

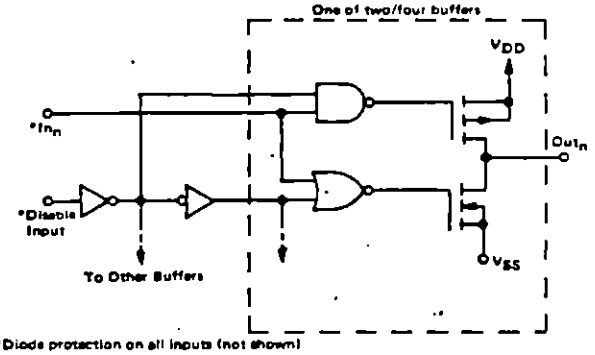
Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	−0.5 to +18	Vdc
Input Voltage, All Inputs	V_{in}	−0.5 to V_{DD} + 0.5	Vdc
DC Current Drain per Input Pin	I	10	mAdc
DC Current Drain per Output Pin	I	25	mAdc
Operating Temperature Range – AL Device CL/CP Device	T_A	−55 to +125 −40 to +85	°C
Storage Temperature Range	T_{stg}	−65 to +150	°C

TRUTH TABLE

In_n	Appropriate Disable Input	Out_n
0	0	0
1	0	1
X	1	High Impedance

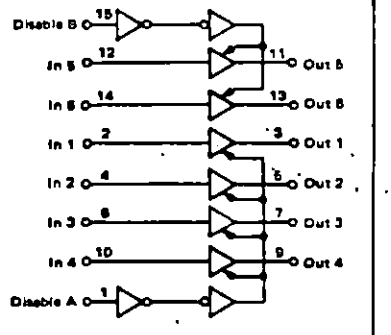
X = Don't Care

CIRCUIT DIAGRAM



*Diode protection on all inputs (not shown)

LOGIC DIAGRAM



V_{DD} = Pin 16
V_{SS} = Pin 8

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields, however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

Unused inputs must always be tied on an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

MC14503B

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage "0" Level	V_{OL}	5.0	–	0.05	–	0	0.05	–	0.05	Vdc
V_{in} = V_{DD} or 0		10	–	0.05	–	0	0.05	–	0.05	
		15	–	0.05	–	0	0.05	–	0.05	
"1" Level	V_{OH}	5.0	4.95	–	4.95	5.0	–	4.95	–	Vdc
V_{in} = 0 or V_{DD}		10	9.95	–	9.95	10	–	9.95	–	
		15	14.95	–	14.95	15	–	14.95	–	
Noise Immunity# "0" Level	V_{IL}									Vdc
(V_O = 3.6 or 1.4 Vdc)		5.0	–	1.5	–	2.25	1.5	–	1.5	
(V_O = 7.2 or 2.8 Vdc)		10	–	3.0	–	4.50	3.0	–	3.0	
(V_O = 11.5 or 3.5 Vdc)		15	–	3.75	–	6.75	3.75	–	3.75	
"1" Level	V_{IH}	5.0	3.5	–	3.5	2.75	–	3.5	–	Vdc
(V_O = 1.4 or 3.6 Vdc)		10	7.0	–	7.0	5.5	–	7.0	–	
(V_O = 2.8 or 7.2 Vdc)		15	11.25	–	11.25	8.25	–	11.25	–	
(V_O = 3.5 or 11.5 Vdc)										
Output Drive Current (AL Device)***	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		4.5	-4.3	–	-3.5	-5.0	–	-2.5	–	
(V_{OH} = 2.5 Vdc)		5.0	-5.8	–	-4.80	-6.1	–	-3.0	–	
(V_{OH} = 4.6 Vdc)		5.0	-1.2	–	-1.02	-1.4	–	-0.7	–	
(V_{OH} = 9.5 Vdc)		10	-3.1	–	-2.60	-3.7	–	-1.8	–	
(V_{OH} = 13.5 Vdc)		15	-8.2	–	-6.80	-14.1	–	-4.8	–	
Sink	I_{OL}									mAdc
(V_{OL} = 0.4 Vdc)		4.5	2.2	–	1.8	2.1	–	1.2	–	
(V_{OL} = 0.4 Vdc)		5.0	2.6	–	2.1	2.3	–	1.3	–	
(V_{OL} = 0.5 Vdc)		10	6.5	–	5.5	6.2	–	3.8	–	
(V_{OL} = 1.5 Vdc)		15	19.2	–	16.10	25.00	–	11.2	–	
Output Drive Current (CL/CP Device)***	I_{OH}						–			mAdc
(V_{OH} = 2.5 Vdc) Source		4.75	-4.0	–	-3.60	-5.5	–	-2.4	–	
(V_{OH} = 2.5 Vdc)		5.0	-4.6	–	-4.20	-6.1	–	-3.0	–	
(V_{OH} = 4.6 Vdc)		5.0	-1.0	–	-0.88	-1.4	–	-0.7	–	
(V_{OH} = 9.5 Vdc)		10	-2.4	–	-2.20	-3.7	–	-1.8	–	
(V_{OH} = 13.5 Vdc)		15	-6.6	–	-6.00	-14.1	–	-4.8	–	
Sink	I_{OL}									mAdc
(V_{OL} = 0.4 Vdc)		4.75	2.1	–	1.95	2.2	–	1.25	–	
(V_{OL} = 0.4 Vdc)		5.0	2.3	–	2.10	2.3	–	1.3	–	
(V_{OL} = 0.5 Vdc)		10	6.0	–	5.45	6.2	–	3.8	–	
(V_{OL} = 1.5 Vdc)		15	15.2	–	13.80	25.00	–	11.2	–	
Input Current (AL Device)	I_{in}	15	–	±0.1	–	±0.00001	±0.1	–	±1.0	µAdc
Input Current (CL/CP Device)	I_{in}	15	–	±0.3	–	±0.00001	±3.0	–	±1.0	µAdc
Input Capacitance (V_{in} = 0)	C_{in}	–	–	–	–	5.0	7.5	–	–	pF
Quiescent Current (AL Device)	I_Q	5.0	–	1.0	–	0.002	1.0	–	30	µAdc
(Per Package)		10	–	2.0	–	0.004	2.0	–	60	
		15	–	4.0	–	0.006	4.0	–	120	
Quiescent Current (CL/CP Device)	I_{DD}	5.0	–	4.0	–	0.002	4.0	–	30	µAdc
(Per Package)		10	–	8.0	–	0.004	8.0	–	60	
		15	–	16	–	0.006	16	–	120	
Total Supply Current**† (Dynamic plus Quiescent, Per Package) (C_L = 50 pF on all outputs) (All outputs switching, 50% Duty Cycle)	I_{DD}	5.0	(I_T = 2.5 µA/kHz) f + I_{DD}							µAdc
		10	(I_T = 5.0 µA/kHz) f + I_{DD}							
		15	(I_T = 10 µA/kHz) f + I_{DD}							
3-State Output Leakage Current (AL Device)	I_{TL}	15	–	±0.1	–	±0.0001	±0.1	–	±3.0	µAdc
			–		–			–		
3-State Output Leakage Current (CL/CP Device)	I_{TL}	15	–	±1.0	–	±0.0001	±1.0	–	±7.5	µAdc
			–		–			–		

*T_{low} = −55°C for AL Device, −40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device
#Noise immunity specified for worst-case input combination
†To calculate total supply current at loads other than 50 pF,
$I_T(C_L) = I_T(50\ pF) + 6 \times 10^{-3} (C_L - 50) V_{DD} f$
I_T is in µA (per package) C_L in pF, V_{DD} in Vdc, and f in kHz is input frequency.
**The formulas given are for the typical characteristics only at 25°C
***Care must be taken not to exceed maximum current ratings (see maximum ratings table and Figure 1).

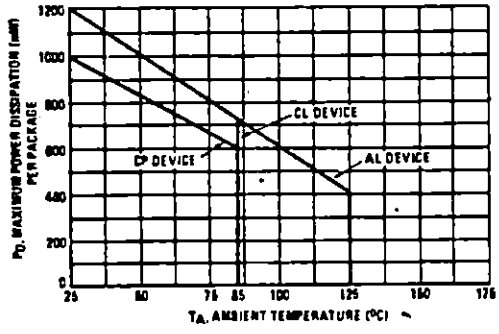
MC14503B

SWITCHING CHARACTERISTICS* (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD} V_{CC}	All Types Typ	All Types Max	Unit
Output Rise Time	t_{TLH}				ns
t_{TLH} = (0.5 ns/pF) C_L + 20 ns		5.0	45	90	
t_{TLH} = (0.3 ns/pF) C_L + 8.0 ns		10	23	45	
t_{TLH} = (0.2 ns/pF) C_L + 8.0 ns		15	18	35	
Output Fall Time	t_{THL}				ns
t_{THL} = (0.5 ns/pF) C_L + 20 ns		5.0	45	90	
t_{THL} = (0.3 ns/pF) C_L + 8.0 ns		10	23	45	
t_{THL} = (0.2 ns/pF) C_L + 8.0 ns		15	18	35	
Turn-Off Delay Time, all Outputs	t_{PLH}				ns
t_{PLH} = (0.3 ns/pF) C_L + 60 ns		5.0	75	150	
t_{PLH} = (0.15 ns/pF) C_L + 27 ns		10	35	70	
t_{PLH} = (0.1 ns/pF) C_L + 20 ns		15	25	50	
Turn-On Delay Time, all Outputs	t_{PHL}				ns
t_{PHL} = (0.3 ns/pF) C_L + 60 ns		5.0	75	150	
t_{PHL} = (0.15 ns/pF) C_L + 27 ns		10	35	70	
t_{PHL} = (0.1 ns/pF) C_L + 20 ns		15	25	50	
3-State Propagation Delay Time					
Output "1" to High Impedance	t_{PHZ}	5.0	75	150	ns
		10	40	80	
		15	35	70	
Output "0" to High Impedance	t_{PLZ}	5.0	80	160	ns
		10	40	80	
		15	35	70	
High Impedance to "1" Level	t_{PZH}	5.0	65	130	ns
		10	25	50	
		15	20	40	
High Impedance to "0" Level	t_{PZL}	5.0	100	200	ns
		10	35	70	
		15	25	50	

*The formulas given are for the typical characteristics only.

FIGURE 1 – AMBIENT TEMPERATURE POWER DERATING



MC14503B

FIGURE 2 – SWITCHING TIME TEST CIRCUIT AND WAVEFORMS
(t_{TLH}, t_{THL}, t_{PHL}, and t_{PLH})

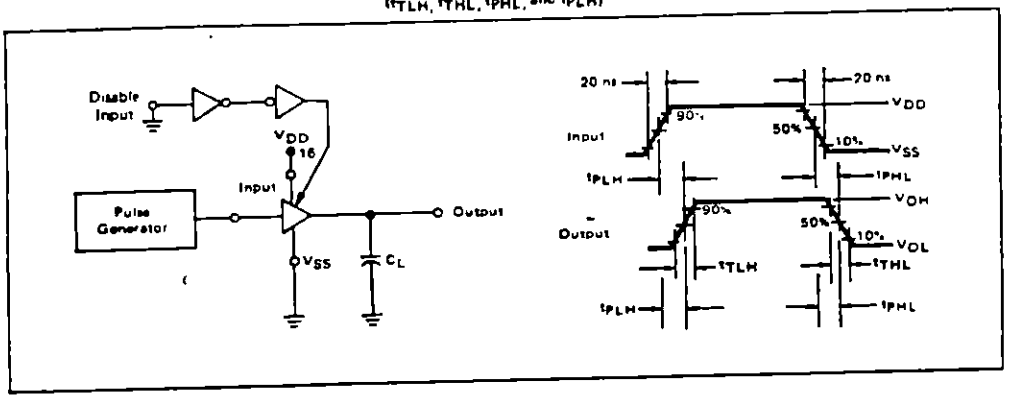
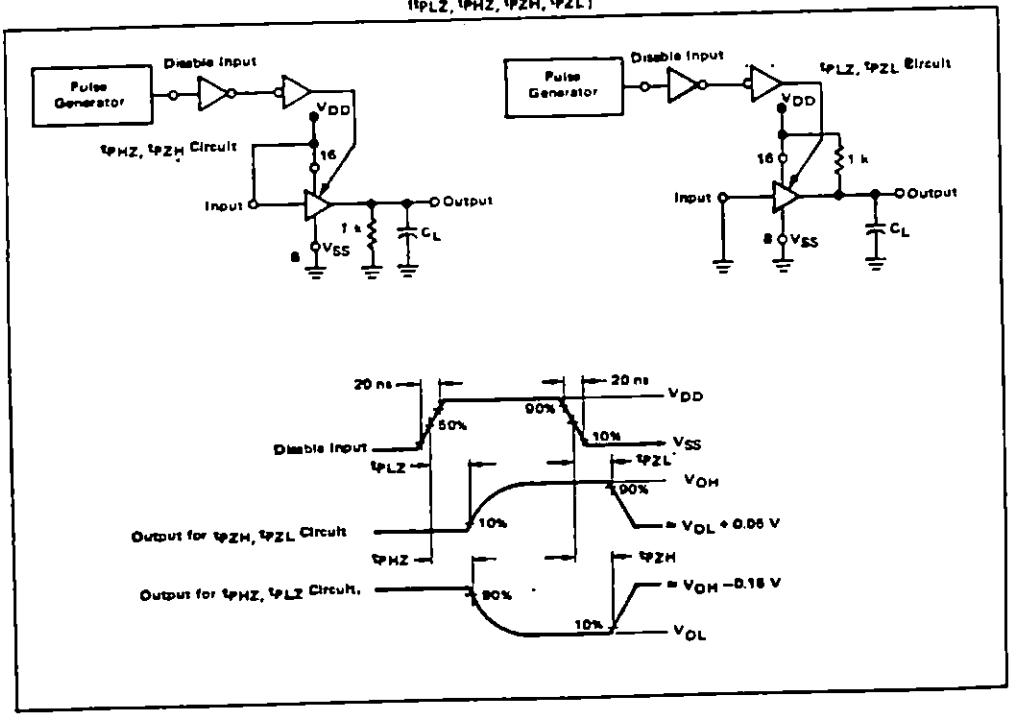


FIGURE 3 – 3 STATE AC TEST CIRCUITS AND WAVEFORMS
(t_{PLZ}, t_{PHZ}, t_{PZH}, t_{PZL})



National Semiconductor

CD4013BM/CD4013BC Dual D Flip-Flop

General Description

The CD4013B dual D flip-flop is a monolithic complementary MOS (CMOS) integrated circuit constructed with N- and P-channel enhancement mode transistors. Each flip-flop has independent data, set, reset, and clock inputs and "Q" and "$\overline{Q}$" outputs. These devices can be used for shift register applications, and by connecting "$\overline{Q}$" output to the data input, for counter and toggle applications. The logic level present at the "D" input is transferred to the Q output during the positive-going transition of the clock pulse. Setting or resetting is independent of the clock and is accomplished by a high level on the set or reset line respectively.

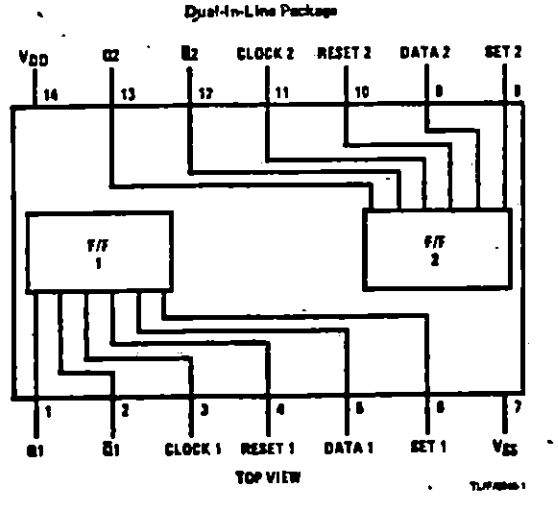
Features

■ Wide supply voltage range	3.0V to 15V
■ High noise immunity	0.45 V_{DD} (typ.)
■ Low power TTL compatibility	fan out of 2 driving 74L or 1 driving 74LS

Applications

- Automotive
- Data terminals
- Instrumentation
- Medical electronics
- Alarm system
- Industrial electronics
- Remote metering
- Computers

Connection Diagram



Order Number CD4013BMJ or CD4013BCJ
See NS Package J14A

Order Number CD4013BMN or CD4013BCN
See NS Package N14A

Truth Table

$CL^{\uparrow}$	D	R	S	Q	$\overline{Q}$
⌐	0	0	0	0	1
⌐	1	0	0	1	0
⌐	x	0	0	Q	$\overline{Q}$
x	x	1	0	0	1
x	x	0	1	1	0
x	x	1	1	1	1

No change
↑ = Level change
x = Don't care case

Absolute Maximum Ratings

(Notes 1 and 2)

V_{DD} dc Supply Voltage	−0.5 to +18 V_{DC}
V_{IN} Input Voltage	−0.5 to V_{DD} +0.5 V_{DC}
T_S Storage Temperature Range	−65°C to +150°C
P_D Package Dissipation	500 mW
T_L Lead Temperature (Soldering, 10 seconds)	260°C

Recommended Operating Conditions

(Note 2)

V_{DD} dc Supply Voltage	+3 to +15 V_{DC}
V_{IN} Input Voltage	0 to V_{DD} V_{DC}
T_A Operating Temperature Range	
CD4013BM	−55°C to +125°C
CD4013BC	−40°C to +85°C

DC Electrical Characteristics CD4013BM (Note 2)

SYM	PARAMETER	CONDITIONS	−55°C		25°C			125°C		UNITS
			MIN	MAX	MIN	TYP	MAX	MIN	MAX	
I_{DD}	Quiescent Device Current	V_{DD} = 5V, V_{IN} = V_{DD} or V_{SS}		1.0			1.0		30	μA
		V_{DD} = 10V, V_{IN} = V_{DD} or V_{SS}		2.0			2.0		60	μA
		V_{DD} = 15V, V_{IN} = V_{DD} or V_{SS}		4.0			4.0		120	μA
V_{OL}	Low Level Output Voltage	$\|I_O\|$ < 1.0μA								
		V_{DD} = 5V		0.05			0.05		0.05	V
		V_{DD} = 10V		0.05			0.05		0.05	V
		V_{DD} = 15V		0.05			0.05		0.05	V
V_{OH}	High Level Output Voltage	$\|I_O\|$ < 1.0μA								
		V_{DD} = 5V	4.95		4.95			4.95		V
		V_{DD} = 10V	9.95		9.95			9.95		V
		V_{DD} = 15V	14.95		14.95			14.95		V
V_{IL}	Low Level Input Voltage	$\|I_O\|$ < 1.0μA								
		V_{DD} = 5V, V_O = 0.5V or 4.5V		1.5			1.5		1.5	V
		V_{DD} = 10V, V_O = 1.0V or 9.0V		3.0			3.0		3.0	V
		V_{DD} = 15V, V_O = 1.5V or 13.5V		4.0			4.0		4.0	V
V_{IH}	High Level Input Voltage	$\|I_O\|$ < 1.0μA								
		V_{DD} = 5V, V_O = 0.5V or 4.5V	3.5		3.5			3.5		V
		V_{DD} = 10V, V_O = 1.0V or 9.0V	7.0		7.0			7.0		V
		V_{DD} = 15V, V_O = 1.5V or 13.5V	11.0		11.0			11.0		V
I_{OL}	Low Level Output Current (Note 3)	V_{DD} = 5V, V_O = 0.4V	0.64		0.51	0.88		0.36		mA
		V_{DD} = 10V, V_O = 0.5V	1.6		1.3	2.25		0.9		mA
		V_{DD} = 15V, V_O = 1.5V	4.2		3.4	8.8		2.4		mA
I_{OH}	High Level Output Current (Note 3)	V_{DD} = 5V, V_O = 4.6V	−0.64		−0.51	−0.88		−0.36		mA
		V_{DD} = 10V, V_O = 9.5V	−1.6		−1.3	−2.25		−0.9		mA
		V_{DD} = 15V, V_O = 13.5V	−4.2		−3.4	−8.8		−2.4		mA
I_{IN}	Input Current	V_{DD} = 15V, V_{IN} = 0V		−0.1		-10^{-5}	−0.1		−1.0	μA
		V_{DD} = 15V, V_{IN} = 15V		0.1		10^{-5}	0.1		1.0	μA

DC Electrical Characteristics CD4013BC (Note 2)

SYM	PARAMETER	CONDITIONS	−40°C		25°C			85°C		UNITS
			MIN	MAX	MIN	TYP	MAX	MIN	MAX	
I_{DD}	Quiescent Device Current	V_{DD} = 5V, V_{IN} = V_{DD} or V_{SS}		4.0			4.0		30	μA
		V_{DD} = 10V, V_{IN} = V_{DD} or V_{SS}		8.0			8.0		60	μA
		V_{DD} = 15V, V_{IN} = V_{DD} or V_{SS}		16.0			16.0		120	μA
V_{OL}	Low Level Output Voltage	$\|I_O\|$ < 1.0μA								
		V_{DD} = 5V		0.05			0.05		0.05	V
		V_{DD} = 10V		0.05			0.05		0.05	V
		V_{DD} = 15V		0.05			0.05		0.05	V
V_{OH}	High Level Output Voltage	$\|I_O\|$ < 1.0μA								
		V_{DD} = 5V	4.95		4.95			4.95		V
		V_{DD} = 10V	9.95		9.95			9.95		V
		V_{DD} = 15V	14.95		14.95			14.95		V
V_{IL}	Low Level Input Voltage	$\|I_O\|$ < 1.0μA								
		V_{DD} = 5V, V_O = 0.5V or 4.5V		1.5			1.5		1.5	V
		V_{DD} = 10V, V_O = 1.0V or 9.0V		3.0			3.0		3.0	V
		V_{DD} = 15V, V_O = 1.5V or 13.5V		4.0			4.0		4.0	V

DC Electrical Characteristics (Cont'd.) CD4013BC (Note 2)

SYM	PARAMETER	CONDITIONS	-40°C		25°C			85°C		UNITS
			MIN	MAX	MIN	TYP	MAX	MIN	MAX	
V_{IH}	High Level Input Voltage	$\|I_O\| < 1.0\mu A$								
		V_{DD} = 5V, V_O = 0.5V or 4.5V	3.5		3.5			3.5		V
		V_{DD} = 10V, V_O = 1.0V or 9.0V	7.0		7.0			7.0		V
		V_{DD} = 15V, V_O = 1.5V or 13.5V	11.0		11.0			11.0		V
I_{OL}	Low Level Output Current (Note 3)	V_{DD} = 5V, V_O = 0.4V	0.52		0.44	0.88		0.36		mA
		V_{DD} = 10V, V_O = 0.5V	1.3		1.1	2.25		0.9		mA
		V_{DD} = 15V, V_O = 1.5V	3.6		3.0	8.8		2.4		mA
I_{OH}	High Level Output Current (Note 3)	V_{DD} = 5V, V_O = 4.6V	-0.52		-0.44	-0.88		-0.36		mA
		V_{DD} = 10V, V_O = 9.5V	-1.3		-1.1	-2.25		-0.9		mA
		V_{DD} = 15V, V_O = 13.5V	-3.6		-3.0	-8.8		-2.4		mA
I_{IN}	Input Current	V_{DD} = 15V, V_{IN} = 0V		-0.3		-10^{-5}	-0.3		-1.0	μA
		V_{DD} = 15V, V_{IN} = 15V		0.3		10^{-5}	0.3		1.0	μA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed, they are not meant to imply that the devices should be operated at these limits. The table of "Recommended Operating Conditions" and "Electrical Characteristics" provides conditions for actual device operation.

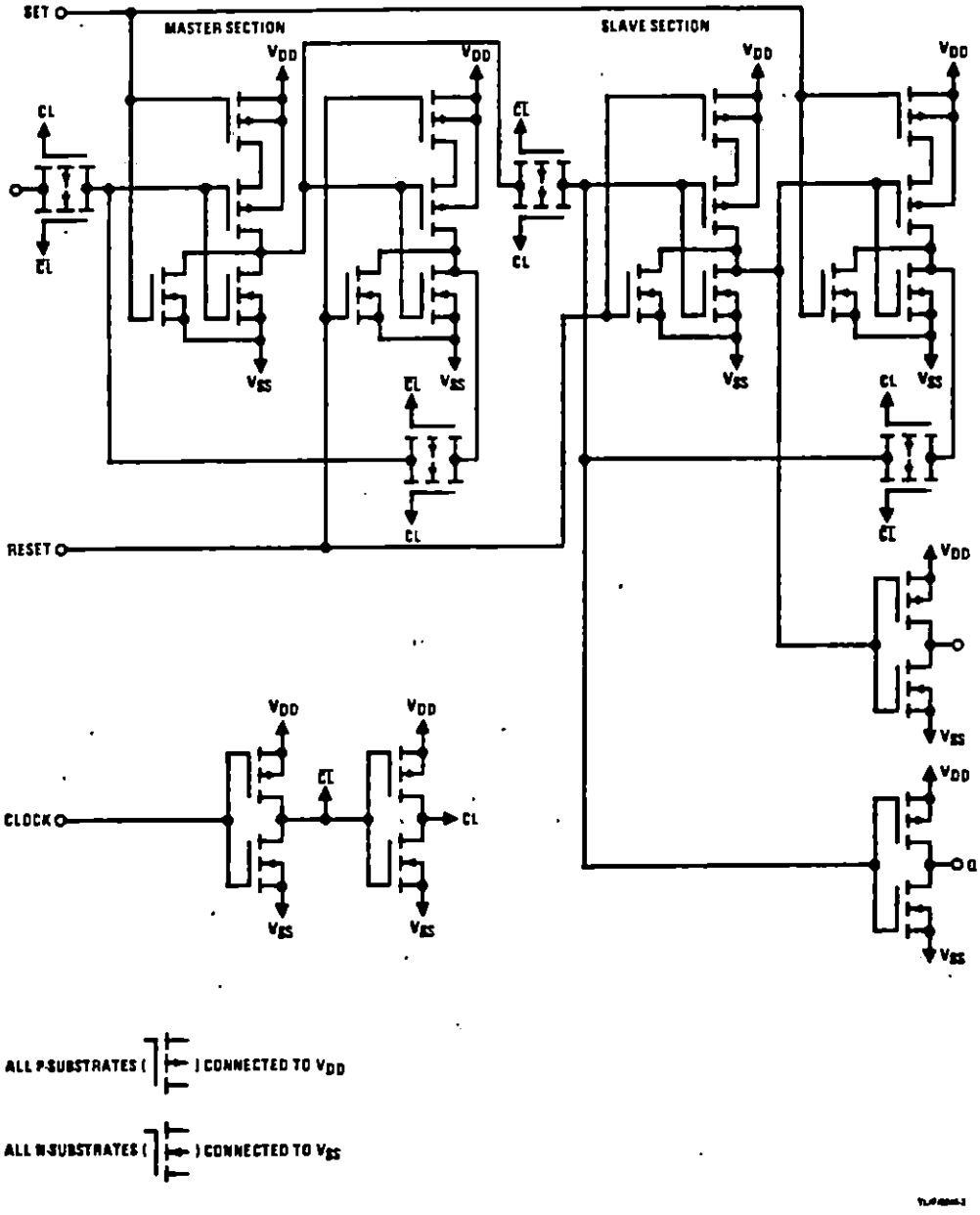
Note 2: V_{SS} = 0V unless otherwise specified.

Note 3: I_{OH} and I_{OL} are measured one output at a time.

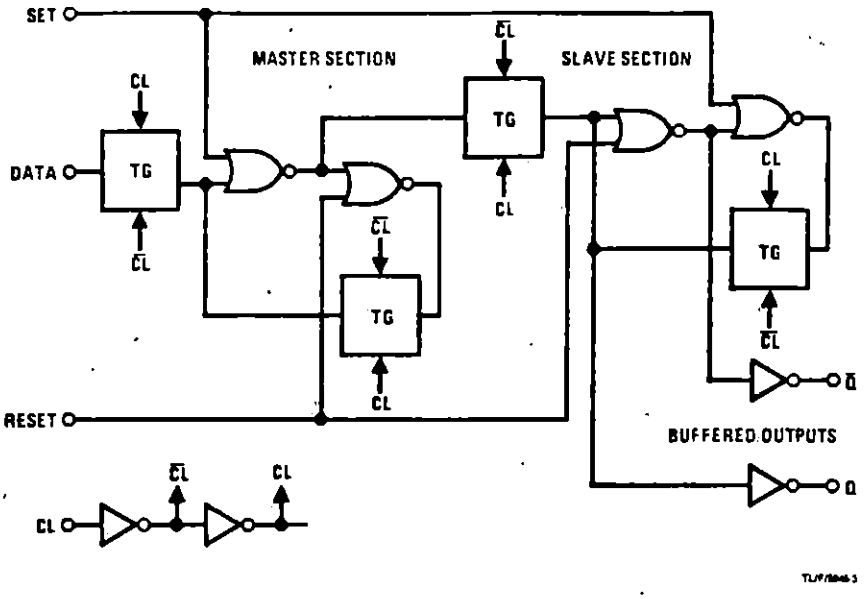
AC Electrical Characteristics $T_A = 25°C$, $C_L = 50\,pF$, $R_L = 200\,k$, unless otherwise noted

SYM	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
CLOCK OPERATION						
t_{PHL}, or t_{PLH}	Propagation Delay Time	V_{DD} = 5V		200	350	ns
		V_{DD} = 10V		80	160	ns
		V_{DD} = 15V		65	120	ns
t_{THL}, or t_{TLH}	Transition Time	V_{DD} = 5V		100	200	ns
		V_{DD} = 10V		50	100	ns
		V_{DD} = 15V		40	80	ns
t_{WL}, or t_{WH}	Minimum Clock Pulse Width	V_{DD} = 5V		100	200	ns
		V_{DD} = 10V		40	80	ns
		V_{DD} = 15V		32	65	ns
t_{RCL}, t_{FCL}	Maximum Clock Rise and Fall Time	V_{DD} = 5V			15	μs
		V_{DD} = 10V			10	μs
		V_{DD} = 15V			5	μs
t_{SU}	Minimum Set-Up Time	V_{DD} = 5V		20	40	ns
		V_{DD} = 10V		15	30	ns
		V_{DD} = 15V		12	25	ns
f_{CL}	Maximum Clock Frequency	V_{DD} = 5V	2.5	5		MHz
		V_{DD} = 10V	6.2	12.5		MHz
		V_{DD} = 15V	7.6	15.5		MHz
SET AND RESET OPERATION						
$t_{PHL(R)}$, $t_{PLH(S)}$	Propagation Delay Time	V_{DD} = 5V		150	300	ns
		V_{DD} = 10V		65	130	ns
		V_{DD} = 15V		45	90	ns
$t_{WH(R)}$, $t_{WH(S)}$	Minimum Set and Reset Pulse Width	V_{DD} = 5V		90	180	ns
		V_{DD} = 10V		40	80	ns
		V_{DD} = 15V		25	50	ns
C_{IN}	Average Input Capacitance	Any Input		5	7.5	pF

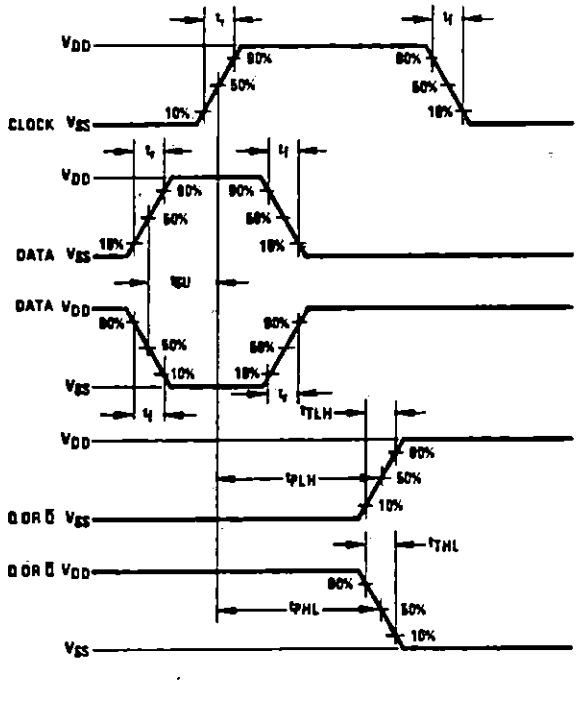
Schematic Diagram



Logic Diagram



Switching Time Waveforms



APPENDIX K

SONAR-RANGING SUBROUTINE FLOW CHART

Figure 9.
Sonar-Ranging Subroutine Flow Chart

