APPENDICES

APPENDIX A

CPU BOARD ELECTRONICS PARTS LIST

CPU Board

Designator	Description	Value, Type
R1, R2, R3, R26, R27, R28, R31, R32, R34, R35, R36, R37, R38, R40, R41, R42, R48, R49, R53, R55, R56, R57, R58	Resistor	10K OHM, 5%, 0.25 watt
R8, R9, R10, R11, R12, R13, R14, R15, R16, R18, R19, R20, R21, R46	Resistor	330 OHM, 5%, 0.25 watt
R22, R23, R24, R25	Resistor	22K OHM, 5%, 0.25 watt
R29, R30	Potentiometer	100K OHM, 5%
R33, R45, R59, R60, R61	Resistor	100K OHM, 5%, 0.25 watt
R39	Resistor	100 OHM, 5%, 0.25 watt
R43	Resistor	2.7K OHM, 5%, 0.25 watt
R44	Resistor	10K OHM, 5%, 0.25 watt
R47	Resistor	5.6K OHM, 5%, 0.25 watt
C2, C3, C4, C5, C6, C7, C14, C15, C16, C17, C18, C19, C20	Capacitor	0.01 UF, 20%, 100 volt

CPU Board (continued)

Designator	Description	Value, Type
C8	Capacitor	300PF, 20%, 100 volt
C9, C10, C11, C21	Capacitor	10 UF, 20%, 16 volt
C12, C22	Capacitor	1 UF, 20%, 16 volt
U1	Decoder	SN74LS139
U4, U20, U23	Programmable I/O	INS8255
U5	Driver	MC1413
U6	Inverter	SN74LS14
U7	Dual AND	SN74LS21
U8	Microprocessor	INS8073
U9	Voltage inverter	ICL7660
U11	Comparator	LM392
U12	Voltage sensor	ICL8211
U13	Hex buffer	CD4503
U14	PROM	2732 socket

APPENDIX B

CPU BOARD CHIP DATA SHEETS

MC1411 (ULN2001A)
MC1412 (ULN2002A)
MC1413 (ULN2003A)
MC1416 (ULN2004A)

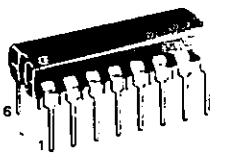
HIGH-VOLTAGE, HIGH-CURRENT DARLINGTON TRANSISTOR ARRAYS

The seven NPN Darlington-connected transistors in these arrays are well suited for driving lamps, relays or printer hammers in a variety of industrial and consumer applications. Their high breakdown voltage and internal suppression diodes insure freedom from problems associated with inductive loads. Peak inrush current to 600 mA permit them to drive incandescent lamps.

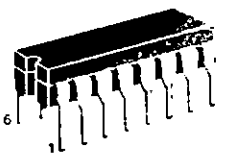
The MC1411 device is a general-purpose array for use with DTL, TTL, PMOS, or CMOS Logic. The MC1412 contains a zener diode and resistor in series with the input to limit input current for use with 14 to 25 Volt PMOS Logic. The MC1413 with a 2.7 kΩ series input resistor is well suited for systems utilizing 5 Volt TTL or CMOS Logic. The MC1416 uses a series 10.5 kΩ resistor and is useful in 8-18 Volt MOS systems.

PERIPHERAL DRIVER ARRAYS

SILICON MONOLITHIC INTEGRATED CIRCUITS



P OR PW= SUFFIX
PLASTIC PACKAGE
CASE 648



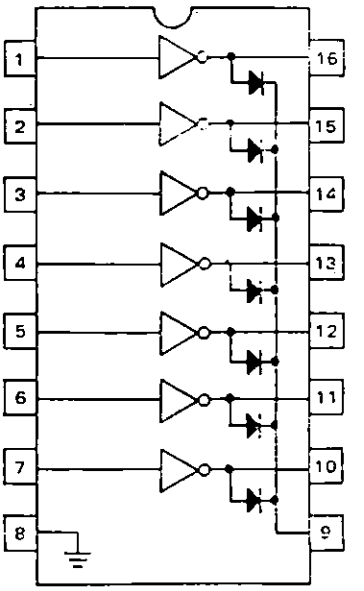
L SUFFIX
CERAMIC PACKAGE
CASE 620

MAXIMUM RATINGS (T_A = 25°C and rating apply to any one device in the package unless otherwise noted.)

Rating	Symbol	Value	Unit
Output Voltage	V_O	50*	V
Input Voltage (Except MC1411)	V_I	30	V
Collector Current – Continuous	I_C	500	mA
Base Current – Continuous	I_B	25	mA
Operating Ambient Temperature Range	T_A	0 to +85	°C
Storage Temperature Range	T_{stg}	-55 to +150	°C
Junction Temperature	T_J	150	°C

Maximum Package Power Dissipation (See Thermal Information Section)
*Higher voltage selection available. See your local representative.

PIN CONNECTIONS



DEVICE CROSS REFERENCE LISTING

9665 – SN75476 – ULN2001A – order MC1411P or PW=
9666 – SN75477 – ULN2002A – order MC1412P or PW
9667 – SN75478 – ULN2003A – order MC1413P or PW
9668 – – ULN2004A – order MC1416P or PW

=PW Package contains an internal heat spreading bar.

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
Output Leakage Current		I_{CEX}				μA
*(V_O = 50 V, T_A = +70°C)	All Types		–	–	100	
*(V_O = 50 V, T_A = +25°C)	All Types		–	–	50	
*(V_O = 50 V, T_A = +70°C, V_I = 6.0 V)	MC1412		–	–	500	
*(V_O = 50 V, T_A = +70°C, V_I = 1.0 V)	MC1416		–	–	500	
Collector-Emitter Saturation Voltage		$V_{CE(sat)}$				V
(I_C = 350 mA, I_B = 500 μA)			–	1.1	1.6	
(I_C = 200 mA, I_B = 350 μA)			–	0.95	1.3	
(I_C = 100 mA, I_B = 250 μA)			–	0.85	1.1	
Input Current – On Condition		$I_{I(on)}$				mA
(V_I = 17 V)	MC1412		–	0.85	1.3	
(V_I = 3.85 V)	MC1413			0.93	1.35	
(V_I = 5.0 V)	MC1416		–	0.35	0.5	
(V_I = 12 V)	MC1416		–	1.0	1.45	
Input Voltage – On Condition		$V_{I(on)}$				V
(V_{CE} = 2.0 V, I_C = 300 mA)	MC1412		–	–	13	
(V_{CE} = 2.0 V, I_C = 200 mA)	MC1413		–	–	2.4	
(V_{CE} = 2.0 V, I_C = 250 mA)	MC1413		–	–	2.7	
(V_{CE} = 2.0 V, I_C = 300 mA)	MC1413		–	–	3.0	
(V_{CE} = 2.0 V, I_C = 125 mA)	MC1416		–	–	5.0	
(V_{CE} = 2.0 V, I_C = 200 mA)	MC1416		–	–	6.0	
(V_{CE} = 2.0 V, I_C = 275 mA)	MC1416		–	–	7.0	
(V_{CE} = 2.0 V, I_C = 350 mA)	MC1416		–	–	8.0	
Input Current – Off Condition (I_C = 500 μA, T_A = +70°C)		$I_{I(off)}$	50	100	–	μA
DC Current Gain (V_{CE} = 2.0 V, I_C = 350 mA)	MC1411	h_{FE}	1000	–	–	–
Input Capacitance		C_I	–	15	30	pF
Turn-On Delay Time (50% E_I to 50% E_O)		t_{on}	–	0.25	1.0	μs
Turn-Off Delay Time (50% E_I to 50% E_O)		t_{off}	–	0.25	1.0	μs
Clamp Diode Leakage Current (V_R = 50 V)	T_A = +25°C T_A = +70°C	I_R	–	–	50 100	μA
Clamp Diode Forward Voltage (I_F = 350 mA)		V_F	–	1.5	2.0	V

*Higher voltage selections available, contact your local representative.

TYPICAL PERFORMANCE CURVES – T_A = 25°C

FIGURE 1 – OUTPUT CURRENT versus INPUT VOLTAGE

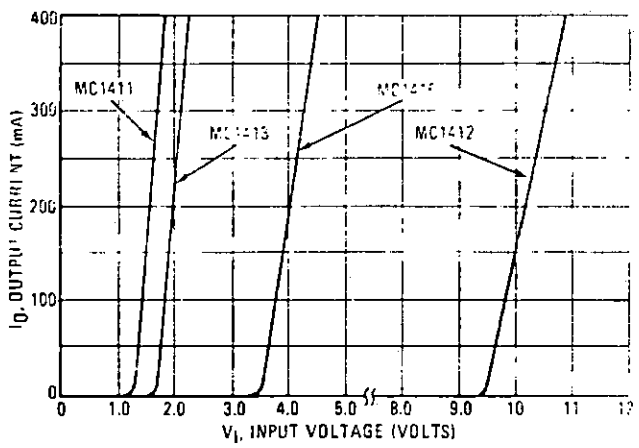
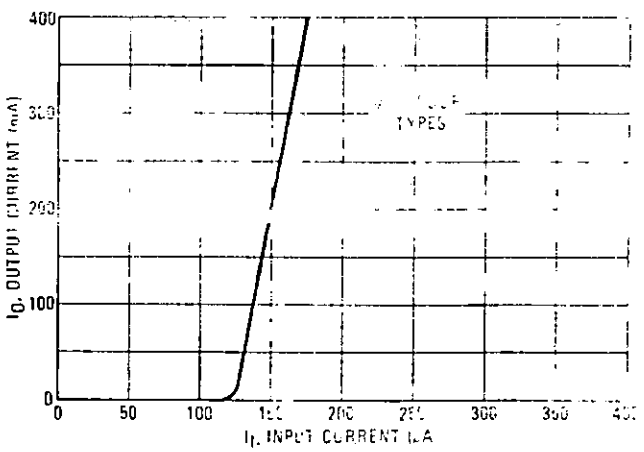


FIGURE 2 – OUTPUT CURRENT versus INPUT CURRENT



TYPICAL CHARACTERISTIC CURVES – T_A = 25°C (continued)

FIGURE 3 – TYPICAL OUTPUT CHARACTERISTICS

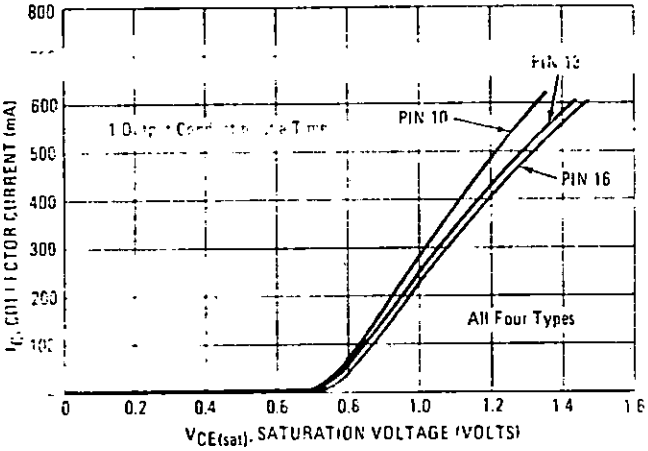


FIGURE 4 – INPUT CHARACTERISTICS – MC1412

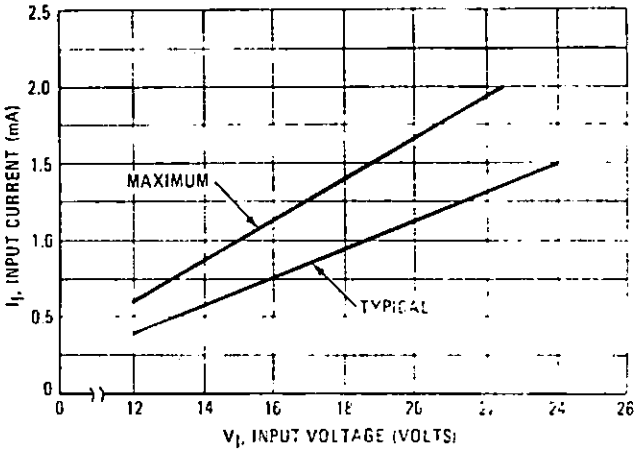


FIGURE 5 – INPUT CHARACTERISTICS – MC1413

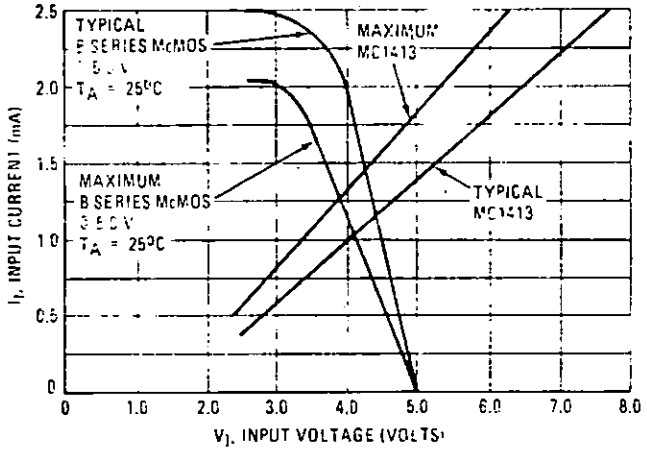


FIGURE 6 – INPUT CHARACTERISTICS – MC1416

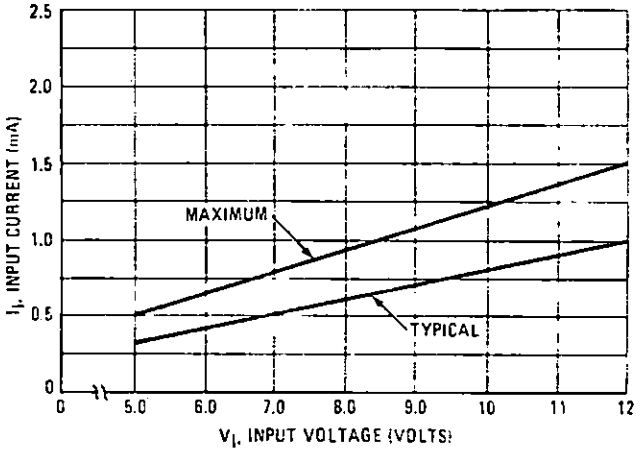


FIGURE 7 – MAXIMUM COLLECTOR CURRENT versus DUTY CYCLE (AND NUMBER OF DRIVERS IN USE) – CERAMIC

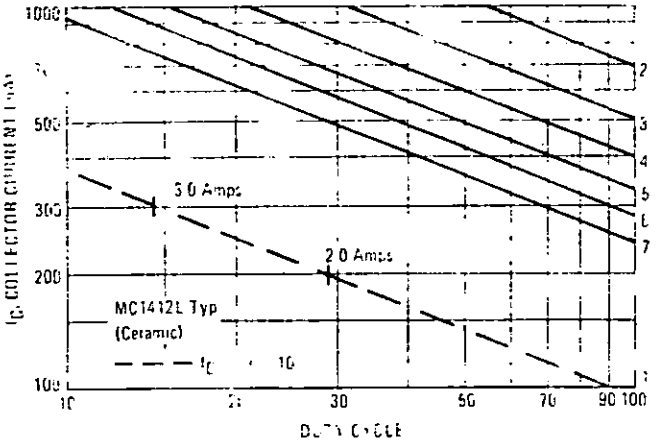
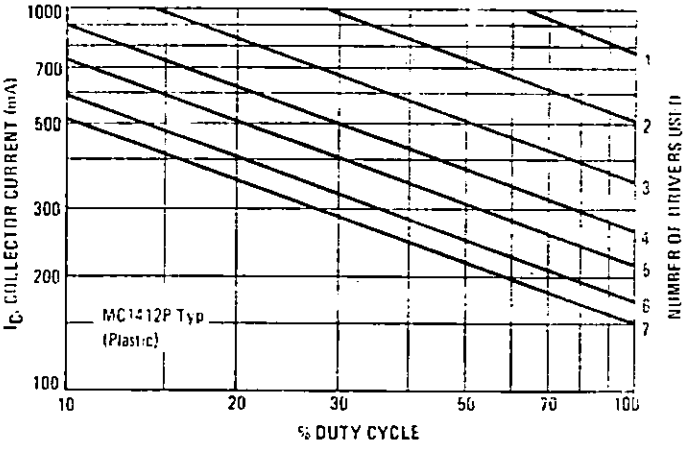


FIGURE 8 – MAXIMUM COLLECTOR CURRENT versus DUTY CYCLE (AND NUMBER OF DRIVERS IN USE) – PLASTIC



THERMAL INFORMATION

The maximum power consumption an integrated circuit can tolerate at a given operating ambient temperature, can be found from the equation

$$P_{D(T_A)} = \frac{T_{J(max)} - T_A}{R_{\theta JA(Typ)}} \geq I_C V_{CE}$$

Where

$P_{D(T_A)}$ = Power Dissipation allowable at a given operating ambient temperature.

$T_{J(max)}$ = Maximum Operating Junction Temperature as listed in the Maximum Ratings Section

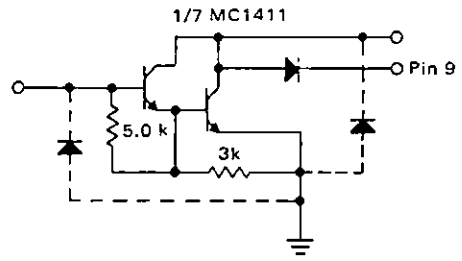
T_A = Maximum Desired Operating Ambient Temperature

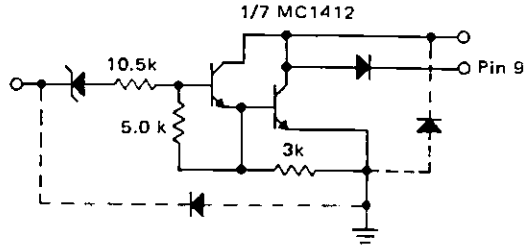
$R_{\theta JA(Typ)}$ = Typical Thermal Resistance Junction to Ambient

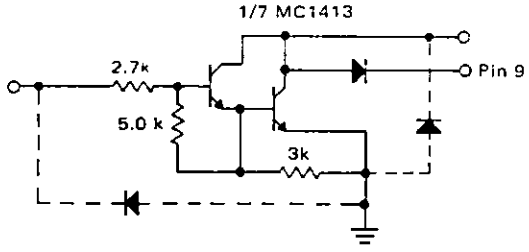
I_C = Total Sink Current

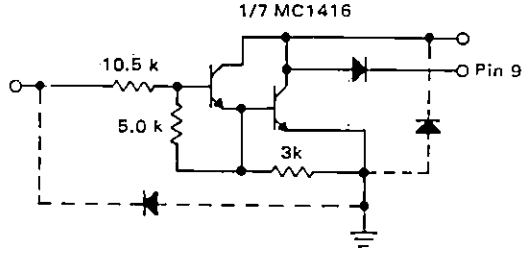
V_{CE} = Collector Voltage

REPRESENTATIVE CIRCUIT SCHEMATICS

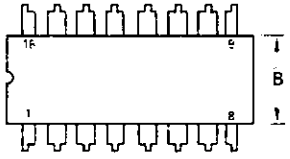


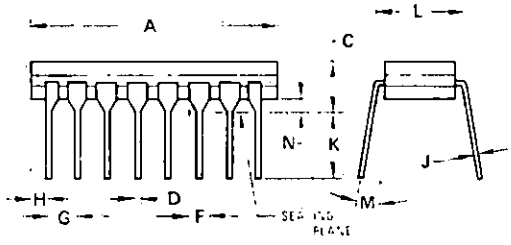






PACKAGE DIMENSIONS

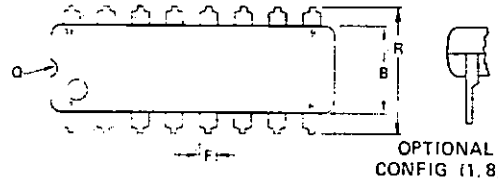


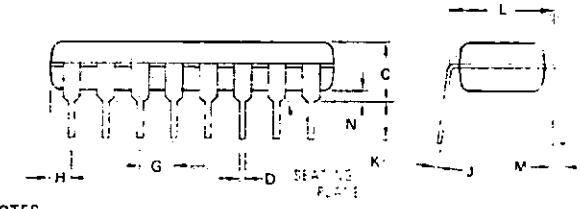


NOTES
1. LEADS WITHIN 0.13 mm (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION.
2. PACKAGE INDEX, NOTCH IN LEAD NOTCH IN CERAMIC OR INK DOT
3. DIM "A" AND "B" (620-06) DO NOT INCLUDE GLASS RUN OUT
4. DIM "L" TO INSIDE OF LEADS (MEASURED 0.51 mm (0.020) BELOW BODY)

DIM	MILLIMETERS MIN	MAX	INCHES MIN	MAX
A	19.05	19.94	0.750	0.785
B	6.22	7.11	0.245	0.280
C	3.94	5.08	0.155	0.200
D	0.38	0.51	0.015	0.020
F	0.89	1.65	0.035	0.065
G	2.54 BSC		0.100 BSC	
H	0.38	1.52	0.015	0.060
J	0.20	0.30	0.008	0.012
K	3.18	5.08	0.125	0.200
L	7.37	8.13	0.290	0.320
M	–	15°	–	15°
N	0.51	1.27	0.020	0.050

CASE 620-03





NOTES
1. LEADS WITHIN 0.13 mm (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION
2. DIMENSION "L" TO CENTER OF LEADS WHEN FORMED PARALLEL
3. DIMENSION "B" DOES NOT INCLUDE MOLD FLASH.
4. "F" DIMENSION IS FOR FULL LEADS. "HALF" LEADS ARE OPTIONAL AT LEAD POSITIONS 1, 8, 9, and 16).
5. DIMENSION "R" TO BE MEASURED AT THE TOP OF THE LEADS (NOT AT THE TIPS)

DIM	MILLIMETERS MIN	MAX	INCHES MIN	MAX
A		22.10	–	0.870
B	6.10	6.60	0.240	0.260
C		5.08	–	0.200
D	0.35	0.53	0.015	0.021
F		1.78		0.070
G	2.54 BSC		0.100 BSC	
H	0.38	2.41	0.015	0.095
J	0.20	0.38	0.008	0.015
K	2.92	–	0.115	
L	7.62 BSC		0.300 BSC	
M		15°	0°	15°
N	0.51		0.020	
R		5.26		

CASE 648-04

TYPES TIL413, TIL413S
LARGE-AREA SILICON PHOTODIODES

D2588, JULY 1980—REVISED JANUARY 1983

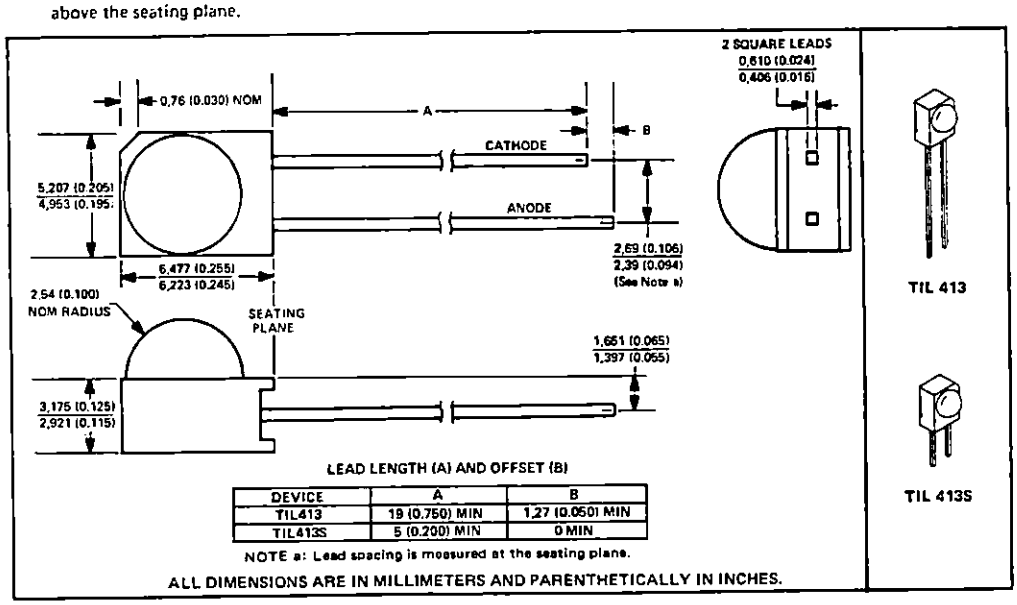
- High Photosensitivity
- Fast Response
- Low-Cost Plastic Package
- Designed for Infrared Remote-Control Systems
- Compatible with TIL38, TIL39, TIL905, and TIL906 IR Emitters

description

The TIL413 and TIL413S are high-speed PIN photodiodes designed to operate in the reverse-bias mode. These devices provide low capacitance with high speed and high photosensitivity suitable for near-infrared applications.

mechanical data

The photodiode chip is mounted on a lead frame and molded in black infrared-transmissive plastic. The active chip area is typically 4,4 square millimeters (0.0067 square inch). The centerline is nominally 3,8 millimeters (0.150 inch) above the seating plane.



LEAD LENGTH (A) AND OFFSET (B)

DEVICE	A	B
TIL413	19 (0.750) MIN	1,27 (0.050) MIN
TIL413S	5 (0.200) MIN	0 MIN

NOTE a: Lead spacing is measured at the seating plane.

ALL DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES.

PHOTODETECTORS

absolute maximum ratings at 25°C free-air temperature (unless otherwise noted)

Reverse Voltage	30 V
Continuous Power Dissipation at (or below) 25°C Free-Air Temperature (See Note 1)	150 mW
Operating Free-Air Temperature Range	−25°C to 80°C
Storage Temperature Range	−25°C to 100°C
Lead Temperature 1,6 mm (1/16 Inch) from Case for 5 Seconds	240°C

NOTE 1: Derate linearly to 80°C free-air temperature at the rate of 2.73 mW/°C.

TYPES TIL413, TIL413S
LARGE-AREA SILICON PHOTODIODES

electrical characteristics at 25 C free-air temperature

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$V_{(BR)}$	Breakdown Voltage	I_R = 100 μA,	E_e = 0	30			V
I_D	Dark Current	V_R = 10 V,	E_e = 0		5	50	nA
I_L	Light Current	V_R = 10 V,	E_e = 250 μW/cm², See Note 2	10	15		μA
C_T	Total Capacitance	V_R = 3 V,	E_e = 0, f = 1 MHz		15	50	pF
t_r	Rise Time	V_R = 10 V,	R_L = 1 kΩ		100		ns
t_f	Fall Time	V_R = 10 V,	R_L = 1 kΩ		100		ns

TYPICAL CHARACTERISTICS

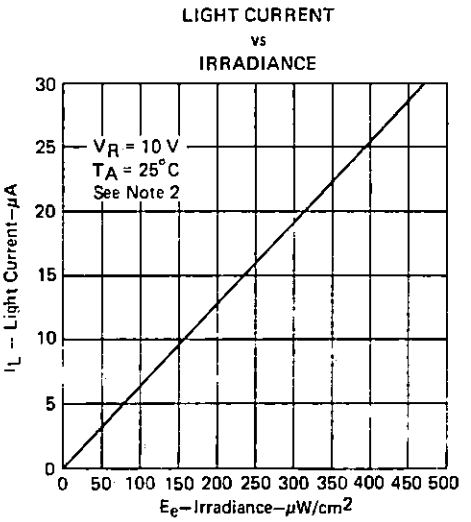


FIGURE 1

NOTE 2: Irradiance (E_e) is the radiant power per unit area incident upon a surface. For these measurements the source is an infrared emitting diode, wavelength at peak emission is 930 nm, and spectral bandwidth is 45 nm.

LOGIC PRODUCTS

SCHMITT TRIGGERS

54/74132, LS132

Quad 2-Input NAND Schmitt Trigger

DESCRIPTION

The '132 contains four 2-input NAND gates which accept standard TTL input signals and provide standard TTL output levels. They are capable of transforming slowly changing input signals into sharply defined, jitter-free output signals. In addition, they have greater noise margin than conventional NAND gates.

Each circuit contains a 2-input Schmitt trigger followed by a Darlington level shifter and a phase splitter driving a TTL totem-pole output. The Schmitt trigger uses positive feedback to effectively speed-up slow input transition, and provide different input threshold voltages for positive and negative-going transitions. This hysteresis between the positive-going and negative-going input threshold (typically 800mW) is determined internally by resistor ratios and is essentially insensitive to temperature and supply voltage variations. As long as one input remains at a more positive voltage than $V_{T+\,MAX}$, the gate will respond to the transitions of the other input as shown in Waveform 1.

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (Total)
74132	15ns	21mA
74LS132	15ns	7mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGES V_{CC} = 5V ± 5%; T_A = 0°C to +70°C	MILITARY RANGES V_{CC} = 5V ± 10%; T_A = −55°C to +125°C
Plastic DIP	N74132N • N74LS132N	
Ceramic DIP		S54132F • S54LS132F
Flatpack		S54132W • S54LS132W

FUNCTION TABLE

INPUTS		OUTPUT
A	B	Y
L	L	H
L	H	H
H	L	H
H	H	L

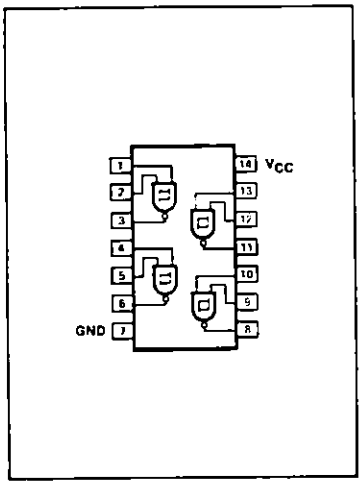
H = HIGH voltage level
L = LOW voltage level

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

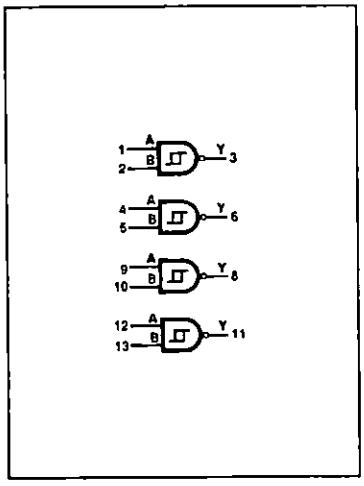
PINS	DESCRIPTION	54/74	54/74LS
A, B	Inputs	1ul	1LSul
Y	Ouput	10ul	10LSul

NOTE
Where a 54/74 unit load (ul) is understood to be 40µA I_{IH} and −1.6mA I_{IL}, and a 54/74LS unit load (LSul) is 20µA I_{IH} and −0.4mA I_{IL}.

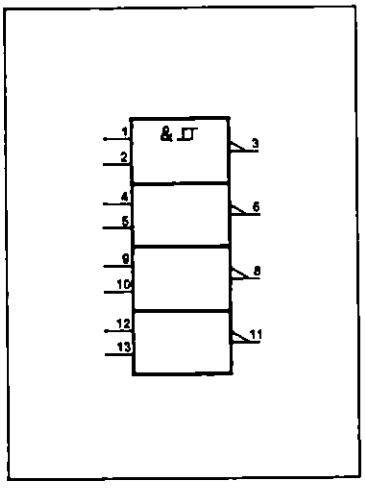
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



LOGIC PRODUCTS

SCHMITT TRIGGERS — 54/74132, LS132

ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

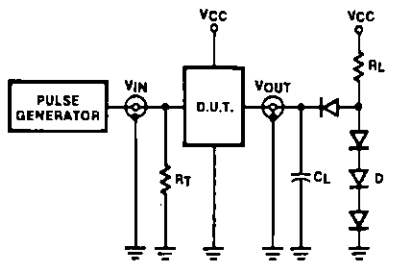
PARAMETER		54	54LS	74	74LS	UNIT
V_{CC}	Supply voltage	7.0	7.0	7.0	7.0	V
V_{IN}	Input voltage	−0.5 to +5.5	−0.5 to +7.0	−0.5 to +5.5	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +5	−30 to +1	−30 to +5	−30 to +1	mA
V_{OUT}	Voltage applied to output in HIGH output state	−0.5 to +V_{CC}	−0.5 to +V_{CC}	−0.5 to +V_{CC}	−0.5 to +V_{CC}	V
T_A	Operating free-air temperature range	−55 to +125		0 to 70		°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER			54/74			54/74LS			UNIT
			Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply voltage	Mil	4.5	5.0	5.5	4.5	5.0	5.5	V
		Com'l	4.75	5.0	5.25	4.75	5.0	5.25	V
I_{IK}	Input clamp current				−12			−18	mA
I_{OH}	HIGH-level output current				−800			−400	µA
I_{OL}	LOW-level output current	Mil			16			4	mA
		Com'l			16			8	mA
T_A	Operating free-air temperature	Mil	−55		+125	−55		+125	°C
		Com'l	0		70	0		70	°C

TEST CIRCUITS AND WAVEFORMS

TEST CIRCUIT FOR 54/74 TOTEM-POLE OUTPUTS



DEFINITIONS

R_L = Load resistor to V_{CC}; see AC CHARACTERISTICS for value

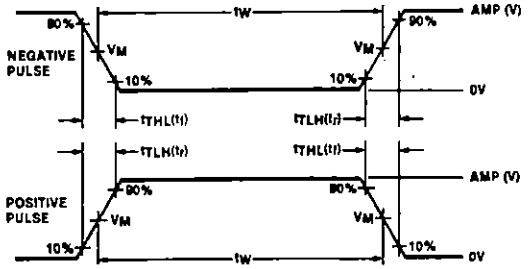
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.

D = Diodes are 1N916, 1N3064, or equivalent.

t_{TLH}, t_{THL} Values should be less than or equal to the table entries..

INPUT PULSE DEFINITIONS



V_M = 1.3V for 54LS/74LS; V_M = 1.5V for all other TTL families.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
54/74	3.0V	1MHz	500ns	7ns	7ns
54LS/74LS	3.0V	1MHz	500ns	15ns	6ns
54S/74S	3.0V	1MHz	500ns	2.5ns	2.5ns

LOGIC PRODUCTS

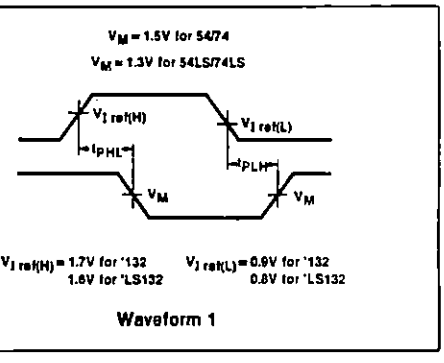
SCHMITT TRIGGERS — 54/74132, LS132

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER		TEST CONDITIONS[1]			54/74132			54/74LS132			UNIT
					Min	Typ[2]	Max	Min	Typ[2]	Max	
V_{T+}	Positive-going threshold	V_{CC} = 5.0V			1.5	1.7	2.0	1.4	1.6	1.9	V
V_{T-}	Negative-going threshold	V_{CC} = 5.0V			0.6	0.9	1.1	0.5	0.8	1.0	V
ΔV_T	Hysteresis ($V_{T+} - V_{T-}$)	V_{CC} = 5.0V			0.4	0.8		0.4	0.8		V
V_{OH}	HIGH-level output voltage	V_{CC} = MIN, V_I = V_{T-MIN+}, I_{OH} = MAX		Mil	2.4	3.4		2.5	3.4		V
				Com'l	2.4	3.4		2.7	3.4		V
V_{OL}	LOW-level output voltage	V_{CC} = MIN, V_I = V_{T+MAX}	I_{OL} = MAX	Mil		0.2	0.4		0.25	0.4	V
				Com'l		0.2	0.4		0.35	0.5	V
			I_{OL} = 4mA	74LS					0.25	0.4	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = I_{IK}					-1.5			-1.5	V
I_{T+}	Input current at positive-going threshold	V_{CC} = 5.0V, V_I = V_{T+}				-0.43			-0.14		mA
I_{T-}	Input current at negative-going threshold	V_{CC} = 5.0V, V_I = V_{T-}				-0.56			-0.18		mA
I_I	Input current at maximum input voltage	V_{CC} = MAX	V_I = 5.5V				1.0				mA
			V_I = 7.0V							0.1	mA
I_{IH}	HIGH-level input current	V_{CC} = MAX	V_I = 2.4V				40				μA
			V_I = 2.7V							20	μA
I_{IL}	LOW-level input current	V_{CC} = MAX, V_I = 0.4V					-1.2			-0.4	mA
I_{OS}	Short-circuit output current[3]	V_{CC} = MAX		Mil	-18		-55	-20		-100	mA
				Com'l	-18		-55	-20		-100	mA
I_{CC}	Supply current (total)	V_{CC} = MAX	I_{CCH}	Outputs HIGH		15	24		5.9	11	mA
			I_{CCL}	Outputs LOW		26	40		8.2	14	mA

NOTES
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. I_{OS} is tested with V_{OUT} = +0.5V and V_{CC} = V_{CC} MAX + 0.5V. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.

AC WAVEFORMS



Waveform 1

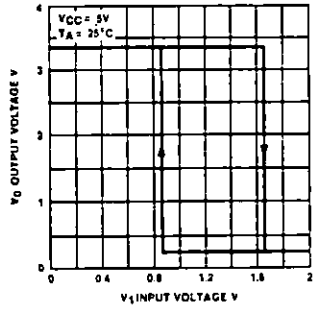
AC CHARACTERISTICS T_A = 25°C, V_{CC} = 5.0V

PARAMETER		TEST CONDITIONS	54/74		54LS/74LS		UNIT
			C_L = 15pF, R_L = 400Ω		C_L = 15pF, R_L = 2kΩ		
			Min	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay	Waveform 1		22 22		22 22	ns

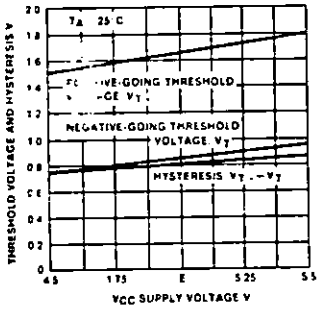
SCHMITT TRIGGERS — 54/74132, LS132

TYPICAL CHARACTERISTICS

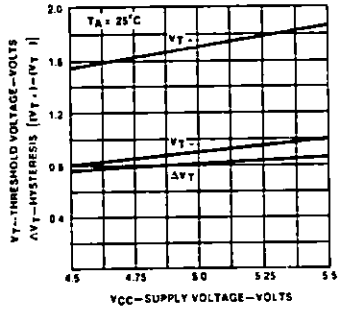
(54/74, 54LS/74LS)
V_{IN} vs V_{OUT} TRANSFER FUNCTION



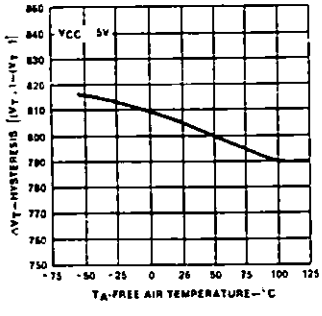
(54/74)
THRESHOLD VOLTAGE AND HYSTERESIS vs POWER SUPPLY VOLTAGE



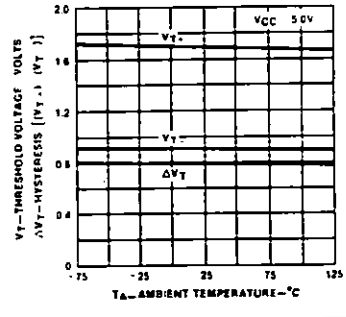
(54LS/74LS)
THRESHOLD VOLTAGE AND HYSTERESIS vs POWER SUPPLY VOLTAGE



(54/74)
HYSTERESIS vs TEMPERATURE



(54LS/74LS)
THRESHOLD VOLTAGE AND HYSTERESIS vs AMBIENT TEMPERATURE



LOGIC PRODUCTS

SCHMITT TRIGGERS

54/7414, LS14

Hex Inverter Schmitt Trigger

DESCRIPTION

The '14 contains six logic inverters which accept standard TTL input signals and provide standard TTL output levels. They are capable of transforming slowly changing input signals into sharply defined, jitter-free output signals. In addition, they have greater noise margin than conventional inverters.

Each circuit contains a Schmitt trigger followed by a Darlington level shifter and a phase splitter driving a TTL totem-pole output. The Schmitt trigger uses positive feedback to effectively speed-up slow input transition, and provide different input threshold voltages for positive and negative-going transitions. This hysteresis between the positive-going and negative-going input thresholds (typically 800mV) is determined internally by resistor ratios and is essentially insensitive to temperature and supply voltage variations.

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (Total)
7414	15ns	31mA
74LS14	15ns	10mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGES V_{CC} = 5V ±5%; T_A = 0°C to +70°C	MILITARY RANGES V_{CC} = 5V ±10%; T_A = −55°C to +125°C
Plastic DIP	N7414N • N74LS14N	
Plastic SO	N74LS14D	
Ceramic DIP		S5414F • S54LS14F
Flatpack		S5414W • S54LS14W

FUNCTION TABLE

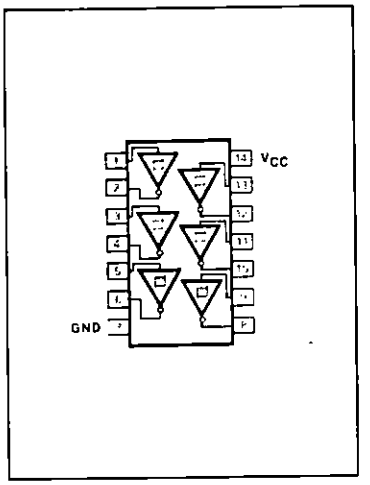
INPUT	OUTPUT
A	Y
0	1
1	0

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

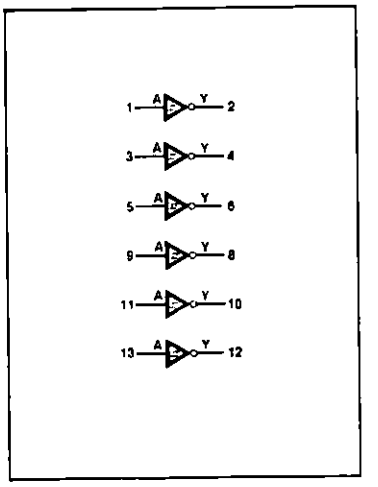
PINS	DESCRIPTION	54/74	54/74LS
A	Inputs	1ul	1LSul
Y	Output	10ul	10LSul

NOTE
Where a 54/74 unit load (ul) is understood to be 40μA I_{IH} and −1.6mA I_{IL}, and a 54/74LS unit load (LSul) is 20μA I_{IH} and −0.4mA I_{IL}.

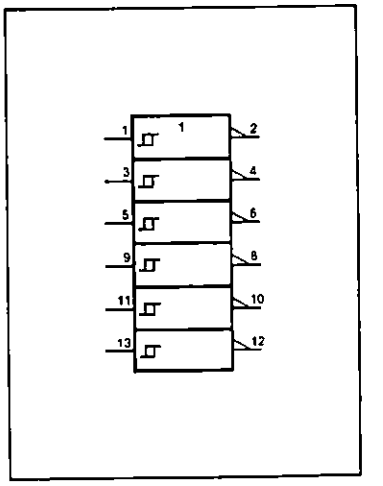
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



LOGIC PRODUCTS

SCHMITT TRIGGERS — 54/7414, LS14

ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

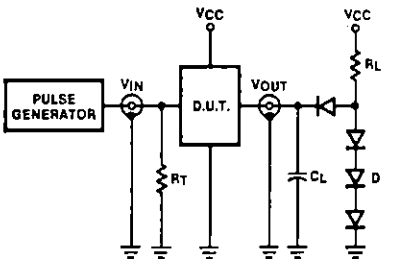
PARAMETER		54	54LS	74	74LS	UNIT
V_{CC}	Supply voltage	7.0	7.0	7.0	7.0	V
V_{IN}	Input voltage	−0.5 to +5.5	−0.5 to +7.0	−0.5 to +5.5	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +5	−30 to +1	−30 to +5	−30 to +1	mA
V_{OUT}	Voltage applied to output in HIGH output state	−0.5 to +V_{CC}	−0.5 to +V_{CC}	−0.5 to +V_{CC}	−0.5 to +V_{CC}	V
T_A	Operating free-air temperature range	−55 to +125		0 to 70		°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER			54/74			54/74LS			UNIT
			Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply voltage	Mil	4.5	5.0	5.5	4.5	5.0	5.5	V
		Com'l	4.75	5.0	5.25	4.75	5.0	5.25	V
I_{IK}	Input clamp current				−12			−18	mA
I_{OH}	HIGH-level output current				−800			−400	μA
I_{OL}	LOW-level output current	Mil			16			4	mA
		Com'l			16			8	mA
T_A	Operating free-air temperature	Mil	−55		+125	−55		+125	°C
		Com'l	0		70	0		70	°C

TEST CIRCUITS AND WAVEFORMS

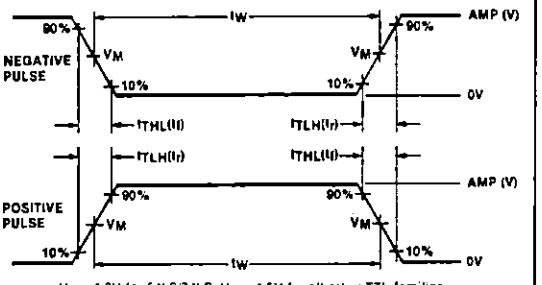
TEST CIRCUIT FOR 54/74 TOTEM-POLE OUTPUTS



DEFINITIONS

R_L = Load resistor to V_{CC}; see AC CHARACTERISTICS for value
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value
R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators
D = Diodes are 1N916, 1N3064 or equivalent
t_{TLH}, t_{THL} Values should be less than or equal to the table entries.

INPUT PULSE DEFINITIONS



V_M = 1.3V for 54LS/74LS. V_M = 1.5V for all other TTL families

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
54/74	3.0V	1MHz	500ns	7ns	7ns
54LS/74LS	3.0V	1MHz	500ns	15ns	6ns
54S/74S	3.0V	1MHz	500ns	2.5ns	2.5ns

LOGIC PRODUCTS

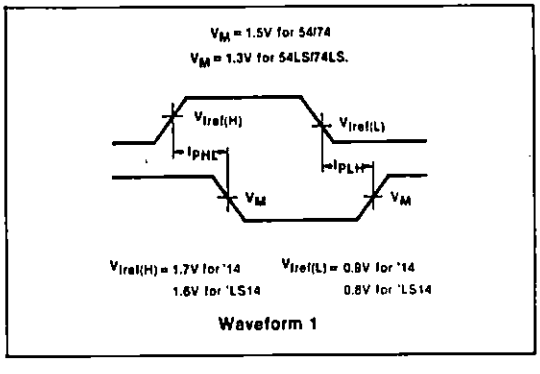
SCHMITT TRIGGERS — 54/7414, LS14

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER		TEST CONDITIONS[1]			54/7414			54/74LS14			UNIT
					Min	Typ[2]	Max	Min	Typ[2]	Max	
V_{T+}	Positive-going threshold	V_{CC} = 5.0V			1.5	1.7	2.0	1.4	1.6	1.9	V
V_{T-}	Negative-going threshold	V_{CC} = 5.0V			0.6	0.9	1.1	0.5	0.8	1.0	V
ΔV_T	Hysteresis ($V_{T+} - V_{T-}$)	V_{CC} = 5.0V			0.4	0.8		0.4	0.8		V
V_{OH}	HIGH-level output voltage	V_{CC} = MIN, $V_I = V_{T-MIN}$, I_{OH} = MAX		Mil	2.4	3.4		2.5	3.4		V
				Com'l	2.4	3.4		2.7	3.4		V
V_{OL}	LOW-level output voltage	V_{CC} = MIN, $V_I = V_{T+MAX}$	I_{OL} = MAX	Mil		0.2	0.4		0.25	0.4	V
				Com'l		0.2	0.4		0.35	0.5	V
			I_{OL} = 4mA	74LS					0.25	0.4	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, $I_I = I_{IK}$					-1.5			-1.5	V
I_{T+}	Input current at positive-going threshold	V_{CC} = 5.0V, $V_I = V_{T+}$				-0.43			-0.14		mA
I_{T-}	Input current at negative-going threshold	V_{CC} = 5.0V, $V_I = V_{T-}$				-0.56			-0.18		mA
I_I	Input current at maximum input voltage	V_{CC} = MAX	V_I = 5.5V				1.0				mA
			V_I = 7.0V							0.1	mA
I_{IH}	HIGH-level input current	V_{CC} = MAX	V_I = 2.4V				40				µA
			V_I = 2.7V							20	µA
I_{IL}	LOW-level input current	V_{CC} = MAX, V_I = 0.4V					-1.2			-0.4	mA
I_{OS}	Short-circuit output current[3]	V_{CC} = MAX		Mil	-20		-55	-20		-100	mA
				Com'l	-18		-55	-20		-100	mA
I_{CC}	Supply current (total)	V_{CC} = MAX	I_{CCH}	Outputs HIGH		22	36		8.6	16	mA
			I_{CCL}	Outputs LOW		39	60		12	21	mA

NOTES
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. I_{OS} is tested with V_{OUT} = +0.5V and $V_{CC} = V_{CC}$ MAX + 0.5V. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.

AC WAVEFORMS



Waveform 1

AC CHARACTERISTICS T_A = 25°C, V_{CC} = 5.0V

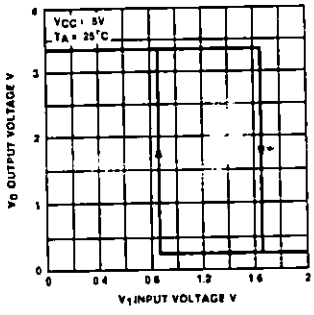
PARAMETER		TEST CONDITIONS	54/74		54LS/74LS		UNIT
			C_L = 15pF, R_L = 400Ω		C_L = 15pF, R_L = 2kΩ		
			Min	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay	Waveform 1		22 22		22 22	ns

SCHMITT TRIGGERS

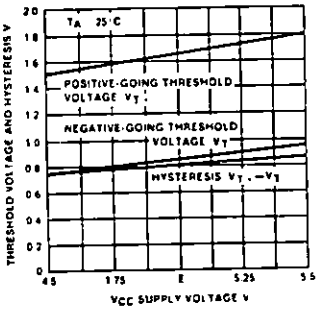
54/7414, LS14

TYPICAL CHARACTERISTICS

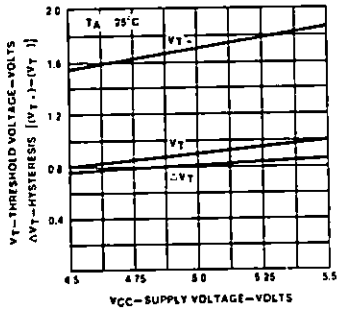
(54/74, 54LS/74LS)
V_{IN} vs V_{OUT}
TRANSFER FUNCTION



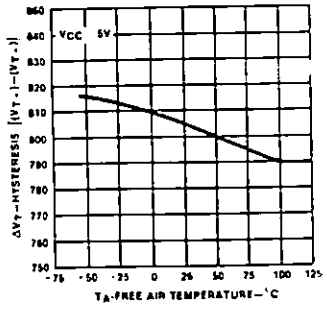
(54/74)
THRESHOLD VOLTAGE AND
HYSTERESIS vs
POWER SUPPLY VOLTAGE



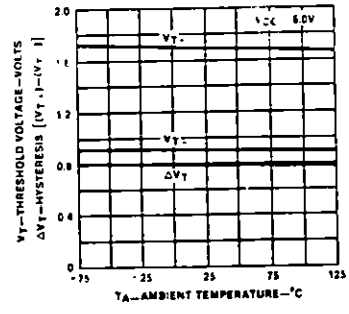
(54LS/74LS)
THRESHOLD VOLTAGE AND
HYSTERESIS vs
POWER SUPPLY VOLTAGE



(54/74)
HYSTERESIS vs TEMPERATURE



(54LS/74LS)
THRESHOLD VOLTAGE AND
HYSTERESIS vs
AMBIENT TEMPERATURE



LOGIC PRODUCTS

DECODERS/DEMULTIPLEXERS

54/74LS138, S138

1-Of-8 Decoder/Demultiplexer

- Demultiplexing capability
- Multiple input enable for easy expansion
- Ideal for memory chip select decoding
- Direct replacement for Intel 3205

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (Total)
74LS138	20ns	6.3mA
74S138	7ns	49mA

DESCRIPTION

The '138 decoder accepts three binary weighted inputs (A_0, A_1, A_2) and when enabled, provides eight mutually exclusive, active LOW outputs ($\overline{0}$-$\overline{7}$). The device features three Enable inputs: two active LOW ($\overline{E}_1$, $\overline{E}_2$) and one active HIGH (E_3). Every output will be HIGH unless $\overline{E}_1$ and $\overline{E}_2$ are LOW and E_3 is HIGH. This multiple enable function allows easy parallel expansion of the device to a 1-of-32 (5 lines to 32 lines) decoder with just four '138s and one inverter.

The device can be used as an eight output demultiplexer by using one of the active LOW Enable inputs as the Data input and the remaining Enable inputs as strobes. Enable inputs not used must be permanently tied to their appropriate active HIGH or active LOW state.

ORDERING CODE

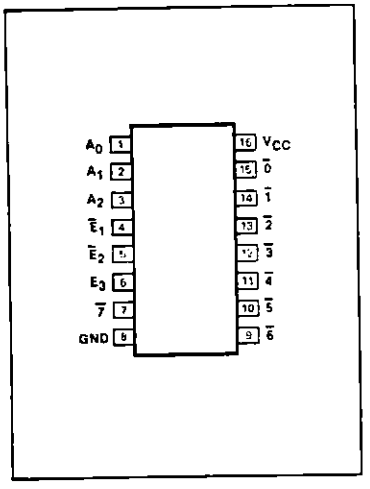
PACKAGES	COMMERCIAL RANGES V_{CC} = 5V ± 5%; T_A = 0°C to +70°C	MILITARY RANGES V_{CC} = 5V ± 10%; T_A = −55°C to +125°C
Plastic DIP	N74S138N • N74LS138N	
Plastic SO	N74LS138D • N74S138D	
Ceramic DIP		S54S138F • S54LS138F
Flatpack		S54S138W • S54LS138W
LLCC		S54LS138G

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

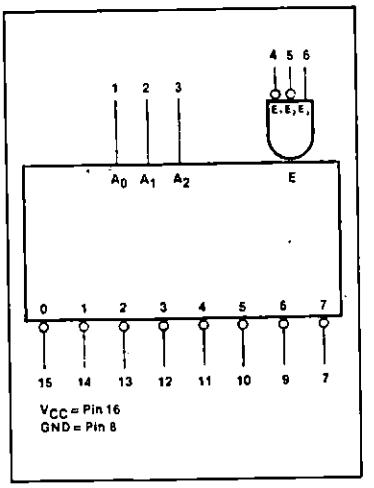
PINS	DESCRIPTION	54/74S	54/74LS
All	Inputs	1SuI	1LSuI
All	Outputs	10SuI	10LSuI

NOTE
Where a 54/74S unit load (SuI) is 50μA I_{IH} and −2.0mA I_{IL}, and a 54/74LS unit load (LSuI) is 20μA I_{IH} and −0.4mA I_{IL}.

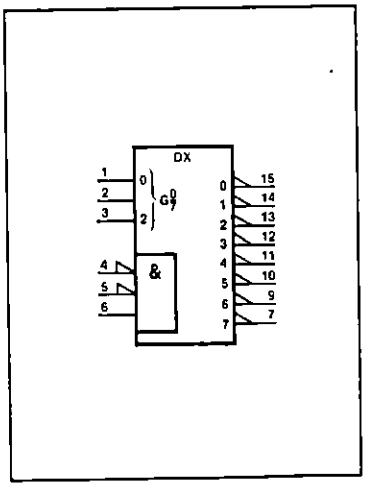
PIN CONFIGURATION



LOGIC SYMBOL



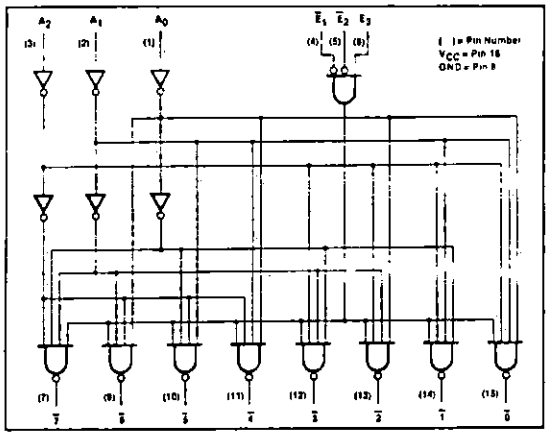
LOGIC SYMBOL (IEEE/IEC)



LOGIC PRODUCTS

DECODERS/DEMULTIPLEXERS 54/74LS138, S138

LOGIC DIAGRAM



FUNCTION TABLE

INPUTS						OUTPUTS							
$\overline{E}_1$	$\overline{E}_2$	E_3	A_0	A_1	A_2	$\overline{0}$	$\overline{1}$	$\overline{2}$	$\overline{3}$	$\overline{4}$	$\overline{5}$	$\overline{6}$	$\overline{7}$
H	X	X	X	X	X	H	H	H	H	H	H	H	H
X	H	X	X	X	X	H	H	H	H	H	H	H	H
X	X	L	X	X	X	H	H	H	H	H	H	H	H
L	L	H	L	L	L	L	H	H	H	H	H	H	H
L	L	H	H	L	L	H	L	H	H	H	H	H	H
L	L	H	L	H	L	H	H	L	H	H	H	H	H
L	L	H	H	H	L	H	H	H	L	H	H	H	H
L	L	H	L	L	H	H	H	H	H	L	H	H	H
L	L	H	H	L	H	H	H	H	H	H	L	H	H
L	L	H	L	H	H	H	H	H	H	H	H	L	H
L	L	H	H	H	H	H	H	H	H	H	H	H	L

NOTES
H = HIGH voltage level
L = LOW voltage level
X = Don't care

ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER		54LS	54S	74LS	74S	UNIT
V_{CC}	Supply voltage	7.0	7.0	7.0	7.0	V
V_{IN}	Input voltage	−0.5 to +7.0	−0.5 to +5.5	−0.5 to +7.0	−0.5 to +5.5	V
I_{IN}	Input current	−30 to +1	−30 to +5	−30 to +1	−30 to +5	mA
V_{OUT}	Voltage applied to output in HIGH output state	−0.5 to +V_{CC}	−0.5 to +V_{CC}	−0.5 to +V_{CC}	−0.5 to +V_{CC}	V
T_A	Operating free-air temperature range	−55 to +125		0 to 70		°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER			54/74LS			54/74S			UNIT
			Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply voltage	Mil	4.5	5.0	5.5	4.5	5.0	5.5	V
		Com'l	4.75	5.0	5.25	4.75	5.0	5.25	V
V_{IH}	HIGH-level input voltage		2.0			2.0			V
V_{IL}	LOW-level input voltage	Mil			+0.7			+0.8	V
		Com'l			+0.8			+0.8	V
I_{IK}	Input clamp current				−18			−18	mA
I_{OH}	HIGH-level output current				−400			−1000	µA
I_{OL}	LOW-level output current	Mil			4			20	mA
		Com'l			8			20	mA
T_A	Operating free-air temperature	Mil	−55		+125	−55		+125	°C
		Com'l	0		70	0		70	°C

NOTE
V_{IL} = +0.7V MAX for 54S at T_A = +125°C only

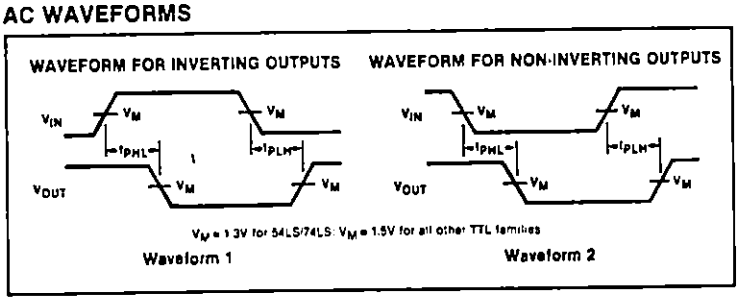
DECODERS/DEMULTIPLEXERS 54/74LS138, S138

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER		TEST CONDITIONS[1]			54/74LS138			54/74S138			UNIT
					Min	Typ[2]	Max	Min	Typ[2]	Max	
V_{OH}	HIGH-level output voltage	V_{CC} = MIN, V_{IH} = MIN, V_{IL} = MAX, I_{OH} = MAX		Mil	2.5	3.4		2.5	3.4		V
				Com'l	2.7	3.4		2.7	3.4		V
V_{OL}	LOW-level output voltage	V_{CC} = MIN, V_{IH} = MIN, V_{IL} = MAX	I_{OL} = MAX	Mil		0.25	0.4			0.5[5]	V
				Com'l		0.35	0.5			0.5	V
			I_{OL} = 4mA	74LS		0.25	0.4				V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = I_{IK}					– 1.5			– 1.2	V
I_I	Input current at maximum input voltage	V_{CC} = MAX	V_I = 5.5V							1.0	mA
			V_I = 7.0V				0.1				mA
I_{IH}	HIGH-level input current	V_{CC} = MAX, V_I = 2.7V					20			50	μA
I_{IL}	LOW-level input current	V_{CC} = MAX	V_I = 0.4V				– 0.4				mA
			V_I = 0.5V							– 2	mA
I_{OS}	Short-circuit output current[3]	V_{CC} = MAX			– 20		– 100	– 40		– 100	mA
I_{CC}	Supply current[4] (total)	V_{CC} = MAX				6.3	10		49	74	mA

NOTES
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. I_{OS} is tested with V_{OUT} = + 0.5V and V_{CC} = V_{CC} MAX + 0.5V. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
4. To measure I_{CC}, outputs must be enabled and open.
5. V_{OL} = + 0.45V MAX for 54S at T_A = + 125°C only.

AC WAVEFORMS



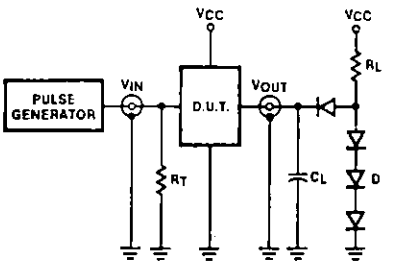
AC CHARACTERISTICS T_A = 25°C, V_{CC} = 5.0V

PARAMETER		TEST CONDITIONS	54/74LS C_L = 15pF, R_L = 2kΩ		54/74S C_L = 15pF, R_L = 280Ω		UNIT
			Min	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay Address to output	Waveform 2 2 logic levels		20 41		7 10.5	ns
t_{PLH} t_{PHL}	Propagation delay Address to output	Waveform 1 3 logic levels		27 39		12 12	ns
t_{PLH} t_{PHL}	Propagation delay Enable to output	Waveform 2 2 logic levels		18 32		8 11	ns
t_{PLH} t_{PHL}	Propagation delay Enable to output	Waveform 1 3 logic levels		26 38		11 11	ns

DECODERS/DEMULTIPLEXERS 54/74LS138, S138

TEST CIRCUITS AND WAVEFORMS

TEST CIRCUIT FOR 54/74 TOTEM-POLE OUTPUTS



DEFINITIONS

R_L = Load resistor to V_{CC}; see AC CHARACTERISTICS for value

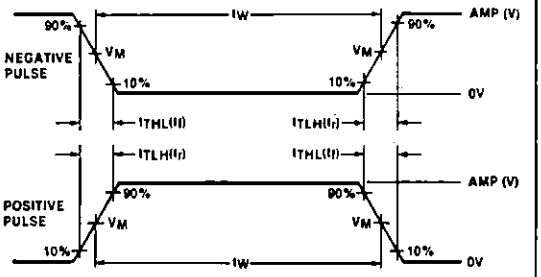
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value

R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators

D = Diodes are 1N916, 1N3064, or equivalent.

t_{TLH}, t_{THL} Values should be less than or equal to the table entries

INPUT PULSE DEFINITIONS



V_M = 1.3V for 54LS/74LS, V_M = 1.5V for all other TTL families

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
54/74	3.0V	1MHz	500ns	7ns	7ns
54LS/74LS	3.0V	1MHz	500ns	15ns	6ns
54S/74S	3.0V	1MHz	500ns	2.5ns	2.5ns

LOGIC PRODUCTS

DECODERS/DEMULTIPLEXERS 54/74LS139, S139

Dual 1-of-4 Decoder/Demultiplexer

- Demultiplexing capability
- Two independent 1-of-4 decoders
- Multifunction capability
- Replaces 9321 and 93L21 for higher performance

TYPE	TYPICAL PROPAGATION DELAY (Enable at 2 logic levels)	TYPICAL SUPPLY CURRENT (Total)
74LS139	19ns	6.8mA
74S139	6ns	60mA

DESCRIPTION

The '139 is a high-speed, dual 1-of-4 decoder/demultiplexer. This device has two independent decoders, each accepting two binary weighted inputs (A_0, A_1) and providing four mutually exclusive active LOW outputs ($\overline{0}$-$\overline{3}$). Each decoder has an active LOW Enable ($\overline{E}$). When $\overline{E}$ is HIGH, every output is forced HIGH. The Enable can be used as the Data input for a 1-of-4 demultiplexer application.

ORDERING CODE

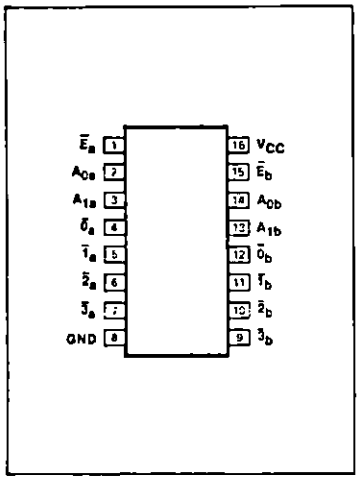
PACKAGES	COMMERCIAL RANGES V_{CC} = 5V ±5%; T_A = 0°C to +70°C	MILITARY RANGES V_{CC} = 5V ±10%; T_A = −55°C to +125°C
Plastic DIP	N74S139N • N74LS139N	
Plastic SO	N74LS139D • N74S139D	
Ceramic DIP		S54S139F • S54LS139F
Flatpack		S54S139W • S54LS139W
LLCC		S54LS139G

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

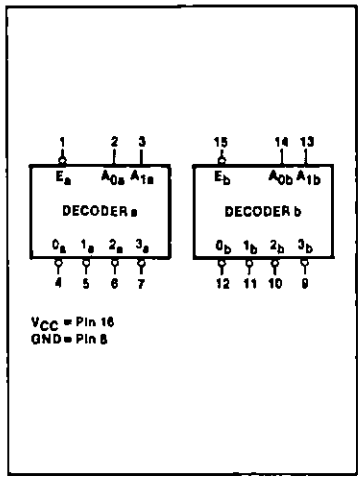
PINS	DESCRIPTION	54/74S	54/74LS
All	Inputs	1Sul	1LSul
All	Outputs	10Sul	10LSul

NOTE
A 54/74S unit load (Sul) is 50μA I_{IH} and −2.0mA I_{IL}, and a 54/74LS unit load (LSul) is 20μA I_{IH} and −0.4mA I_{IL}.

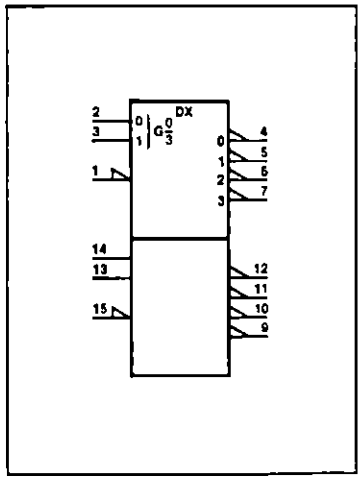
PIN CONFIGURATION



LOGIC SYMBOL



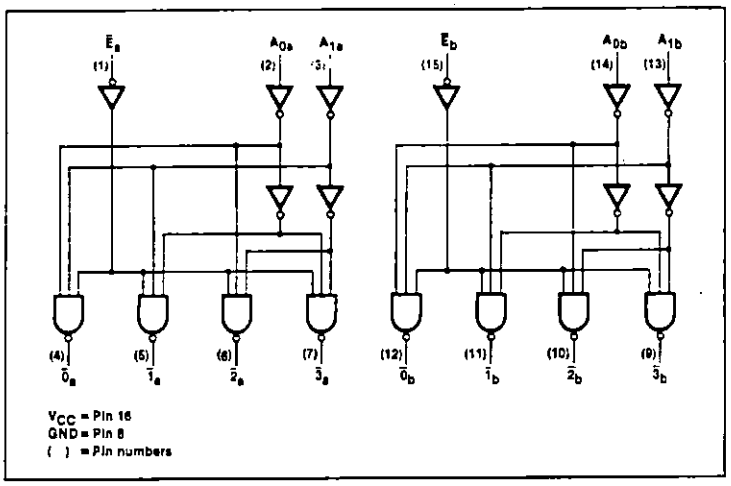
LOGIC SYMBOL (IEEE/IEC)



LOGIC PRODUCTS

DECODERS/DEMULTIPLEXERS — 54/74LS139, S139

LOGIC DIAGRAM



FUNCTION TABLE

INPUTS			OUTPUTS			
$\overline{E}$	A_0	A_1	$\overline{0}$	$\overline{1}$	$\overline{2}$	$\overline{3}$
H	X	X	H	H	H	H
L	L	L	L	H	H	H
L	H	L	H	L	H	H
L	L	H	H	H	L	H
L	H	H	H	H	H	L

H = HIGH voltage level
L = LOW voltage level

ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER		54LS	54S	74LS	74S	UNIT
V_{CC}	Supply voltage	7.0	7.0	7.0	7.0	V
V_{IN}	Input voltage	−0.5 to +7.0	−0.5 to +5.5	−0.5 to +7.0	−0.5 to +5.5	V
I_{IN}	Input current	−30 to +1	−30 to +5	−30 to +1	−30 to +5	mA
V_{OUT}	Voltage applied to output in HIGH output state	−0.5 to +V_{CC}	−0.5 to +V_{CC}	−0.5 to +V_{CC}	−0.5 to +V_{CC}	V
T_A	Operating free-air temperature range	−55 to +125		0 to 70		°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER			54/74LS			54/74S			UNIT
			Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply voltage	Mil	4.5	5.0	5.5	4.5	5.0	5.5	V
		Com'l	4.75	5.0	5.25	4.75	5.0	5.25	V
V_{IH}	HIGH-level input voltage		2.0			2.0			V
V_{IL}	LOW-level input voltage	Mil			+0.7			+0.8	V
		Com'l			+0.8			+0.8	V
I_{IK}	Input clamp current				−18			−18	mA
I_{OH}	HIGH-level output current				−400			−1000	μA
I_{OL}	LOW-level output current	Mil			4			20	mA
		Com'l			8			20	mA
T_A	Operating free-air temperature	Mil	−55		+125	−55		+125	°C
		Com'l	0		70	0		70	°C

NOTE
V_{IL} = +0.7V MAX for 54S at T_A = +125°C only

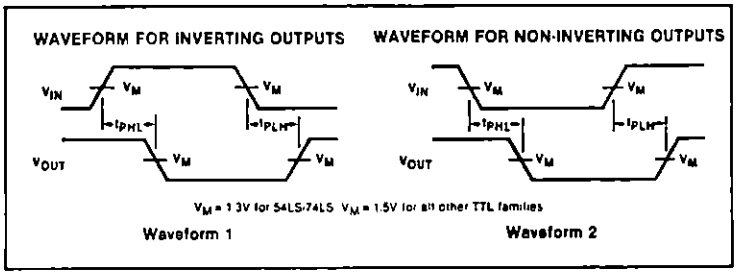
DECODERS/DEMULTIPLEXERS 54/74LS139, S139

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER		TEST CONDITIONS[1]			54/74LS139			54/74S139			UNIT
					Min	Typ[2]	Max	Min	Typ[2]	Max	
V_{OH}	HIGH-level output voltage	V_{CC} = MIN, V_{IH} = MIN, V_{IL} = MAX, I_{OH} = MAX		Mil	2.5	3.4		2.5	3.4		V
				Com'l	2.7	3.4		2.7	3.4		V
V_{OL}	LOW-level output voltage	V_{CC} = MIN, V_{IH} = MIN, V_{IL} = MAX	I_{OL} = MAX	Mil		0.25	0.4			0.5[5]	V
				Com'l		0.35	0.5			0.5	V
			I_{OL} = 4mA	74LS		0.25	0.4				V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = I_{IK}					− 1.5			− 1.2	V
I_I	Input current at maximum input voltage	V_{CC} = MAX	V_I = 5.5V							1.0	mA
			V_I = 7.0V				0.1				mA
I_{IH}	HIGH-level input current	V_{CC} = MAX, V_I = 2.7V					20			50	μA
I_{IL}	LOW-level input current	V_{CC} = MAX	V_I = 0.4V				− 0.4				mA
			V_I = 0.5V							− 2	mA
I_{OS}	Short-circuit output current[3]	V_{CC} = MAX			− 15		− 100	− 40		− 100	mA
I_{CC}	Supply current[4] (total)	V_{CC} = MAX				6.8	11		60	90	mA

NOTES
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. I_{OS} is tested with V_{OUT} = +0.5V and V_{CC} = V_{CC} MAX + 0.5V. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
4. To measure I_{CC}, outputs must be enabled and open.
5. V_{OL} = +0.45V MAX for 54S at T_A = +125°C only.

AC WAVEFORMS



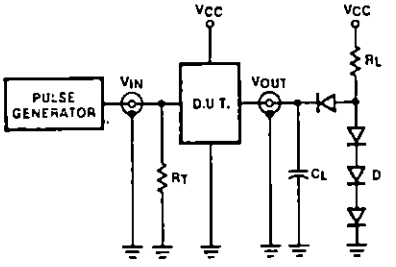
AC CHARACTERISTICS T_A = 25°C, V_{CC} = 5.0V

PARAMETER		TEST CONDITIONS	54/74LS		54/74S		UNIT
			C_L = 15pF, R_L = 2kΩ		C_L = 15pF, R_L = 280Ω		
			Min	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay Address to output	Waveform 2 2 logic levels		20 33		7.5 10	ns
t_{PLH} t_{PHL}	Propagation delay Address to output	Waveform 1 3 logic levels		29 38		12 12	ns
t_{PLH} t_{PHL}	Propagation delay Enable to output	Waveform 2 2 logic levels		24 32		8 10	ns

DECODERS/DEMULTIPLEXERS 54/74LS139, S139

TEST CIRCUITS AND WAVEFORMS

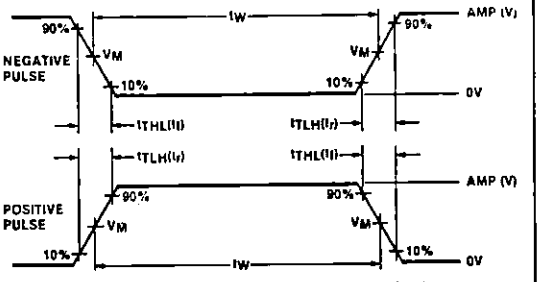
TEST CIRCUIT FOR 54/74 TOTEM-POLE OUTPUTS



DEFINITIONS

R_L = Load re... V_{CC}, see AC ... RACTERISTICS for value.
C_L = Load ca... ce includes jig ... robe capacitance, see AC CHARACTERISTICS for value.
R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.
D = Diodes are 1N916, 1N3064, or equivalent.
t_{TLH}, t_{THL} values should be less than or equal to the table entries.

INPUT PULSE DEFINITIONS



V_M = 1.3V for 54LS/74LS. V_M = 1.5V for all ... TL families

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
54/74	3.0V	1MHz	500ns	7ns	7ns
54LS/74LS	3.0V	1MHz	500ns	15ns	6ns
54S/74S	3.0V	1MHz	500ns	2.5ns	2.5ns

LOGIC PRODUCTS

DECODER/DEMULTIPLEXERS

54/74154, LS154

1-of-16 Decoder/Demultiplexer

- **16-line demultiplexing capability**
- **Mutually exclusive outputs**
- **2-input enable gate for strobing or expansion**

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (Total)
74154	21ns	34mA
74LS154	15ns	9mA

DESCRIPTION

The '154 decoder accepts four active HIGH binary address inputs and provides 16 mutually exclusive active LOW outputs. The 2-input enable gate can be used to strobe the decoder to eliminate the normal decoding "glitches" on the outputs, or it can be used for expansion of the decoder. The enable gate has two AND'ed inputs which must be LOW to enable the outputs.

The '154 can be used as a 1-of-16 demultiplexer by using one of the enable inputs as the multiplexed data input. When the other enable is LOW, the addressed output will follow the state of the applied data.

ORDERING CODE

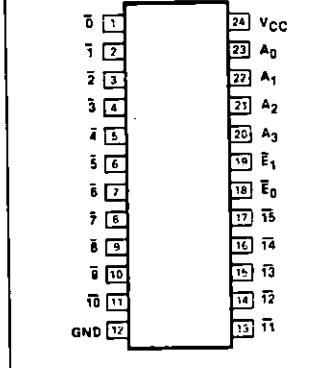
PACKAGES	COMMERCIAL RANGES V_{CC} = 5V ± 5%; T_A = 0°C to +70°C	MILITARY RANGES V_{CC} = 5V ± 10%; T_A = −55°C to +125°C
Plastic DIP	N74154N • N74LS154N	
Ceramic DIP		S54154F • S54LS154F
Flatpack		S54154W • S54LS154W

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

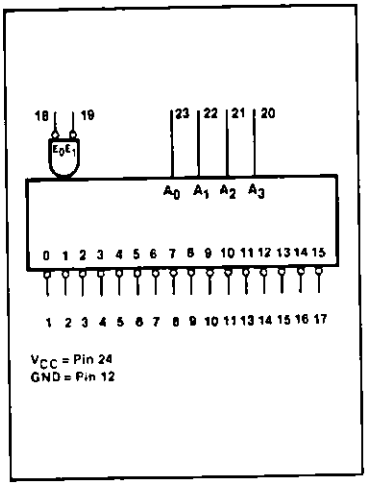
PINS	DESCRIPTION	54/74	54/74LS
All	Inputs	1ul	1LSul
All	Ouputs	10ul	10LSul

NOTE
Where a 54/74 unit load (ul) is understood to be 40μA I_{IH} and −1.6mA I_{IL}, and a 54/74LS unit load (LSul) is 20μA I_{IH} and −0.4mA I_{IL}.

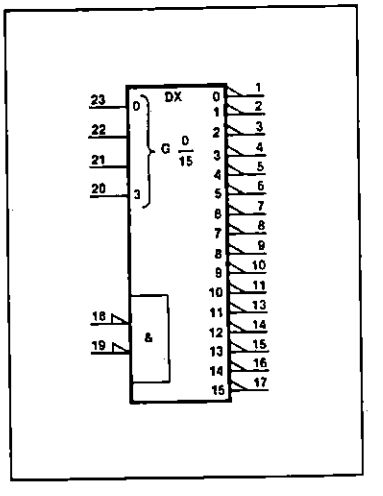
PIN CONFIGURATION



LOGIC SYMBOL



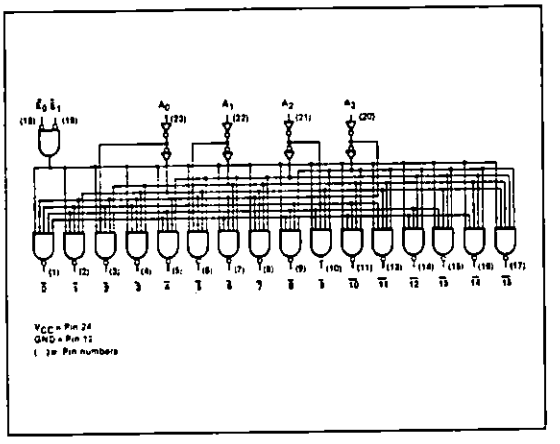
LOGIC SYMBOL (IEEE/IEC)



LOGIC PRODUCTS

DECODER/DEMULTIPLEXERS 54/74154, LS154

LOGIC DIAGRAM



FUNCTION TABLE

INPUTS						OUTPUTS														
E_0	E_1	A_3	A_2	A_1	A_0	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
L	H	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
H	L	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
H	H	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	L	L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	H	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	H	L	L	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H
L	L	L	H	L	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H
L	L	L	H	H	L	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H
L	L	L	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H
L	L	H	L	L	L	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H
L	L	H	L	L	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H
L	L	H	L	H	L	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H
L	L	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H
L	L	H	H	L	L	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H
L	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H
L	L	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H
L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L

H = HIGH voltage level.
L = LOW voltage level
X = Don't care

ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER		54	54LS	74	74LS	UNIT
V_{CC}	Supply voltage	7.0	7.0	7.0	7.0	V
V_{IN}	Input voltage	−0.5 to +5.5	−0.5 to +7.0	−0.5 to +5.5	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +5	−30 to +1	−30 to +5	−30 to +1	mA
V_{OUT}	Voltage applied to output in HIGH output state	−0.5 to +V_{CC}	−0.5 to +V_{CC}	−0.5 to +V_{CC}	−0.5 to +V_{CC}	V
T_A	Operating free-air temperature range	−55 to +125		0 to 70		°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER			54/74			54/74LS			UNIT
			Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply voltage	Mil	4.5	5.0	5.5	4.5	5.0	5.5	V
		Com'l	4.75	5.0	5.25	4.75	5.0	5.25	V
V_{IH}	HIGH-level input voltage		2.0			2.0			V
V_{IL}	LOW-level input voltage	Mil			+0.8			+0.7	V
		Com'l			+0.8			+0.8	V
I_{IK}	Input clamp current				−12			−18	mA
I_{OH}	HIGH-level output current				−800			−400	μA
I_{OL}	LOW-level output current	Mil			16			4	mA
		Com'l			16			8	mA
T_A	Operating free-air temperature	Mil	−55		+125	−55		+125	°C
		Com'l	0		70	0		70	°C

LOGIC PRODUCTS

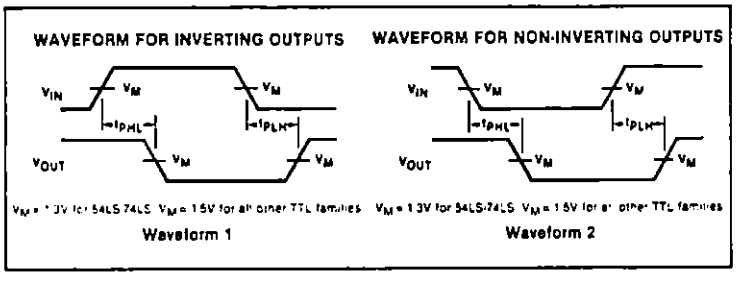
DECODER/DEMULTIPLEXERS 54/74154, LS154

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free air temperature range unless otherwise noted.)

PARAMETER		TEST CONDITIONS[1]			54/74154			54/74LS154			UNIT
					Min	Typ[2]	Max	Min	Typ[2]	Max	
V_{OH}	HIGH-level output voltage	V_{CC} = MIN, V_{IH} = MIN, V_{IL} = MAX, I_{OH} = MAX		Mil	2.4	3.4		2.5	3.4		V
				Com'l	2.4	3.4		2.7	3.4		V
V_{OL}	LOW-level output voltage	V_{CC} = MIN, V_{IH} = MIN, V_{IL} = MAX	I_{OL} = MAX	Mil		0.2	0.4		0.25	0.4	V
				Com'l		0.2	0.4		0.35	0.5	V
			I_{OL} = 4mA	74LS					0.25	0.4	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = I_{IK}					– 1.5			– 1.5	V
I_I	Input current at maximum input voltage	V_{CC} = MAX	V_I = 5.5V				1.0				mA
			V_I = 7.0V							0.1	mA
I_{IH}	HIGH-level input current	V_{CC} = MAX	V_I = 2.4V				40				μA
			V_I = 2.7V							20	μA
I_{IL}	LOW-level input current	V_{CC} = MAX, V_I = 0.4V					– 1.6			– 0.4	mA
I_{OS}	Short-circuit output current[3]	V_{CC} = MAX		Mil	– 20		– 55	– 15		– 100	mA
				Com'l	– 18		– 57	– 15		– 100	mA
I_{CC}	Supply current[4] (total)	V_{CC} = MAX		Mil		34	49		9	14	mA
				Com'l		34	56		9	14	mA

NOTES
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. I_{OS} is tested with V_{OUT} = + 0.5V and V_{CC} = V_{CC} MAX + 0.5V. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
4. Measure I_{CC} with all inputs grounded and all outputs open.

AC WAVEFORMS



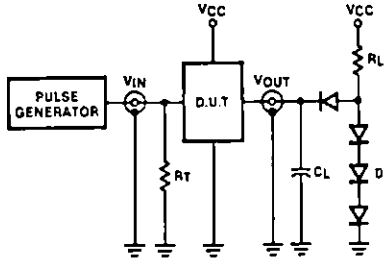
AC CHARACTERISTICS T_A = 25°C, V_{CC} = 5.0V

PARAMETER		TEST CONDITIONS	54/74		54/74LS		UNIT
			C_L = 15pF, R_L = 400Ω		C_L = 15pF, R_L = 2kΩ		
			Min	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay Address to output	Waveform 1		36 33		36 33	ns
t_{PLH} t_{PHL}	Propagation delay Enable to output	Waveform 2		30 27		30 27	ns

DECODER/DEMULTIPLEXERS 54/74154, LS154

TEST CIRCUITS AND WAVEFORMS

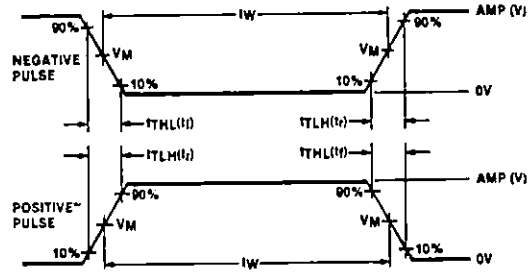
TEST CIRCUIT FOR 54/74 TOTEM-POLE OUTPUTS



DEFINITIONS

R_L = Load resistor to V_{CC}; see AC CHARACTERISTICS for value.
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.
D = Diodes are 1N916, 1N3064, or equivalent.
^tTLH, ^tTHL Values should be less than or equal to the table entries.

INPUT PULSE DEFINITIONS



V_M = 1.3V for 54LS/74LS; V_M = 1.5V for all other TTL families

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	^tTLH	^tTHL
54/74	3.0V	1MHz	500ns	7ns	7ns
54LS/74LS	3.0V	1MHz	500ns	15ns	6ns
54S/74S	3.0V	1MHz	500ns	2.5ns	2.5ns

LOGIC PRODUCTS

GATES

54/7420, 54/7421, LS20, LS21, S20

Dual Four-Input NAND ('20), AND ('21) Gate

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (Total)
7420	10ns	8mA
74LS20	10ns	0.8mA
74S20	3ns	8mA
7421	12ns	8mA
74LS21	9ns	1.7mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGES V_{CC} = 5V ± 5%; T_A = 0°C to + 70°C	MILITARY RANGES V_{CC} = 5V ± 10%; T_A = − 55°C to + 125°C
Plastic DIP '20	N7420N • N74LS20N N74S20N	
'21	N7421N • N74LS21N	
Plastic SO	N74LS20D • N74S20D N74LS21D	
Ceramic DIP '20		S5420F • S54LS20F S54S20F
Flatpack '20		S5420W • S54LS20W S54S20W
LLCC		S54LS20G

FUNCTION TABLE

INPUTS				OUTPUTS	
A	B	C	D	Y('20)	Y('21)
L	X	X	X	H	L
X	L	X	X	H	L
X	X	L	X	H	L
X	X	X	L	H	L
H	H	H	H	L	H

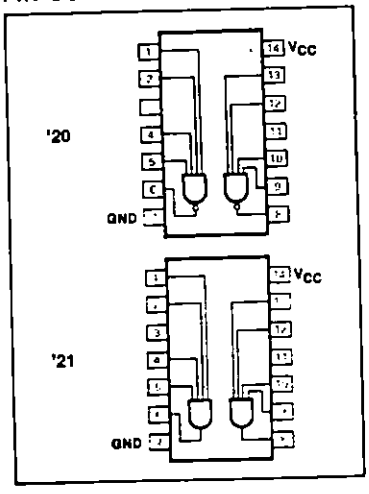
H = HIGH voltage level
L = LOW voltage level
X = Don't care

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

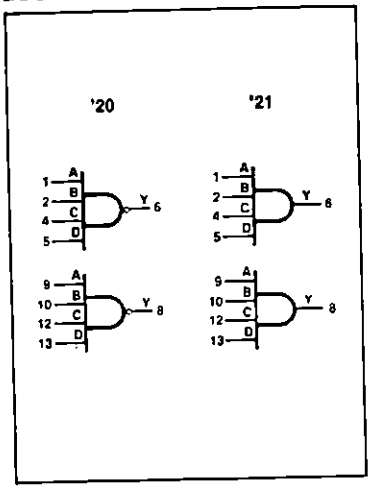
PINS	DESCRIPTION	54/74	54/74S	54/74LS
A-D	Inputs	1ul	1Sul	1LSul
Y	Output	10ul	10Sul	10LSul

NOTE
Where a 54/74 unit load (ul) is understood to be 40μA I_{IH} and − 1.6mA I_{IL}, a 54/74S unit load (Sul) is 50μA I_{IH} and − 2.0mA I_{IL} and 54/74LS unit load (LSul) is 20μA I_{IH} and − 0.4mA I_{IL}.

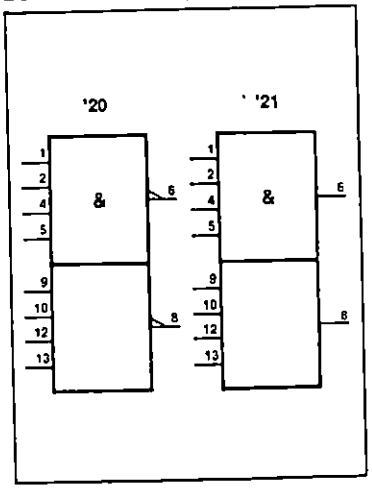
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



LOGIC PRODUCTS

GATES — 54/7420, 54/7421, LS20, LS21, S20

ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER		54	54LS	54S	74	74LS	74S	UNIT
V_{CC}	Supply voltage	7.0	7.0	7.0	7.0	7.0	7.0	V
V_{IN}	Input voltage	−0.5 to +5.5	−0.5 to +7.0	−0.5 to +5.5	−0.5 to +5.5	−0.5 to +7.0	−0.5 to +5.5	V
I_{IN}	Input current	−30 to +5	−30 to +1	−30 to +5	−30 to +5	−30 to +1	−30 to +5	mA
V_{OUT}	Voltage applied to output in HIGH output state	−0.5 to +V_{CC}	−0.5 to +V_{CC}	−0.5 to +V_{CC}	−0.5 to +V_{CC}	−0.5 to +V_{CC}	−0.5 to +V_{CC}	V
T_A	Operating free-air temperature range	−55 to +125			0 to 70			°C

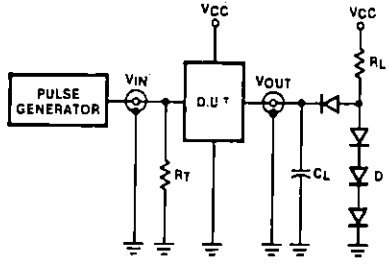
RECOMMENDED OPERATING CONDITIONS

PARAMETER			54/74			54/74LS			54/74S			UNIT
			Min	Nom	Max	Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply voltage	Mil	4.5	5.0	5.5	4.5	5.0	5.5	4.5	5.0	5.5	V
		Com'l	4.75	5.0	5.25	4.75	5.0	5.25	4.75	5.0	5.25	V
V_{IH}	HIGH-level input voltage		2.0			2.0			2.0			V
V_{IL}	LOW-level input voltage	Mil			+0.8			+0.7			+0.8	V
		Com'l			+0.8			+0.8			+0.8	V
I_{IK}	Input clamp current				−12			−18			−18	mA
I_{OH}	HIGH-level output current	'20			−400			−400			−1000	µA
		'21			−800			−400			−1000	µA
I_{OL}	LOW-level output current	Mil			16			4			20	mA
		Com'l			16			8			20	mA
T_A	Operating free-air temperature	Mil	−55		+125	−55		+125	−55		+125	°C
		Com'l	0		70	0		70	0		70	°C

NOTE
V_{IL} = +0.7V MAX for 54S at T_A = +125°C only.

TEST CIRCUITS AND WAVEFORMS

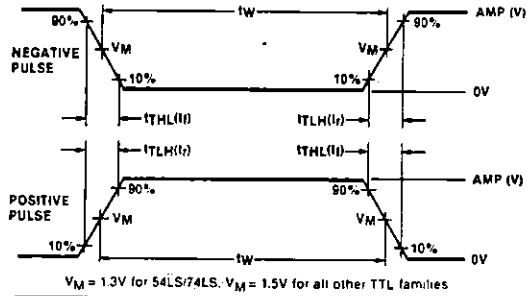
TEST CIRCUIT FOR 54/74 TOTEM-POLE OUTPUTS



DEFINITIONS

R_L = Load resistor to V_{CC}; see AC CHARACTERISTICS for value
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value
R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators
D = Diodes are 1N916, 1N3064, or equivalent
t_{TLH}, t_{THL} Values should be less than or equal to the table entries

INPUT PULSE DEFINITIONS



V_M = 1.3V for 54LS/74LS; V_M = 1.5V for all other TTL families

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
54/74	3.0V	1MHz	500ns	7ns	7ns
54LS/74LS	3.0V	1MHz	500ns	15ns	6ns
54S/74S	3.0V	1MHz	500ns	2.5ns	2.5ns

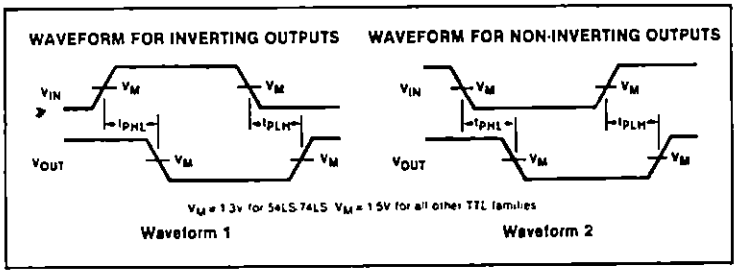
GATES — 54/7420, 54/7421, LS20, LS21, S20

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER	TEST CONDITIONS[1]			54/7420, 21			54/74LS20, 21			54/74S20			UNIT
				Min	Typ[2]	Max	Min	Typ[2]	Max	Min	Typ[2]	Max	
V_{OH} HIGH-level output voltage	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN, I_{OH} = MAX		Mil	2.4	3.4		2.5	3.4		2.5	3.4		V
			Com'l	2.4	3.4		2.7	3.4		2.7	3.4		V
V_{OL} LOW-level output voltage	V_{CC} = MIN, V_{IH} = MIN, V_{IL} = MAX	I_{OL} = MAX	Mil		0.2	0.4		0.25	0.4			0.5[4]	V
			Com'l		0.2	0.4		0.35	0.5			0.5	V
		I_{OL} = 4mA	74LS					0.25	0.4				V
V_{IK} Input clamp voltage	V_{CC} = MIN, I_I = I_{IK}					– 1.5			– 1.5			– 1.2	V
I_I Input current at maximum input voltage	V_{CC} = MAX	V_I = 5.5V				1.0						1.0	mA
		V_I = 7.0V							0.1				mA
I_{IH} HIGH-level input current	V_{CC} = MAX	V_I = 2.4V				40							μA
		V_I = 2.7V							20			50	μA
I_{IL} LOW-level input current	V_{CC} = MAX	V_I = 0.4V				– 1.6			– 0.4				mA
		V_I = 0.5V										– 2.0	mA
I_{OS} Short-circuit output current[3]	V_{CC} = MAX		Mil	– 20		– 55	– 20		– 100	– 40		– 100	mA
			Com'l	– 18		– 55	– 20		– 100	– 40		– 100	mA
I_{CC} Supply current (total)	V_{CC} = MAX	I_{CCH} Outputs HIGH	'20		2	4		0.4	0.8		5	8	mA
		I_{CCL} Outputs LOW	'20		6	11		1.2	2.2		10	18	mA
		I_{CCH} Outputs HIGH	'21		6	8		1.2	2.4				mA
		I_{CCL} Outputs LOW	'21		11	13		2.2	4.4				mA

NOTES
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. I_{OS} is tested with V_{OUT} = + 0.5V and V_{CC} = V_{CC} MAX + 0.5V. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
4. V_{OL} = + 0.45V MAX for 54S at T_A = + 125°C only.

AC WAVEFORMS



AC CHARACTERISTICS T_A = 25°C, V_{CC} = 5.0V

PARAMETER	TEST CONDITIONS	54/74		54/74LS		54/74S		UNIT
		C_L = 15pF, R_L = 400Ω		C_L = 15pF, R_L = 2kΩ		C_L = 15pF, R_L = 280Ω		
		Min	Max	Min	Max	Min	Max	
t_{PLH} / t_{PHL} Propagation delay	Waveform 1, '20		22 15		15 15		4.5 5.0	ns
t_{PLH} / t_{PHL} Propagation delay	Waveform 2, '21		27 19		15 20			ns

TTL USER'S GUIDE

INTRODUCTION

The TTL Logic devices described in this data manual differ widely in function, complexity and performance, but their electrical input and output characteristics are very similar and are defined and tested to guarantee compatibility. The data sheets that make up this book cover four major categories of TTL circuits and a series of TTL compatible interface products.

The oldest TTL product category is the gold-doped double-diffused type which is made up of the 54/7400 family of devices. This family reflects the same performance ranges and differ only in functions and pin configuration.

The remaining two categories of products are fabricated with a non-saturating Schottky clamped transistor technique. The 54S/74S00 family of TTL products are very high performance high power devices. The most popular TTL category is the 54LS/74LS Low Power Schottky family. These products feature the performance of the 54/74 family at about 1/4 the power.

ABSOLUTE MAXIMUM RATINGS

The absolute maximum ratings constitute limiting values above which serviceability of the device may be impaired. Provisions should be made in system design and testing to limit voltages and currents as shown below.

OPERATING TEMPERATURE AND VOLTAGE RANGES

The nominal supply voltage (V_{CC}) for all TTL circuits is +5.0 volts. Commercial grade parts are guaranteed to perform with a ±5% supply tolerance (±250mV) over an ambient temperature range of 0°C to 70°C.

The Military grade parts are guaranteed to perform with a ±10% supply tolerance (±500mV) over an ambient temperature range of −55°C to +125°C.

The actual junction temperature can be calculated by multiplying the power dissipation of the device with the thermal resistance of the package and adding it to the measured ambient temperature T_A or package (case) temperature T_C. The thermal resistance for the various packages in which the TTL products are offered is specified with the Package Information in Section 7 of this manual.

GENERAL TTL CIRCUIT CHARACTERISTICS

All TTL products are derived from a common NAND logic structure. The NAND circuit is actually five subcircuits as shown in Figure 1 and each performs a separate function. The input circuit (1) is an AND gate usually fabricated with a multi-emitter transistor which characterizes TTL technology. Many Schottky processed circuits have been designed with PNP or diode inputs in order to optimize the speed/power performance of the circuits.

NAND Gate Example

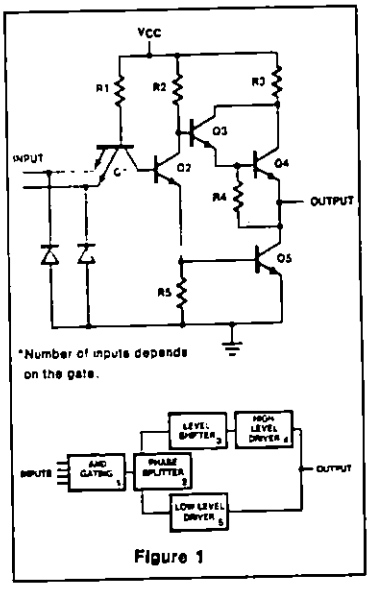


Figure 1

The phase splitter (2) provides the inversion and amplification in the circuit. It determines whether the outputs are active level HIGH or active level LOW. The level shifter (3) provides noise immunity between the HIGH and LOW output levels, and minimizes the possibility of having both HIGH level driver (4) and LOW level driver (5) on simultaneously.

ABSOLUTE MAXIMUM RATINGS

PARAMETER	54/74	54S/74S	54LS/74LS
V_{CC} supply voltage, continuous (Note a)	7.0V	7.0V	7.0V
Input voltage, continuous (Notes a and b)	−0.5V to +5.5V	−0.5V to +5.5V	−0.5V to +7.0V[b]
Input current, continuous	−30mA to +5mA	−30mA to +5mA	−30mA to +1mA
Voltage applied to HIGH outputs (Note a)	−0.5V to V_{CC}	−0.5V to 7.0V	−0.5V to V_{CC}
Voltage applied to "off" Open Collector outputs (Notes a and c)	−0.5V to 7.0V	−0.5V to 7.0V	−0.5V to 7.0V
Current into LOW standard output, continuous	30mA	40mA	15mA
Current into LOW buffer output, continuous	80mA	100mA	50mA
Operating free air temperature range (Mil)	−55°C to +125°C		
Operating free air temperature range (Com'l)	0°C to +70°C		
Storage temperature range	−65°C to +150°C		

NOTES

a. Voltages are referenced to device ground terminal

b. LS devices are generally limited to 7.0V minimum input voltage. Exceptions are called out on individual product data sheets

c. Some open collector devices are specially processed to handle higher output voltages of from 15V to 30V. The Absolute Maximum voltage for these devices is 10% over the specified V_{OUT} test condition.

TTL INPUT CONFIGURATIONS

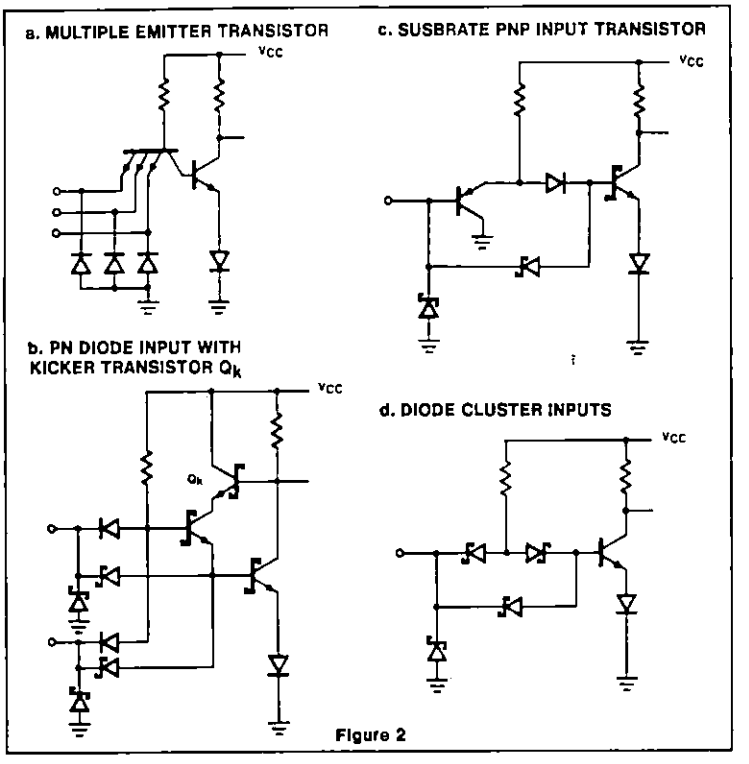


Figure 2

The level shifter (3) and HIGH level driver (4) combine to form an emitter follower circuit that tracks the voltage at the collector of the phase splitter. This circuit is usually designed to drive very heavy capacitive loads so that the initial rise time of the output is determined primarily by the rise time at the phase splitter collector. The LOW level driver (5) is usually a saturating transistor for the gold doped process devices, or a Schottky diode clamped transistor for the Schottky processed devices. These output transistors are designed to sink the rated fan-out current which characterizes the various TTL families.

Input Circuits

The input circuits as described above are basically AND gate configurations designed with multiple-emitter NPN transistors (MET), substrate PNP transistors, or various junction and Schottky diodes as shown in Figure 2. All of the circuit configurations have very high impedance in the HIGH state. When the input voltage is above the circuit threshold voltage, all of the inputs act like reversed biased diodes. The MET transistors are actually operated in the inverse mode, but the gain is so low there is very little current flowing into the devices.

The LOW level input impedance of the MET and diode inputs is determined by the internal pull-up resistor. This resistor is nominally 2KΩ for 54S/74S inputs, and it is 16KΩ to 20KΩ for the 54LS/74LS inputs. Some 54LS/74LS buffer devices have substrate PNP inputs which exhibit very high impedance at both HIGH and LOW input logic levels. This is used to minimize the input load factor and produce better output drive and performance.

The inputs to all Signetics TTL devices have clamp diodes to ground to minimize negative ringing effects. These diodes are designed to operate in the ac mode and cannot handle heavy dc currents for long periods.

Output Circuits

The output circuit configurations used for the TTL products in this manual are shown in Figure 3. The basic advantages and disadvantages of each configuration are given for reference. The different circuits are used to optimize the functional and performance requirements of the various devices, and are not necessarily restricted to individual TTL families. The pull-down circuit (not shown) on the base of the LOW level driver is usually a resistor which provides a means of turning off the output transistor. The majority of the 54S/74S and 54LS/74LS devices use a resistor-transistor network which acts to square-up the V_{IN}-V_{OUT} transfer characteristics of the device.

A resistive pull-up can be added to any TTL output circuit increasing V_{OH} to almost V_{CC}, but only circuits "c," "d," and "e" can be pulled higher than V_{CC}, e.g., to +7.0V for driving MOS circuits. Configurations "a" and "b" have a diode associated with the resistor at the output which clamps the output one diode drop above V_{CC}. This is an important consideration in large systems where sections might be powered down (V_{CC} = 0). In this state, the outputs of circuits "a" and "b" represent a very low impedance at a fairly low voltage (<1.0V), while the outputs of circuits "c," "d," and "e" represent a high impedance and thus a logic HIGH, more appropriate for isolation from the rest of the system.

The output impedance of a typical TTL device in both the LOW and HIGH state is shown in Figure 4. In the LOW state, the output impedance is determined by a saturated transistor (about 8Ω to 10Ω). However, at very high sinking current, especially at low temperature, the output device is not able to stay in saturation and the output impedance rises as shown.

When switching from the LOW to the HIGH state, the totem-pole output structure provides a low output impedance capable of rapidly charging capacitive loads. However, charge and discharge currents must also flow through the V_{CC} and the ground distribution networks. The V_{CC} and ground lines should therefore be short and adequately decoupled.

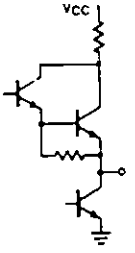
3-State Outputs

Some of the buffers and registers have 3-state outputs designed for "busing." This type of output electrically performs as a totem-pole output with the additional feature that the output may be disabled, neither sinking nor sourcing current. The 3-state outputs are designed to be tied together, but they are not designed to be active simultaneously. In order to minimize noise and protect the outputs from

TTL USER'S GUIDE

TTL OUTPUT CONFIGURATIONS

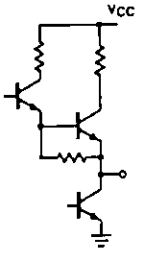
a. DARLINGTON



ADVANTAGE:
High ac drive capability
$V_{OH} = V_{CC} - V_{BE}$ at $I_O = 0$
Small size (transistors share one common isolation)

DISADVANTAGE:
Output cannot be pulled higher than one diode drop above V_{CC}

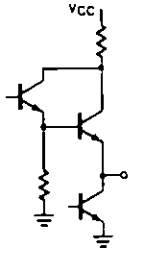
b. 2-STAGE EMITTER FOLLOWER ("DARLINGTON SPLIT")



ADVANTAGE:
High ac drive capability
$V_{OH} = V_{CC} - V_{BE}$ at $I_O = 0$

DISADVANTAGE:
Larger than circuit A
Output cannot be pulled higher than one diode drop above V_{CC}

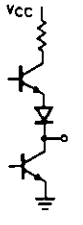
c. DARLINGTON WITH RESISTOR TO GROUND



ADVANTAGE
High ac drive capability
Lower $V_{OH} = (V_{CC} - 2\ V_{BE})$ increases speed
Outputs can be pulled higher than V_{CC}

DISADVANTAGE
Higher dissipation
Lower noise immunity in the HIGH state

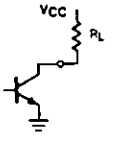
d. TRANSISTOR—DIODE



ADVANTAGE:
Lowest power consumption
Small size
Outputs can be pulled higher than VCC

DISADVANTAGE
Less ac drive capability

e. OPEN COLLECTOR



ADVANTAGE:
Bussable, allows collector ANDing (Wired-OR)

DISADVANTAGE:
High output impedance in the HIGH state
Slow, especially with capacitive loading
Requires additional resistor

Figure 3

TYPICAL INPUT/OUTPUT CHARACTERISTICS

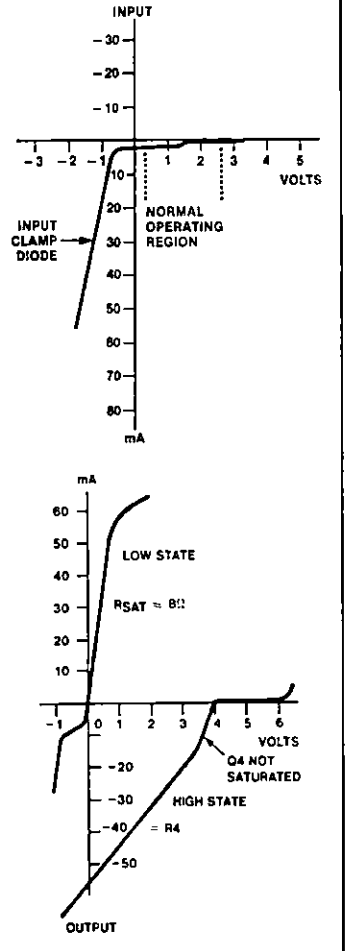


FIGURE 4

excessive power dissipation, only one 3-state output should be active at any time.

DESIGN CONSIDERATIONS

The properties of high speed TTL logic circuits dictate that some care be used in the design and layout of a system. Some general "design considerations" are included in this section. This is not intended to be a thorough guideline for designing TTL systems, but a reference for some of the constraints and techniques to be considered when designing the system.

Mixing 54'74 and 54LS'74LS is less restrictive, and the overall system design need not be so elaborate. Standard two sided PC boards can be used with good well decoupled power and ground grid systems. The signal transitions are slower and therefore generate less noise. However, good high speed design techniques are still required, especially when working with counters, registers, or other devices with memory.

Clock Pulse Requirements

Most TTL flip-flop circuits are master-slave devices which makes their clock inputs level sensitive. This is an improvement over ac coupled clock inputs, but it does not make the devices fully insensitive to clock edge rates. The dc level at which the data in the master (input section) is transferred to the slave (output section) is the normal threshold voltage for the devices. For most Signetics TTL devices this level is 1.4V at 25°C, and it changes at a rate of about −4mV/°C.

When the clock input reaches the threshold voltage, the internal gates and the changing outputs start to dump current into the ground lead of the device. If there are enough internal gates or loaded outputs changing at the same time, the chip ground reference level (and therefore the clock input reference level) can rise by as much as 500mV. This ground noise is the algebraic sum of the internal and external ground plane noise. If the clock input of a positive edge triggered device is at or near the threshold of the device during the ground noise transient period, it is quite possible for the internal device to receive multiple clock pulses.

For this reason the rise time on positive edge-triggered devices should be less than the nominal clock to output delay time measured between the 0.8V and 2.0V levels of the clock driver. This edge rate is obtainable from almost any Signetics TTL device of the same family, as long as it is driving no more than rated fan out and no more than 12 to 16 inches of line. When clock pulses are distributed on lines over 16 inches long, all of the clock inputs should be clustered at the receiving end of the line to avoid reflection problems at the driving end.

Special Note

Some of the Signetics Counters and registers have been designed with a special clock buffer that includes a small amount of hysteresis to minimize clock edge rate and noise problems. The LS160A, LS161A, LS162A, LS163A, LS364, and LS374 all have the special clock buffers to increase their tolerance of slow positive clock edges and heavy ground noise.

TTL OUTPUTS TIED TOGETHER

The only TTL outputs that are designed to be tied together are open collector and 3-state outputs. Standard TTL outputs should not be tied together unless their logic levels will always be the same; either all HIGH or all LOW. When connecting open collector or 3-state outputs together some general guidelines must be observed:

Open Collector

These devices must be used whenever two or more OR-tied outputs will be at opposite logic levels at the same time. These devices must have a pull-up resistor (or resistors) added between the OR-tie connector and V_{CC} to establish an active HIGH level. Only special high voltage buffers can be tied to a higher voltage than V_{CC}. The minimum and maximum size of the pull-up resistor is determined as follows:

$$R(Min) = \frac{V_{CC}(Max) - V_{OL}}{I_{OL} - N_2(I_{IL})}$$

$$R(Max) = \frac{V_{CC}(Min) - V_{OH}}{N_1(I_{OH}) + N_2(I_{IH})}$$

where: I_{OL} = Minimum I_{OL} guarantee or OR-tied elements.

$N_2(I_{IL})$ = Cumulative maximum input LOW current for all inputs tied to OR-tie connection.

$N_1(I_{OH})$ = Cumulative maximum output HIGH leakage current for all outputs tied to OR-tie connection.

$N_2(I_{IH})$ = Cumulative maximum input HIGH leakage current for all inputs tied to OR-tie connection.

If a resistor divider network is used to provide the HIGH level, the R(Max) must be decreased enough to provide the required (V_{OH}/R(pull-down)) current.

Minimum propagation delay results when the minimum value of external pull-up resistor is used in Load Circuit 1, Figure 5.

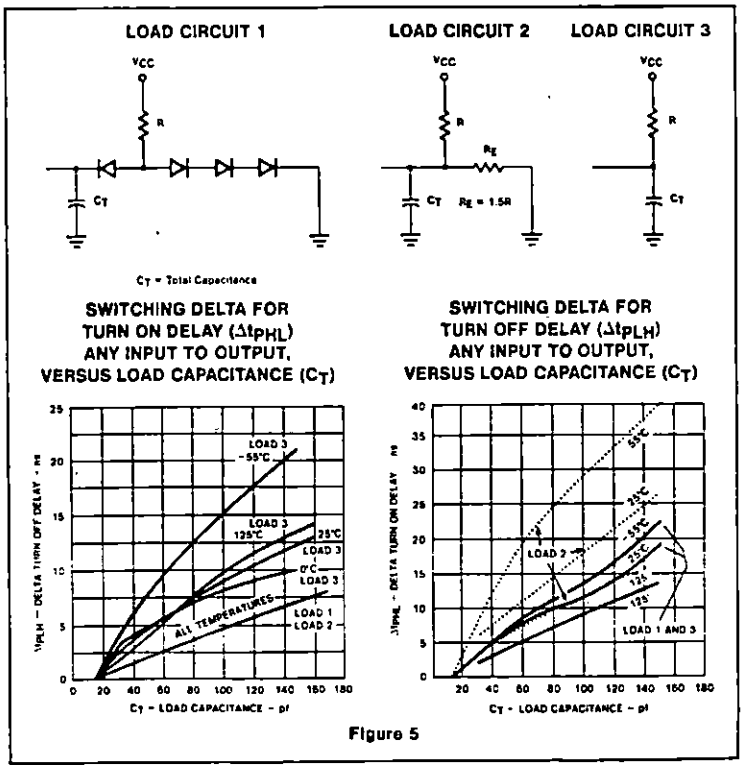


Figure 5

TTL USER'S GUIDE

Diodes should be fast recovery 1N4376 or equivalent. External pull-up resistor Load Circuits 2 and 3 give progressively slower propagation delays.

3-STATE OUTPUTS

3-State Outputs are designed to be tied together, but they are not designed to be active simultaneously. In order to minimize noise and protect the outputs from excessive power dissipation, only one 3-state output should be active at any time. This generally requires that the Output Enable signals be non-overlapping. When TTL decoders are used to enable 3-state outputs, the decoder should be disabled while the address is being changed. Since all TTL decoder outputs are subject to decoding spikes, non-overlapping signals cannot normally be guaranteed when the address is changing.

Since most 3-state Output Enable signals are active LOW, shift registers or edge-triggered storage registers provide good Output Enable buffers. Shift registers with one circulating LOW bit, like the "164" or "194" are ideal for sequential enable signals. The "174" or '273" can be used to buffer enable signals from TTL decoders or microcode (ROM) devices. Since the outputs of these registers will change from LOW-to-HIGH faster than from HIGH-to-LOW, the selection of one device at a time is assured.

POWER SUPPLY DECOUPLING

Power supply capacitance decoupling is required for any TTL system. Generally 0.01 μF per synchronously driven gate and at least 1 μF for each 20 gates is required regardless of synchronization. Counters and shift registers are especially susceptible to power and ground line noise. They should be decoupled with a 0.1μF capacitor for each eight internal flip-flops, or one capacitor for each two devices put as close as possible to the devices. Buffers and line drivers should be heavily decoupled at the driver power pins, due to the large current transients needed to charge and discharge the lines.

On-Board Regulation

In most digital systems, there is a large current requirement, and the current supplied usually comes from a main supply. TTL logic tends to generate current spikes during switching due to the overlap in conduction of both upper and lower transistors, thus creating V_{CC} noise. An on-board regulator would not only regulate the power supplied ot the circuits on-board, but also would isolate the noise otherwise propagated to the reset of the system. Systems designed using this technique would not need tight regulation on the main power supply.

LINE DRIVING AND RECEIVING

Open wire connections between TTL circuits should not be bundled, tied, or routed together. Instead, point-to-point wiring should be used, preferably above a ground plane which reduces coupling between conductors.

Single line wire interconnections should not exceed two feet; for wires longer than 15 inches, a ground plane is essential to provide adequate system performance. Over 2-foot twisted pairs or coaxial cable should be used. The characteristic impedance of an open wire over a ground plane is about 150Ω, while for twisted pairs of #26 wire the impedance is about 120Ω. For added protection against crosstalk, coaxial cables can be used but coaxial cables having very low characteristic impedances are difficult to drive. For best performance, coaxial cables with a characteristic impedance R_O of 100Ω should be used. Resistive pull-ups at the receiving end can be used to increase noise margins. If reflection effects are unacceptable, the line must be terminated in its characteristic impedance. One method is shown in Figure 6 where the output of the line is tied to V_{CC} through a resistor equivalent to the characteristic impedance of the line. Therefore, R_O is fairly small, and the driving gate must sink the current through it in addition to the current from the inputs being driven. Terminating the line in a voltage divider with two resistors, each twice the line impedance, reduces the extra sink current by 50%. It is preferable to dedicate gates solely for line driving if the line length is in excess of five feet.

TTL DRIVING TWISTED PAIR

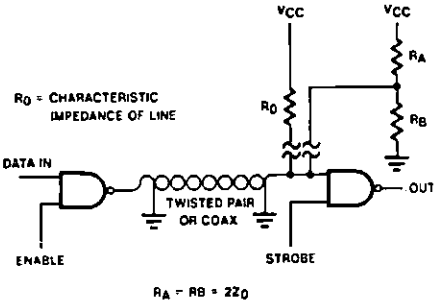


Figure 6

LOGIC PRODUCTS

GATES — 54/7400, LS00, S00

Quad Two-Input NAND Gate

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (Total)
7400	9ns	8mA
74LS00	9.5ns	1.6mA
74S00	3ns	15mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGES V_{CC} = 5V ± 5%; T_A = 0°C to +70°C	MILITARY RANGES V_{CC} = 5V ± 10%; T_A = −55°C to +125°C
Plastic DIP	N7400N • N74LS00N N74S00N	
Plastic SO	N74LS00D N74S00D	
Ceramic DIP		S5400F • S54LS00F S54S00F
Flatpack		S5400W • S54LS00W S54S00W
LLCC		S54LS00G

FUNCTION TABLE

INPUTS		OUTPUT
A	B	Y
L	L	H
L	H	H
H	L	H
H	H	L

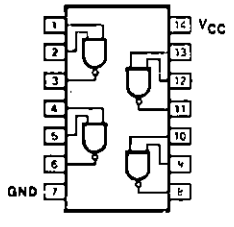
H = HIGH voltage level
L = LOW voltage level

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

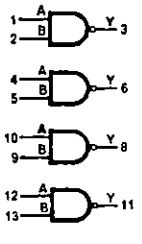
PINS	DESCRIPTION	54/74	54/74S	54/74LS
A, B	Inputs	1ul	1Sul	1LSul
Y	Output	10ul	10Sul	10LSul

NOTE
Where a 54/74 unit load (ul) is understood to be 40μA I_{IH} and −1.6mA I_{IL}, a 54/74S unit load (Sul) is 50μA I_{IH} and −2.0mA I_{IL}, and 54/74LS unit load (LSul) is 20μA I_{IH} and −0.4mA I_{IL}.

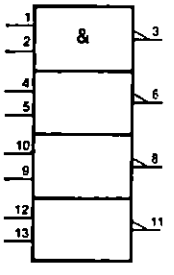
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



LOGIC PRODUCTS

GATES — 54/7400, LS00, S00

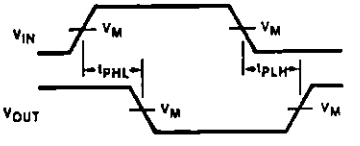
DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER	TEST CONDITIONS[1]			54/7400			54/74LS00			54/74S00			UNIT
				Min	Typ[2]	Max	Min	Typ[2]	Max	Min	Typ[2]	Max	
V_{OH} HIGH-level output voltage	V_{CC} = MIN, V_{IH} = MIN, V_{IL} = MAX, I_{OH} = MAX		Mil	2.4	3.4		2.5	3.4		2.5	3.4		V
			Com'l	2.4	3.4		2.7	3.4		2.7	3.4		V
V_{OL} LOW-level output voltage	V_{CC} = MIN, V_{IH} = MIN	I_{OL} = MAX	Mil		0.2	0.4		0.25	0.4			0.5[4]	V
			Com'l		0.2	0.4		0.35	0.5			0.5	V
		I_{OL} = 4mA	74LS					0.25	0.4				V
V_{IK} Input clamp voltage	V_{CC} = MIN, I_I = I_{IK}					– 1.5			– 1.5			– 1.2	V
I_I Input current at maximum input voltage	V_{CC} = MAX	V_I = 5.5V				1.0						1.0	mA
		V_I = 7.0V							0.1				mA
I_{IH} HIGH-level input current	V_{CC} = MAX	V_I = 2.4V				40							μA
		V_I = 2.7V							20			50	μA
I_{IL} LOW-level input current	V_{CC} = MAX	V_I = 0.4V				– 1.6			– 0.4				mA
		V_I = 0.5V										– 2.0	mA
I_{OS} Short-circuit output current[3]	V_{CC} = MAX		Mil	– 20		– 55	– 20		– 100	– 40		– 100	mA
			Com'l	– 18		– 55	– 20		– 100	– 40		– 100	mA
I_{CC} Supply current (total)	V_{CC} = MAX	I_{CCH} Outputs HIGH			4	8		0.8	1.6		10	16	mA
		I_{CCL} Outputs LOW			12	22		2.4	4.4		20	36	mA

NOTES
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. I_{OS} is tested with V_{OUT} = + 0.5V and V_{CC} = V_{CC} MAX + 0.5V. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second
4. V_{OL} = + 0.45V MAX for 54S at T_A = + 125°C only

AC WAVEFORM

WAVEFORM FOR INVERTING OUTPUTS



V_M = 1.3V for 54LS/74LS. V_M = 1.5V for all other TTL families

Waveform 1

AC CHARACTERISTICS T_A = 25°C, V_{CC} = 5.0V

PARAMETER	TEST CONDITIONS	54/74		54/74LS		54/74S		UNIT
		C_L = 15pF, R_L = 400Ω		C_L = 15pF, R_L = 2kΩ		C_L = 15pF, R_L = 280Ω		
		Min	Max	Min	Max	Min	Max	
t_{PLH} / t_{PHL} Propagation delay	Waveform 1		22 15		15 15		4.5 5.0	ns

LOGIC PRODUCTS

GATES — 54/7400, LS00, S00

ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER		54	54LS	54S	74	74LS	74S	UNIT
V_{CC}	Supply voltage	7.0	7.0	7.0	7.0	7.0	7.0	V
V_{IN}	Input voltage	−0.5 to +5.5	−0.5 to +7.0	−0.5 to +5.5	−0.5 to +5.5	−0.5 to +7.0	−0.5 to +5.5	V
I_{IN}	Input current	−30 to +5	−30 to +1	−30 to +5	−30 to +5	−30 to +1	−30 to +5	mA
V_{OUT}	Voltage applied to output in HIGH output state	−0.5 to +V_{CC}	−0.5 to +V_{CC}	−0.5 to +V_{CC}	−0.5 to +V_{CC}	−0.5 to +V_{CC}	−0.5 to +V_{CC}	V
T_A	Operating free-air temperature range	−55 to +125			0 to 70			°C

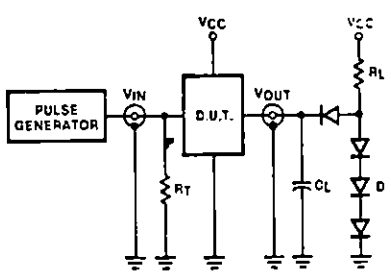
RECOMMENDED OPERATING CONDITIONS

PARAMETER			54/74			54/74LS			54/74S			UNIT
			Min	Nom	Max	Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply voltage	Mil	4.5	5.0	5.5	4.5	5.0	5.5	4.5	5.0	5.5	V
		Com'l	4.75	5.0	5.25	4.75	5.0	5.25	4.75	5.0	5.25	V
V_{IH}	HIGH-level input voltage		2.0			2.0			2.0			V
V_{IL}	LOW-level input voltage	Mil			+0.8			+0.7			+0.8	V
		Com'l			+0.8			+0.8			+0.8	V
I_{IK}	Input clamp current				−12			−18			−18	mA
I_{OH}	HIGH-level output current				−400			−400			−1000	µA
I_{OL}	LOW-level output current	Mil			16			4			20	mA
		Com'l			16			8			20	mA
T_A	Operating free-air temperature	Mil	−55		+125	−55		+125	−55		+125	°C
		Com'l	0		70	0		70	0		70	°C

NOTE
V_{IL} = +0.7V MAX for 54S at T_A = +125°C only

TEST CIRCUITS AND WAVEFORMS

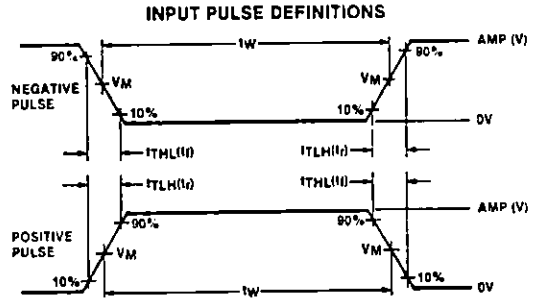
TEST CIRCUIT FOR 54/74 TOTEM-POLE OUTPUTS



DEFINITIONS

R_L = Load resistor to V_{CC}, see AC CHARACTERISTICS for value
C_L = Load capacitance includes jig and probe capacitance, see AC CHARACTERISTICS for value
R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators
D = Diodes are 1N916, 1N3064 or equivalent
t_{TLH}, t_{THL} Values should be less than or equal to the table entries

INPUT PULSE DEFINITIONS



V_M = 1.3V for 54LS/74LS. V_M = 1.5V for all other TTL families

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
54/74	3.0V	1MHz	500ns	7ns	7ns
54LS/74LS	3.0V	1MHz	500ns	15ns	6ns
54S/74S	3.0V	1MHz	500ns	2.5ns	2.5ns

MOTOROLA

MC14503B

HEX NON-INVERTING 3-STATE BUFFER

The MC14503B is a hex non-inverting buffer with 3-state outputs, and a high current source and sink capability. The 3-state outputs make it useful in common bussing applications. Two disable controls are provided. A high level on the Disable A input causes the outputs of buffers 1 through 4 to go into a high impedance state and a high level on the Disable B input causes the outputs of buffers 5 and 6 to go into a high impedance state.

- 3-State Outputs
- TTL Compatible – Will Drive One TTL Load Over Full Temperature Range
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Symmetrical Turn-On and Turn-off Delays
- Symmetrical Output Rise and Fall Times
- Two Disable Controls for Added Versatility
- Pin for Pin Replacement for MM80C97 and 340097

CMOS SSI

(LOW-POWER COMPLEMENTARY MOS)

HEX 3-STATE BUFFER



L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648

ORDERING INFORMATION

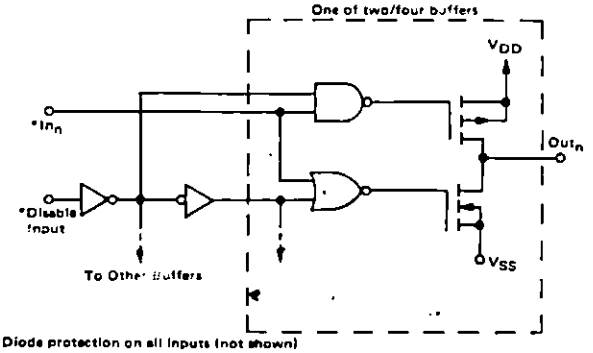
MC14XXXB — Suffix

Suffix	Denotes
L	Ceramic Package
P	Plastic Package
A	Extended Operating Temperature Range
C	Limited Operating Temperature Range

MAXIMUM RATINGS (Voltages referenced to V_{SS}, Pin 8)

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	−0.5 to +18	Vdc
Input Voltage, All Inputs	V_{in}	−0.5 to V_{DD} + 0.5	Vdc
DC Current Drain per Input Pin	I	10	mAdc
DC Current Drain per Output Pin	I	25	mAdc
Operating Temperature Range – AL Device CL/CP Device	T_A	−55 to +125 −40 to +85	°C
Storage Temperature Range	T_{stg}	−65 to +150	°C

CIRCUIT DIAGRAM



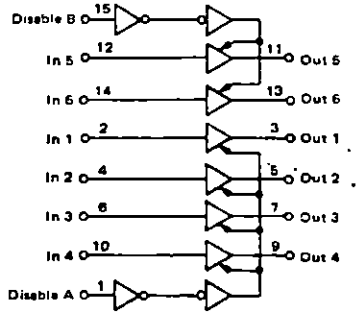
*Diode protection on all inputs (not shown)

TRUTH TABLE

In_n	Appropriate Disable Input	Out_n
0	0	0
1	0	1
X	1	High Impedance

X = Don't Care

LOGIC DIAGRAM



V_{DD} = Pin 16
V_{SS} = Pin 8

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

Unused inputs must always be tied on an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

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ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage "0" Level	V_{OL}	5.0		0.05	–	0	0.05	–	0.05	Vdc
V_{in} = V_{DD} or 0		10		0.05	–	0	0.05	–	0.05	
		15		0.05	–	0	0.05	–	0.05	
"1" Level	V_{OH}	5.0	4.95	–	4.95	5.0	–	4.95	–	Vdc
V_{in} = 0 or V_{DD}		10	9.95	–	9.95	10	–	9.95	–	
		15	14.95	–	14.95	15	–	14.95	–	
Noise Immunity# "0" Level	V_{IL}									Vdc
(V_O = 3.6 or 1.4 Vdc)		5.0		1.5		2.25	1.5	–	1.5	
(V_O = 7.2 or 2.8 Vdc)		10	–	3.0	–	4.50	3.0	–	3.0	
(V_O = 11.5 or 3.5 Vdc)		15	–	3.75	–	6.75	3.75	–	3.75	
"1" Level	V_{IH}	5.0	3.5	–	3.5	2.75	–	3.5	–	Vdc
(V_O = 1.4 or 3.6 Vdc)		10	7.0	–	7.0	5.5	–	7.0	–	
(V_O = 2.8 or 7.2 Vdc)		15	11.25	–	11.25	8.25	–	11.25	–	
(V_O = 3.5 or 11.5 Vdc)										
Output Drive Current (AL Device)***	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		4.6	-4.3	–	-3.6	-5.0	–	-2.5	–	
(V_{OH} = 2.5 Vdc)		5.0	-5.8	–	-4.80	-6.1	–	-3.0	–	
(V_{OH} = 4.6 Vdc)		5.0	-1.2	–	-1.02	-1.4	–	-0.7	–	
(V_{OH} = 9.5 Vdc)		10	-3.1	–	-2.60	-3.7	–	-1.8	–	
(V_{OH} = 13.5 Vdc)		15	-8.2	–	-6.80	-14.1	–	-4.8	–	
Sink	I_{OL}									mAdc
(V_{OL} = 0.4 Vdc)		4.6	2.2	–	1.8	2.1	–	1.2	–	
(V_{OL} = 0.4 Vdc)		5.0	2.6	–	2.1	2.3	–	1.3	–	
(V_{OL} = 0.5 Vdc)		10	6.5	–	5.5	6.2	–	3.8	–	
(V_{OL} = 1.5 Vdc)		15	19.2	–	16.10	25.00	–	11.2	–	
Output Drive Current (CL/CP Device)***	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		4.75	-4.0		-3.60	-5.5	–	-2.4	–	
(V_{OH} = 2.5 Vdc)		5.0	-4.6	–	-4.20	-6.1	–	-3.0	–	
(V_{OH} = 4.6 Vdc)		5.0	-1.0	–	-0.88	-1.4	–	-0.7	–	
(V_{OH} = 9.5 Vdc)		10	-2.4	–	-2.20	-3.7	–	-1.8	–	
(V_{OH} = 13.5 Vdc)		15	-6.6		-6.00	-14.1	–	-4.8	–	
Sink	I_{OL}									mAdc
(V_{OL} = 0.4 Vdc)		4.75	2.1	–	1.95	2.2	–	1.25	–	
(V_{OL} = 0.4 Vdc)		5.0	2.3	–	2.10	2.3	–	1.3	–	
(V_{OL} = 0.5 Vdc)		10	6.0	–	5.45	6.2	–	3.8	–	
(V_{OL} = 1.5 Vdc)		15	15.2	–	13.80	25.00	–	11.2	–	
Input Current (AL Device)	I_{in}	15	–	±0.1	–	±0.00001	±0.1	–	±1.0	µAdc
Input Current (CL/CP Device)	I_{in}	15	–	±0.3	–	±0.00001	±3.0	–	±1.0	µAdc
Input Capacitance (V_{in} = 0)	C_{in}	–	–	–	–	5.0	7.5	–	–	pF
Quiescent Current (AL Device)	I_Q	5.0	–	1.0	–	0.002	1.0	–	30	µAdc
(Per Package)		10	–	2.0	–	0.004	2.0	–	60	
		15	–	4.0	–	0.006	4.0	–	120	
Quiescent Current (CL/CP Device)	I_{DD}	5.0	–	4.0	–	0.002	4.0	–	30	µAdc
(Per Package)		10	–	8.0	–	0.004	8.0	–	60	
		15	–	16	–	0.006	16	–	120	
Total Supply Current**†	I_{DD}	5.0	(I_T = 2.5 µA/kHz) f + I_{DD}							µAdc
(Dynamic plus Quiescent, Per Package)		10	(I_T = 6.0 µA/kHz) f + I_{DD}							
(C_L = 50 pF on all outputs)		15	(I_T = 10 µA/kHz) f + I_{DD}							
(All outputs switching, 50% Duty Cycle)										
3-State Output Leakage Current	I_{TL}	15	–	±0.1	–	±0.0001	±0.1	–	±3.0	µAdc
(AL Device)			–		–			–		
3-State Output Leakage Current	I_{TL}	15	–	±1.0	–	±0.0001	±1.0	–	±7.5	µAdc
(CL/CP Device)			–		–			–		

*T_{low} = −55°C for AL Device, −40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device
#Noise immunity specified for worst-case input combination.
†To calculate total supply current at loads other than 50 pF,
$I_T(C_L) = I_T(50\ pF) + 6 \times 10^{-3} (C_L - 50) V_{DD} f$
I_T is in µA (per package) C_L in pF, V_{DD} in Vdc, and f in kHz is input frequency.
**The formulas given are for the typical characteristics only at 25°C
***Care must be taken not to exceed maximum current ratings (see maximum ratings table and Figure 1)

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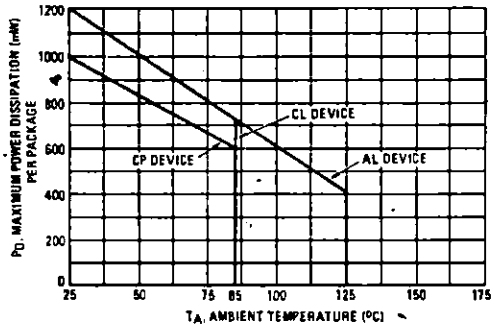
SWITCHING CHARACTERISTICS* (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD} V_{CC}	All Types Typ	All Types Max	Unit
Output Rise Time	t_{TLH}				ns
t_{TLH} = (0.5 ns/pF) C_L + 20 ns		5.0	45	90	
t_{TLH} = (0.3 ns/pF) C_L + 8.0 ns		10	23	45	
t_{TLH} = (0.2 ns/pF) C_L + 8.0 ns		15	18	35	
Output Fall Time	t_{THL}				ns
t_{THL} = (0.5 ns/pF) C_L + 20 ns		5.0	45	90	
t_{THL} = (0.3 ns/pF) C_L + 8.0 ns		10	23	45	
t_{THL} = (0.2 ns/pF) C_L + 8.0 ns		15	18	35	
Turn-Off Delay Time, all Outputs	t_{PLH}				ns
t_{PLH} = (0.3 ns/pF) C_L + 60 ns		5.0	75	150	
t_{PLH} = (0.15 ns/pF) C_L + 27 ns		10	35	70	
t_{PLH} = (0.1 ns/pF) C_L + 20 ns		15	25	50	
Turn-On Delay Time, all Outputs	t_{PHL}				ns
t_{PHL} = (0.3 ns/pF) C_L + 60 ns		5.0	75	150	
t_{PHL} = (0.15 ns/pF) C_L + 27 ns		10	35	70	
t_{PHL} = (0.1 ns/pF) C_L + 20 ns		15	25	50	
3-State Propagation Delay Time Output "1" to High Impedance	t_{PHZ}	5.0	75	150	ns
		10	40	80	
		15	35	70	
Output "0" to High Impedance	t_{PLZ}	5.0	80	160	ns
		10	40	80	
		15	35	70	
High Impedance to "1" Level	t_{PZH}	5.0	65	130	ns
		10	25	50	
		15	20	40	
High Impedance to "0" Level	t_{PZL}	5.0	100	200	ns
		10	35	70	
		15	25	50	

*The formulas given are for the typical characteristics only.

FIGURE 1 – AMBIENT TEMPERATURE POWER DERATING



MC14503B

FIGURE 2 – SWITCHING TIME TEST CIRCUIT AND WAVEFORMS
(t_{TLH}, t_{THL}, t_{PHL}, and t_{PLH})

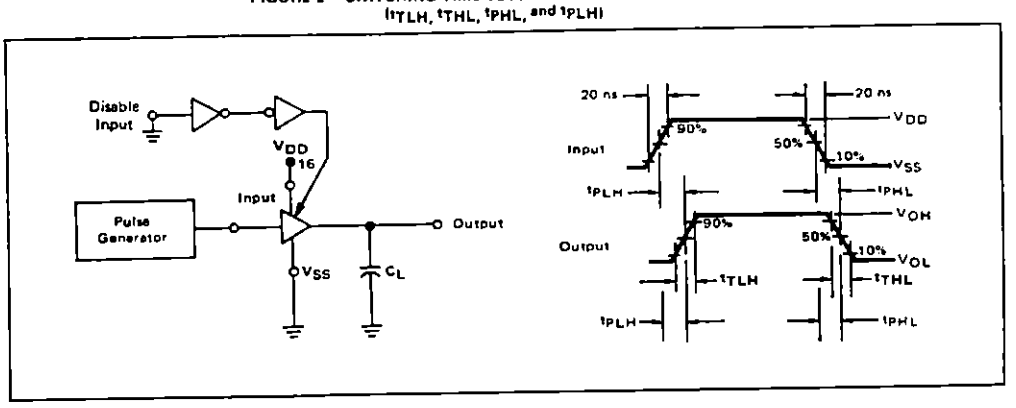
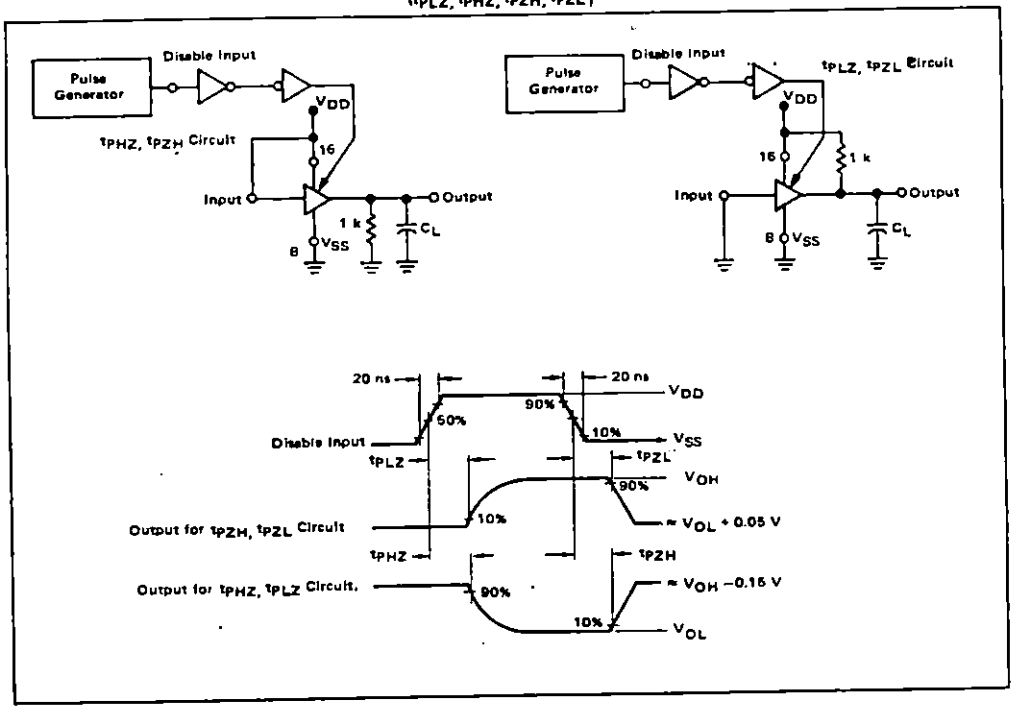


FIGURE 3 – 3 STATE AC TEST CIRCUITS AND WAVEFORMS
(t_{PLZ}, t_{PHZ}, t_{PZH}, t_{PZL})



National Semiconductor

CD4001M/CD4001C Quadruple 2-Input NOR Gate
CD4011M/CD4011C Quadruple 2-Input NAND Gate

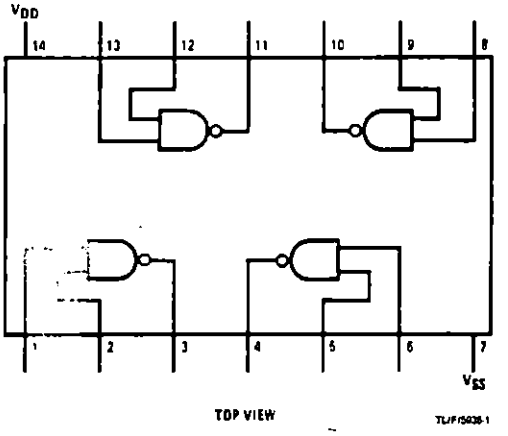
General Description

The CD4001M/CD4001C, CD4011M/CD4011C are monolithic complementary MOS (CMOS) quadruple two-input NOR and NAND gate integrated circuits. N- and P-channel enhancement mode transistors provide a symmetrical circuit with output swings essentially equal to the supply voltage. This results in high noise immunity over a wide supply voltage range. No DC power other than that caused by leakage current is consumed during static conditions. All inputs are protected against static discharge and latching conditions.

Features

■ Wide supply voltage range	3.0V to 15V
■ Low power	10nW (typ.)
■ High noise immunity	0.45 V_{DD} (typ.)

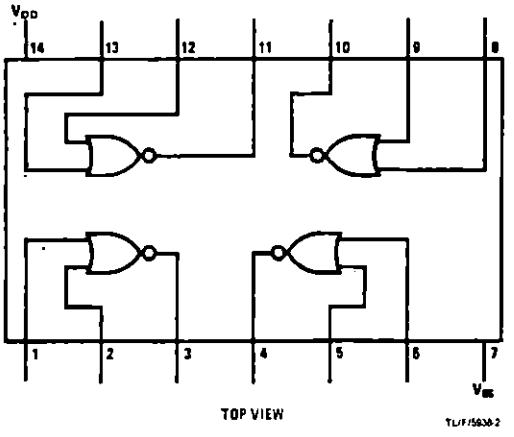
Connection Diagrams Dual-In-Line Packages



TOP VIEW

TL/F/5638-1

Order Number CD4001MJ, CD4001CJ, CD4011MJ or CD4011CJ
See NS Package J14A



TOP VIEW

TL/F/5638-2

Order Number CD4001MN, CD4001CN, CD4011MN or CD4011CN
See NS Package N14A

Absolute Maximum Ratings (Note 1)

Voltage an Any Pin	$V_{SS}-0.3\,V$ to $V_{DD}+0.3\,V$	Storage Temperature Range	−65°C to +150°C
Operating Temperature Range		Package Dissipation	500 mW
CD4001M, CD4011M	−55°C to +125°C	Operating V_{DD} Range	$V_{SS}+3.0\,V$ to $V_{SS}+15\,V$
CD4001C, CD4011C	−40°C to +85°C	Lead Temperature (Soldering, 10 seconds)	260°C

DC Electrical Characteristics — CD4001M, CD4011M

Sym	Parameter	Conditions	Limits							Units
			−55°C		25°C			125°C		
			Min	Max	Min	Typ	Max	Min	Max	
I_L	Quiescent Device Current	$V_{DD}=5.0V$		0.05		0.001	0.05		3.0	μA
		$V_{DD}=10V$		0.1		0.001	0.1		6.0	μA
P_D	Quiescent Device Dissipation/Package	$V_{DD}=5.0V$		0.25		0.005	0.25		15	μW
		$V_{DD}=10V$		1.0		0.01	1.0		60	μW
V_{OL}	Output Voltage Low Level	$V_{DD}=5.0V$, $V_I=V_{DD}$, $I_O=0A$		0.05		0	0.05		0.05	V
		$V_{DD}=10V$, $V_I=V_{DD}$, $I_O=0A$		0.05		0	0.05		0.05	V
V_{OH}	Output Voltage High Level	$V_{DD}=5.0V$, $V_I=V_{SS}$, $I_O=0A$	4.95		4.95	5.0		4.95		V
		$V_{DD}=10V$, $V_I=V_{SS}$, $I_O=0A$	9.95		9.95	10		9.95		V
V_{NL}	Noise Immunity (All Inputs)	$V_{DD}=5.0V$, $V_O=3.6V$, $I_O=0A$	1.5		1.5	2.25		1.4		V
		$V_{DD}=10V$, $V_O=7.2V$, $I_O=0A$	3.0		3.0	4.5		2.9		V
V_{NH}	Noise Immunity (All Inputs)	$V_{DD}=5.0V$, $V_O=0.95V$, $I_O=0A$	1.4		1.5	2.25		1.5		V
		$V_{DD}=10V$, $V_O=2.9V$, $I_O=0A$	2.9		3.0	4.5		3.0		V
I_DN	Output Drive Current N-Channel (4001) (Note 2)	$V_{DD}=5.0V$, $V_O=0.4V$, $V_I=V_{DD}$	0.5		0.40	1.0		0.28		mA
		$V_{DD}=10V$, $V_O=0.5V$, $V_I=V_{DD}$	1.1		0.9	2.5		0.65		mA
I_DP	Output Drive Current P-Channel (4001) (Note 2)	$V_{DD}=5.0V$, $V_O=2.5V$, $V_I=V_{SS}$	−0.62		−0.5	−2.0		−0.35		mA
		$V_{DD}=10V$, $V_O=9.5V$, $V_I=V_{SS}$	−0.62		−0.5	−1.0		−0.35		mA
I_DN	Output Drive Current N-Channel (4011) (Note 2)	$V_{DD}=5.0V$, $V_O=0.4V$, $V_I=V_{DD}$	0.31		0.25	0.5		0.175		mA
		$V_{DD}=10V$, $V_O=0.5V$, $V_I=V_{DD}$	0.63		0.5	0.6		0.35		mA
I_DP	Output Drive Current P-Channel (4011) (Note 2)	$V_{DD}=5.0V$, $V_O=2.5V$, $V_I=V_{SS}$	−0.31		−0.25	−0.5		−0.175		mA
		$V_{DD}=10V$, $V_O=9.5V$, $V_I=V_{SS}$	−0.75		−0.6	−1.2		−0.4		mA
I_I	Input Current					10				pA

DC Electrical Characteristics — CD4001C, CD4011C

Sym	Parameter	Conditions	Limits							Units
			−40°C		25°C			80°C		
			Min	Max	Min	Typ	Max	Min	Max	
I_L	Quiescent Device Current	$V_{DD} = 5.0V$ $V_{DD} = 10V$		0.5 5.0		0.005 0.005	0.5 5.0		15 30	μA μA
P_D	Quiescent Device Dissipation/Package	$V_{DD} = 5.0V$ $V_{DD} = 10V$		2.5 50		0.025 0.05	2.5 50		75 300	μW μW
V_{OL}	Output Voltage Low Level	$V_{DD} = 5.0V$, $V_I = V_{DD}$, $I_O = 0A$ $V_{DD} = 10V$, $V_I = V_{DD}$, $I_O = 0A$		0.05 0.05		0 0	0.05 0.05		0.05 0.05	V V
V_{OH}	Output Voltage High Level	$V_{DD} = 5.0V$, $V_I = V_{SS}$, $I_O = 0A$ $V_{DD} = 10V$, $V_I = V_{SS}$, $I_O = 0A$	4.95 9.95		4.95 9.95	5.0 10		4.95 9.95		V V
V_{NL}	Noise Immunity (All Inputs)	$V_{DD} = 5.0V$, $V_O = 3.6V$, $I_O = 0A$ $V_{DD} = 10V$, $V_O = 7.2V$, $I_O = 0A$	1.5 3.0		1.5 3.0	2.25 4.5		1.4 2.9		V V
V_{NH}	Noise Immunity (All Inputs)	$V_{DD} = 5.0V$, $V_O = 0.95V$, $I_O = 0A$ $V_{DD} = 10V$, $V_O = 2.9V$, $I_O = 0A$	1.4 2.9		1.5 3.0	2.25 4.5		1.5 3.0		V V
I_DN	Output Drive Current N-Channel (4001) (Note 2)	$V_{DD} = 5.0V$, $V_O = 0.4V$, $V_I = V_{DD}$ $V_{DD} = 10V$, $V_O = 0.5V$, $V_I = V_{DD}$	0.35 0.72		0.3 0.6	1.0 2.5		0.24 0.48		mA mA
I_DP	Output Drive Current P-Channel (4001) (Note 2)	$V_{DD} = 5.0V$, $V_O = 2.5V$, $V_I = V_{SS}$ $V_{DD} = 10V$, $V_O = 9.5V$, $V_I = V_{SS}$	−0.35 −0.3		−0.3 −0.25	−2.0 −1.0		−0.24 −0.2		mA mA
I_DN	Output Drive Current N-Channel (4011) (Note 2)	$V_{DD} = 5.0V$, $V_O = 0.4V$, $V_I = V_{DD}$ $V_{DD} = 10V$, $V_O = 0.5V$, $V_I = V_{DD}$	0.145 0.3		0.12 0.25	0.5 0.6		0.095 0.2		mA mA
I_DP	Output Drive Current P-Channel (4011) (Note 2)	$V_{DD} = 5.0V$, $V_O = 2.5V$, $V_I = V_{SS}$ $V_{DD} = 10V$, $V_O = 9.5V$, $V_I = V_{SS}$	−0.145 −0.35		−0.12 −0.3	−0.5 −1.2		−0.095 −0.24		mA mA
I_I	Input Current					10				pA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: I_DN and I_DP are tested one output at a time.

AC Electrical Characteristics $T_A = 25°C$, $C_L = 15\,pF$, and input rise and fall times = 20 ns.

Typical temperature coefficient for all values of $V_{DD} = 0.3\%/°C$

Sym	Parameter	Conditions	Min	Typ	Max	Units
CD4001M						
t_{PHL}	Propagation Delay Time High to Low Level	$V_{DD} = 5.0V$ $V_{DD} = 10V$		35 25	50 40	ns ns
t_{PLH}	Propagation Delay Time Low to High Level	$V_{DD} = 5.0V$ $V_{DD} = 10V$		35 25	65 40	ns ns
t_{THL}	Transition Time High to Low Level	$V_{DD} = 5.0V$ $V_{DD} = 10V$		65 35	125 70	ns ns
t_{TLH}	Transition Time Low to High Level	$V_{DD} = 5.0V$ $V_{DD} = 10V$		65 35	175 75	ns ns
C_{IN}	Input Capacitance	Any Input		5.0		pF
CD4001C						
t_{PHL}	Propagation Delay Time High to Low Level	$V_{DD} = 5.0V$ $V_{DD} = 10V$		35 25	80 55	ns ns
t_{PLH}	Propagation Delay Time Low to High Level	$V_{DD} = 5.0V$ $V_{DD} = 10V$		35 25	120 65	ns ns
t_{THL}	Transition Time High to Low Level	$V_{DD} = 5.0V$ $V_{DD} = 10V$		65 35	200 115	ns ns
t_{TLH}	Transition Time Low to High Level	$V_{DD} = 5.0V$ $V_{DD} = 10V$		65 35	300 125	ns ns
C_{IN}	Input Capacitance	Any Input		5.0		pF

AC Electrical Characteristics $T_A = 25°C$, $C_L = 15\,pF$, and input rise and fall times = 20 ns.

Typical temperature coefficient for all values of $V_{DD} = 0.3\%/°C$

Sym	Parameter	Conditions	Min	Typ	Max	Units
CD4011M						
t_{PHL}	Propagation Delay Time High to Low Level	$V_{DD} = 5.0V$ $V_{DD} = 10V$		50 25	75 40	ns ns
t_{PLH}	Propagation Delay Time Low to High Level	$V_{DD} = 5.0V$ $V_{DD} = 10V$		50 25	75 40	ns ns
t_{THL}	Transition Time High to Low Level	$V_{DD} = 5.0V$ $V_{DD} = 10V$		75 50	125 75	ns ns
t_{TLH}	Transition Time Low to High Level	$V_{DD} = 5.0V$ $V_{DD} = 10V$		75 40	100 60	ns ns
C_{IN}	Input Capacitance	Any Input		5.0		pF
CD4011C						
t_{PHL}	Propagation Delay Time High to Low Level	$V_{DD} = 5.0V$ $V_{DD} = 10V$		50 25	100 50	ns ns
t_{PLH}	Propagation Delay Time Low to High Level	$V_{DD} = 5.0V$ $V_{DD} = 10V$		50 25	100 50	ns ns
t_{THL}	Transition Time High to Low Level	$V_{DD} = 5.0V$ $V_{DD} = 10V$		75 50	150 100	ns ns
t_{TLH}	Transition Time Low to High Level	$V_{DD} = 5.0V$ $V_{DD} = 10V$		75 40	125 75	ns ns
C_{IN}	Input Capacitance	Any Input		5.0		pF

National Semiconductor

CD4002M/CD4002C Dual 4-Input NOR Gate
CD4012M/CD4012C Dual 4-Input NAND Gate

General Description

These NOR and NAND gates are monolithic complementary MOS (CMOS) integrated circuits. The N- and P-channel enhancement mode transistors provide a symmetrical circuit with output swing essentially equal to the supply voltage. This results in high noise immunity over a wide supply voltage range. No DC power other than that caused by leakage current is consumed during static conditions. All inputs are protected against static discharge and latching conditions.

Features

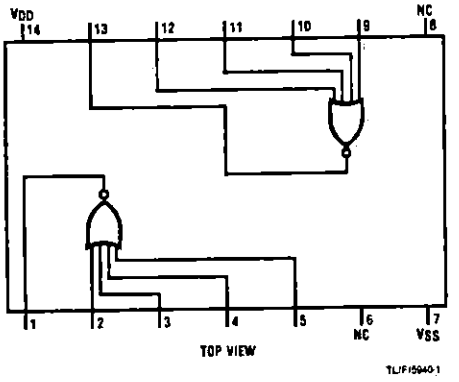
■ Wide supply voltage range	3.0V to 15V
■ Low power	10nW (typ.)
■ High noise immunity	0.45 V_{DD} (typ.)

Applications

- Automotive
- Data terminals
- Instrumentation
- Medical Electronics
- Alarm system
- Industrial controls
- Remote metering
- Computers

Connection Diagrams Dual-In-Line Packages

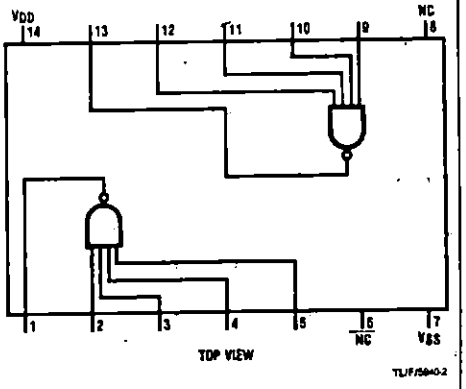
CD4002



TOP VIEW

TL/F/5940-1

CD4012



TOP VIEW

TL/F/5940-2

Absolute Maximum Ratings (Note 1)

Voltage an Any Pin V_{SS} − 0.3 V to V_{DD} + 0.3 V
Operating Temperature Range
CD4002M, CD4012M −55°C to +125°C
CD4002C, CD4012C −40°C to +85°C

Storage Temperature Range −65°C to +150°C
Package Dissipation 500 mW
Operating V_{DD} Range V_{SS} + 3.0 V to V_{SS} + 15 V
Lead Temperature (Soldering, 10 seconds) 260°C

DC Electrical Characteristics — CD4002M, CD4012M

Sym	Parameter	Conditions	Limits							Units
			−55°C		25°C			125°C		
			Min	Max	Min	Typ	Max	Min	Max	
I_L	Quiescent Device Current	V_{DD} = 5.0V V_{DD} = 10V		0.05 0.1		0.001 0.001	0.05 0.1		3.0 6.0	μA μA
P_D	Quiescent Device Dissipation/Package	V_{DD} = 5.0V V_{DD} = 10V		0.25 1.0		0.005 0.01	0.25 1.0		15 60	μW μW
V_{OL}	Output Voltage Low Level	V_{DD} = 5.0V, V_I = V_{DD}, I_O = 0A V_{DD} = 10V, V_I = V_{DD}, I_O = 0A		0.05 0.05		0 0	0.05 0.05		0.05 0.05	V V
V_{OH}	Output Voltage High Level	V_{DD} = 5.0V, V_I = V_{SS}, I_O = 0A V_{DD} = 10V, V_I = V_{SS}, I_O = 0A	4.95 9.95		4.95 9.95	5.0 10		4.95 9.95		V V
V_{NL}	Noise Immunity (All Inputs)	V_{DD} = 5.0V, V_O = 3.6V, I_O = 0A V_{DD} = 10V, V_O = 7.2V, I_O = 0A	1.5 3.0		1.5 3.0	2.25 4.5		1.4 2.9		V V
V_{NH}	Noise Immunity (All Inputs)	V_{DD} = 5.0V, V_O = 0.95V, I_O = 0A V_{DD} = 10V, V_O = 2.9V, I_O = 0A	1.4 2.9		1.5 3.0	2.25 4.5		1.5 3.0		V V
I_DN	Output Drive Current N-Channel (4002) (Note 2)	V_{DD} = 5.0V, V_O = 0.4V, V_I = V_{DD} V_{DD} = 10V, V_O = 0.5V, V_I = V_{DD}	0.5 1.1		0.40 0.9	1.0 2.5		0.28 0.65		mA mA
I_DP	Output Drive Current P-Channel (4002) (Note 2)	V_{DD} = 5.0V, V_O = 2.5V, V_I = V_{SS} V_{DD} = 10V, V_O = 9.5V, V_I = V_{SS}	−0.62 −0.62		−0.5 −0.5	−2.0 −1.0		−0.35 −0.35		mA mA
I_DN	Output Drive Current N-Channel (4012) (Note 2)	V_{DD} = 5.0V, V_O = 0.4V, V_I = V_{DD} V_{DD} = 10V, V_O = 0.5V, V_I = V_{DD}	0.31 0.63		0.25 0.5	0.5 0.6		0.175 0.35		mA mA
I_DP	Output Drive Current P-Channel (4012) (Note 2)	V_{DD} = 5.0V, V_O = 2.5V, V_I = V_{SS} V_{DD} = 10V, V_O = 9.5V, V_I = V_{SS}	−0.31 −0.75		−0.25 −0.6	−0.5 −1.2		−0.175 −0.4		mA mA
I_I	Input Current					10				pA

DC Electrical Characteristics — CD4002C, CD4012C

Sym	Parameter	Conditions	Limits							Units
			−40°C		25°C			85°C		
			Min	Max	Min	Typ	Max	Min	Max	
I_L	Quiescent Device Current	$V_{DD} = 5.0V$ $V_{DD} = 10V$		0.5 5.0		0.005 0.005	0.5 5.0		15 30	μA μA
P_D	Quiescent Device Dissipation/Package	$V_{DD} = 5.0V$ $V_{DD} = 10V$		2.5 50		0.025 0.05	2.5 50		75 300	μW μW
V_{OL}	Output Voltage Low Level	$V_{DD} = 5.0V$, $V_I = V_{DD}$, $I_O = 0A$ $V_{DD} = 10V$, $V_I = V_{DD}$, $I_O = 0A$		0.05 0.05		0 0	0.05 0.05		0.05 0.05	V V
V_{OH}	Output Voltage High Level	$V_{DD} = 5.0V$, $V_I = V_{SS}$, $I_O = 0A$ $V_{DD} = 10V$, $V_I = V_{SS}$, $I_O = 0A$	4.95 9.95		4.95 9.95	5.0 10		4.95 9.95		V V
V_{NL}	Noise Immunity (All Inputs)	$V_{DD} = 5.0V$, $V_O \geq 3.5V$, $I_O = 0A$ $V_{DD} = 10V$, $V_O \geq 7.2V$, $I_O = 0A$	1.5 3.0		1.5 3.0	2.25 4.5		1.4 2.9		V V
V_{NH}	Noise Immunity (All Inputs)	$V_{DD} = 5.0V$, $V_O \leq 1.5V$, $I_O = 0A$ $V_{DD} = 10V$, $V_O \leq 3.5V$, $I_O = 0A$	1.4 2.9		1.5 3.0	2.25 4.5		1.5 3.0		V V
I_DN	Output Drive Current N-Channel (4002) (Note 2)	$V_{DD} = 5.0V$, $V_O = 0.4V$, $V_I = V_{DD}$ $V_{DD} = 10V$, $V_O = 0.5V$, $V_I = V_{DD}$	0.35 0.72		0.3 0.6	1.0 2.5		0.24 0.48		mA mA
I_DN	Output Drive Current N-Channel (4012) (Note 2)	$V_{DD} = 5.0V$, $V_O = 0.4V$, $V_I = V_{DD}$ $V_{DD} = 10V$, $V_O = 0.5V$, $V_I = V_{DD}$	0.145 0.3		0.12 0.25	0.5 0.6		0.095 0.2		mA mA
I_DP	Output Drive Current P-Channel (4002) (Note 2)	$V_{DD} = 5.0V$, $V_O = 2.5V$, $V_I = V_{SS}$ $V_{DD} = 10V$, $V_O = 9.5V$, $V_I = V_{SS}$	−0.35 −0.3		−0.3 −0.25	−2.0 −1.0		−0.24 −0.2		mA mA
I_DP	Output Drive Current P-Channel (4012) (Note 2)	$V_{DD} = 5.0V$, $V_O = 2.5V$, $V_I = V_{SS}$ $V_{DD} = 10V$, $V_O = 9.5V$, $V_I = V_{SS}$	−0.145 −0.35		−0.12 −0.3	−0.5 −1.2		−0.095 −0.24		mA mA
I_I	Input Current					10				pA

AC Electrical Characteristics $T_A = 25°C$, $C_L = 15pF$, and input rise and fall times = 20ns.

Typical temperature coefficient for all values of $V_{DD} = 0.3\%/°C$

Sym	Parameter	Conditions	Min	Typ	Max	Units
CD4002M						
t_{PHL}	Propagation Delay Time High to Low Level	$V_{DD} = 5.0V$ $V_{DD} = 10V$		35 25	50 40	ns ns
t_{PLH}	Propagation Delay Time Low to High Level	$V_{DD} = 5.0V$ $V_{DD} = 10V$		35 25	50 40	ns ns
t_{THL}	Transition Time High to Low Level	$V_{DD} = 5.0V$ $V_{DD} = 10V$		65 35	175 75	ns ns
t_{TLH}	Transition Time Low to High Level	$V_{DD} = 5.0V$ $V_{DD} = 10V$		65 35	125 70	ns ns
C_{IN}	Input Capacitance	Any Input		5.0		pF
CD4002C						
t_{PHL}	Propagation Delay Time High to Low Level	$V_{DD} = 5.0V$ $V_{DD} = 10V$		35 25	120 65	ns ns
t_{PLH}	Propagation Delay Time Low to High Level	$V_{DD} = 5.0V$ $V_{DD} = 10V$		35 25	80 55	ns ns
t_{THL}	Transition Time High to Low Level	$V_{DD} = 5.0V$ $V_{DD} = 10V$		65 35	300 125	ns ns
t_{TLH}	Transition Time Low to High Level	$V_{DD} = 5.0V$ $V_{DD} = 10V$		65 35	200 115	ns ns
C_{IN}	Input Capacitance	Any Input		5.0		pF

AC Electrical Characteristics $T_A = 25°C$, $C_L = 15pF$, and input rise and fall times = 20ns.

Typical temperature coefficient for all values of $V_{DD} = 0.3\%/°C$

Sym	Parameter	Conditions	Min	Typ	Max	Units
CD4012M						
t_{PHL}	Propagation Delay Time High to Low Level	$V_{DD} = 5.0V$ $V_{DD} = 10V$		50 25	75 40	ns ns
t_{PLH}	Propagation Delay Time Low to High Level	$V_{DD} = 5.0V$ $V_{DD} = 10V$		50 25	75 40	ns ns
t_{THL}	Transition Time High to Low Level	$V_{DD} = 5.0V$ $V_{DD} = 10V$		75 50	125 75	ns ns
t_{TLH}	Transition Time Low to High Level	$V_{DD} = 5.0V$ $V_{DD} = 10V$		75 40	100 60	ns ns
C_{IN}	Input Capacitance	Any Input		5.0		pF
CD4012C						
t_{PHL}	Propagation Delay Time High to Low Level	$V_{DD} = 5.0V$ $V_{DD} = 10V$		50 25	100 50	ns ns
t_{PLH}	Propagation Delay Time Low to High Level	$V_{DD} = 5.0V$ $V_{DD} = 10V$		50 25	100 50	ns ns
t_{THL}	Transition Time High to Low Level	$V_{DD} = 5.0V$ $V_{DD} = 10V$		75 50	150 100	ns ns
t_{TLH}	Transition Time Low to High Level	$V_{DD} = 5.0V$ $V_{DD} = 10V$		75 40	125 75	ns ns
C_{IN}	Input Capacitance	Any Input		5.0		pF

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: I_DN and I_DP are tested one output at a time.

National Semiconductor

MM54C00/MM74C00 Quad 2-Input NAND Gate
MM54C02/MM74C02 Quad 2-Input NOR Gate
MM54C04/MM74C04 Hex Inverter
MM54C10/MM74C10 Triple 3-Input NAND Gate
MM54C20/MM74C20 Dual 4-Input NAND Gate

General Description

These logic gates employ complementary MOS (CMOS) to achieve wide power supply operating range, low power consumption, high noise immunity and symmetric controlled rise and fall times. With features such as this the 54C/74C logic family is close to ideal for use in digital systems. Function and pin out compatibility with series 54/74 devices minimizes design time for those designers already familiar with the standard 54/74 logic family.

All inputs are protected from damage due to static discharge by diode clamps to V_{CC} and GND.

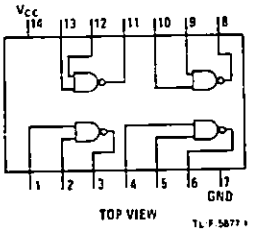
Features

■ Wide supply voltage range	3.0V to 15V
■ Guaranteed noise margin	1.0V
■ High noise immunity	0.45 V_{CC} (typ.)
■ Low power consumption	10 nW/package (typ.)
■ Low power TTL compatibility	fan out of 2 driving 74L

Connection Diagrams

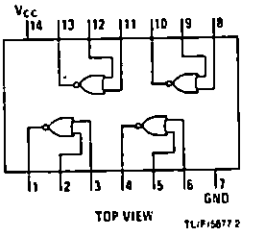
Dual-In-Line Packages

MM54C00/MM74C00



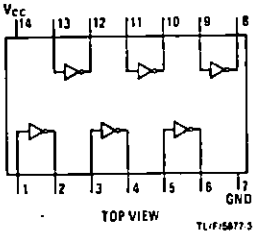
Order Number MM54C00J, MM74C00J, MM54C00N or MM74C00N
See NS Package J14A or N14A

MM54C02/MM74C02



Order Number MM54C02J, MM74C02J, MM54C02N or MM74C02N
See NS Package J14A or N14A

MM54C04/MM74C04



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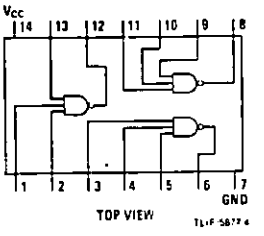
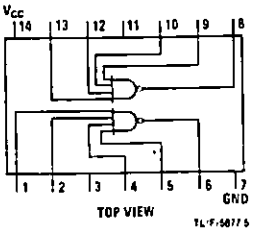
See NS Package J14A or N14A

MM54C10/MM74C10



MM54C20/MM74C20



Absolute Maximum Ratings

Voltage at Any Pin	−0.3V to V_{CC} + 0.3V	Operating V_{CC} Range	3.0V to 15V
Operating Temperature Range		Maximum V_{CC} Voltage	18V
54C	−55°C to +125°C	Package Dissipation	500 mW
74C	−40°C to +85°C	Lead Temperature (Soldering, 10 seconds)	300°C
Storage Temperature Range	−65°C to +150°C		

DC Electrical Characteristics

Min/max limits apply across the guaranteed temperature range unless otherwise noted.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
CMOS to CMOS						
$V_{IN(1)}$	Logical "1" Input Voltage	V_{CC} = 5.0V V_{CC} = 10V	3.5 8.0			V V
$V_{IN(0)}$	Logical "0" Input Voltage	V_{CC} = 5.0V V_{CC} = 10V			1.5 2.0	V V
$V_{OUT(1)}$	Logical "1" Output Voltage	V_{CC} = 5.0V, I_O = −10μA V_{CC} = 10V, I_O = −10μA	4.5 9.0			V V
$V_{OUT(0)}$	Logical "0" Output Voltage	V_{CC} = 5.0V, I_O = +10μA V_{CC} = 10V, I_O = +10μA			0.5 1.0	V V
$I_{IN(1)}$	Logical "1" Input Current	V_{CC} = 15V, V_{IN} = 15V		0.005	1.0	μA
$I_{IN(0)}$	Logical "0" Input Current	V_{CC} = 15V, V_{IN} = 0V	−1.0	−0.005		μA
I_{CC}	Supply Current	V_{CC} = 15V		0.01	15	μA
Low Power to CMOS						
$V_{IN(1)}$	Logical "1" Input Voltage	54C, V_{CC} = 4.5V 74C, V_{CC} = 4.75V	V_{CC} − 1.5 V_{CC} − 1.5			V V
$V_{IN(0)}$	Logical "0" Input Voltage	54C, V_{CC} = 4.5V 74C, V_{CC} = 4.75V			0.8 0.8	V V
$V_{OUT(1)}$	Logical "1" Output Voltage	54C, V_{CC} = 4.5V, I_O = −10μA 74C, V_{CC} = 4.75V, I_O = −10μA	4.4 4.4			V V
$V_{OUT(0)}$	Logical "0" Output Voltage	54C, V_{CC} = 4.5V, I_O = +10μA 74C, V_{CC} = 4.75V, I_O = +10μA			0.4 0.4	V V
CMOS to Low Power						
$V_{IN(1)}$	Logical "1" Input Voltage	54C, V_{CC} = 4.5V 74C, V_{CC} = 4.75V	4.0 4.0			V V
$V_{IN(0)}$	Logical "0" Input Voltage	54C, V_{CC} = 4.5V 74C, V_{CC} = 4.75V			1.0 1.0	V V
$V_{OUT(1)}$	Logical "1" Output Voltage	54C, V_{CC} = 4.5V, I_O = −360μA 74C, V_{CC} = 4.75V, I_O = −360μA	2.4 2.4			V V
$V_{OUT(0)}$	Logical "0" Output Voltage	54C, V_{CC} = 4.5V, I_O = 360μA 74C, V_{CC} = 4.75V, I_O = 360μA			0.4 0.4	V V
Output Drive (See 54C/74C Family Characteristics Data Sheet) (short circuit current)						
I_{SOURCE}	Output Source Current	V_{CC} = 5.0V, $V_{IN(0)}$ = 0V T_A = 25°C, V_{OUT} = 0V	−1.75			mA
I_{SOURCE}	Output Source Current	V_{CC} = 10V, $V_{IN(0)}$ = 0V T_A = 25°C, V_{OUT} = 0V	−8.0			mA
I_{SINK}	Output Sink Current	V_{CC} = 5.0V, $V_{IN(1)}$ = 5.0V T_A = 25°C, V_{OUT} = V_{CC}	1.75			mA
I_{SINK}	Output Sink Current	V_{CC} = 10V, $V_{IN(1)}$ = 10V T_A = 25°C, V_{OUT} = V_{CC}	8.0			mA

AC Electrical Characteristics

$T_A = 25°C$, $C_L = 50\,pF$, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
MM54C00/MM74C00, MM54C02/MM74C02, MM54C04/MM74C04						
t_{pd0}, t_{pd1}	Propagation Delay Time to Logical "1" or "0"	$V_{CC} = 5.0V$		50	90	ns
		$V_{CC} = 10V$		30	60	ns
C_{IN}	Input Capacitance	(Note 2)		6.0		pF
C_{PD}	Power Dissipation Capacitance	(Note 3) Per Gate or Inverter		12		pF
MM54C10/MM74C10						
t_{pd0}, t_{pd1}	Propagation Delay Time to Logical "1" or "0"	$V_{CC} = 5.0V$		60	100	ns
		$V_{CC} = 10V$		35	70	ns
C_{IN}	Input Capacitance	(Note 2)		7.0		pF
C_{PD}	Power Dissipation Capacitance	(Note 3) Per Gate		18		pF
MM54C20/MM74C20						
t_{pd0}, t_{pd1}	Propagation Delay Time to Logical "1" or "0"	$V_{CC} = 5.0V$		70	115	ns
		$V_{CC} = 10V$		40	80	ns
C_{IN}	Input Capacitance	(Note 2)		9		pF
C_{PD}	Power Dissipation Capacitance	(Note 3) Per Gate		30		pF

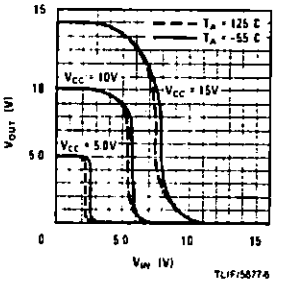
Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Capacitance is guaranteed by periodic testing.

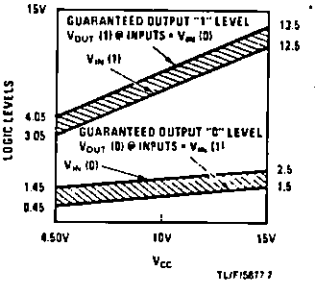
Note 3: C_{PD} determines the no load ac power consumption of any CMOS device. For complete explanation see 54C/74C Family Characteristics application note — AN-90.

Typical Performance Characteristics

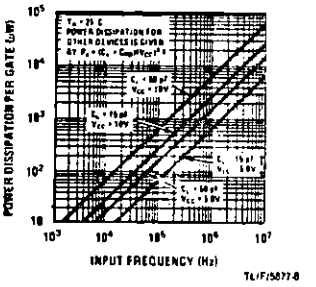
Gate Transfer Characteristics



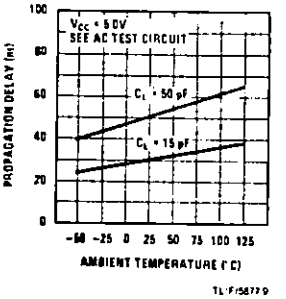
Guaranteed Noise Margin Over Temperature vs V_{CC}



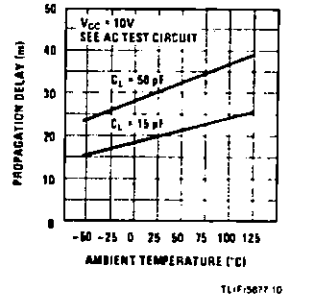
Power Dissipation vs Frequency MM54C00/MM74C00, MM54C02/MM74C02, MM54C04/MM74C04



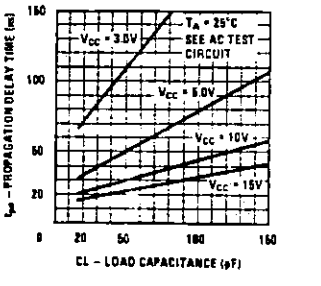
Propagation Delay vs Ambient Temperature MM54C00/MM74C00, MM54C02/MM74C02, MM54C04/MM74C04



Propagation Delay vs Ambient Temperature MM54C00/MM74C00, MM54C02/MM74C02, MM54C04/MM74C04

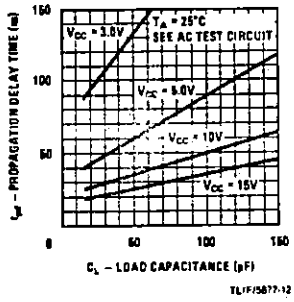


Propagation Delay Time vs Load Capacitance MM54C00/MM74C00, MM54C02/MM74C02, MM54C04/MM74C04

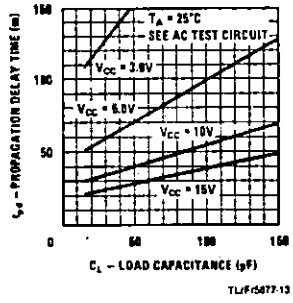


Typical Performance Characteristics (Cont'd)

Propagation Delay Time vs
Load Capacitance
MM54C10/MM74C10

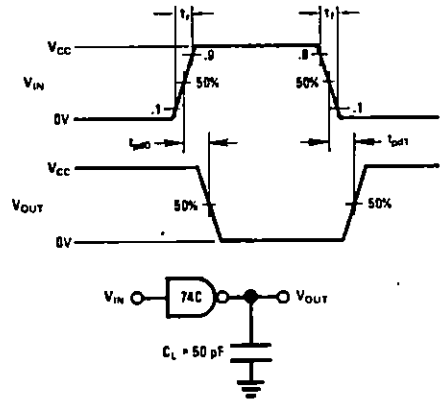


Propagation Delay Time vs
Load Capacitance
MM54C20/MM74C20



Switching Time Waveforms and AC Test Circuit

CMOS to CMOS



NOTE: DELAYS MEASURED WITH INPUT t_r, $t_f \leq 20$ ns.

TL/F/5877-14

National Semiconductor

CD4002BM/CD4002BC Dual 4-Input NOR Gate
CD4012BM/CD4012BC Dual 4-Input NAND Gate

General Description

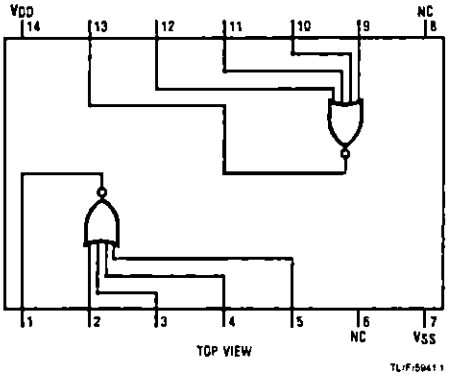
These dual gates are monolithic complementary MOS (CMOS) integrated circuits constructed with N-and P-channel enhancement mode transistors. They have equal source and sink current capabilities and conform to standard B series output drive. The devices also have buffered outputs which improve transfer characteristics by providing very high gain. All inputs are protected against static discharge with diodes to V_{DD} and V_{SS}.

Features

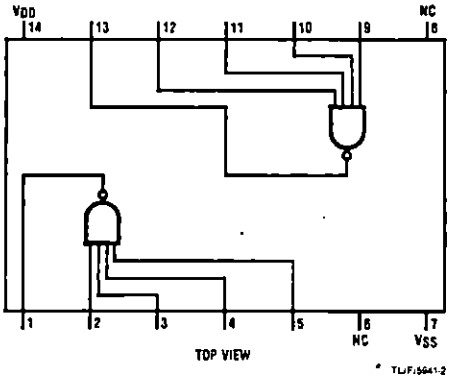
- Wide supply voltage range — 3.0V to 15V
- High noise immunity — 0.45 V_{DD} (typ.)
- Low power TTL compatibility — fanout of 2 driving 74L or 1 driving 74LS
- 5V-10V-15V parametric ratings
- Symmetrical output characteristics
- Maximum input leakage 1 μA at 15V over full temperature range

Connection Diagrams Dual-In-Line Packages

CD4002BM/CD4002BC



CD4012BM/CD4012BC



Order Number CD4002BMJ, CD4002BCJ,
CD4012BMJ or CD4012BCJ
See NS Package J14A

Order Number CD4002BMN, CD4002BCN,
CD4012BMN or CD4012BCN
See NS Package N14A

Absolute Maximum Ratings (Notes 1 and 2)

V_{DD} Supply Voltage	−0.5 V to +18 V
V_{IN} Input Voltage	−0.5 to V_{DD}0.5 V
T_S Storage Temperature Range	−65°C to +150°C
P_D Package Dissipation	500 mW
T_L Lead Temperature (soldering, 10 seconds)	260°C

Recommended Operating Conditions (Note 2)

V_{DD} Supply Voltage	3.0 to 15 V
V_{IN} Input Voltage	0 V to V_{DD} V
T_A Operating Temperature Range	
CD4002BM, CD4012BM	−55°C to +125°C
CD4002BC, CD4012BC	−40°C to +85°C

DC Electrical Characteristics (Note 2) — CD4002BM, CD4012BM

Sym	Parameter	Conditions	−55°C		25°C			125°C		Units
			Min	Max	Min	Typ	Max	Min	Max	
I_{DD}	Quiescent Device Current	V_{DD} = 5.0 V, V_{IN} = V_{DD} or V_{SS}		0.25		0.004	0.25		7.5	μA
		V_{DD} = 10 V, V_{IN} = V_{DD} or V_{SS}		0.5		0.005	0.5		15	μA
		V_{DD} = 15 V, V_{IN} = V_{DD} or V_{SS}		1.0		0.006	1.0		30	μA
V_{OL}	Low Level Output Voltage	V_{DD} = 5.0 V		0.05		0	0.05		0.05	V
		V_{DD} = 10 V		0.05		0	0.05		0.05	V
		V_{DD} = 15 V		0.05		0	0.05		0.05	V
V_{OH}	High Level Output Voltage	V_{DD} = 5.0 V	4.95		4.95	5.0		4.95		V
		V_{DD} = 10 V	9.95		9.95	10		9.95		V
		V_{DD} = 15 V	14.95		14.95	15		14.95		V
V_{IL}	Low Level Input Voltage	V_{DD} = 5.0 V, V_O = 0.5 V or 4.5 V		1.5		2.25	1.5		1.5	V
		V_{DD} = 10 V, V_O = 1.0 V or 9.0 V		3.0		4.50	3.0		3.0	V
		V_{DD} = 15 V, V_O = 1.5 V or 13.5 V		4.0		6.75	4.0		4.0	V
V_{IH}	High Level Input Voltage	V_{DD} = 5.0 V, V_O = 0.5 V or 4.5 V	3.5		3.5	2.75		3.5		V
		V_{DD} = 10 V, V_O = 1.0 V or 9.0 V	7.0		7.0	5.50		7.0		V
		V_{DD} = 15 V, V_O = 1.5 V or 13.5 V	11.0		11.0	8.25		11.0		V
I_{OL}	Low Level Output Current (Note 3)	V_{DD} = 5.0 V, V_O = 0.4 V	0.64		0.51	0.88		0.36		mA
		V_{DD} = 10 V, V_O = 0.5 V	1.6		1.3	2.2		0.90		mA
		V_{DD} = 15 V, V_O = 1.5 V	4.2		3.4	8.0		2.4		mA
I_{OH}	High Level Output Current (Note 3)	V_{DD} = 5.0 V, V_O = 4.6 V	−0.64		−0.51	−0.88		−0.36		mA
		V_{DD} = 10 V, V_O = 9.5 V	−1.6		−1.3	−2.2		−0.90		mA
		V_{DD} = 15 V, V_O = 13.5 V	−4.2		−3.4	−8.0		−2.4		mA
I_{IN}	Input Current	V_{DD} = 15 V, V_{IN} = 0 V		−0.10		-10^{-5}	−0.10		−1.0	μA
		V_{DD} = 15 V, V_{IN} = 15 V		0.10		10^{5}	0.10		1.0	μA

National Semiconductor

CD4013BM/CD4013BC Dual D Flip-Flop

General Description

The CD4013B dual D flip-flop is a monolithic complementary MOS (CMOS) integrated circuit constructed with N- and P-channel enhancement mode transistors. Each flip-flop has independent data, set, reset, and clock inputs and "Q" and "$\overline{Q}$" outputs. These devices can be used for shift register applications, and by connecting "$\overline{Q}$" output to the data input, for counter and toggle applications. The logic level present at the "D" input is transferred to the Q output during the positive-going transition of the clock pulse. Setting or resetting is independent of the clock and is accomplished by a high level on the set or reset line respectively.

Features

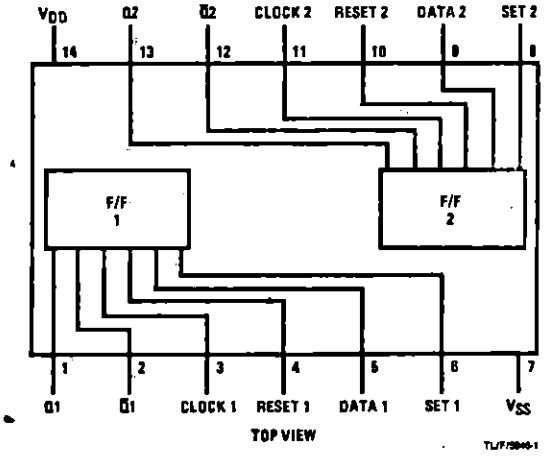
■ Wide supply voltage range	3.0V to 15V
■ High noise immunity	0.45 V_{DD} (typ.)
■ Low power TTL compatibility	fan out of 2 driving 74L or 1 driving 74LS

Applications

- Automotive
- Data terminals
- Instrumentation
- Medical electronics
- Alarm system
- Industrial electronics
- Remote metering
- Computers

Connection Diagram

Dual-In-Line Package



Order Number CD4013BMJ or CD4013BCJ
See NS Package J14A

Order Number CD4013BMN or CD4013BCN
See NS Package N14A

Truth Table

CL↑	D	R	S	Q	$\overline{Q}$
↑	0	0	0	0	1
↑	1	0	0	1	0
↓	x	0	0	Q	$\overline{Q}$
x	x	1	0	0	1
x	x	0	1	1	0
x	x	1	1	1	1

No change
↑ = Level change
x = Don't care case

Absolute Maximum Ratings

(Notes 1 and 2)

V_{DD} dc Supply Voltage	−0.5 to +18 V_{DC}
V_{IN} Input Voltage	−0.5 to V_{DD} +0.5 V_{DC}
T_S Storage Temperature Range	−65°C to +150°C
P_D Package Dissipation	500 mW
T_L Lead Temperature (Soldering, 10 seconds)	260°C

Recommended Operating Conditions

(Note 2)

V_{DD} dc Supply Voltage	+3 to +15 V_{DC}
V_{IN} Input Voltage	0 to V_{DD} V_{DC}
T_A Operating Temperature Range	
CD4013BM	−55°C to +125°C
CD4013BC	−40°C to +85°C

DC Electrical Characteristics CD4013BM (Note 2)

SYM	PARAMETER	CONDITIONS	−55°C		25°C			125°C		UNITS
			MIN	MAX	MIN	TYP	MAX	MIN	MAX	
I_{DD}	Quiescent Device Current	V_{DD} = 5V, V_{IN} = V_{DD} or V_{SS}		1.0			1.0		30	μA
		V_{DD} = 10V, V_{IN} = V_{DD} or V_{SS}		2.0			2.0		60	μA
		V_{DD} = 15V, V_{IN} = V_{DD} or V_{SS}		4.0			4.0		120	μA
V_{OL}	Low Level Output Voltage	$\|I_O\|$ < 1.0μA								
		V_{DD} = 5V		0.05			0.05		0.05	V
		V_{DD} = 10V		0.05			0.05		0.05	V
		V_{DD} = 15V		0.05			0.05		0.05	V
V_{OH}	High Level Output Voltage	$\|I_O\|$ < 1.0μA								
		V_{DD} = 5V	4.95		4.95			4.95		V
		V_{DD} = 10V	9.95		9.95			9.95		V
		V_{DD} = 15V	14.95		14.95			14.95		V
V_{IL}	Low Level Input Voltage	$\|I_O\|$ < 1.0μA								
		V_{DD} = 5V, V_O = 0.5V or 4.5V		1.5			1.5		1.5	V
		V_{DD} = 10V, V_O = 1.0V or 9.0V		3.0			3.0		3.0	V
		V_{DD} = 15V, V_O = 1.5V or 13.5V		4.0			4.0		4.0	V
V_{IH}	High Level Input Voltage	$\|I_O\|$ < 1.0μA								
		V_{DD} = 5V, V_O = 0.5V or 4.5V	3.5		3.5			3.5		V
		V_{DD} = 10V, V_O = 1.0V or 9.0V	7.0		7.0			7.0		V
		V_{DD} = 15V, V_O = 1.5V or 13.5V	11.0		11.0			11.0		V
I_{OL}	Low Level Output Current (Note 3)	V_{DD} = 5V, V_O = 0.4V	0.64		0.51	0.88		0.36		mA
		V_{DD} = 10V, V_O = 0.5V	1.6		1.3	2.25		0.9		mA
		V_{DD} = 15V, V_O = 1.5V	4.2		3.4	8.8		2.4		mA
I_{OH}	High Level Output Current (Note 3)	V_{DD} = 5V, V_O = 4.6V	−0.64		−0.51	−0.88		−0.36		mA
		V_{DD} = 10V, V_O = 9.5V	−1.6		−1.3	−2.25		−0.9		mA
		V_{DD} = 15V, V_O = 13.5V	−4.2		−3.4	−8.8		−2.4		mA
I_{IN}	Input Current	V_{DD} = 15V, V_{IN} = 0V		−0.1		-10^{-5}	−0.1		−1.0	μA
		V_{DD} = 15V, V_{IN} = 15V		0.1		10^{-5}	0.1		1.0	μA

DC Electrical Characteristics CD4013BC (Note 2)

SYM	PARAMETER	CONDITIONS	−40°C		25°C			85°C		UNITS
			MIN	MAX	MIN	TYP	MAX	MIN	MAX	
I_{DD}	Quiescent Device Current	V_{DD} = 5V, V_{IN} = V_{DD} or V_{SS}		4.0			4.0		30	μA
		V_{DD} = 10V, V_{IN} = V_{DD} or V_{SS}		8.0			8.0		60	μA
		V_{DD} = 15V, V_{IN} = V_{DD} or V_{SS}		16.0			16.0		120	μA
V_{OL}	Low Level Output Voltage	$\|I_O\|$ < 1.0μA								
		V_{DD} = 5V		0.05			0.05		0.05	V
		V_{DD} = 10V		0.05			0.05		0.05	V
		V_{DD} = 15V		0.05			0.05		0.05	V
V_{OH}	High Level Output Voltage	$\|I_O\|$ < 1.0μA								
		V_{DD} = 5V	4.95		4.95			4.95		V
		V_{DD} = 10V	9.95		9.95			9.95		V
		V_{DD} = 15V	14.95		14.95			14.95		V
V_{IL}	Low Level Input Voltage	$\|I_O\|$ < 1.0μA								
		V_{DD} = 5V, V_O = 0.5V or 4.5V		1.5			1.5		1.5	V
		V_{DD} = 10V, V_O = 1.0V or 9.0V		3.0			3.0		3.0	V
		V_{DD} = 15V, V_O = 1.5V or 13.5V		4.0			4.0		4.0	V

DC Electrical Characteristics (Cont'd.) CD4013BC (Note 2)

SYM	PARAMETER	CONDITIONS	−40°C		25°C			85°C		UNITS
			MIN	MAX	MIN	TYP	MAX	MIN	MAX	
V_{IH}	High Level Input Voltage	$\|I_O\| < 1.0\mu A$								
		V_{DD} = 5V, V_O = 0.5V or 4.5V	3.5		3.5			3.5		V
		V_{DD} = 10V, V_O = 1.0V or 9.0V	7.0		7.0			7.0		V
		V_{DD} = 15V, V_O = 1.5V or 13.5V	11.0		11.0			11.0		V
I_{OL}	Low Level Output Current (Note 3)	V_{DD} = 5V, V_O = 0.4V	0.52		0.44	0.88		0.36		mA
		V_{DD} = 10V, V_O = 0.5V	1.3		1.1	2.25		0.9		mA
		V_{DD} = 15V, V_O = 1.5V	3.6		3.0	8.8		2.4		mA
I_{OH}	High Level Output Current (Note 3)	V_{DD} = 5V, V_O = 4.6V	−0.52		−0.44	−0.88		−0.36		mA
		V_{DD} = 10V, V_O = 9.5V	−1.3		−1.1	−2.25		−0.9		mA
		V_{DD} = 15V, V_O = 13.5V	−3.6		−3.0	−8.8		−2.4		mA
I_{IN}	Input Current	V_{DD} = 15V, V_{IN} = 0V		−0.3		-10^{-5}	−0.3		−1.0	μA
		V_{DD} = 15V, V_{IN} = 15V		0.3		10^{-5}	0.3		1.0	μA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed, they are not meant to imply that the devices should be operated at these limits. The table of "Recommended Operating Conditions" and "Electrical Characteristics" provides conditions for actual device operation.

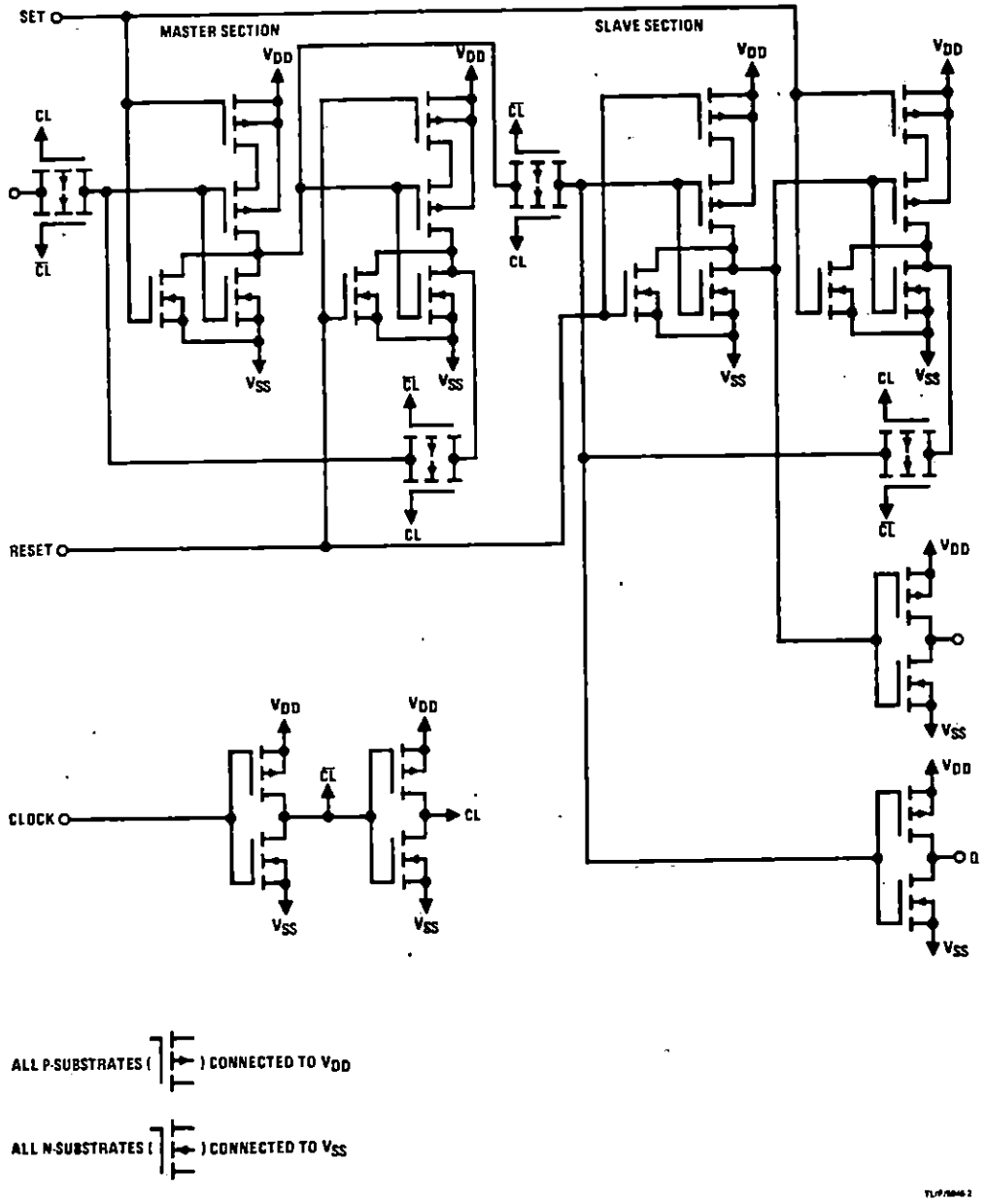
Note 2: V_{SS} = 0V unless otherwise specified.

Note 3: I_{OH} and I_{OL} are measured one output at a time.

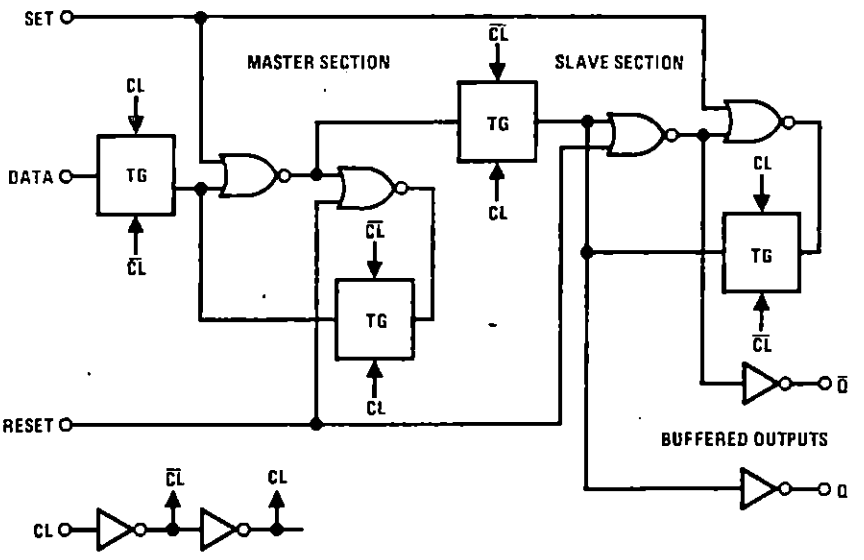
AC Electrical Characteristics $T_A = 25°C$, $C_L = 50\,pF$, $R_L = 200\,k$, unless otherwise noted

SYM	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
CLOCK OPERATION						
t_{PHL}, or t_{PLH}	Propagation Delay Time	V_{DD} = 5V		200	350	ns
		V_{DD} = 10V		80	160	ns
		V_{DD} = 15V		65	120	ns
t_{THL}, or t_{TLH}	Transition Time	V_{DD} = 5V		100	200	ns
		V_{DD} = 10V		50	100	ns
		V_{DD} = 15V		40	80	ns
t_{WL}, or t_{WH}	Minimum Clock Pulse Width	V_{DD} = 5V		100	200	ns
		V_{DD} = 10V		40	80	ns
		V_{DD} = 15V		32	65	ns
t_{RCL}, t_{FCL}	Maximum Clock Rise and Fall Time	V_{DD} = 5V			15	μs
		V_{DD} = 10V			10	μs
		V_{DD} = 15V			5	μs
t_{SU}	Minimum Set-Up Time	V_{DD} = 5V		20	40	ns
		V_{DD} = 10V		15	30	ns
		V_{DD} = 15V		12	25	ns
f_{CL}	Maximum Clock Frequency	V_{DD} = 5V	2.5	5		MHz
		V_{DD} = 10V	6.2	12.5		MHz
		V_{DD} = 15V	7.6	15.5		MHz
SET AND RESET OPERATION						
$t_{PHL(R)}$, $t_{PLH(S)}$	Propagation Delay Time	V_{DD} = 5V		150	300	ns
		V_{DD} = 10V		65	130	ns
		V_{DD} = 15V		45	90	ns
$t_{WH(R)}$, $t_{WH(S)}$	Minimum Set and Reset Pulse Width	V_{DD} = 5V		90	180	ns
		V_{DD} = 10V		40	80	ns
		V_{DD} = 15V		25	50	ns
C_{IN}	Average Input Capacitance	Any Input		5	7.5	pF

Schematic Diagram

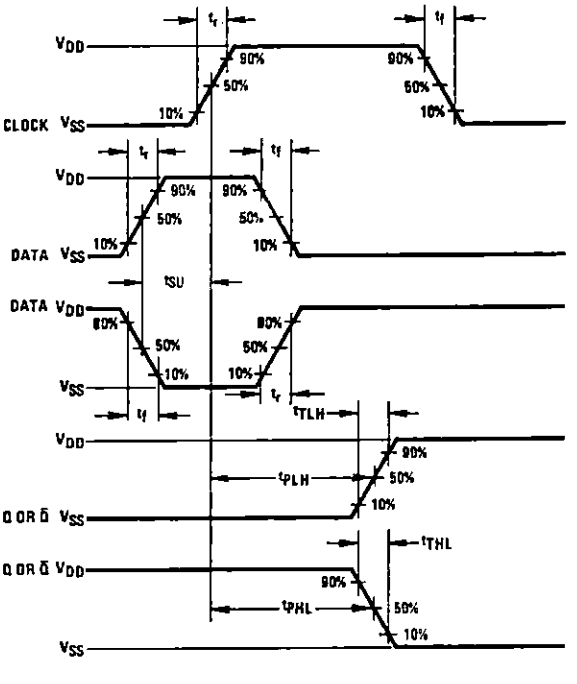


Logic Diagram



TL/F/5046-3

Switching Time Waveforms



TL/F/5046-4

National Semiconductor

Operational Amplifiers/Buffers

LM10/LM10B(L)/LM10C(L) Op Amp and Voltage Reference

General Description

The LM10 series are monolithic linear ICs consisting of a precision reference, an adjustable reference buffer and an independent, high quality op amp.

The unit can operate from a total supply voltage as low as 1.1V or as high as 40V, drawing only 270μA. A complementary output stage swings within 15 mV of the supply terminals or will deliver ±20 mA output current with ±0.4V saturation. Reference output can be as low as 200 mV. Some other characteristics of the LM10 are

■ input-offset voltage	2.0 mV (max)
■ input-offset current	0.7 nA (max)
■ input-bias current	20 nA (max)
■ reference regulation	0.1% (max)
■ offset-voltage drift	2μV/°C
■ reference drift	0.002%/°C

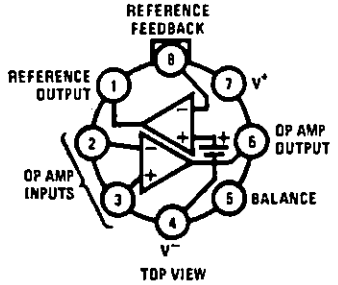
The circuit is recommended for portable equipment and is completely specified for operation from a single power cell. In contrast, high output-drive capability, both voltage and current, along with thermal overload protection, suggest it in demanding general-purpose applications.

The device is capable of operating in a floating mode, independent of fixed supplies. It can function as a remote comparator, signal conditioner, SCR controller or transmitter for analog signals, delivering the processed signal on the same line used to supply power. It is also suited for operation in a wide range of voltage- and current-regulator applications, from low voltages to several hundred volts, providing greater precision than existing ICs.

This series is available in the three standard temperature ranges, with the commercial part having relaxed limits. In addition, a low-voltage specification (suffix "L") is available in the limited temperature ranges at a cost savings.

Connection and Functional Diagrams

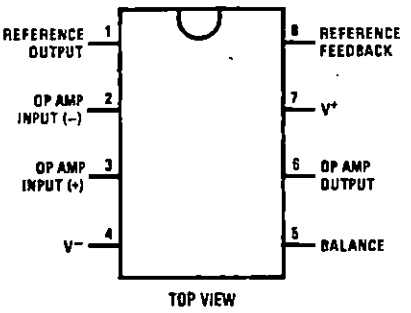
Metal Can Package (H)



TOP VIEW

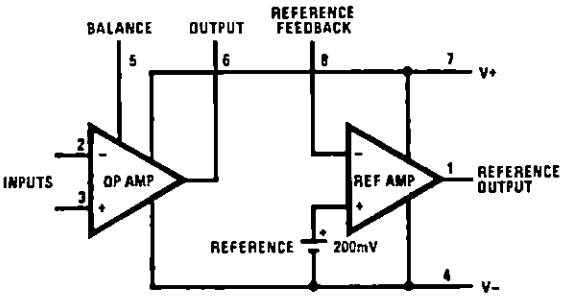
Order Number LM10H, LM10BH, LM10CH, LM10BLH or LM10CLH
See NS Package H08A

Dual-In-Line Package (N)



TOP VIEW

Order Number LM10CN or LM10CLN See NS Package N08B



Absolute Maximum Ratings

	LM10/LM10B/LM10C	LM10BL/LM10CL
Total supply voltage	45V	7V
Differential input voltage (note 1)	±40V	±7V
Power dissipation (note 2)	internally limited	
Output short-circuit duration (note 3)	indefinite	
Storage-temperature range	−55°C to +150°C	
Lead temperature (soldering, 10s)	300°C	

Electrical Characteristics (T_J = 25 C, $T_{MIN} \leq T_J \leq T_{MAX}$, note 4)

(Boldface type refers to limits over temperature range.)

PARAMETER	CONDITIONS	LM10/LM10B			LM10C			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Input offset voltage			0.3	2.0 3.0		0.5	4.0 5.0	mV mV
Input offset current (note 5)			0.25	0.7 1.5		0.4	2.0 3.0	nA nA
Input bias current			10	20 30		12	30 40	nA nA
Input resistance		250 150	500		150 115	400		kΩ kΩ
Large signal voltage gain	V_S = ±20V, I_{OUT} = 0 V_{OUT} = ±19.95V	120 80	400		80 50	400		V/mV V/mV
	V_S = ±20V, V_{OUT} = ±19.4V I_{OUT} = ±20 mA (±15 mA)	50 20	130		25 15	130		V/mV V/mV
	V_S = ±0.6V (0.65V), I_{OUT} = ±2 mA V_{OUT} = ±0.4V (±0.3V), V_{CM} = −0.4V	1.5 0.5	3.0		1.0 0.75	3.0		V/mV V/mV
Shunt gain (note 6)	1.2V (1.3V) ≤ V_{OUT} ≤ 40V, R_L = 1.1 kΩ	14	33		10	33		V/mV
	0.1 mA ≤ I_{OUT} ≤ 5 mA	6			6			V/mV
	1.5V ≤ V^+ ≤ 40V, R_L = 250Ω 0.1 mA ≤ I_{OUT} ≤ 20 mA	8 4	25		6 4	25		V/mV V/mV
Common-mode rejection	−20V ≤ V_{CM} ≤ 19.15V (19V) V_S = ±20V	93 87	102		90 87	102		dB dB
Supply-voltage rejection	−0.2V ≥ V^- ≥ −39V V^+ = 1.0V (1.1V)	90 84	96		87 84	96		dB dB
	1.0V (1.1V) ≤ V^+ ≤ 39.8V V^- = −0.2V	96 90	106		93 90	106		dB dB
Offset voltage drift			2.0			5.0		µV/°C
Offset current drift			2.0			5.0		pA/°C
Bias current drift	T_C < 100°C		60			90		pA/°C
Line regulation	1.2V (1.3V) ≤ V_S ≤ 40V 0 ≤ I_{REF} ≤ 1.0 mA, V_{REF} = 200 mV		0.001	0.003 0.006		0.001	0.008 0.01	%/V %/V
Load regulation	0 ≤ I_{REF} ≤ 1.0 mA $V^+ - V_{REF}$ ≥ 1.0V (1.1V)		0.01	0.1 0.15		0.01	0.15 0.2	% %
Amplifier gain	0.2V ≤ V_{REF} ≤ 35V	50 23	75		25 15	70		V/mV V/mV
Feedback sense voltage		195 194	200	205 206	190 189	200	210 211	mV mV
Feedback current			20	50 65		22	75 90	nA nA
Reference drift			0.002			0.003		%/°C
Supply current			270	400 500		300	500 570	µA µA
Supply current change	1.2V (1.3V) ≤ V_S ≤ 40V		15	75		15	75	µA

Electrical Characteristics ($T_J = 25°C$, $T_{MIN} \leq T_J \leq T_{MAX}$, note 4)

(Boldface type refers to limits over temperature range.)

PARAMETER	CONDITIONS	LM10BL			LM10CL			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Input offset voltage			0.3	2.0 3.0		0.5	4.0 5.0	mV mV
Input offset current (note 5)			0.1	0.7 1.5		0.2	2.0 3.0	nA nA
Input bias current			10	20 30		12	30 40	nA nA
Input resistance		250 150	500		150 115	400		kΩ kΩ
Large signal voltage gain	$V_S = \pm 3.25V$, $I_{OUT} = 0$ $V_{OUT} = \pm 3.2V$	60 40	300		40 25	300		V/mV V/mV
	$V_S = \pm 3.25V$, $I_{OUT} = 10$ mA $V_{OUT} = \pm 2.75V$	10 4	25		5 3	25		V/mV V/mV
	$V_S = \pm 0.6V$ (0.65V), $I_{OUT} = \pm 2$ mA $V_{OUT} = \pm 0.4V$ ($\pm 0.3V$), $V_{CM} = -0.4V$	1.5 0.5	3.0		1.0 0.75	3.0		V/mV V/mV
Shunt gain (note 6)	$1.5V \leq V^+ \leq 6.5V$, $R_L = 500\Omega$ $0.1\text{ mA} \leq I_{OUT} \leq 10$ mA	8 4	30		6 4	30		V/mV V/mV
Common-mode rejection	$-3.25V \leq V_{CM} \leq 2.4V$ (2.25V) $V_S = \pm 3.25V$	89 83	102		80 74	102		dB dB
Supply-voltage rejection	$-0.2V \geq V^- \geq -5.4V$ $V^+ = 1.0V$ (1.2V)	86 80	96		80 74	96		dB dB
	$1.0V$ (1.1V) $\leq V^+ \leq 6.3V$ $V^- = 0.2V$	94 88	106		80 74	106		dB dB
Offset voltage drift			2.0			5.0		μV/°C
Offset current drift			2.0			5.0		pA/°C
Bias current drift			60			90		pA/°C
Line regulation	$1.2V$ (1.3V) $\leq V_S \leq 6.5V$ $0 \leq I_{REF} \leq 0.5$ mA, $V_{REF} = 200$ mV		0.001	0.01 0.02		0.001	0.02 0.03	%/V %/V
Load regulation	$0 \leq I_{REF} \leq 0.5$ mA $V^+ - V_{REF} \geq 1.0V$ (1.1V)		0.01	0.1 0.15		0.01	0.15 0.2	% %
Amplifier gain	$0.2V \leq V_{REF} \leq 5.5V$	30 20	70		20 15	70		V/mV V/mV
Feedback sense voltage		195 194	200	205 206	190 189	200	210 211	mV mV
Feedback current			20	50 65		22	75 90	nA nA
Reference drift			0.002			0.003		%/°C
Supply current			260	400 500		280	500 570	μA μA

Note 1: The input voltage can exceed the supply voltages provided that the voltage from the input to any other terminal does not exceed the maximum differential input voltage and excess dissipation is accounted for when $V_{IN} < V^-$.

Note 2: The maximum, operating-junction temperature is 150°C for the LM10, 100°C for the LM10B(L) and 85°C for the LM10C(L). At elevated temperatures, devices must be derated based on package thermal resistance.

Note 3: Internal thermal limiting prevents excessive heating that could result in sudden failure, but the IC can be subjected to accelerated stress with a shorted output and worst-case conditions.

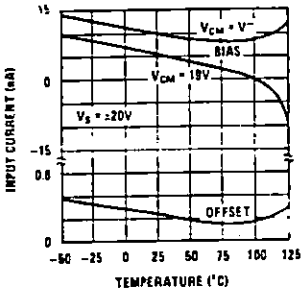
Note 4: These specifications apply for $V^- \leq V_{CM} \leq V^+ - 0.85V$ (1.0V), $1.2V$ (1.3V) $< V_S \leq V_{MAX}$, $V_{REF} = 0.2V$ and $0 \leq I_{REF} \leq 1.0$ mA, unless otherwise specified: $V_{MAX} = 40V$ for the standard part and 6.5V for the low voltage part. Normal typeface indicates 25°C limits. Boldface type indicates limits and altered test conditions for full-temperature-range operation; this is -55°C to 125°C for the LM10, -25°C to 85°C for the LM10B(L) and 0°C to 70°C for the LM10C(L). The specifications do not include the effects of thermal gradients ($\tau_1 \cong 20$ ms), die heating ($\tau_2 \cong 0.2$s) or package heating. Gradient effects are small and tend to offset the electrical error (see curves).

Note 5: For $T_J > 90°C$, I_{OS} may exceed 1.5 nA for $V_{CM} = V^-$. With $T_J = 125°C$ and $V^- \leq V_{CM} \leq V^- + 0.1V$, $I_{OS} \leq 5$ nA.

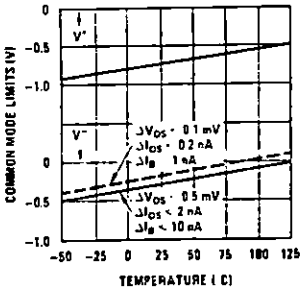
Note 6: This defines operation in floating applications such as the bootstrapped regulator or two-wire transmitter. Output is connected to the V^+ terminal of the IC and input common mode is referred to V^- (see typical applications). Effect of larger output-voltage swings with higher load resistance can be accounted for by adding the positive-supply rejection error.

Typical Performance Characteristics (Op Amp)

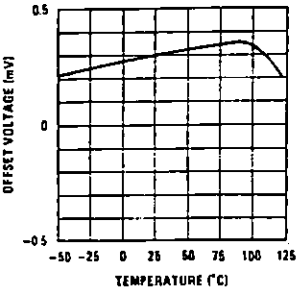
input current



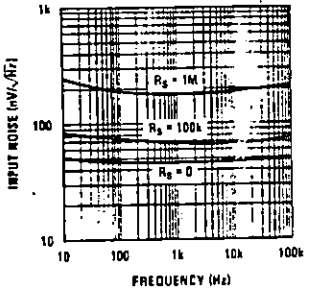
common mode limits



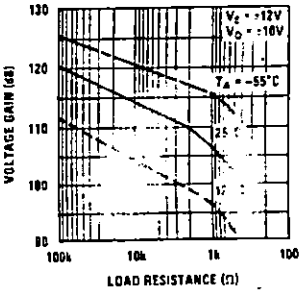
offset voltage drift



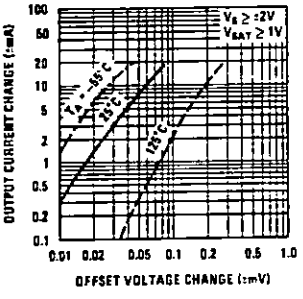
input noise voltage



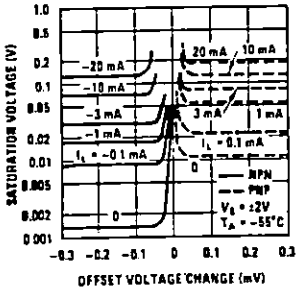
dc voltage gain



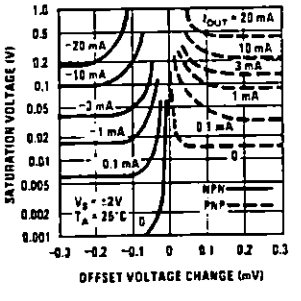
transconductance



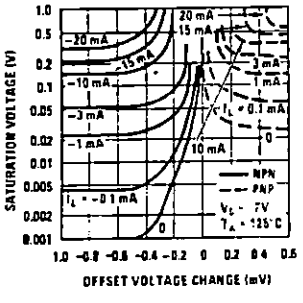
output saturation characteristics



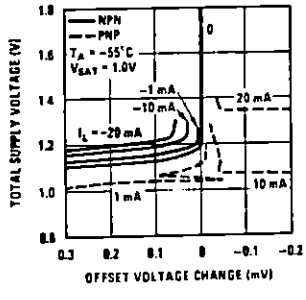
output saturation characteristics



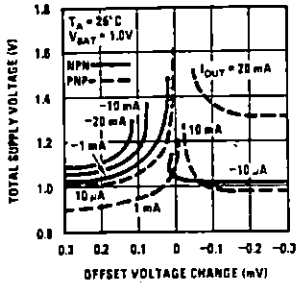
output saturation characteristics



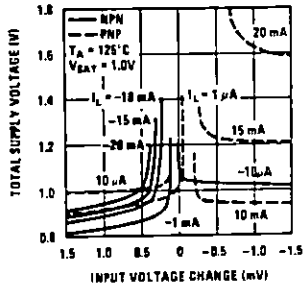
minimum supply voltage



minimum supply voltage

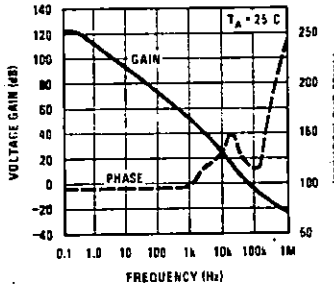


minimum supply voltage

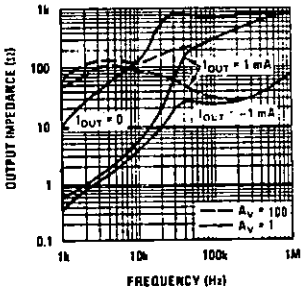


Typical Performance Characteristics (Op Amp)

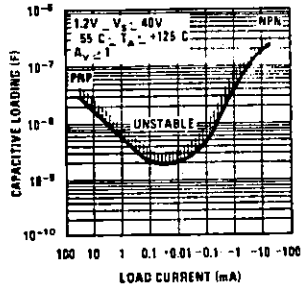
frequency response



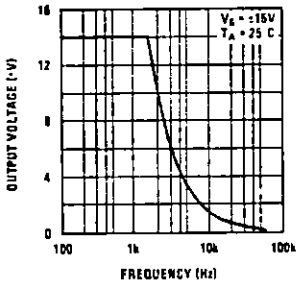
output impedance



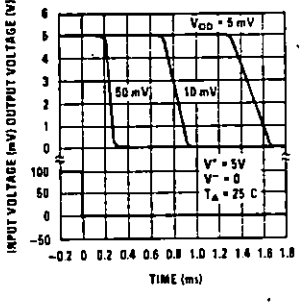
typical stability range



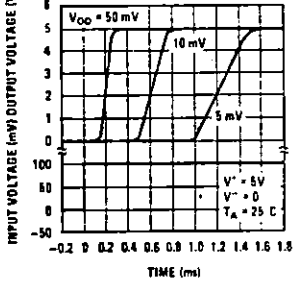
large signal response



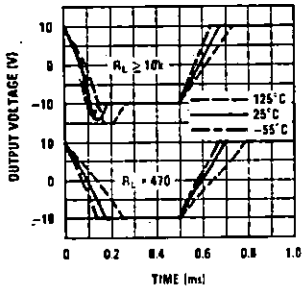
comparator response time for various input overdrives



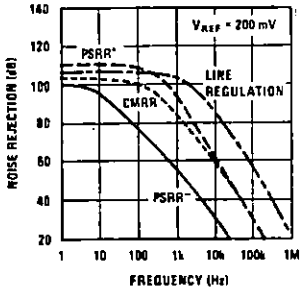
comparator response time for various input overdrives



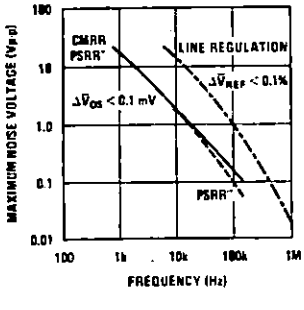
follower pulse response



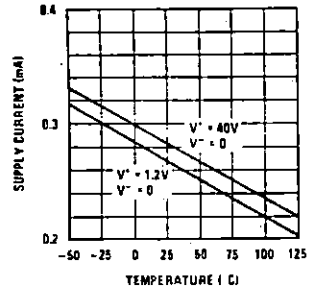
noise rejection



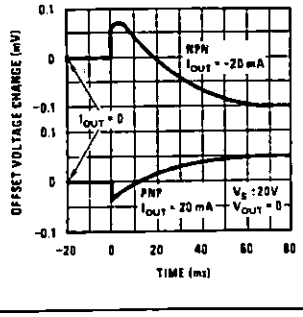
rejection slew limiting



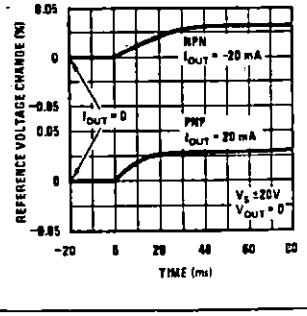
supply current



thermal gradient feedback

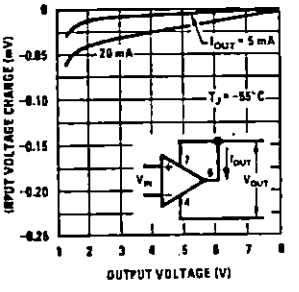


thermal gradient cross-coupling

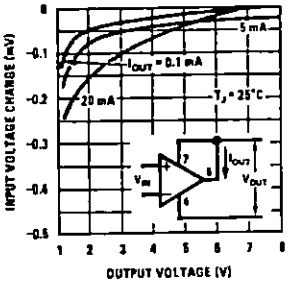


Typical Performance Characteristics (Op Amp)

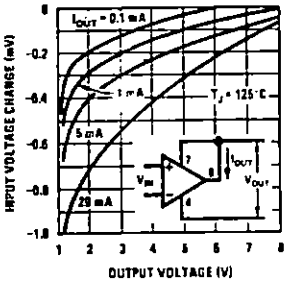
shunt gain



shunt gain

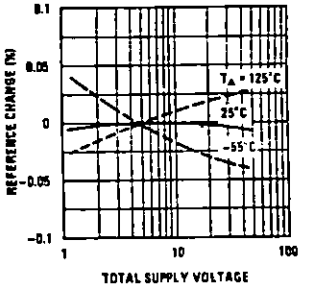


shunt gain

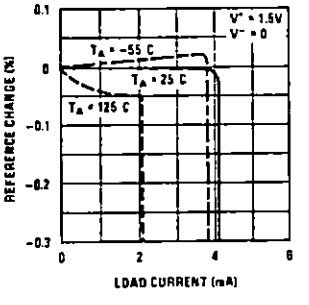


Typical Performance Characteristics (Reference)

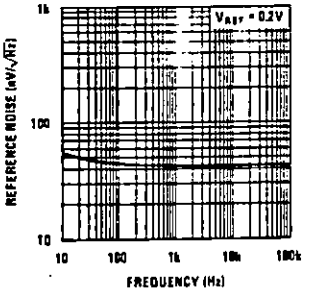
line regulation



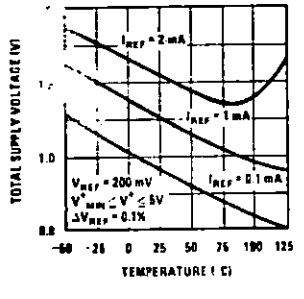
load regulation



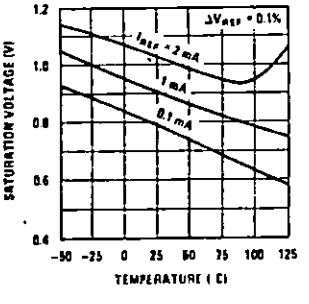
reference noise voltage



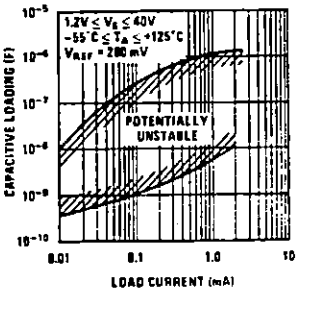
minimum supply voltage



output saturation



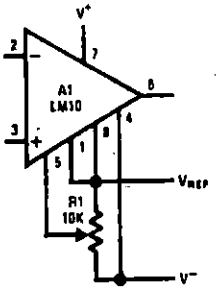
typical stability range



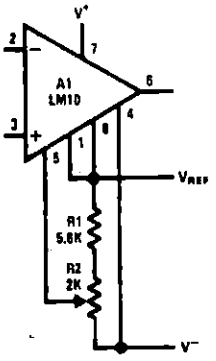
Typical Applications††

op amp offset adjustment

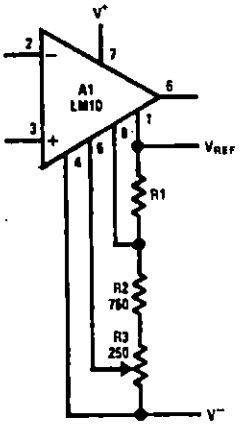
standard



limited range

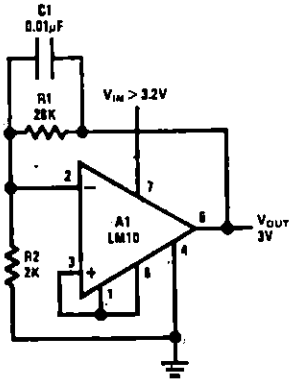


limited range with boosted reference

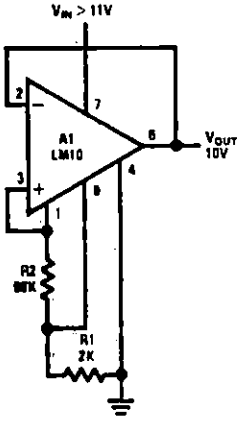


positive regulators†

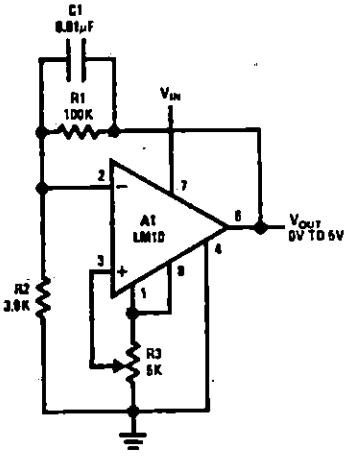
low voltage



best regulation



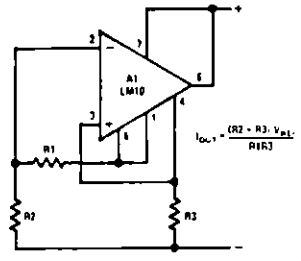
zero output



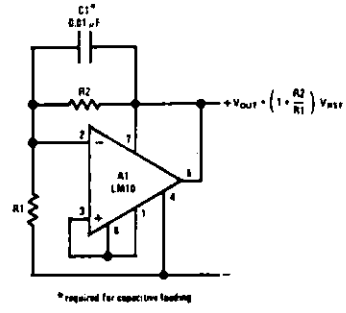
†Use only electrolytic output capacitors.
††Circuit descriptions available in application note AN-211.

Typical Applications ††

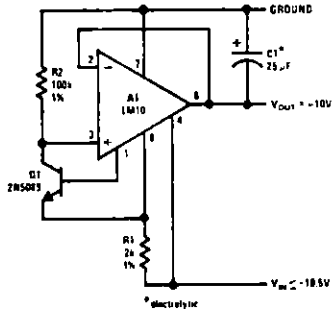
current regulator



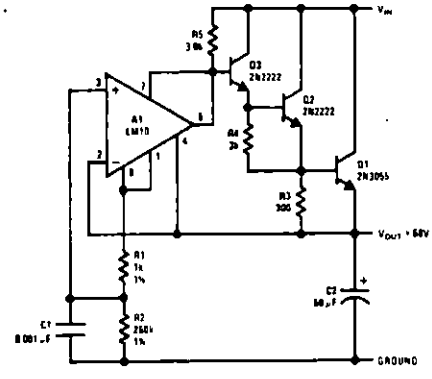
shunt regulator



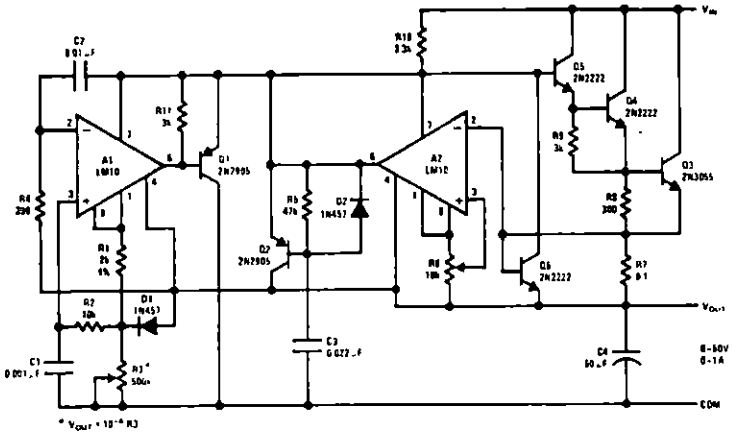
negative regulator



precision regulator



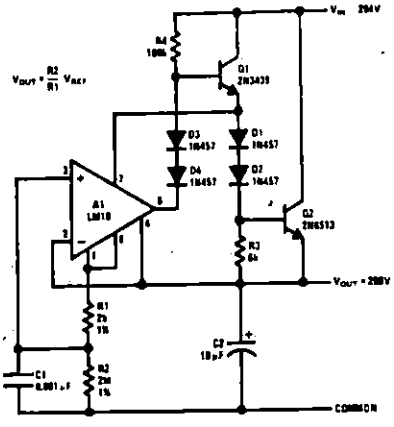
laboratory power supply



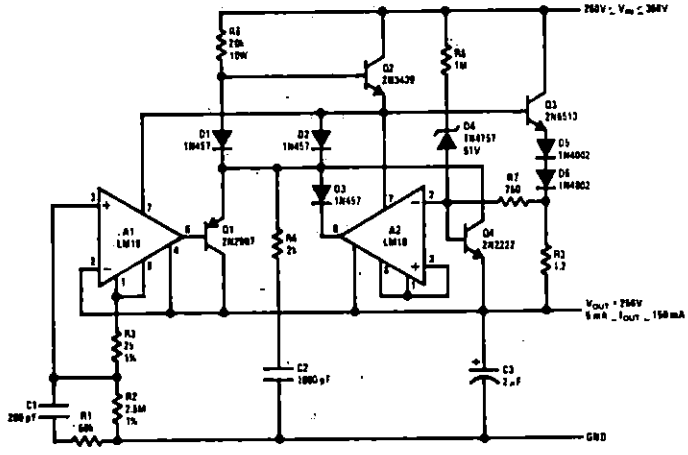
††Circuit descriptions available in application note AN 211.

Typical Applications††

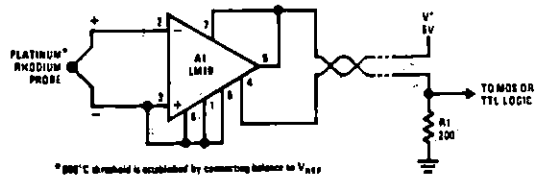
hv regulator



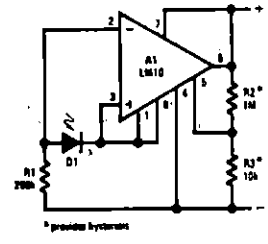
protected hv regulator



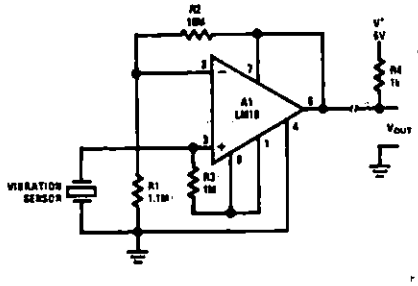
flame detector



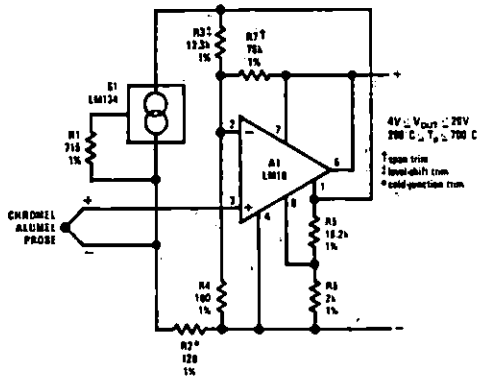
light level sensor



remote amplifier



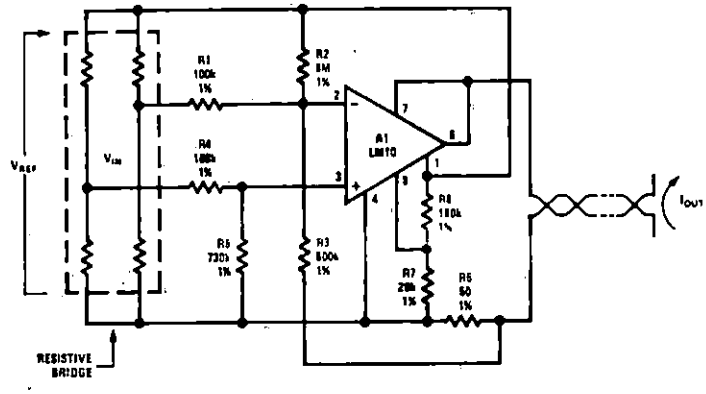
remote thermocouple amplifier



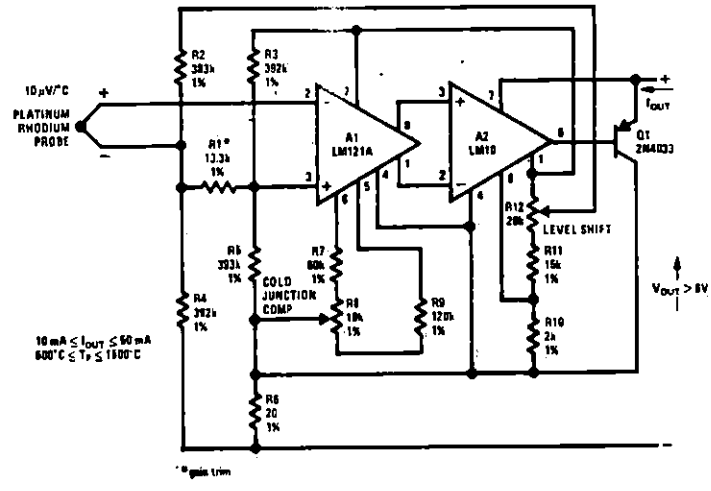
††Circuit descriptions available in application note AN-211.

Typical Applications ††

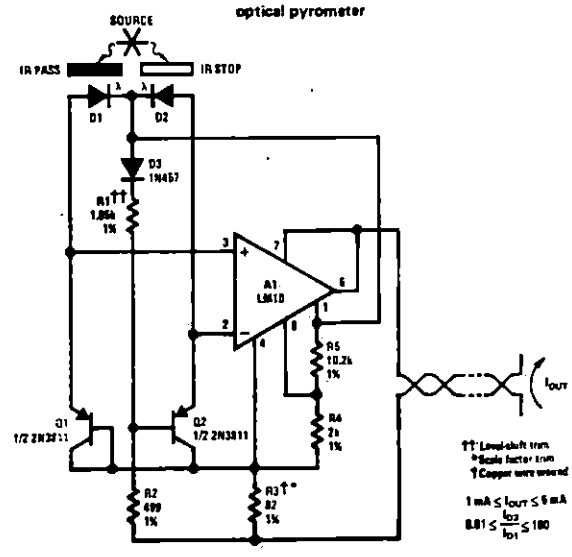
transmitter for bridge sensor



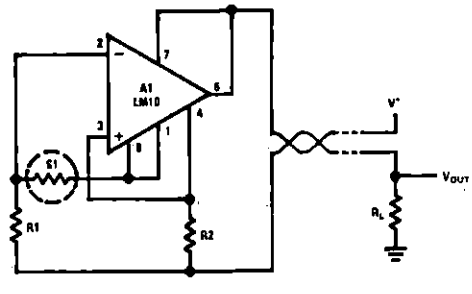
precision thermocouple transmitter



optical pyrometer



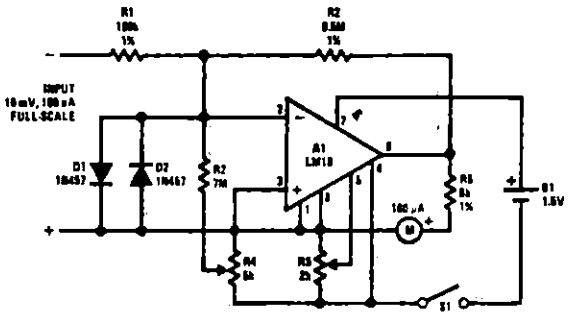
resistance thermometer transmitter



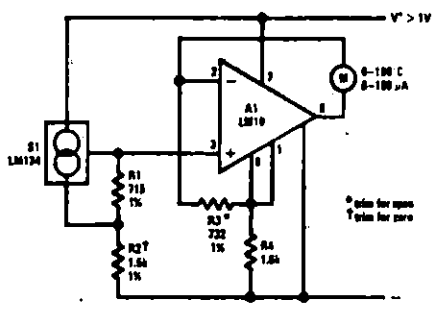
††Circuit descriptions available in application note AN-211.

Typical Applications ††

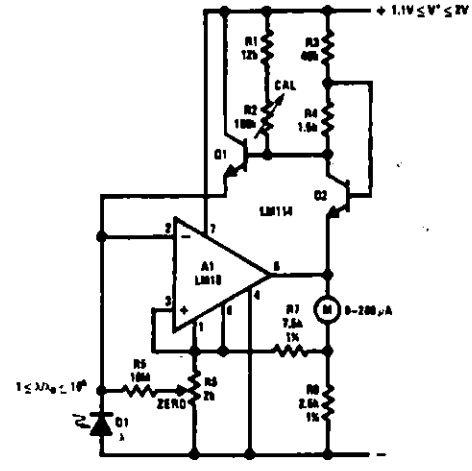
meter amplifier



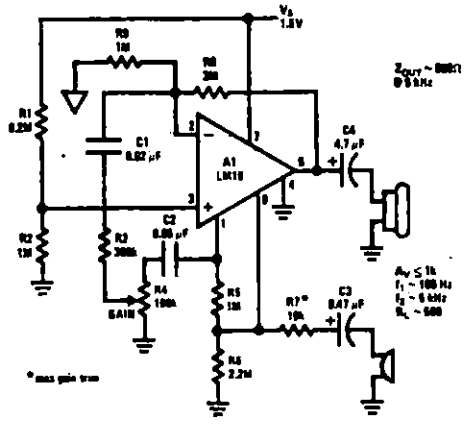
thermometer



light meter



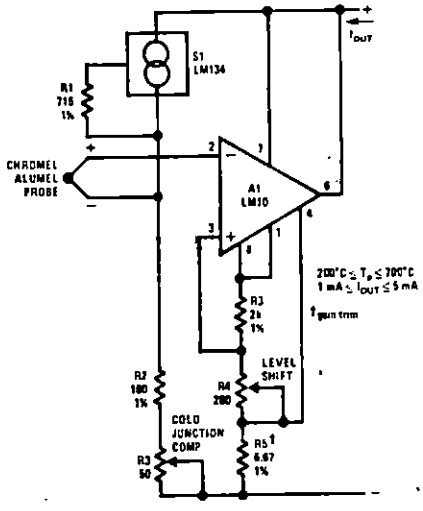
microphone amplifier



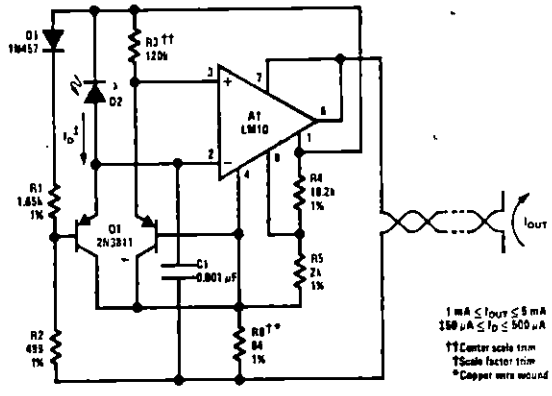
††Circuit descriptions available in application note AN-211.

Typical Applications ††

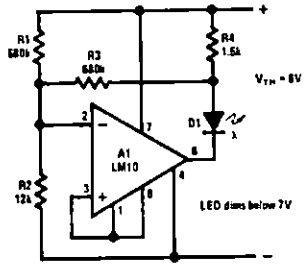
thermocouple transmitter



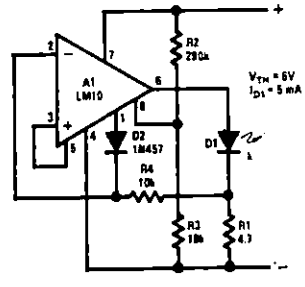
logarithmic light sensor



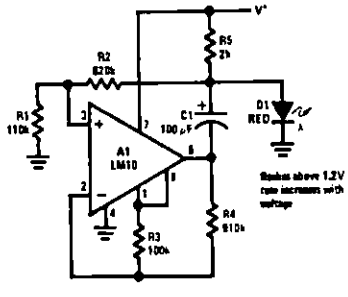
battery-level indicator



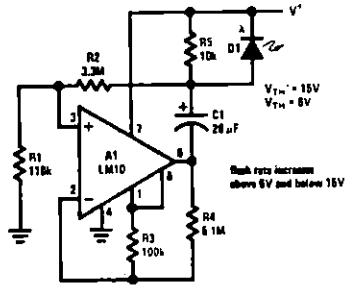
battery-threshold indicator



single-cell voltage monitor



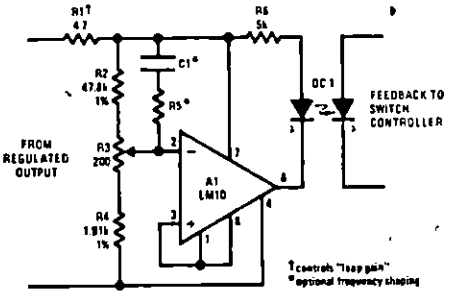
double-ended voltage monitor



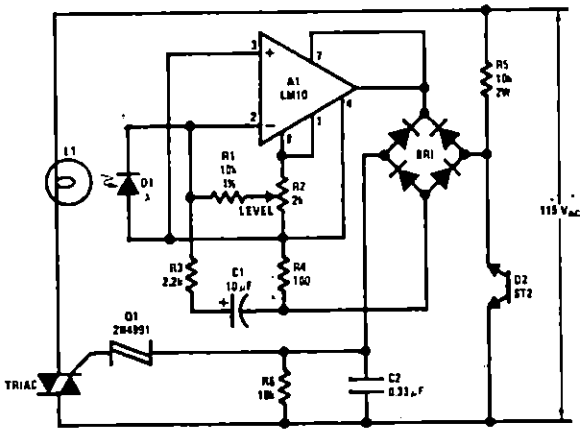
††Circuit descriptions available in application note AN-211.

Typical Applications ††

isolated voltage sensor



light-level controller



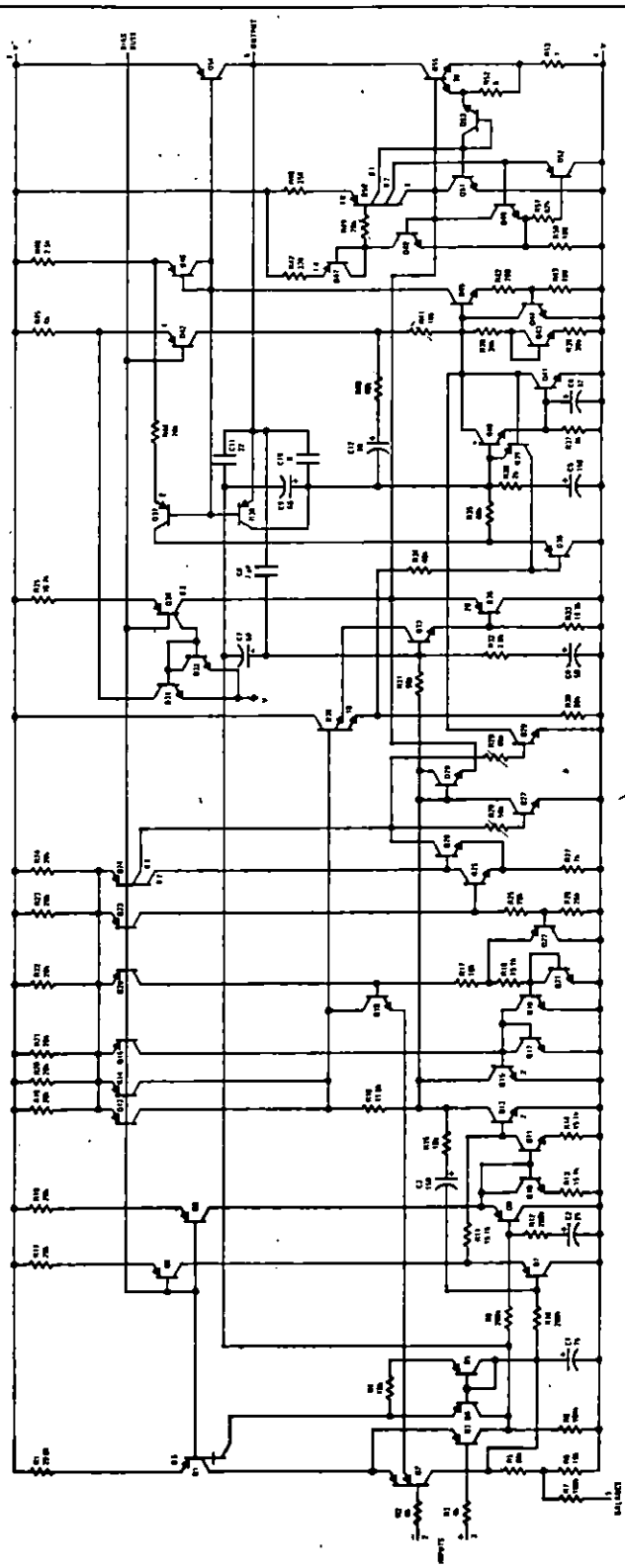
††Circuit descriptions available in application note AN-211.

Application Hints

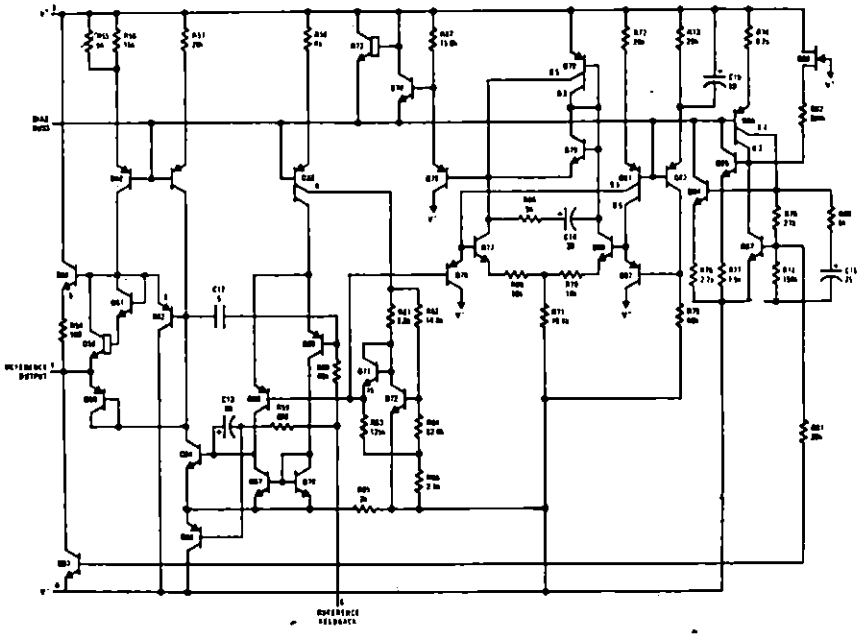
With heavy amplifier loading to V^-, resistance drops in the V^- lead can adversely affect reference regulation. Lead resistance can approach 1Ω. Therefore, the common to the reference circuitry should be connected as close as possible to the package.

LM10/LM10B(L)/LM10C(L)

Operational Amplifier Schematic



Reference and Internal Regulator



Definition of Terms

Input offset voltage: That voltage which must be applied between the input terminals to bias the unloaded output in the linear region.

Input offset current: The difference in the currents at the input terminals when the output is unloaded in the linear region.

Input bias current: The absolute value of the average of the two input currents.

Input resistance: The ratio of the change in input voltage to the change in input current on either input with the other grounded.

Large signal voltage gain: The ratio of the specified output voltage swing to the change in differential input voltage required to produce it.

Shunt gain: The ratio of the specified output voltage swing to the change in differential input voltage required to produce it with output tied to the V^+ terminal of the IC. The load and power source are connected between the V^- and V^- terminals, and input common-mode is referred to V^- terminal.

Common-mode rejection: The ratio of the input voltage range to the change in offset voltage between the extremes.

Supply-voltage rejection: The ratio of the specified supply-voltage change to the change in offset voltage between the extremes.

Line regulation: The average change in reference output voltage over the specified supply voltage range.

Load regulation: The change in reference output voltage from no load to that load specified.

Feedback sense voltage: The voltage, referred to V^-, on the reference feedback terminal while operating in regulation.

Reference amplifier gain: The ratio of the specified reference output change to the change in feedback sense voltage required to produce it.

Feedback current: The absolute value of the current at the feedback terminal when operating in regulation.

Supply current: The current required from the power source to operate the amplifier and reference with their outputs unloaded and operating in the linear range.

LM124/LM224/LM324, LM124A/
LM224A/LM324A, LM2902

National Semiconductor

Operational Amplifiers/Buffers

LM124/LM224/LM324, LM124A/LM224A/LM324A, LM2902 Low Power Quad Operational Amplifiers

General Description

The LM124 series consists of four independent, high gain, internally frequency compensated operational amplifiers which were designed specifically to operate from a single power supply over a wide range of voltages. Operation from split power supplies is also possible and the low power supply current drain is independent of the magnitude of the power supply voltage.

Application areas include transducer amplifiers, dc gain blocks and all the conventional op amp circuits which now can be more easily implemented in single power supply systems. For example, the LM124 series can be directly operated off of the standard +5 V_{DC} power supply voltage which is used in digital systems and will easily provide the required interface electronics without requiring the additional ±15 V_{DC} power supplies.

Unique Characteristics

- In the linear mode the input common-mode voltage range includes ground and the output voltage can also swing to ground, even though operated from only a single power supply voltage.
- The unity gain cross frequency is temperature compensated.
- The input bias current is also temperature compensated.

Advantages

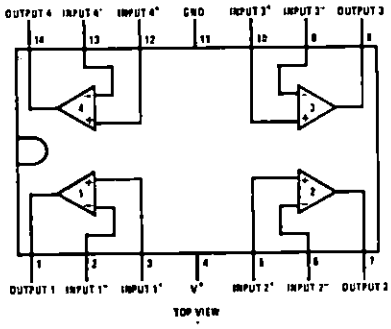
- Eliminates need for dual supplies
- Four internally compensated op amps in a single package
- Allows directly sensing near GND and V_{OUT} also goes to GND
- Compatible with all forms of logic
- Power drain suitable for battery operation

Features

- Internally frequency compensated for unity gain
- Large dc voltage gain — 100 dB
- Wide bandwidth (unity gain) (temperature compensated) — 1 MHz
- Wide power supply range:
  - Single supply — 3 V_{DC} to 30 V_{DC}
  - or dual supplies — ±1.5 V_{DC} to ±15 V_{DC}
- Very low supply current drain (800μA) — essentially independent of supply voltage (1 mW/op amp at +5 V_{DC})
- Low input biasing current (temperature compensated) — 45 nA_{DC}
- Low input offset voltage — 2 mV_{DC}
- and offset current — 5 nA_{DC}
- Input common-mode voltage range includes ground
- Differential input voltage range equal to the power supply voltage
- Large output voltage swing — 0 V_{DC} to V^+ − 1.5 V_{DC}

Connection Diagram

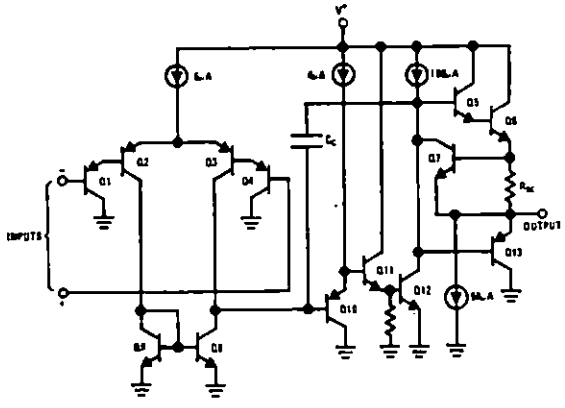
Dual-In-Line Package



Order Number LM124J, LM124AJ, LM224J, LM224AJ, LM324J, LM324AJ or LM2902J
See NS Package J14A

Order Number LM324N, LM324AN or LM2902N
See NS Package N14A

Schematic Diagram (Each Amplifier)



Absolute Maximum Ratings

	LM124/LM224/LM324 LM124A/LM224A/LM324A	LM2902
Supply Voltage, V^+	32 V_{DC} or ±16 V_{DC}	26 V_{DC} or ±13 V_{DC}
Differential Input Voltage	32 V_{DC}	26 V_{DC}
Input Voltage	−0.3 V_{DC} to +26 V_{DC}	−0.3 V_{DC} to +26 V_{DC}
Power Dissipation (Note 1)		
Molded DIP	570 mW	570 mW
Cavity DIP	900 mW	
Flat Pack	800 mW	
Output Short-Circuit to GND (One Amplifier) (Note 2) $V^+ \leq 15\ V_{DC}$ and $T_A = 25°C$	Continuous	Continuous

	LM124/LM224/LM324 LM124A/LM224A/LM324A	LM2902
Input Current ($V_{IN} < -0.3\ V_{DC}$) (Note 3)	50 mA	50 mA
Operating Temperature Range		−40°C to +85°C
LM324/LM324A	0°C to +70°C	
LM224/LM224A	−25°C to +85°C	
LM124/LM124A	−55°C to +125°C	
Storage Temperature Range	−65°C to +150°C	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C	300°C

Electrical Characteristics ($V^+ = +5.0\ V_{DC}$, Note 4)

PARAMETER	CONDITIONS	LM124A			LM224A			LM324A			LM124/LM224			LM324			LM2902			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	$T_A = 25°C$, (Note 5)		1	2		1	3		2	3		±2	±5		±2	±7		±2	±7	mV_{DC}
Input Bias Current (Note 6)	$I_{IN(+)}$ or $I_{IN(-)}$, $T_A = 25°C$		20	50		40	80		45	100		45	150		45	250		45	250	nA_{DC}
Input Offset Current	$I_{IN(+)} - I_{IN(-)}$, $T_A = 25°C$		2	10		2	15		5	30		±3	±30		±5	±50		±5	±50	nA_{DC}
Input Common-Mode Voltage Range (Note 7)	$V^+ = 30\ V_{DC}$, $T_A = 25°C$	0		$V^+-1.5$	0		$V^+-1.5$	0		$V^+-1.5$	0		$V^+-1.5$	0		$V^+-1.5$	0		$V^+-1.5$	V_{DC}
Supply Current	$R_L = \infty$, $V_{CC} = 30V$, (LM2902 $V_{CC} = 26V$)		1.5	3		1.5	3		1.5	3		1.5	3		1.5	3		1.5	3	mA_{DC}
	$R_L = \infty$ On All Op Amps Over Full Temperature Range		0.7	1.2		0.7	1.2		0.7	1.2		0.7	1.2		0.7	1.2		0.7	1.2	mA_{DC}
Large Signal Voltage Gain	$V^+ = 15\ V_{DC}$ (For Large V_O Swing) $R_L \geq 2\ k\Omega$, $T_A = 25°C$	50	100		50	100		25	100		50	100		25	100			100		V/mV
Output Voltage Swing	$R_L = 2\ k\Omega$, $T_A = 25°C$ (LM2902 $R_L \geq 10\ k\Omega$)	0		$V^+-1.5$	0		$V^+-1.5$	0		$V^+-1.5$	0		$V^+-1.5$	0		$V^+-1.5$	0		$V^+-1.5$	V_{DC}
Common-Mode Rejection Ratio	DC, $T_A = 25°C$	70	85		70	85		65	85		70	85		65	70		50	70		dB
Power Supply Rejection Ratio	DC, $T_A = 25°C$	65	100		65	100		65	100		65	100		65	100		50	100		dB
Amplifier-to-Amplifier Coupling (Note 8)	f = 1 kHz to 20 kHz, $T_A = 25°C$ (Input Referred)		−120			−120			−120			−120			−120			−120		dB
Output Current																				
Source	$V_{IN}^+ = 1\ V_{DC}$, $V_{IN}^- = 0\ V_{DC}$, $V^+ = 15\ V_{DC}$, $T_A = 25°C$	20	40		20	40		20	40		20	40		20	40		20	40		mA_{DC}
Sink	$V_{IN}^- = 1\ V_{DC}$, $V_{IN}^+ = 0\ V_{DC}$, $V^+ = 15\ V_{DC}$, $T_A = 25°C$	10	20		10	20		10	20		10	20		10	20		10	20		mA_{DC}
	$V_{IN}^- = 1\ V_{DC}$, $V_{IN}^+ = 0\ V_{DC}$, $T_A = 25°C$, $V_O = 200\ mV_{DC}$	12	50		12	50		12	50		12	50		12	50					μA
Short Circuit to Ground	$T_A = 25°C$, (Note 2)		40	60		40	60		40	60		40	60		40	60		40	60	mA_{DC}

Electrical Characteristics (Continued)

PARAMETER	CONDITIONS	LM124A			LM224A			LM324A			LM124/LM224			LM324			LM2902			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	(Note 5)			4			4			5			±7			±9			±10	mV_{DC}
Input Offset Voltage Drift	$R_S = 0\Omega$		7	20		7	20		7	30		7			7			7		$\mu V/^\circ C$
Input Offset Current	$I_{IN(+)} - I_{IN(-)}$			30			30			75			±100			±150		45	±200	nA_{DC}
Input Offset Current Drift			10	200		10	200		10	300		10			10			10		$pA_{DC}/^\circ C$
Input Bias Current	$I_{IN(+)}$ or $I_{IN(-)}$		40	100		40	100		40	200		40	300		40	500		40	500	nA_{DC}
Input Common-Mode Voltage Range (Note 7)	$V^+ = 30\ V_{DC}$	0		V^+-2	0		V^+-2	0		V^+-2	0		V^+-2	0		V^+-2	0		V^+-2	V_{DC}
Large Signal Voltage Gain	$V^+ = +15\ V_{DC}$ (For Large V_O Swing) $R_L \geq 2\ k\Omega$	25			25			15			25			15			15			V/mV
Output Voltage Swing V_{OH}	$V^+ = +30\ V_{DC}$, $R_L = 2\ k\Omega$	26			26			26			26			26			22			V_{DC}
	$R_L \geq 10\ k\Omega$	27	28		27	28		27	28		27	28		27	28		23	24		V_{DC}
V_{OL}	$V^+ = 5\ V_{DC}$, $R_L \leq 10\ k\Omega$		5	20		5	20		5	20		5	20		5	20		5	100	mV_{DC}
Output Current Source	$V_{IN}^+ = +1\ V_{DC}$, $V_{IN}^- = 0\ V_{DC}$, $V^+ = 15\ V_{DC}$	10	20		10	20		10	20		10	20		10	20		10	20		mA_{DC}
Sink	$V_{IN}^- = +1\ V_{DC}$, $V_{IN}^+ = 0\ V_{DC}$, $V^+ = 15\ V_{DC}$	10	15		5	8		5	8		5	8		5	8		5	8		mA_{DC}
Differential Input Voltage	(Note 7)			32			32			32			32			32			26	V_{DC}

Note 1: For operating at high temperatures, the LM324/LM324A, LM2902 must be derated based on a +125°C maximum junction temperature and a thermal resistance of 175°C/W which applies for the device soldered in a printed circuit board, operating in a still air ambient. The LM224/LM224A and LM124/LM124A can be derated based on a +150°C maximum junction temperature. The dissipation is the total of all four amplifiers—use external resistors, where possible, to allow the amplifier to saturate or to reduce the power which is dissipated in the integrated circuit.

Note 2: Short circuits from the output to V^+ can cause excessive heating and eventual destruction. The maximum output current is approximately 40 mA independent of the magnitude of V^+. At values of supply voltage in excess of +15 V_{DC}, continuous short-circuits can exceed the power dissipation ratings and cause eventual destruction. Destructive dissipation can result from simultaneous shorts on all amplifiers.

Note 3: This input current will only exist when the voltage at any of the input leads is driven negative. It is due to the collector-base junction of the input PNP transistors becoming forward biased and thereby acting as input diode clamps. In addition to this diode action, there is also lateral NPN parasitic transistor action on the IC chip. This transistor action can cause the output voltages of the op amps to go to the V^+ voltage level (or to ground for a large overdrive) for the time duration that an input is driven negative. This is not destructive and normal output states will re-establish when the input voltage, which was negative, again returns to a value greater than −0.3 V_{DC} (at 25°C).

Note 4: These specifications apply for $V^+ = +5\ V_{DC}$ and −55°C ≤ T_A ≤ +125°C, unless otherwise stated. With the LM224/LM224A, all temperature specifications are limited to −25°C ≤ T_A ≤ +85°C, the LM324/LM324A temperature specifications are limited to 0°C ≤ T_A ≤ +70°C, and the LM2902 specifications are limited to −40°C ≤ T_A ≤ +85°C.

Note 5: $V_O \cong 1.4\ V_{DC}$, $R_S = 0\Omega$ with V^+ from 5 V_{DC} to 30 V_{DC}; and over the full input common-mode range (0 V_{DC} to $V^+ - 1.5\ V_{DC}$).

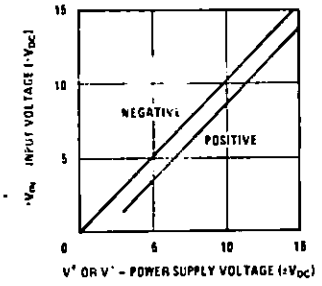
Note 6: The direction of the input current is out of the IC due to the PNP input stage. This current is essentially constant, independent of the state of the output so no loading change exists on the input lines.

Note 7: The input common-mode voltage of either input signal voltage should not be allowed to go negative by more than 0.3V (at 25°C). The upper end of the common-mode voltage range is $V^+ - 1.5V$, but either or both inputs can go to +32 V_{DC} without damage (+26 V_{DC} for LM2902).

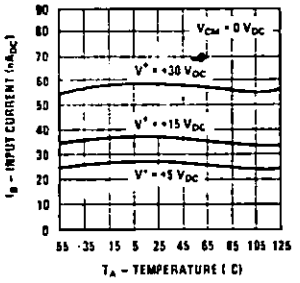
Note 8: Due to proximity of external components, insure that coupling is not originating via stray capacitance between these external parts. This typically can be detected as this type of capacitive increases at higher frequencies.

Typical Performance Characteristics

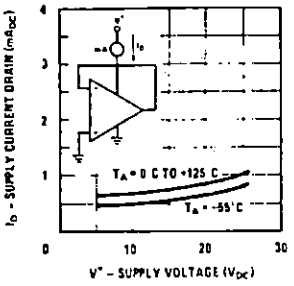
Input Voltage Range



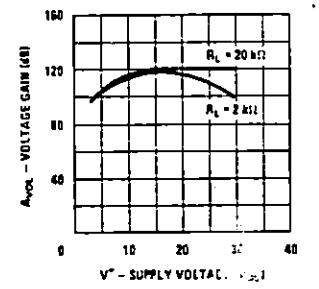
Input Current



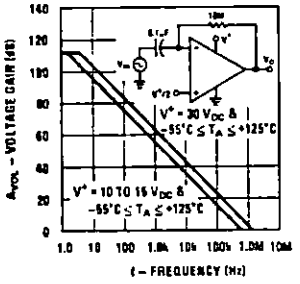
Supply Current



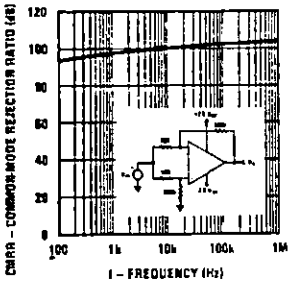
Voltage Gain



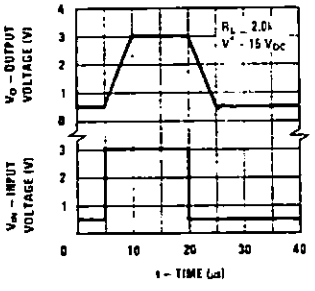
Open Loop Frequency Response



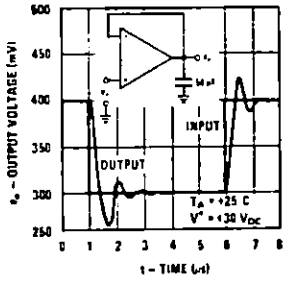
Common Mode Rejection Ratio



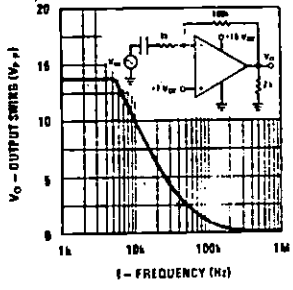
Voltage Follower Pulse Response



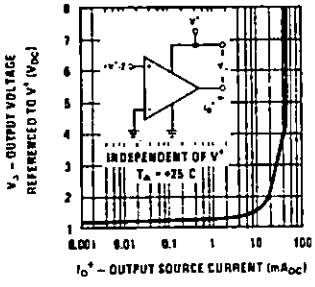
Voltage Follower Pulse Response (Small Signal)



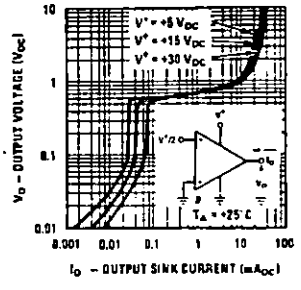
Large Signal Frequency Response



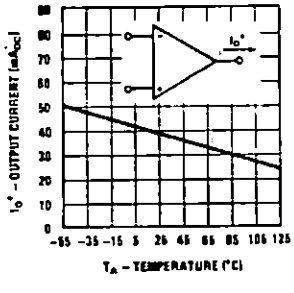
Output Characteristics Current Sourcing



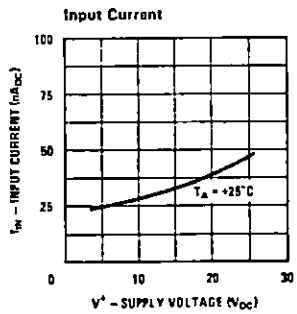
Output Characteristics Current Sinking

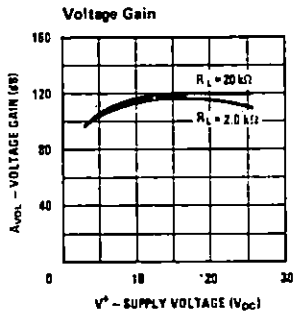


Current Limiting



Typical Performance Characteristics (LM2902 only)





Application Hints

The LM124 series are op amps which operate with only a single power supply voltage, have true-differential inputs, and remain in the linear mode with an input common-mode voltage of 0 V_{DC}. These amplifiers operate over a wide range of power supply voltage with little change in performance characteristics. At 25°C amplifier operation is possible down to a minimum supply voltage of 2.3 V_{DC}.

The pinouts of the package have been designed to simplify PC board layouts. Inverting inputs are adjacent to outputs for all of the amplifiers and the outputs have also been placed at the corners of the package (pins 1, 7, 8, and 14).

Precautions should be taken to insure that the power supply for the integrated circuit never becomes reversed in polarity or that the unit is not inadvertently installed backwards in a test socket as an unlimited current surge through the resulting forward diode within the IC could cause fusing of the internal conductors and result in a destroyed unit.

Large differential input voltages can be easily accommodated and, as input differential voltage protection diodes are not needed, no large input currents result from large differential input voltages. The differential input voltage may be larger than V^+ without damaging the device. Protection should be provided to prevent the input voltages from going negative more than −0.3 V_{DC} (at 25°C). An input clamp diode with a resistor to the IC input terminal can be used.

To reduce the power supply current drain, the amplifiers have a class A output stage for small signal levels which converts to class B in a large signal mode. This allows the amplifiers to both source and sink large output currents. Therefore both NPN and PNP external current boost transistors can be used to extend the power capability of the basic amplifiers. The output voltage needs to raise approximately 1 diode drop above ground to bias the on-chip vertical PNP transistor for output current sinking applications.

For ac applications, where the load is capacitively coupled to the output of the amplifier, a resistor should be used, from the output of the amplifier to ground to increase the class A bias current and prevent crossover distortion. Where the load is directly coupled, as in dc applications, there is no crossover distortion.

Capacitive loads which are applied directly to the output of the amplifier reduce the loop stability margin. Values of 50 pF can be accommodated using the worst-case non-inverting unity gain connection. Large closed loop gains or resistive isolation should be used if larger load capacitance must be driven by the amplifier.

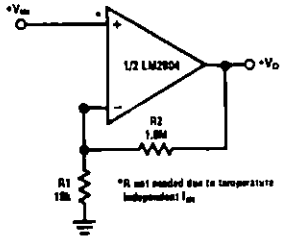
The bias network of the LM124 establishes a drain current which is independent of the magnitude of the power supply voltage over the range of from 3 V_{DC} to 30 V_{DC}.

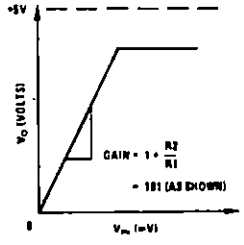
Output short circuits either to ground or to the positive power supply should be of short time duration. Units can be destroyed, not as a result of the short circuit current causing metal fusing, but rather due to the large increase in IC chip dissipation which will cause eventual failure due to excessive junction temperatures. Putting direct short-circuits on more than one amplifier at a time will increase the total IC power dissipation to destructive levels, if not properly protected with external dissipation limiting resistors in series with the output leads of the amplifiers. The larger value of output source current which is available at 25°C provides a larger output current capability at elevated temperatures (see typical performance characteristics) than a standard IC op amp.

The circuits presented in the section on typical applications emphasize operation on only a single power supply voltage. If complementary power supplies are available, all of the standard op amp circuits can be used. In general, introducing a pseudo-ground (a bias voltage reference of $V^+/2$) will allow operation above and below this value in single power supply systems. Many application circuits are shown which take advantage of the wide input common-mode voltage range which includes ground. In most cases, input biasing is not required and input voltages which range to ground can easily be accommodated.

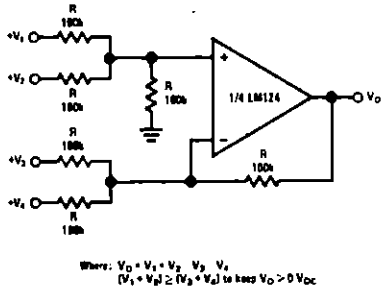
Typical Single-Supply Applications (V^+ = 5.0 V_{DC})

Non-Inverting DC Gain (0V Input = 0V Output)



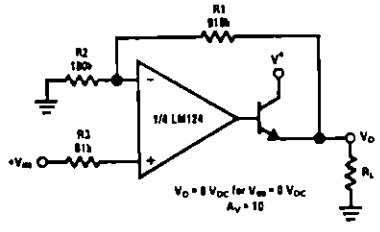


DC Summing Amplifier
(V_{IN}'S ≥ 0 V_{DC} AND V_O ≥ 0 V_{DC})

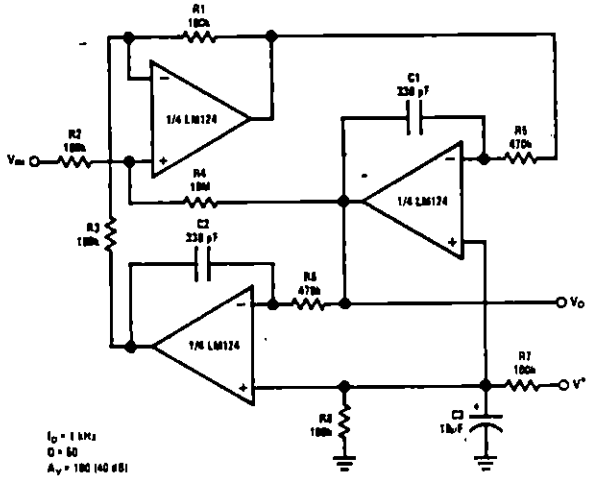


Where: $V_O = V_1 + V_2 - V_3 - V_4$
$(V_1 + V_2) \geq (V_3 + V_4)$ to keep $V_O > 0$ V_{DC}

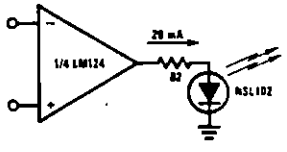
Power Amplifier



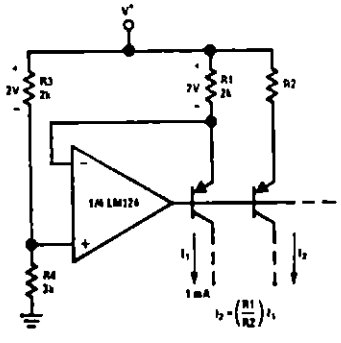
"BI-QUAD" RC Active Bandpass Filter



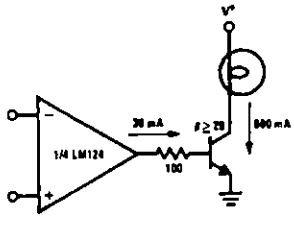
LED Driver



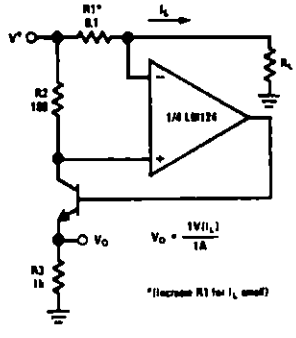
Fixed Current Sources



Lamp Driver

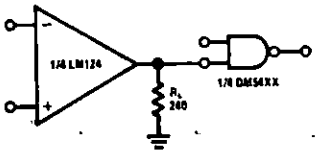


Current Monitor

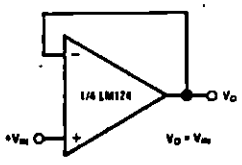


Typical Single-Supply Applications (Continued) (V^+ = 5.0 V_{DC})

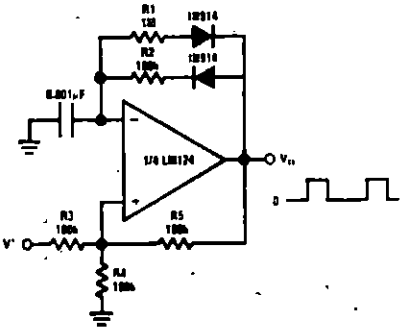
Driving TTL



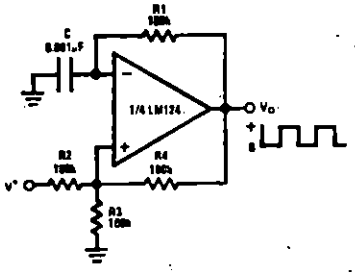
Voltage Follower



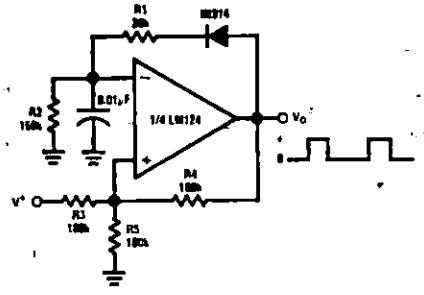
Pulse Generator



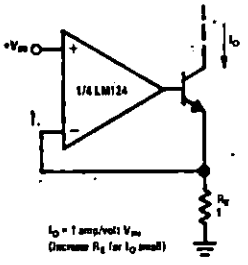
Squarewave Oscillator



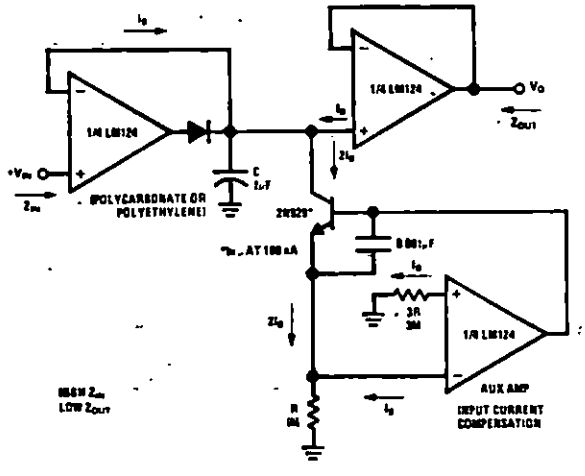
Pulse Generator



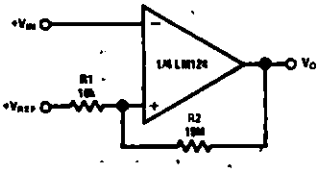
High Compliance Current Sink



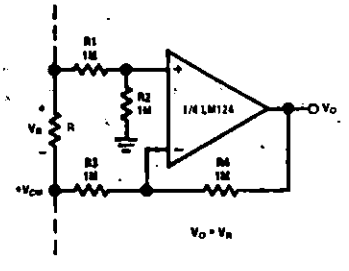
Low Drift Peak Detector



Comparator with Hysteresis



Ground Referencing A Differential Input Signal



Typical Single-Supply Applications (Continued) (V^+ = 5.0 V_{DC})

Voltage Controlled Oscillator Circuit

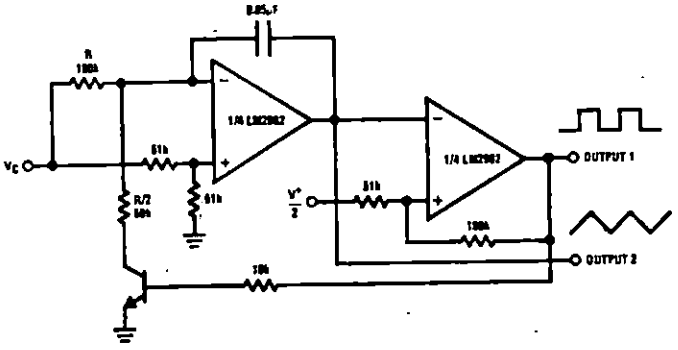
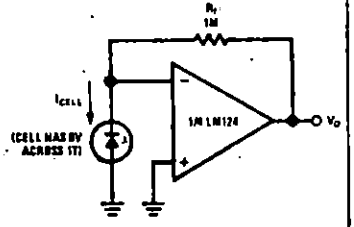
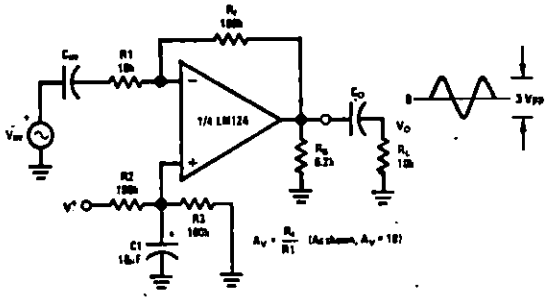


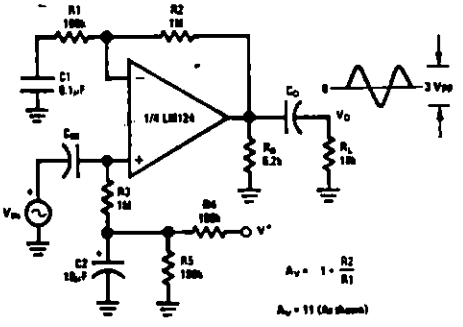
Photo Voltaic-Cell Amplifier



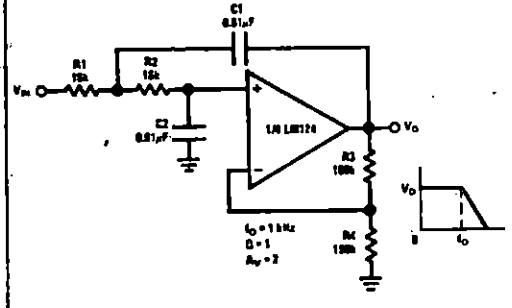
AC Coupled Inverting Amplifier



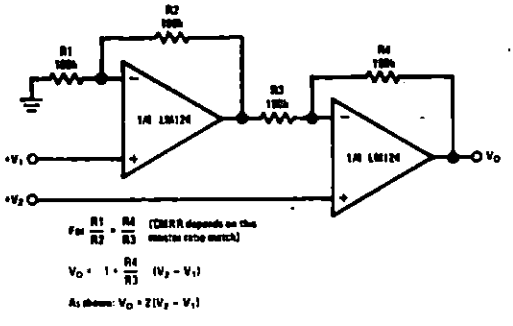
AC Coupled Non-Inverting Amplifier



DC Coupled Low-Pass RC Active Filter

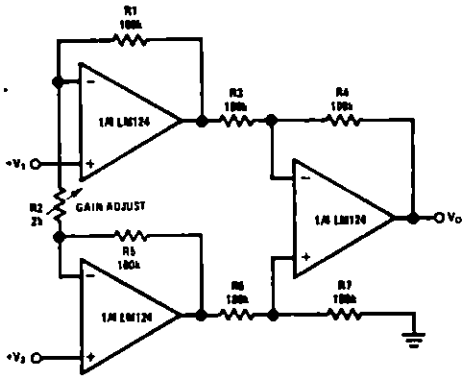


High Input Z, DC Differential Amplifier



Typical Single-Supply Applications (Continued) (V^+ = 5.0 V_{DC})

High Input Z Adjustable-Gain
DC Instrumentation Amplifier

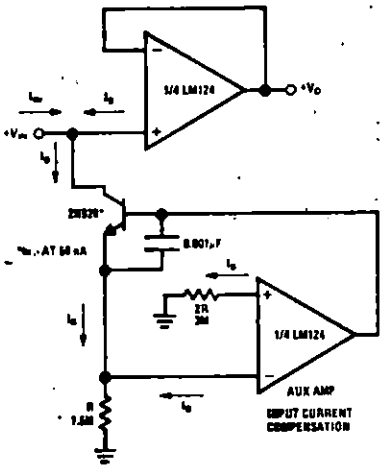


If R1 = R5 & R3 = R4 = R6 = R7 (CMRR depends on match)

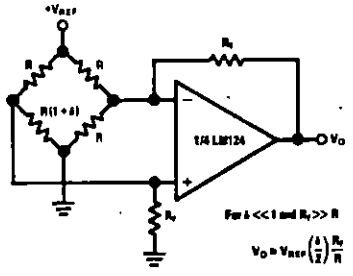
$$V_O = 1 + \frac{2R1}{R2}(V_2 - V_1)$$

As shown $V_O = 101(V_2 - V_1)$

Using Symmetrical Amplifiers to
Reduce Input Current (General Concept)



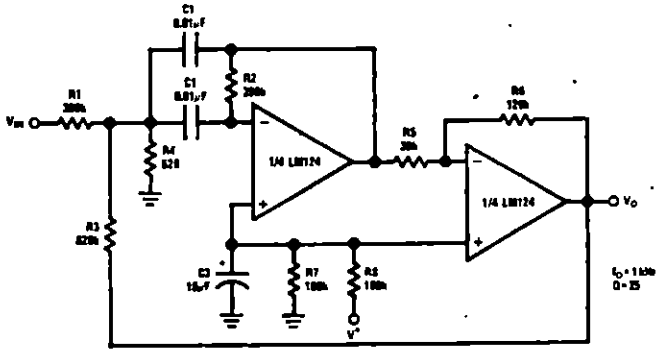
Bridge Current Amplifier



For $\delta \ll 1$ and $R_F \gg R$

$$V_O = V_{REF}\left(\frac{\delta}{2}\right)\frac{R_F}{R}$$

Bandpass Active Filter



National Semiconductor

Industrial Blocks

LM135/LM235/LM335, LM135A/LM235A/LM335A Precision Temperature Sensors

General Description

The LM135 series are precision, easily-calibrated, integrated circuit temperature sensors. Operating as a 2-terminal zener, the LM135 has a breakdown voltage directly proportional to absolute temperature at +10 mV/°K. With less than 1Ω dynamic impedance the device operates over a current range of 400 μA to 5 mA with virtually no change in performance. When calibrated at 25°C the LM135 has typically less than 1°C error over a 100°C temperature range. Unlike other sensors the LM135 has a linear output.

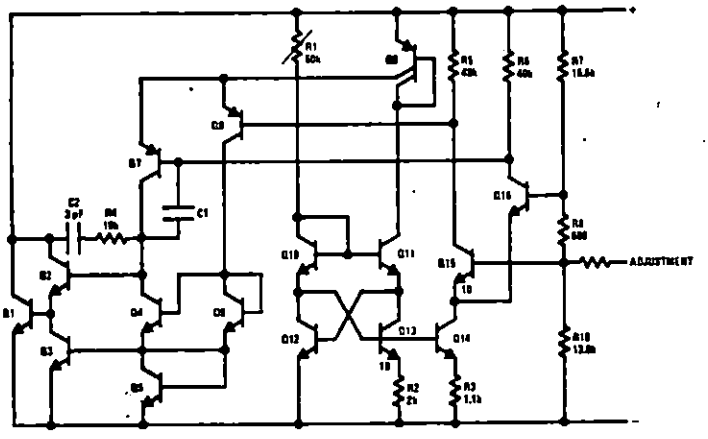
Applications for the LM135 include almost any type of temperature sensing over a −55°C to +150°C temperature range. The low impedance and linear output make interfacing to readout or control circuitry especially easy.

The LM135 operates over a −55°C to +150°C temperature range while the LM235 operates over a −40°C to +125°C temperature range. The LM335 operates from −40°C to +100°C. The LM135/LM235/LM335 are available packaged in hermetic TO-46 transistor packages while the LM335 is also available in plastic TO-92 packages.

Features

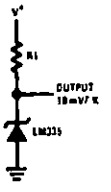
- Directly calibrated in °Kelvin
- 1°C initial accuracy available
- Operates from 400 μA to 5 mA
- Less than 1Ω dynamic impedance
- Easily calibrated
- Wide operating temperature range
- 200°C overrange
- Low cost

Schematic Diagram

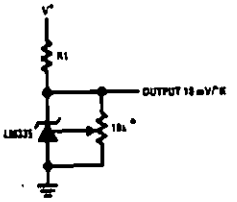


Typical Applications

Basic Temperature Sensor

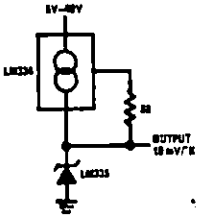


Calibrated Sensor



*Calibrate for 2.982V at 25°C

Wide Operating Supply



Absolute Maximum Ratings

Reverse Current		15 mA
Forward Current		10 mA
Storage Temperature		
TO-46 Package		−60°C to +180°C
TO-92 Package		−60°C to +150°C
Specified Operating Temperature Range		
	Continuous	Intermittent (Note 2)
LM135, LM135A	−55°C to +150°C	150°C to 200°C
LM235, LM235A	−40°C to +125°C	125°C to 150°C
LM335, LM335A	−40°C to +100°C	100°C to 125°C
Lead Temperature (Soldering, 10 seconds)		300°C

Temperature Accuracy LM135/LM235, LM135A/LM235A (Note 1)

PARAMETER	CONDITIONS	LM135A/LM235A			LM135/LM235			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Operating Output Voltage	$T_C = 25°C$, $I_R = 1$ mA	2.97	2.98	2.99	2.95	2.98	3.01	V
Uncalibrated Temperature Error	$T_C = 25°C$, $I_R = 1$ mA		0.5	1		1	3	°C
Uncalibrated Temperature Error	$T_{MIN} < T_C < T_{MAX}$, $I_R = 1$ mA		1.3	2.7		2	5	°C
Temperature Error with 25°C Calibration	$T_{MIN} < T_C < T_{MAX}$, $I_R = 1$ mA		0.3	1		0.5	1.5	°C
Calibrated Error at Extended Temperatures	$T_C = T_{MAX}$ (Intermittent)		2			2		°C
Non-Linearity	$I_R = 1$ mA		0.3	0.5		0.3	1	°C

Temperature Accuracy LM335, LM335A (Note 1)

PARAMETER	CONDITIONS	LM335A			LM335			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Operating Output Voltage	$T_C = 25°C$, $I_R = 1$ mA	2.95	2.98	3.01	2.92	2.98	3.04	V
Uncalibrated Temperature Error	$T_C = 25°C$, $I_R = 1$ mA		1	3		2	6	°C
Uncalibrated Temperature Error	$T_{MIN} < T_C < T_{MAX}$, $I_R = 1$ mA		2	5		4	9	°C
Temperature Error with 25°C Calibration	$T_{MIN} < T_C < T_{MAX}$, $I_R = 1$ mA		0.5	1		1	2	°C
Calibrated Error at Extended Temperatures	$T_C = T_{MAX}$ (Intermittent)		2			2		°C
Non-Linearity	$I_R = 1$ mA		0.3	1.5		0.3	1.5	°C

Electrical Characteristics (Note 1)

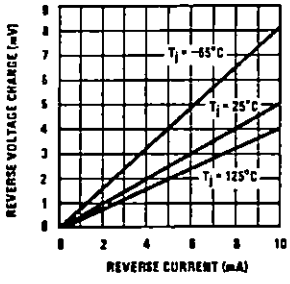
PARAMETER	CONDITIONS	LM135/LM235 LM135A/LM235A			LM335 LM335A			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Operating Output Voltage Change with Current	400 μA < I_R < 5 mA At Constant Temperature		2.5	10		3	14	mV
Dynamic Impedance	$I_R = 1$ mA		0.5			0.6		Ω
Output Voltage Temperature Drift			+10			+10		mV/°C
Time Constant	Still Air		80			80		sec
	100 ft/Min Air		10			10		sec
	Stirred Oil		1			1		sec
Time Stability	$T_C = 125°C$		0.2			0.2		°C/khr

Note 1: Accuracy measurements are made in a well-stirred oil bath. For other conditions, self heating must be considered.

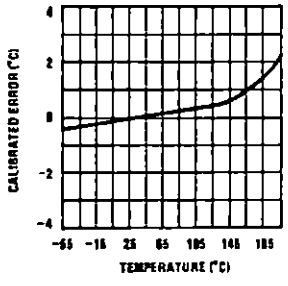
Note 2: Continuous operation at these temperatures for 10,000 hours for H package and 5,000 hours for Z package may decrease life expectancy of the device.

Typical Performance Characteristics

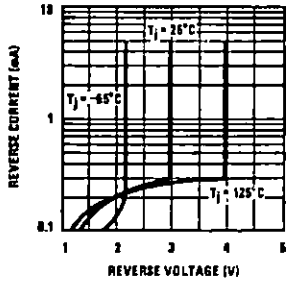
Reverse Voltage Change



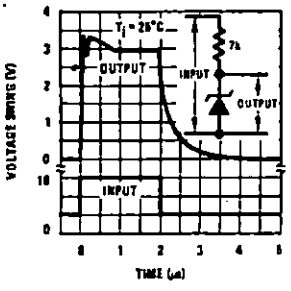
Calibrated Error



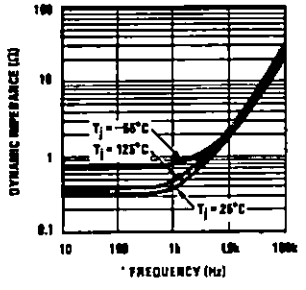
Reverse Characteristics



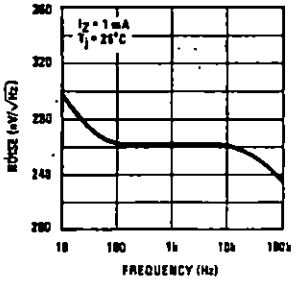
Response Time



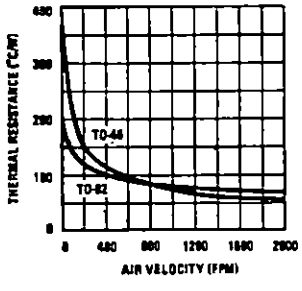
Dynamic Impedance



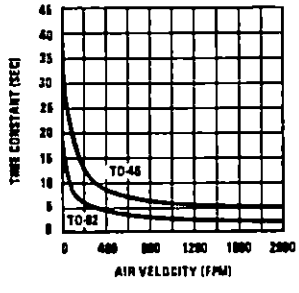
Noise Voltage



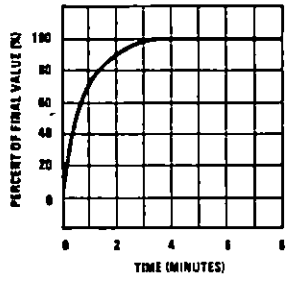
Thermal Resistance Junction to Air



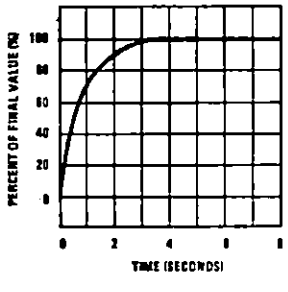
Thermal Time Constant



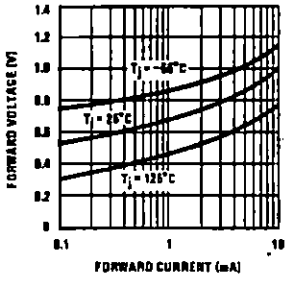
Thermal Response in Still Air



Thermal Response in Stirred Oil Bath



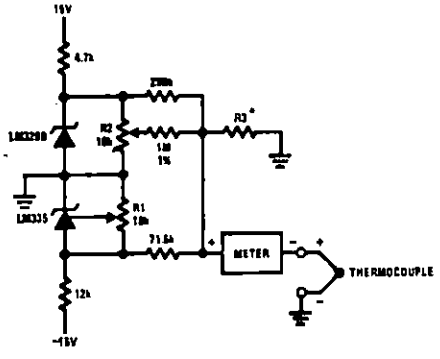
Forward Characteristics



Typical Applications (Continued)

THERMOCOUPLE COLD JUNCTION COMPENSATION

Compensation for Grounded Thermocouple



*Select R3 for proper thermocouple type

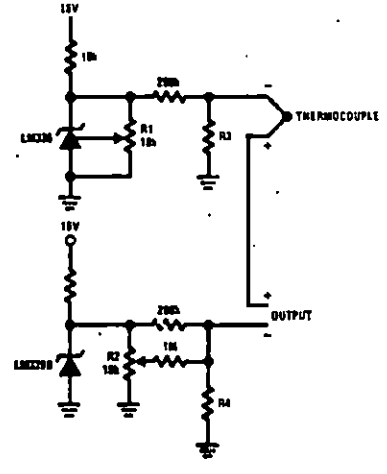
THERMOCOUPLE	R3	SEEBECK COEFFICIENT
J	377Ω	52.3 μV/°C
T	308Ω	42.8 μV/°C
K	293Ω	40.8 μV/°C
S	45.8Ω	6.4 μV/°C

Adjustments: Compensates for both sensor and resistor tolerances

1. Short LM329B
2. Adjust R1 for Seebeck Coefficient times ambient temperature (in degrees K) across R3
3. Short LM335 and adjust R2 for voltage across R3 corresponding to thermocouple type

J	14.32 mV	K	11.17 mV
T	11.79 mV	S	1.768 mV

Single Power Supply Cold Junction Compensation



*Select R3 and R4 for thermocouple type

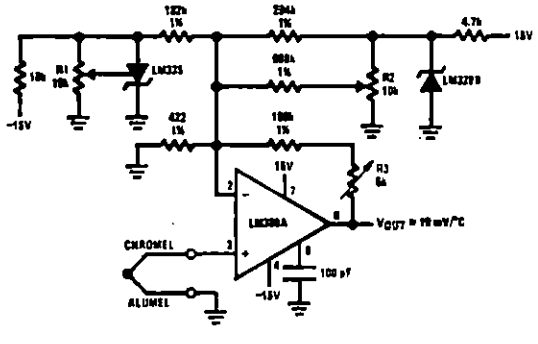
THERMOCOUPLE	R3	R4	SEEBECK COEFFICIENT
J	1.05K	385Ω	52.3 μV/°C
T	856Ω	315Ω	42.8 μV/°C
K	816Ω	300Ω	40.8 μV/°C
S	128Ω	46.3Ω	6.4 μV/°C

Adjustments:

1. Adjust R1 for the voltage across R3 equal to the Seebeck Coefficient times ambient temperature in degrees Kelvin.
2. Adjust R2 for voltage across R4 corresponding to thermocouple

J	14.32 mV	K	11.17 mV
T	11.79 mV	S	1.768 mV

Centigrade Calibrated Thermocouple Thermometer



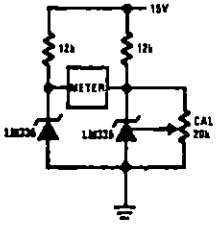
Terminate thermocouple reference junction in close proximity to LM335.

Adjustments:

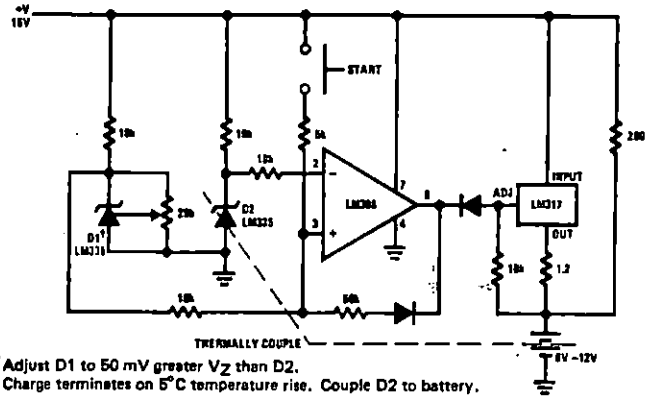
1. Apply signal in place of thermocouple and adjust R3 for a gain of 245.7.
2. Short non-inverting input of LM308A and output of LM329B to ground.
3. Adjust R1 so that V_{OUT} = 2.982V @ 25°C.
4. Remove short across LM329B and adjust R2 so that V_{OUT} = 246 mV @ 25°C.
5. Remove short across thermocouple.

Typical Applications (Continued)

Differential Temperature Sensor

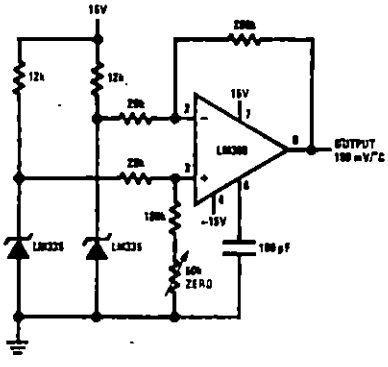


Fast Charger for Nickel-Cadmium Batteries

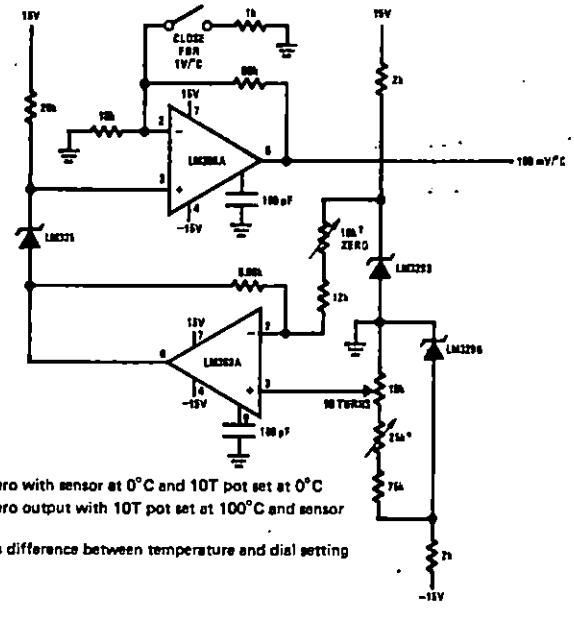


†Adjust D1 to 50 mV greater V_Z than D2.
Charge terminates on 5°C temperature rise. Couple D2 to battery.

Differential Temperature Sensor

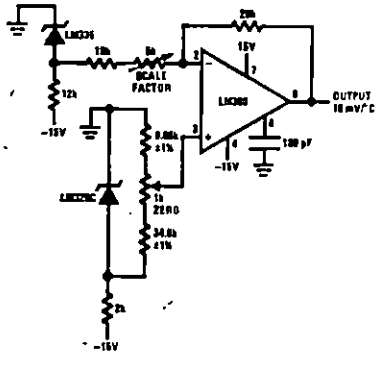


Variable Offset Thermometer‡

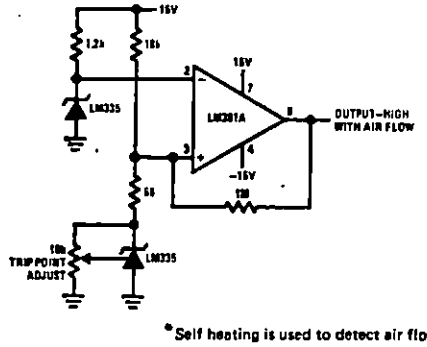


†Adjust for zero with sensor at 0°C and 10T pot set at 0°C
*Adjust for zero output with 10T pot set at 100°C and sensor at 100°C
‡Output reads difference between temperature and dial setting of 10T pot

Ground Referred Centigrade Thermometer



Air Flow Detector*



*Self heating is used to detect air flow

Definition of Terms

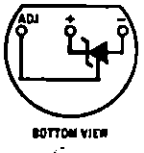
Operating Output Voltage: The voltage appearing across the positive and negative terminals of the device at specified conditions of operating temperature and current.

Uncalibrated Temperature Error: The error between the operating output voltage at 10 mV/°K and case temperature at specified conditions of current and case temperature.

Calibrated Temperature Error: The error between operating output voltage and case temperature at 10 mV/°K over a temperature range at a specified operating current with the 25°C error adjusted to zero.

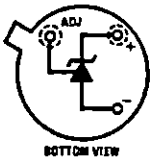
Connection Diagrams

TO-92
Plastic Package



Order Number LM335Z
or LM335AZ
See NS Package Z03A

TO-46
Metal Can Package*



*Case is connected to negative pin

Order Number LM135H,
LM235H, LM335H, LM135AH,
LM235AH or LM335AH
See NS Package H03H