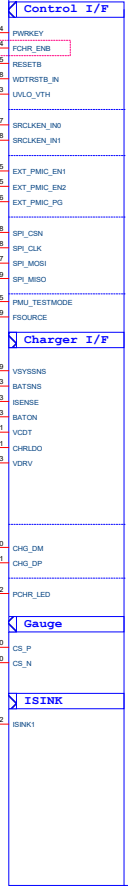


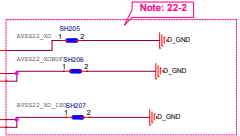
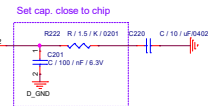
علي البجر فريق الهارد خطب تك

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Doc	Document Number	Contents	Rev
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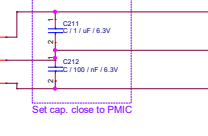
**MT6357**



Note: 22-3

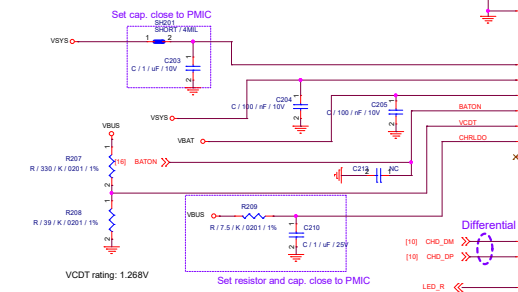


Note: 22-4



Note: 22-1

Route AVDD18\_AUXADC, AUXADC\_VIN, and AVSS18\_AUXADC with 3mils width traces and well GND shielding



- Note 22-1: Please refer to MT6765\_MT6357 Co-Clock Design Notice for co-layout guide
- Note 22-2: 1. Please Connect P1 and R1 ball first and then to GND  
2. Please Connect P2 and N2 ball first and then to GND  
3. Please connect DCXO GND to main GND by independent L1-2 GND via.; DO NOT connect it through L1 GND
- Note 22-3: Let floating if disable HOMEKEY function
- Note 22-4: Please follow MT6765\_MT6357 Co-Clock Design Notice for Layout guide of VAUX18, then R210 can use 0 ohm to replace BEAD.

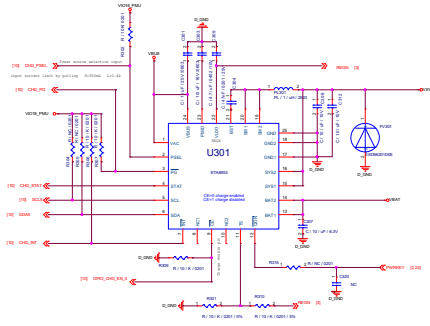
File	Amman
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على البجر فريق الهارد خب توك

# Switching Charger Power Path

STA6953 address: 0x80 BQ25601 address: 0x88

10  
BOM check status for power path hardware. Contact to the PMIC for details.  
Approved by the hardware team.  
Approved by the software team.  
Approved by the test team.  
Approved by the manufacturing team.  
Approved by the marketing team.

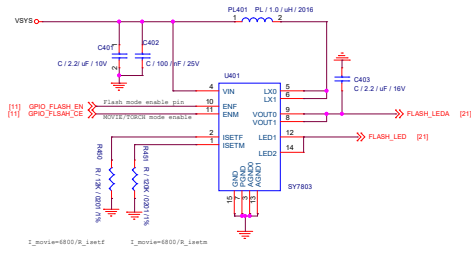


Revision	
1	Initial Release
2	AL_POWER_LOADS_IN_PLANS
3	AL_POWER_LOADS_IN_PLANS

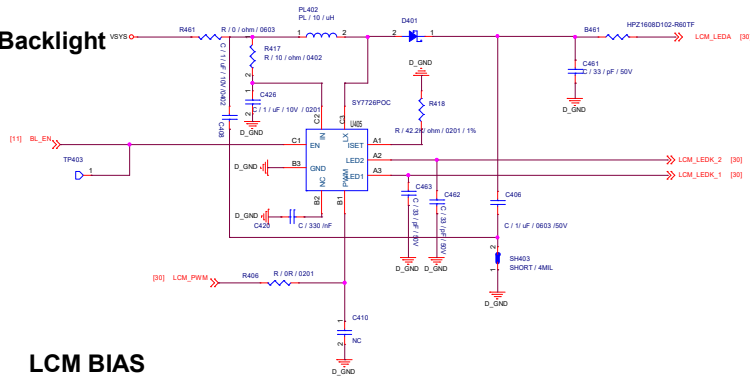
11\_POWER\_SubPMIC-General  
MTK Confidential

علي البجر فريق الهارد خبب تك

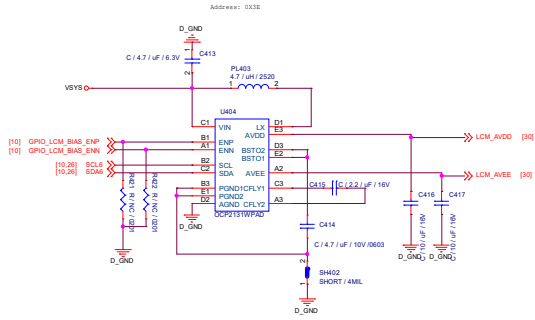
# Flash LED Driver



# Backlight

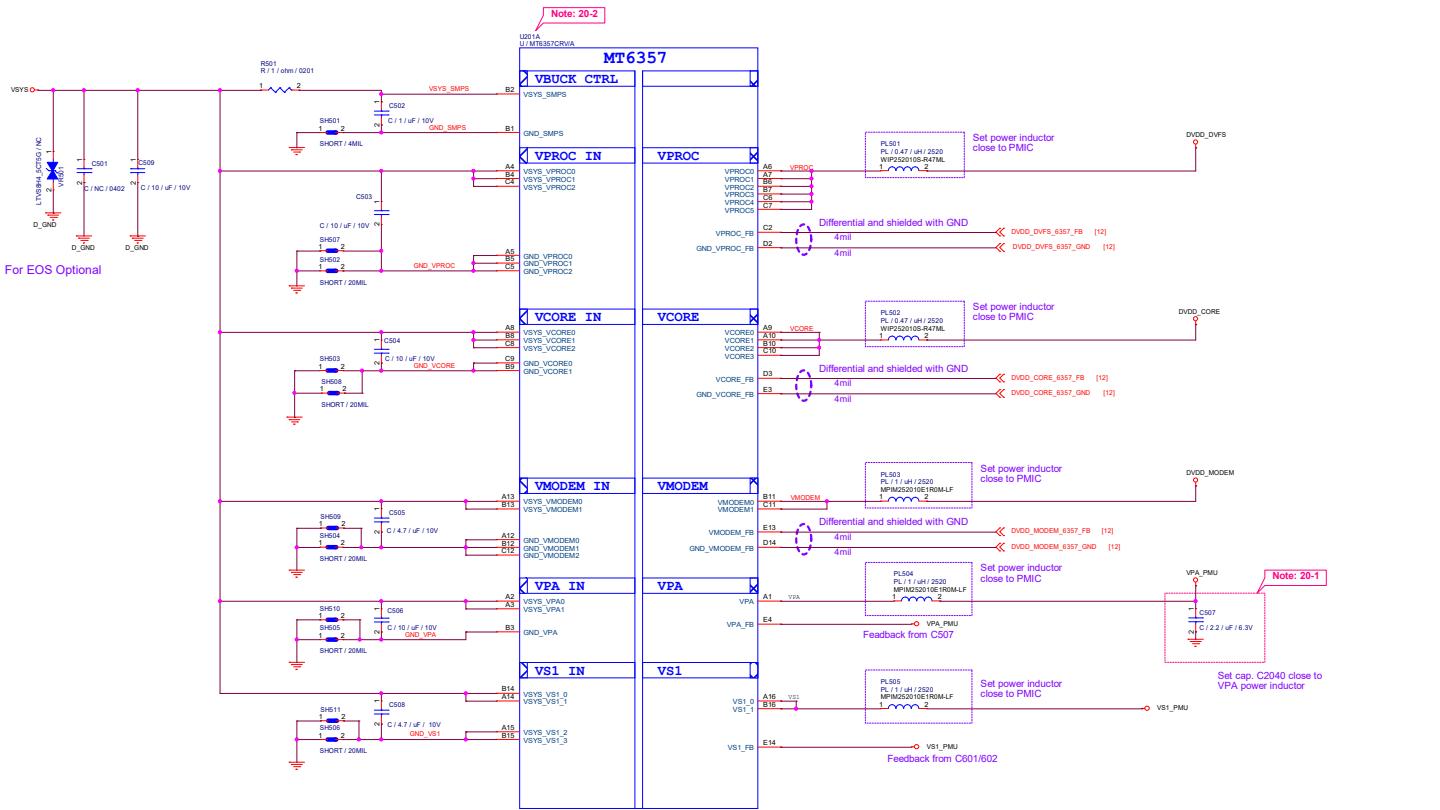


# LCM BIAS



علي البجر فريق الهارد خب تک

Rev	Amman	
Doc	Document Number	04_POWER_LCMBIAS_BL_FLASH
Ver		V1.0
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For EOS Optional

Note 20-1: C507, please choose 0402 size

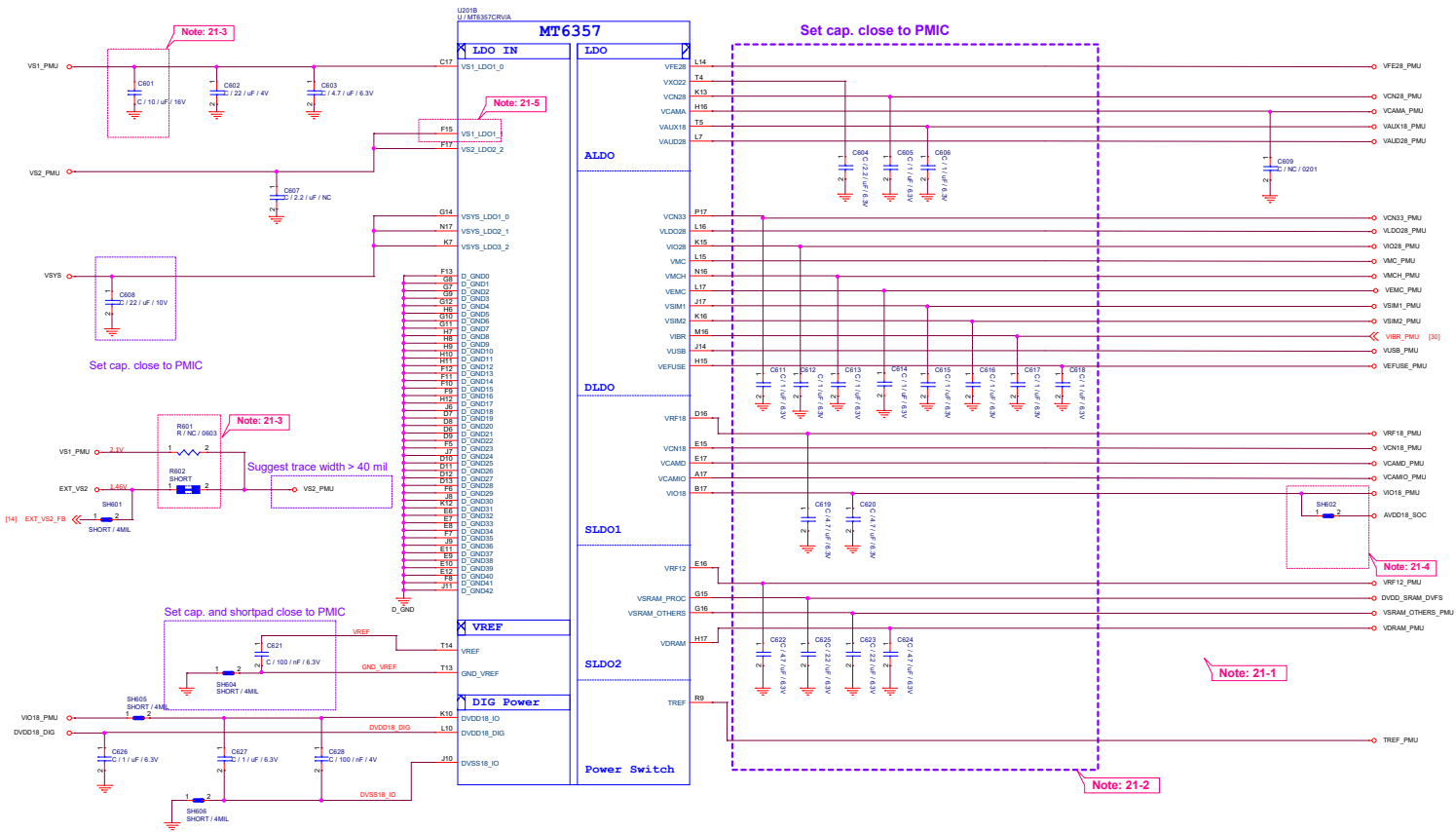
Note 20-2: PMIC Part number notice for MT6765/62/61 platform

MTK Platform	PMIC
MT6765 / 62	MT6357 CRV
MT6761	MT6357 MRV

Asman	
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علي البجر فريق الهارد خلب تك

1. "Typical Cap" defined in design notice is the minimum cap. to LDO Cout. 2. NC cap can move to application, if (PCB L<20nH, PCB R<0.2 ohm) => value and placement of Cap, please refer design notice



Note 21-1: If these power trace can meet LDO layout constraint, these CAP can be NC or removed. Please refer to MT6357 design notice.

Note 21-2: Output cap range please follow MT6357CRV LDO design notice

Note 21-3: Ext Buck BOM option

	Ext. buck option	
	w/ EXT VS2 Buck	w/o EXT VS2 Buck
C601	10uF	22uF_0603
R602	0-ohm_0603	NC
R601	NC	0-ohm_0603

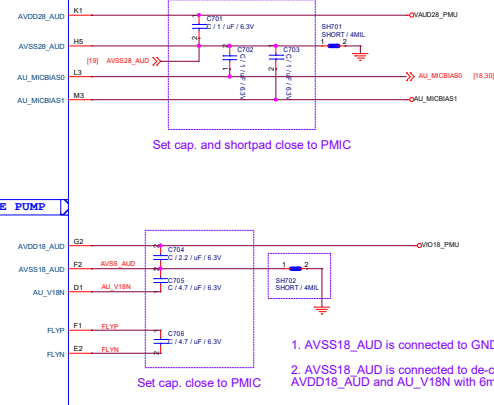
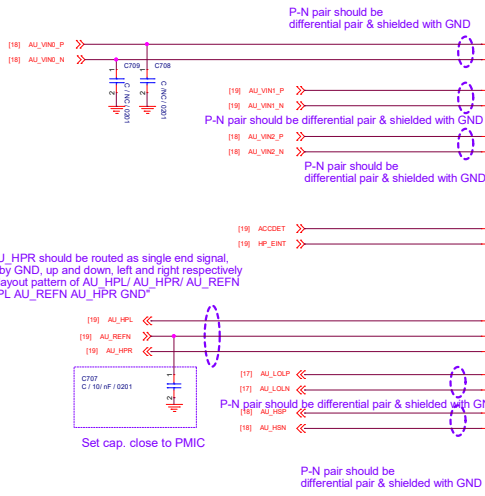
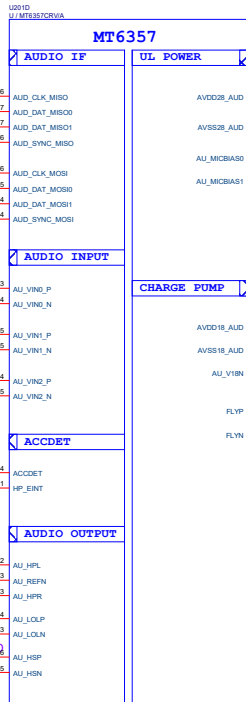
Note 21-4: Please set SH602 and SH603 close to C620, making star connection among VIO18\_PMU, AVDD18\_SOC, and EMI\_VDD1 near to LDO cap. C620. Please also refer to MT6357 design notice for further detail design information

Note 21-5: Please connect VS2\_LDO1(F15) to VS1\_PMU if voltage applied to VCAMD(E17) >= 1.3 V

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Doc	Document Number	POWER_MT6357_LDO	V1.0
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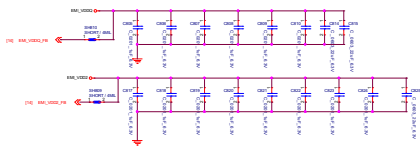
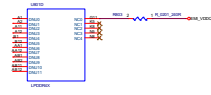
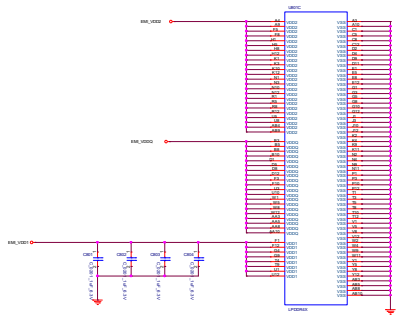
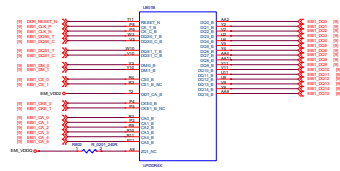
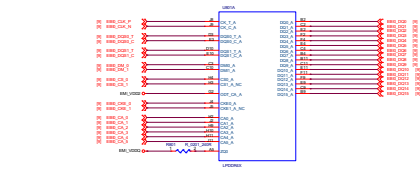
علي السراج  
المهندس الهارد  
الخطب توك





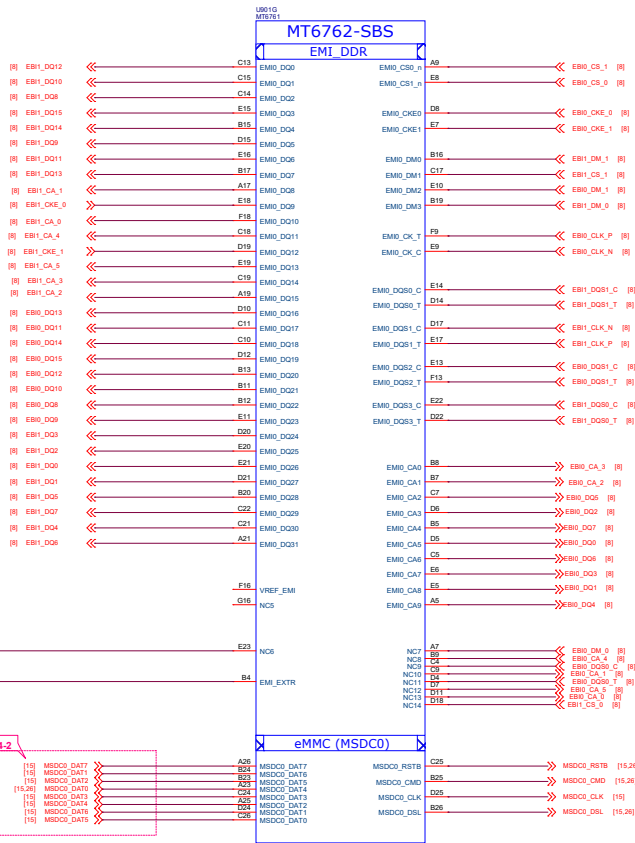
علي البجر فريق الهارد خب توك

File	Amman		
Doc C	Document Number	POWER_mt6357_Audio	Rev V1.0
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Project	
Project Name	74VHC00 NAND Gate
Project Number	74VHC00 NAND Gate
Project Date	2023-10-27

علي البجر فريق الهارد خبب تك

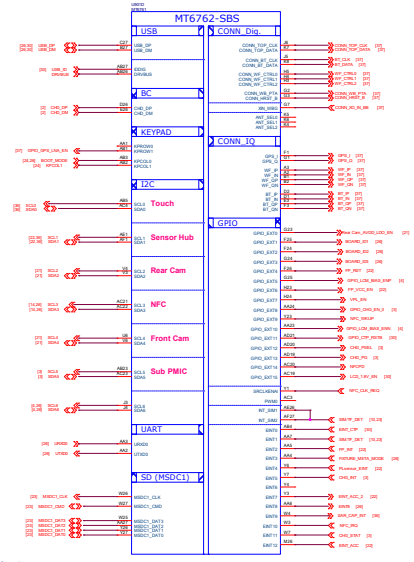
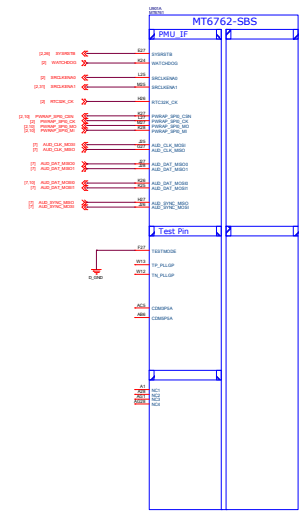


Note 14-1: R4001 please select 34.8 ohm (1%) resistor

Note 14-2: Please check eMCP LP3 and eMCP LP4X pin mux

علي البجر فريق الهارد خب ترك

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Doc C	Print
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Doc C	Rev
Doc C	V1.0



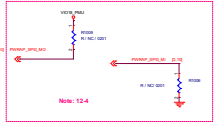
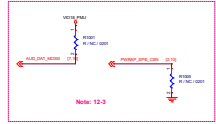
Note 12-3: \*PWRAP\_SPI0\_CS# and \*AUD\_DAT\_MOSD0 are bootstrap pins to select which interface will be the JTAG pin out.

PWRAP_SPI0_CS#	AUD_DAT_MOSD0	AP JTAG	MO JTAG	JTAG Function
HI	LO	NA	NA	
HI	HI	SPD-EN15	SPD-EN15	
LO	LO	SPD-EN15	SPD-EN15	
LO	HI	MSDC1	NA	

Note 12-4: PWRAP\_SPI0\_MI is DDR type feature in bootstrap

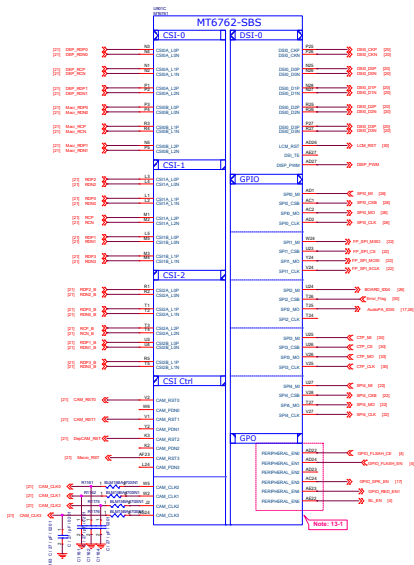
PWRAP_SPI0_MI	DDR	MSDC0 pin mux
LO	LPDDR3	Follow LP3 Ref SCH
HI	LPDDR4X	Follow LP4X Ref SCH

PWRAP_SPI0_MI	PWRAP_SPI0_MO	DDR	MSDC0 pin mux
default/PU	default/PO	DDR	MSDC0 pin mux
LO	LO	LPDDR3	Follow LP3 Ref SCH
LO	HI	NA	NA
HI	LO	LPDDR4X	Follow LP4X Ref SCH
HI	HI	LPDDR4	Follow LP4X Ref SCH

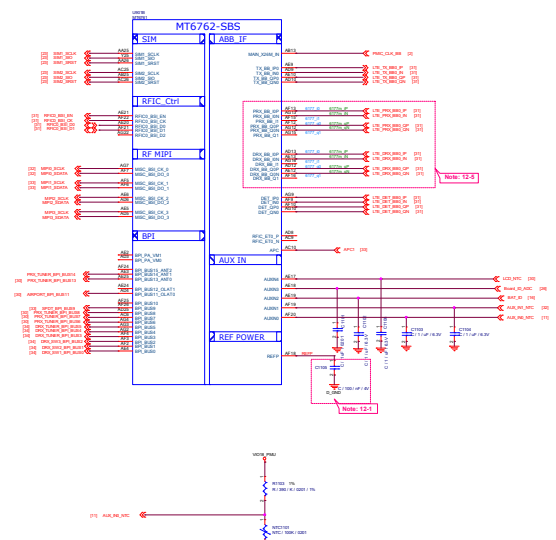


Pin	Function
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Note 12-1: The de-coupling cap. for REFP (AF18 ball) have to be placed as close to BB as possible.  
 Note 12-2: To shunt a 1uF capacitor in the AUXIN ADC input to prevent noise coupling. It should be placed as close to BB as possible. Connect the unused AUX\_ADC input to GND.  
 Note 12-5: Please set unused IQ pins in NC  
 Note 13-1: The middle pin of acoustic or optoelectronic devices (e.g. SPK, AMP/Backlight/Charger OCP/OVP) suggest to use Peripheral\_EN[0-5].  
 If use other GPIOs as enable pin, suggest to reserve G201 NC to GND

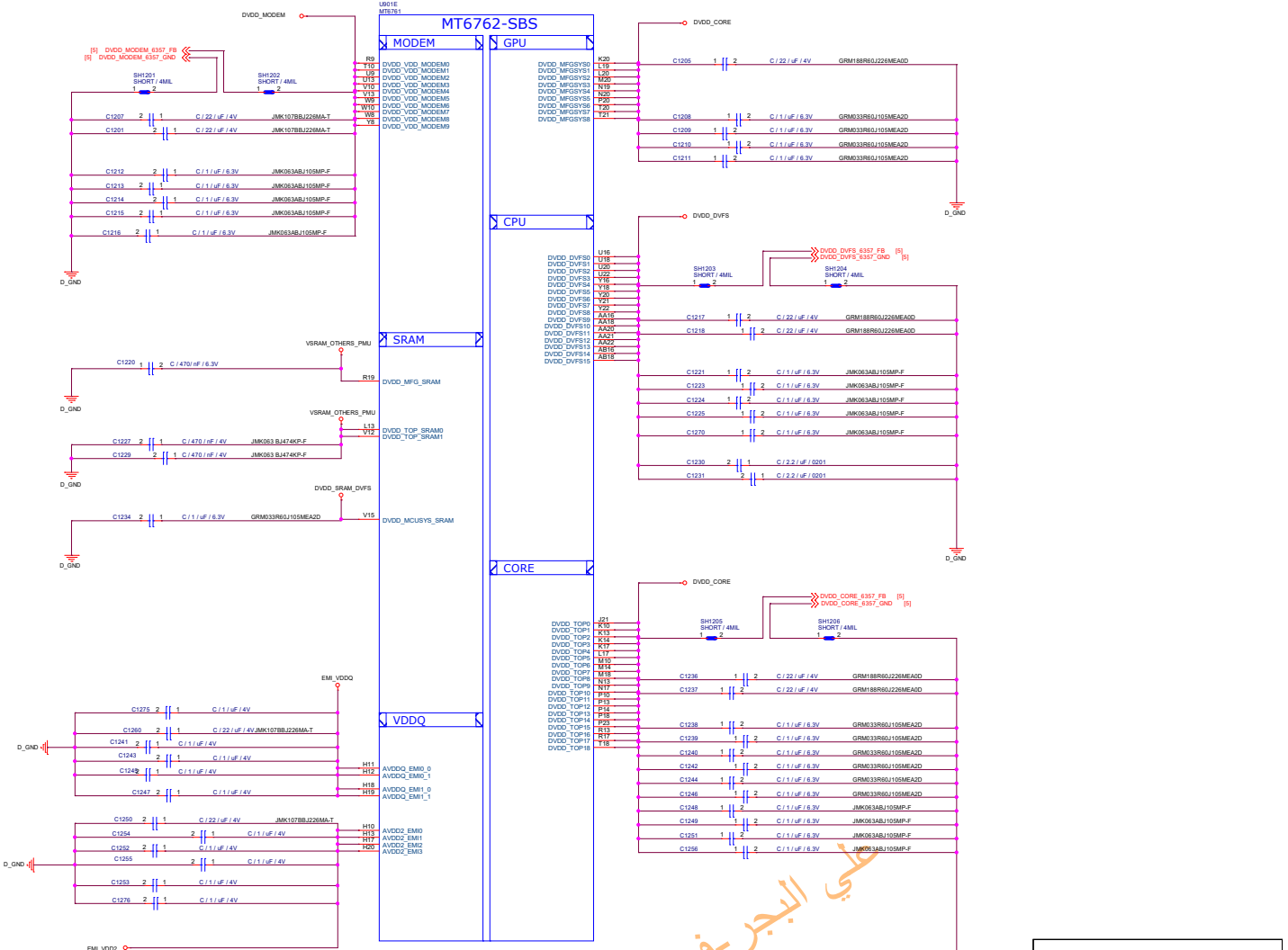


**Thermistor to sense AP temperature**

- 1. NTC109H have long a distance about 6-8 mm away from AP and far from other heat sources. If use it alone.
- 2. The distance is the shortest distance from package edge to edge.

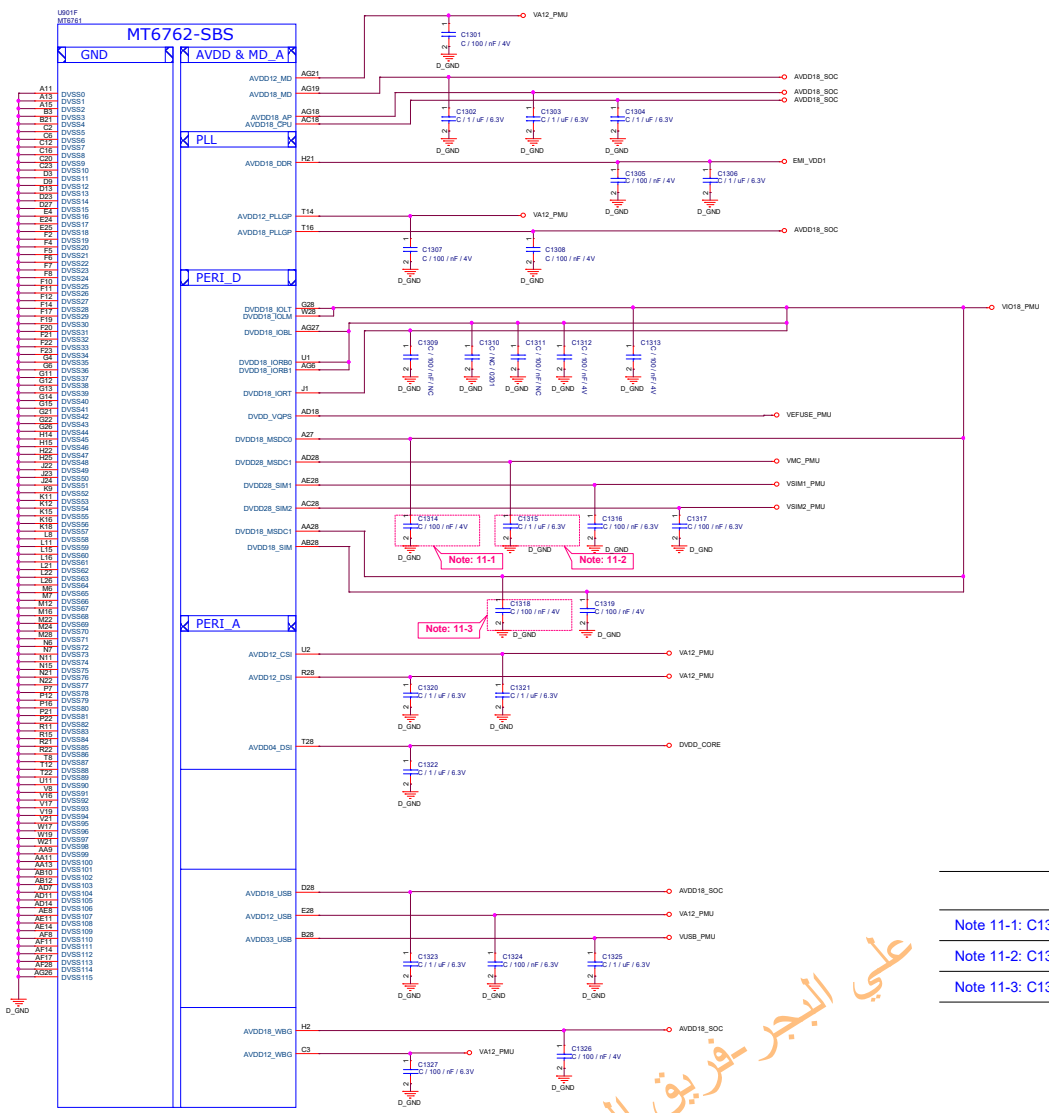
Revision	
1.0	Initial Release
1.1	Revise AP and RF related
1.2	Revise AP and RF related

علي البجر فريق الهارد خب توك



طلي البجر فريق الهارد خلب تك

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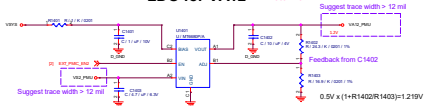


- Note 11-1: C1314 closed DVDD18\_MSDC0 150mil
- Note 11-2: C1315 closed DVDD28\_MSDC1 150mil
- Note 11-3: C1318 closed DVDD18\_MSDC1 150mil

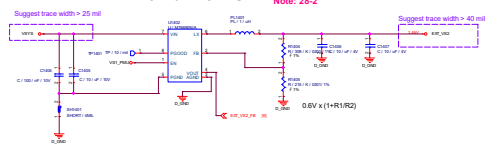
علي البجر فريق الهارد خلب تك

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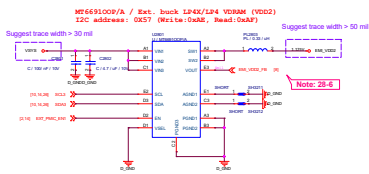
**LDO for VA12** Note: 28-1



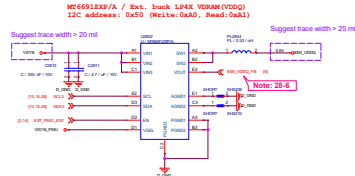
**Ext. Bulk for VS2** Note: 28-2



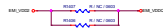
**Ext. buck LPDDR4X/LPDDR4 VDRAM** Note: 28-4



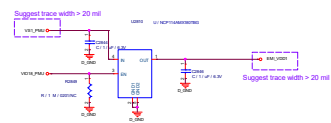
**Ext. buck LPDDR4X VDDQ** Note: 28-4



Reserved for LP4 DRAM [VDDQ=1.1V]



**LPDDR4X/LPDDR4 VDD1 1.8V LDO** Note: 28-5



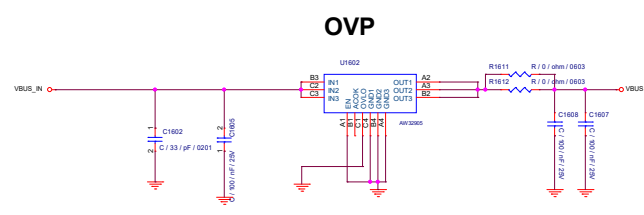
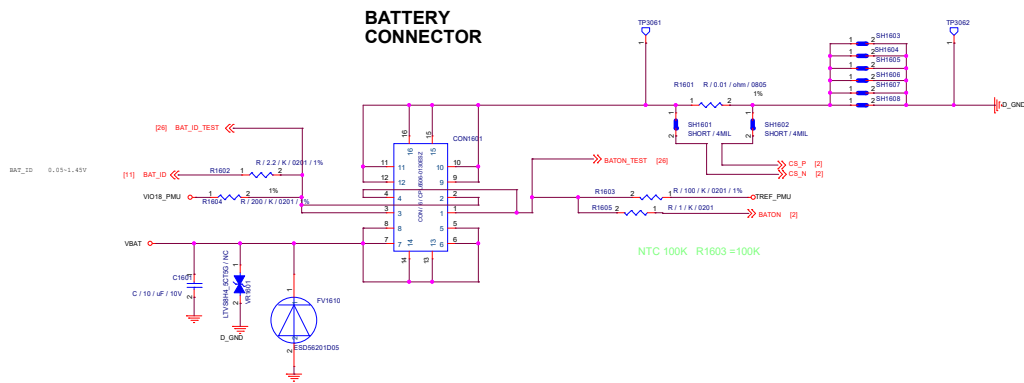
- Note 28-1: VA12 Layout placement please close to AP
- Note 28-2: VS2 Buck Layout placement please close to PMIC M76357, only used for M76762, NC for M76761

Rev	0
Author	PMIC/Design/Power
Check	
Approved	
Release Date	

علي البجر فريق الهارد خب توك



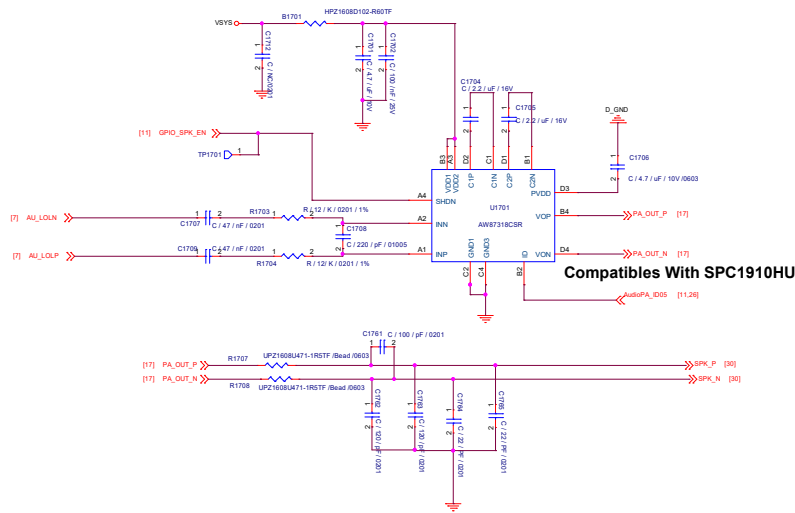




علي البجر فريق الهارد خب ترك

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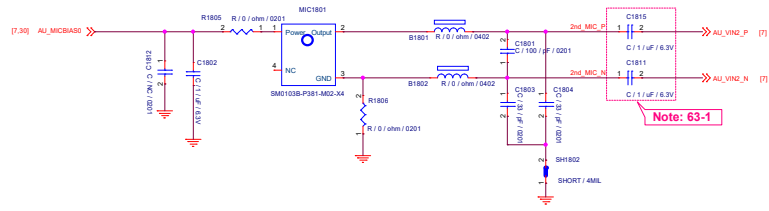
### Class K PA



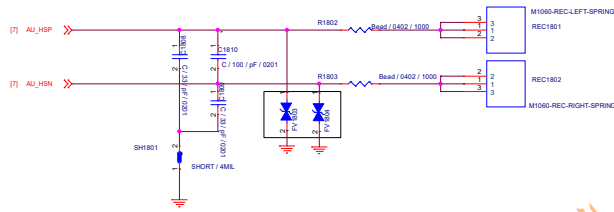
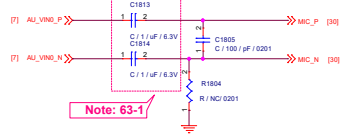
علي البجر فريق الهارد خب توك

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### MIC2



### MIC1



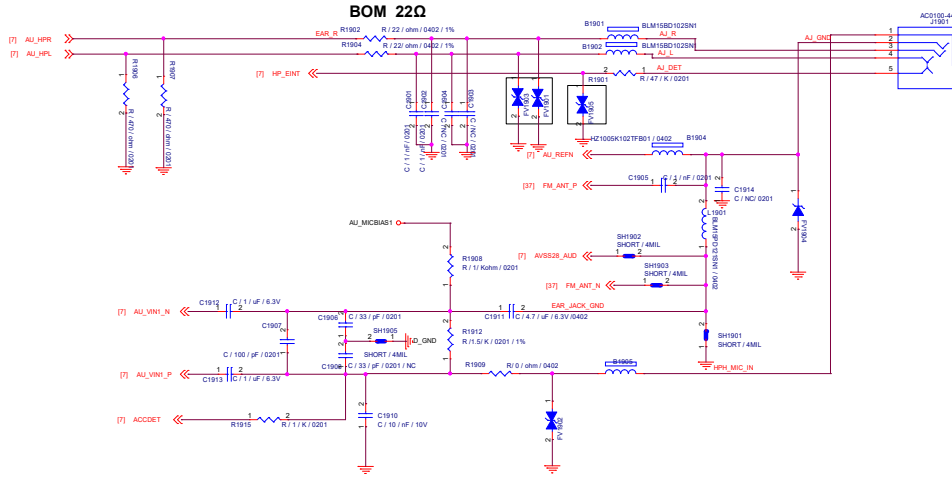
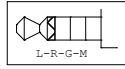
Schematic design notice of "63\_PERI\_AUDIO\_IO" page.

Note 63-1: 1 uF for ACC mode  
0 ohm for DCC mode

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Amman			
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علي البجر فريق الهارد خطب تك

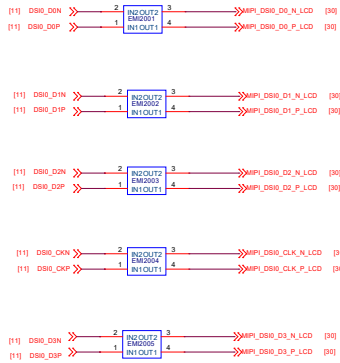
### 3.5mm Headphone Jack



علي البجر فريق الهارد خب توك

File	Amman
Doc	Document Number Earphone
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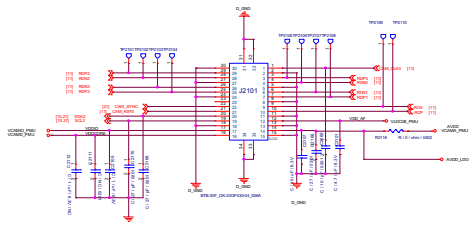
## Main LCM



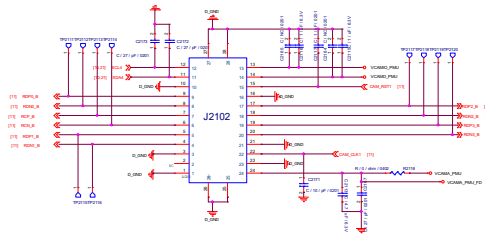
علي البجر فريق الهارد خب ترك

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C			V1.0
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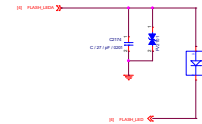
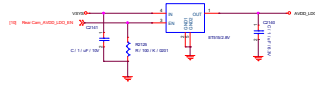
### Main Camera



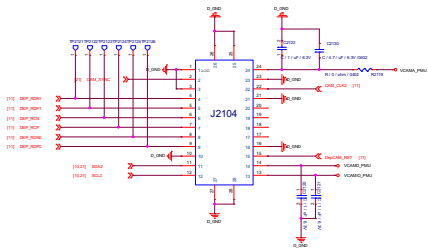
### Front Camera



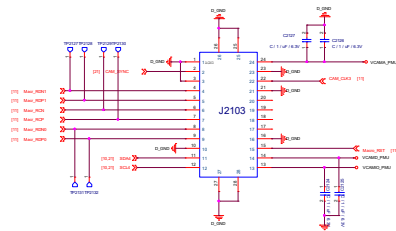
### Main Flash LED



### Macro Camera



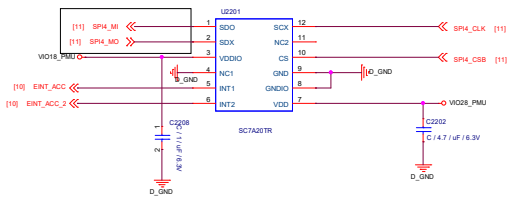
### Dep Camera



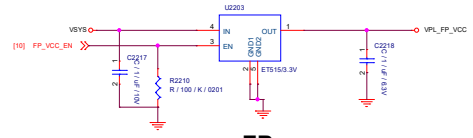
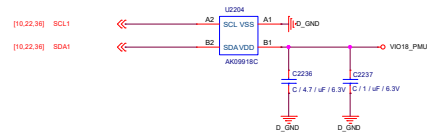
Rev	01
Created	2023/01/10
Checked	2023/01/10
Approved	2023/01/10

علي البجر فريق الهارد خب ترك

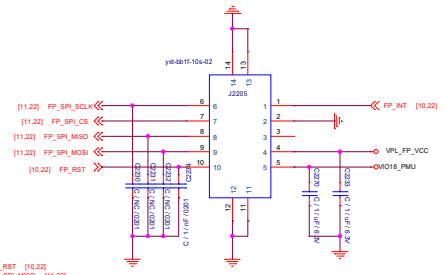
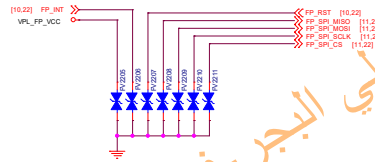
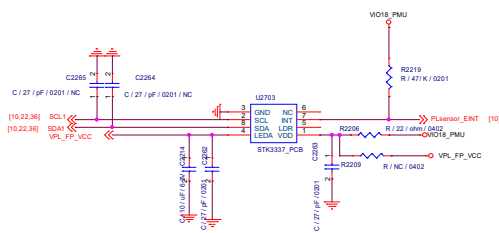
## G-Sensor



## M SENSOR



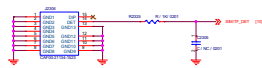
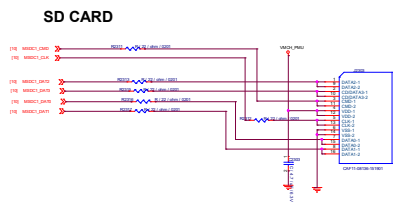
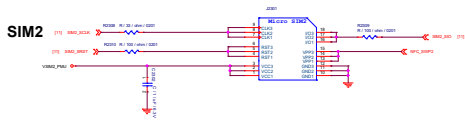
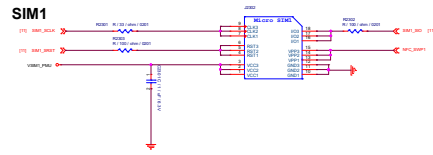
## FP



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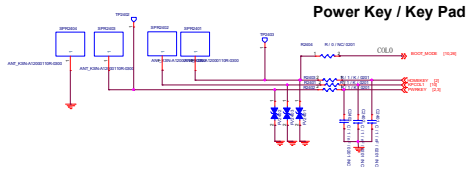
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Date	2023-07-01
Author	Abdelhakim
Project	ESP32
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Project Name	
Project Number	
Project Date	
Project Status	

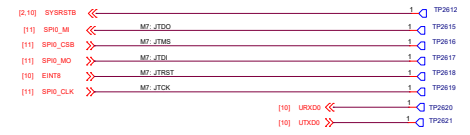
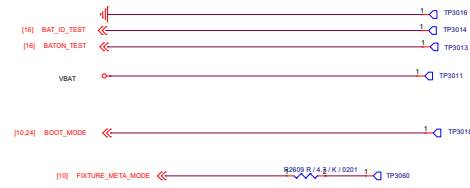
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## USB



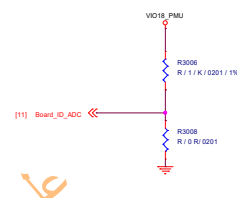
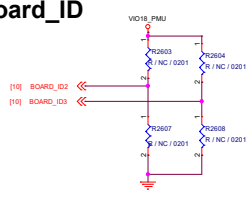
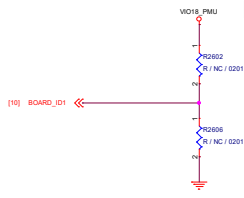
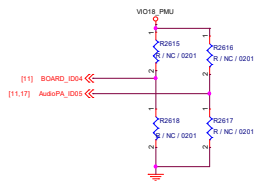
## BAT



## eMMC



## Board\_ID



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Note 52-1: NFC host I/F and power info are listed in the above connector, NFC COB reference schematic is in the file named "MTK ST NFC Reference Schematic\_20170809"

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Note 52-2: When NFC is applied, please keep  
1. 0ohm NC between VSIM1\_PMU and SIM1\_VCC  
2. 0ohm NC between VSIM2\_PMU and SIM2\_VCC

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Note 52-3: When NFC is applied, please follow NFC COB reference schematic to draw NFC COB schematic

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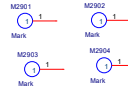
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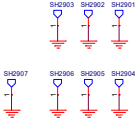
贴片器件，钢网要开



Shielding frame



Marks point



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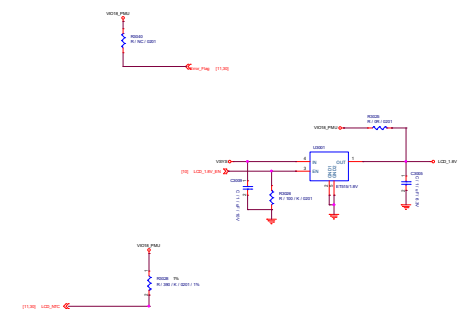
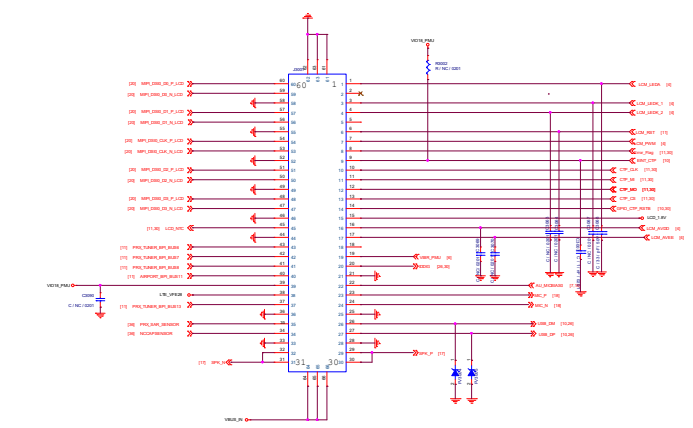
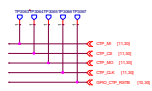
MAIN\_SUB\_CON

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Legend	
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[Symbol]	Component Name
[Symbol]	Component Name

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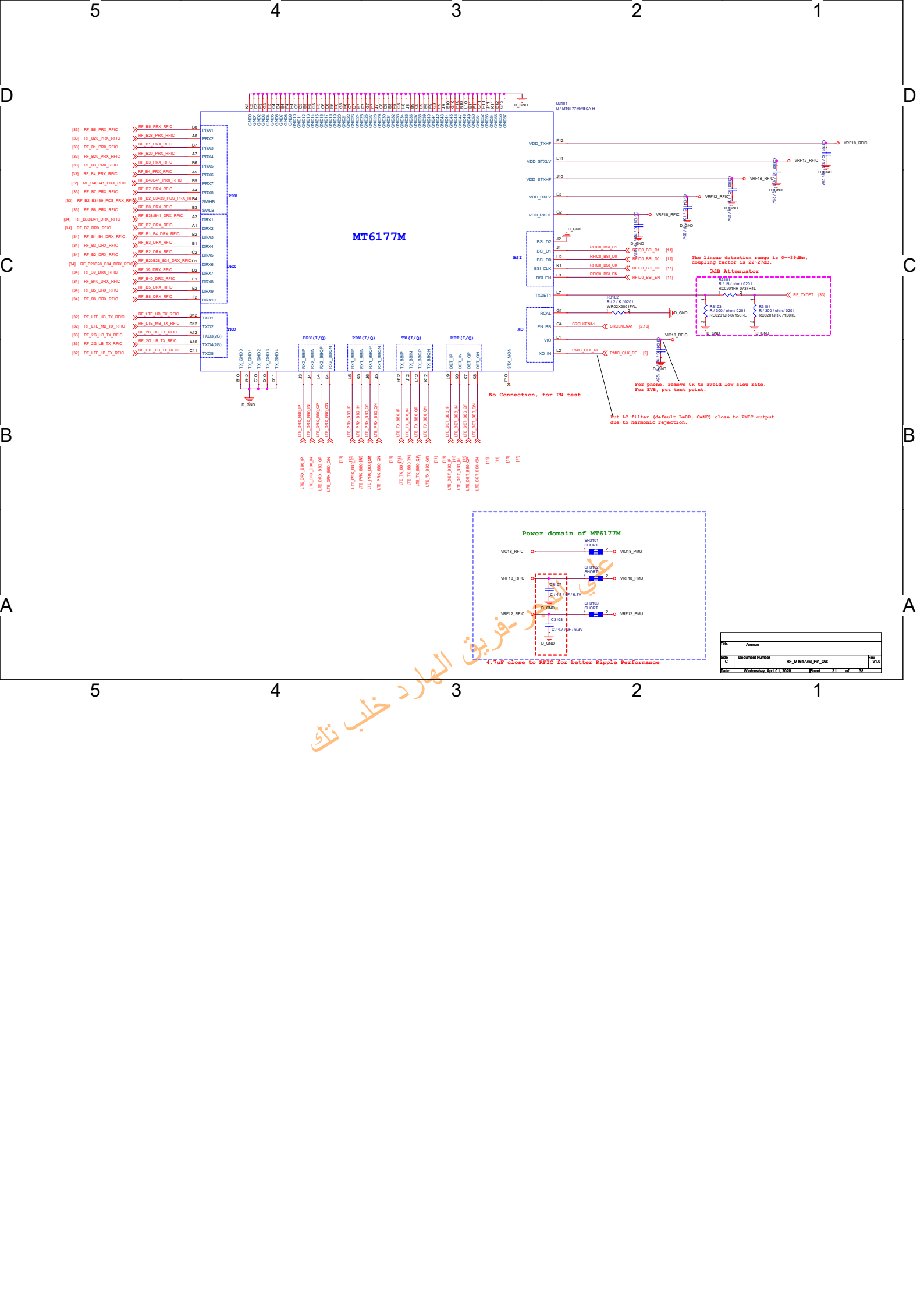
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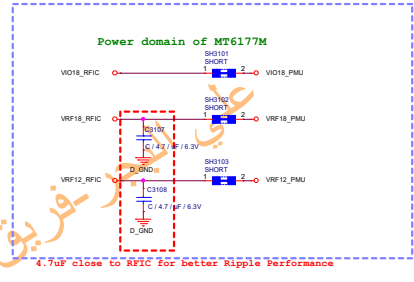
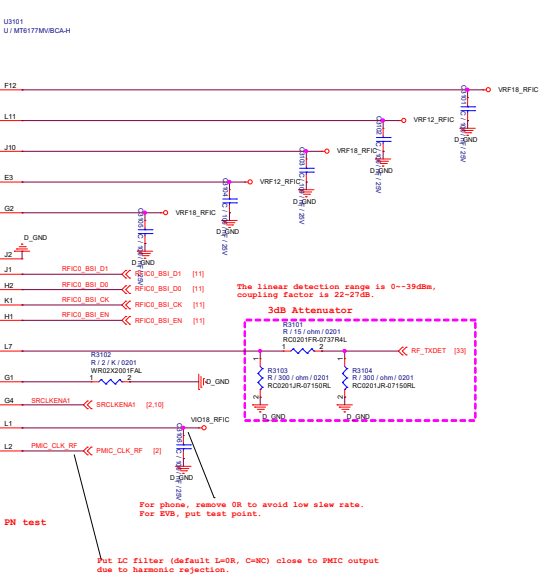
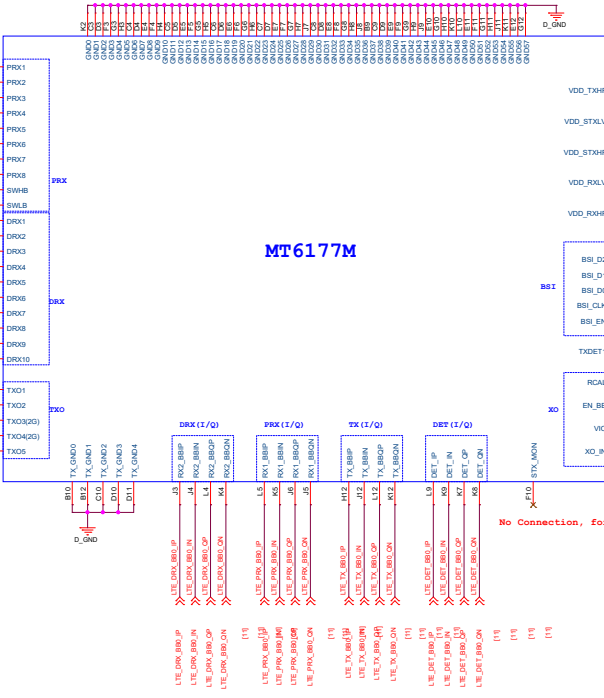
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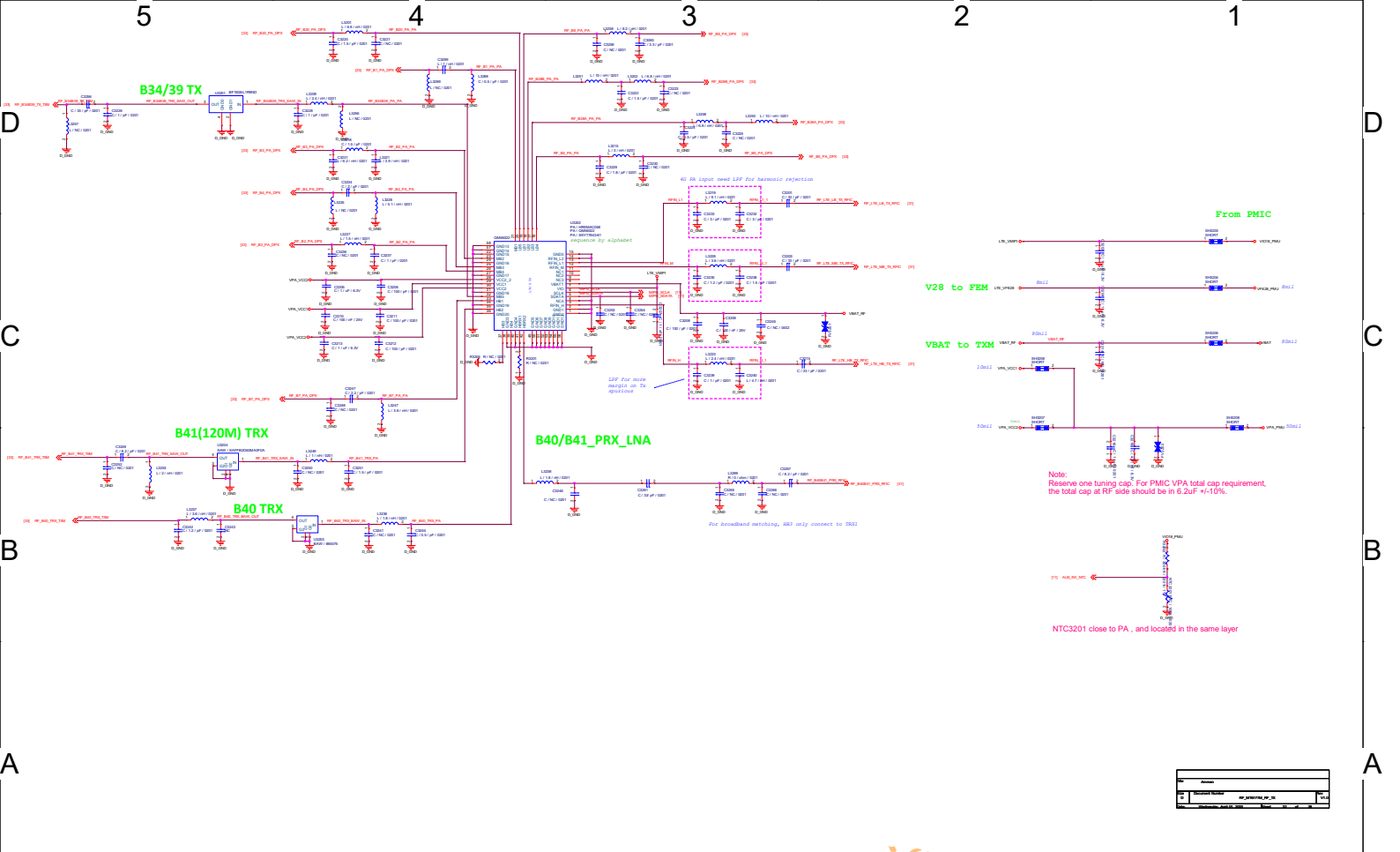


- [33] RF\_B5\_PRX\_RFIC >> RF\_B5\_PRX\_RFIC B5 PRX1
- [33] RF\_B28\_PRX\_RFIC >> RF\_B28\_PRX\_RFIC A8 PRX2
- [33] RF\_B1\_PRX\_RFIC >> RF\_B1\_PRX\_RFIC B7 PRX3
- [33] RF\_B20\_PRX\_RFIC >> RF\_B20\_PRX\_RFIC A7 PRX4
- [33] RF\_B3\_PRX\_RFIC >> RF\_B3\_PRX\_RFIC B6 PRX5
- [33] RF\_B4\_PRX\_RFIC >> RF\_B4\_PRX\_RFIC A5 PRX6
- [32] RF\_B40841\_PRX\_RFIC >> RF\_B40841\_PRX\_RFIC B5 PRX7
- [33] RF\_B7\_PRX\_RFIC >> RF\_B7\_PRX\_RFIC A4 PRX8
- [33] RF\_B2\_B3439\_PCS\_PRX\_RFIC >> RF\_B2\_B3439\_PCS\_PRX\_RFIC B4 BWH8
- [33] RF\_B8\_PRX\_RFIC >> RF\_B8\_PRX\_RFIC B3 BSW8
- [34] RF\_B38841\_DRX\_RFIC >> RF\_B38841\_DRX\_RFIC A2 DRX1
- [34] RF\_B7\_DRX\_RFIC >> RF\_B7\_DRX\_RFIC A1 DRX2
- [34] RF\_B1\_S4\_DRX\_RFIC >> RF\_B1\_S4\_DRX\_RFIC B2 DRX3
- [34] RF\_B3\_DRX\_RFIC >> RF\_B3\_DRX\_RFIC C1 DRX4
- [34] RF\_B2\_DRX\_RFIC >> RF\_B2\_DRX\_RFIC C3 DRX5
- [34] RF\_B20828\_B34\_DRX\_RFIC >> RF\_B20828\_B34\_DRX\_RFIC D1 DRX6
- [34] RF\_S3\_DRX\_RFIC >> RF\_S3\_DRX\_RFIC E2 DRX7
- [34] RF\_S4\_DRX\_RFIC >> RF\_S4\_DRX\_RFIC E1 DRX8
- [34] RF\_S5\_DRX\_RFIC >> RF\_S5\_DRX\_RFIC E2 DRX9
- [34] RF\_S8\_DRX\_RFIC >> RF\_S8\_DRX\_RFIC F2 DRX10
- [32] RF\_LTE\_HB\_TX\_RFIC >> RF\_LTE\_HB\_TX\_RFIC D12 TX01
- [32] RF\_LTE\_MB\_TX\_RFIC >> RF\_LTE\_MB\_TX\_RFIC C12 TX02
- [33] RF\_20\_HB\_TX\_RFIC >> RF\_20\_HB\_TX\_RFIC A12 TX03(20)
- [33] RF\_20\_LB\_TX\_RFIC >> RF\_20\_LB\_TX\_RFIC A10 TX04(20)
- [34] RF\_LTE\_LB\_TX\_RFIC >> RF\_LTE\_LB\_TX\_RFIC C11 TX05

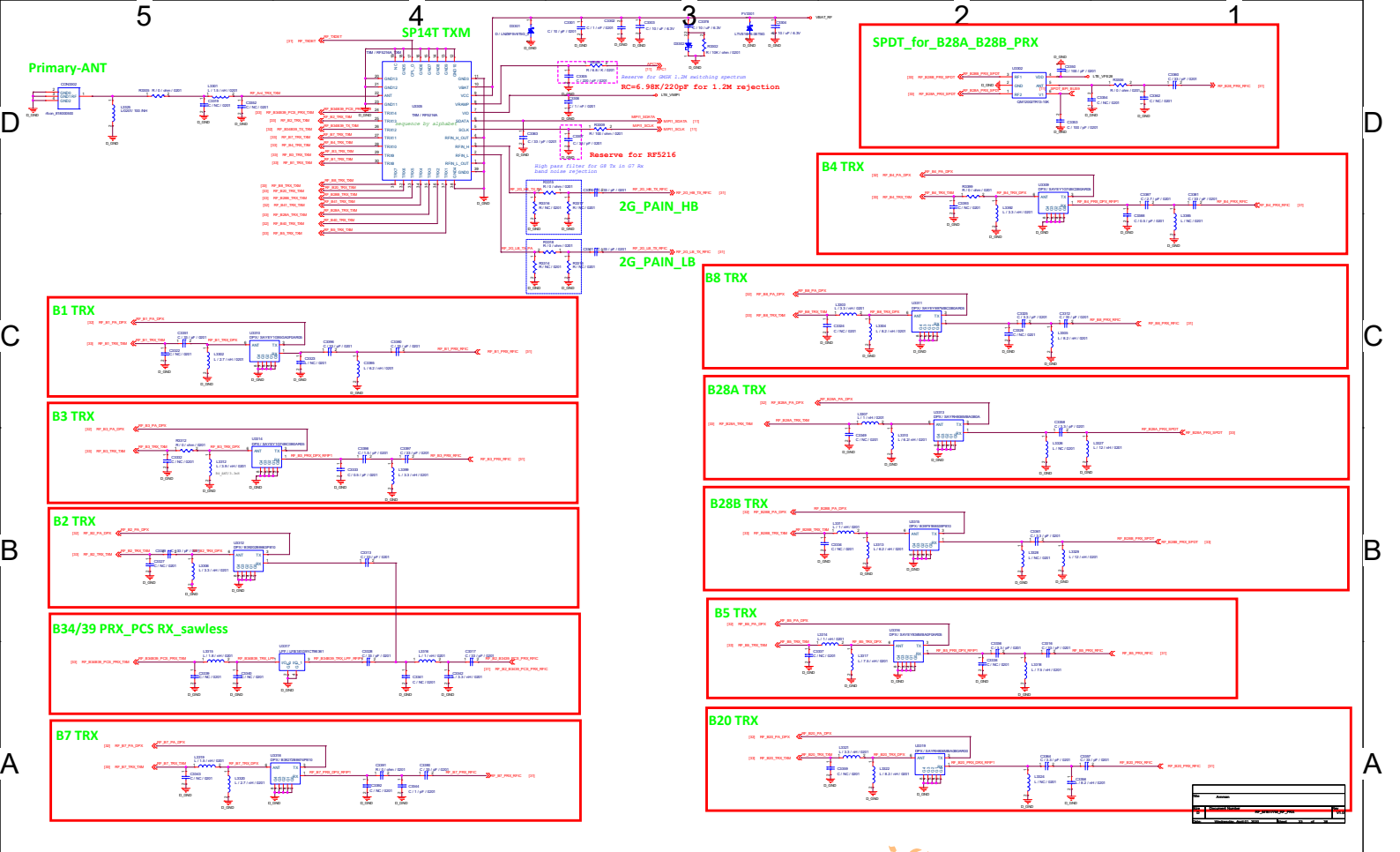


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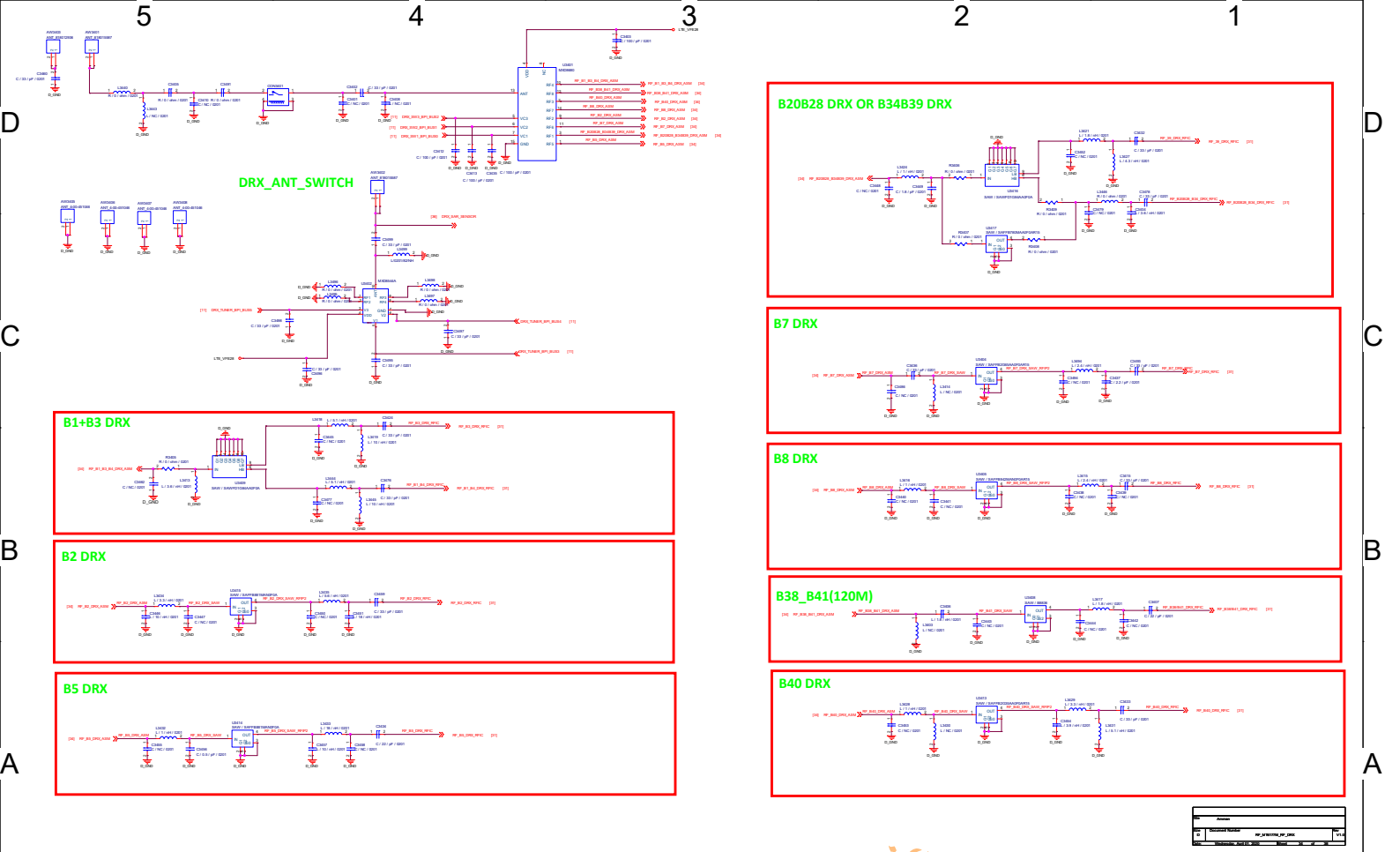




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علي البجر فريق الهارد خلب تك



علي البجر فريق الهارد خب توك

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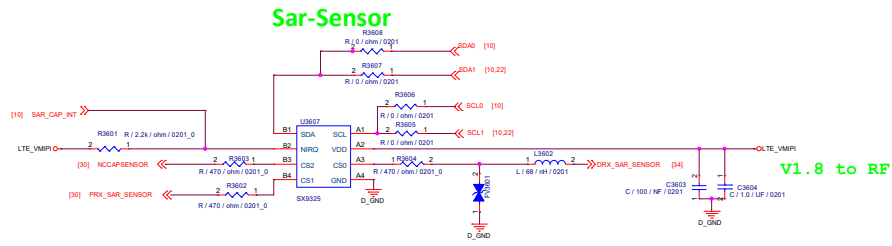
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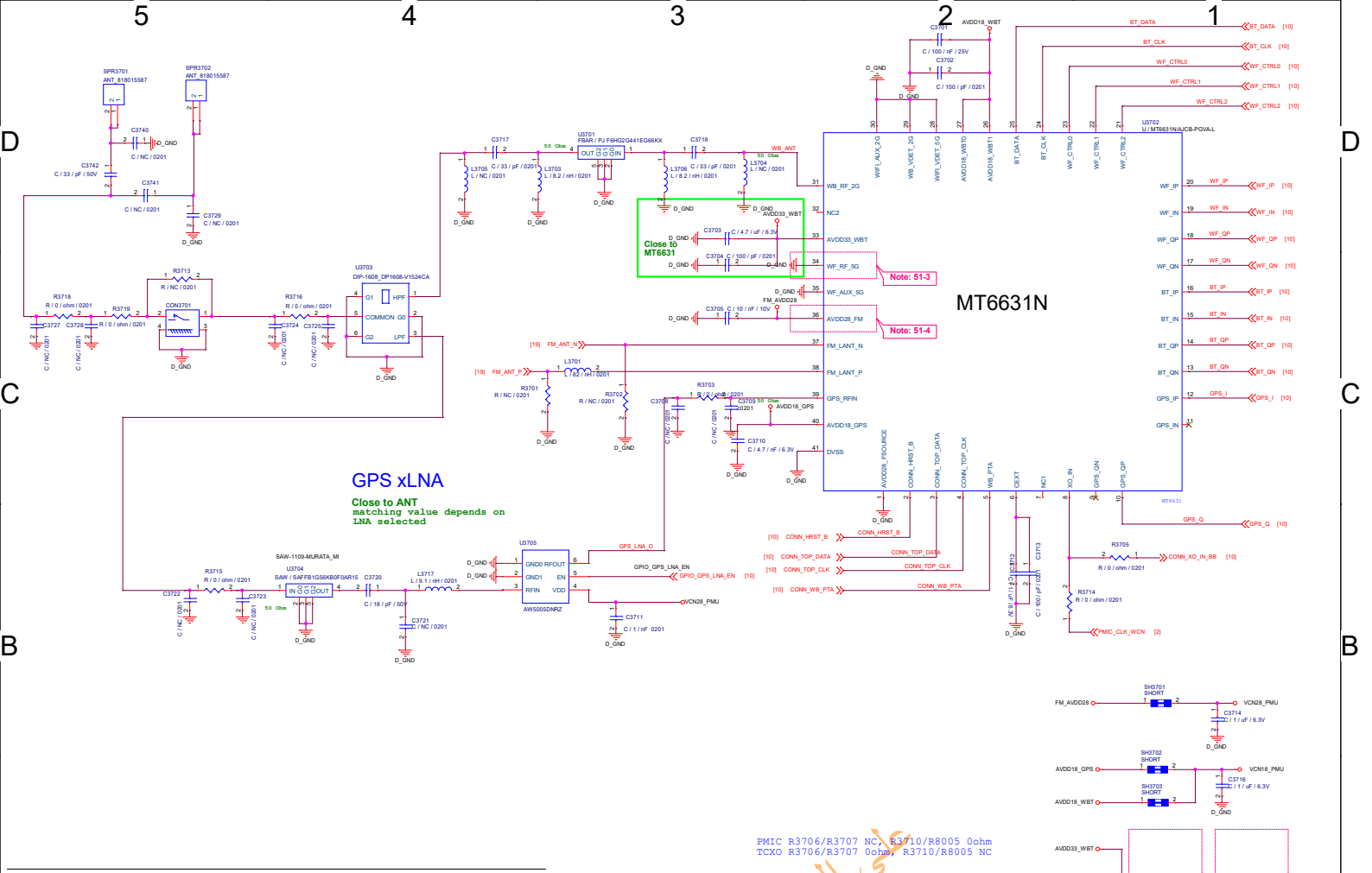
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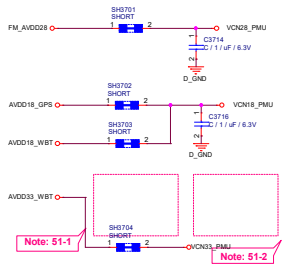
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- Note 51-1: For R3712 size, please select 0402 size or larger one
- Note 51-2: Please refer to MT6765 Baseband design notice for VCN33 LDO selection guide
- Note 51-3: If WiFi 5G not support, connect pin 34(WF\_RF\_5G) to GND
- Note 51-4: Pin 36 (AVDD28\_FM) must be connected to VCN28 even if FM not support

PMIC R3706/R3707 NC, R3710/R8005 0ohm  
 TCXO R3706/R3707 0ohm, R3710/R8005 NC



- Note: 51-1
- Note: 51-2

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