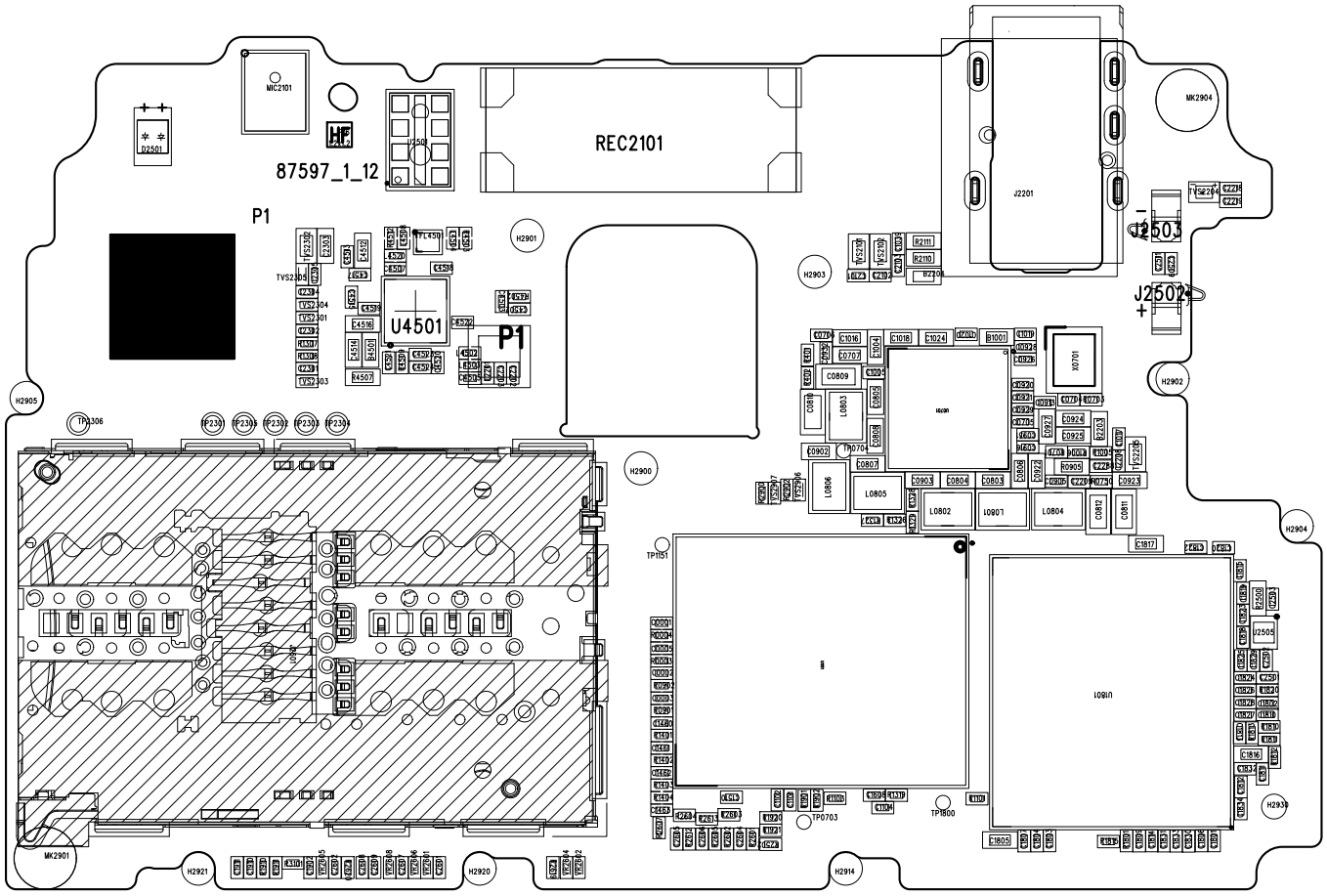
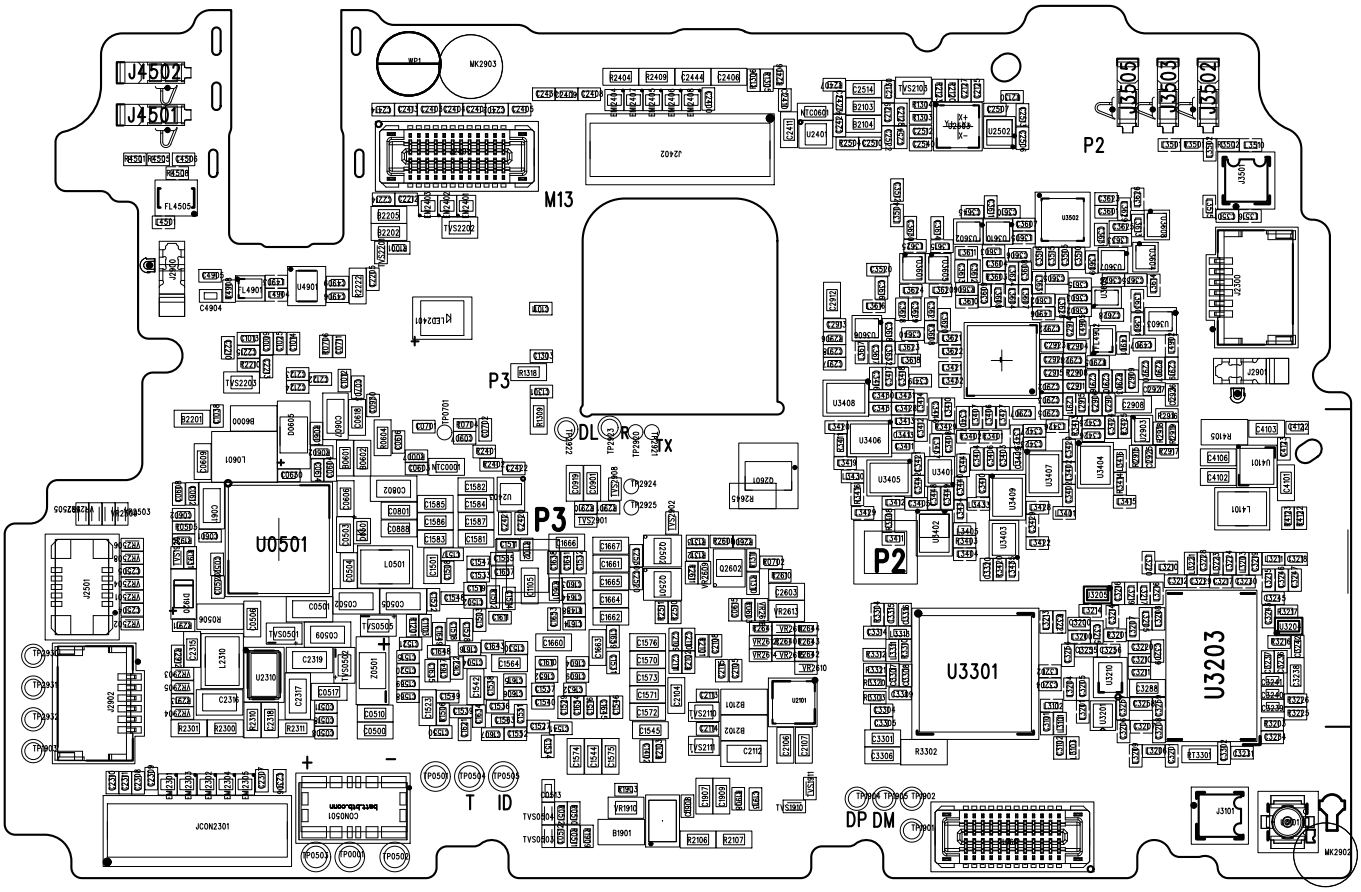
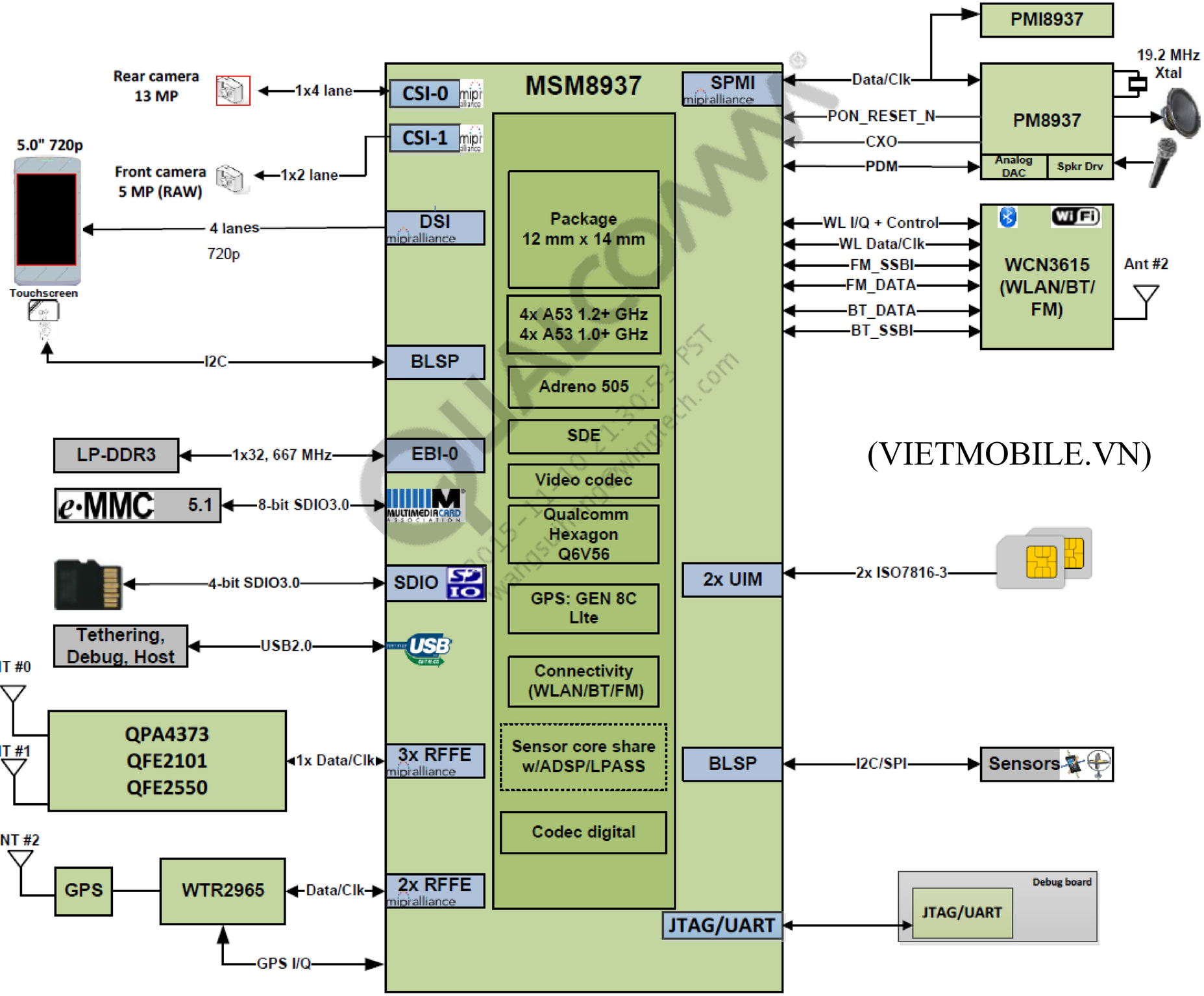
(VIETMOBILE.VN)



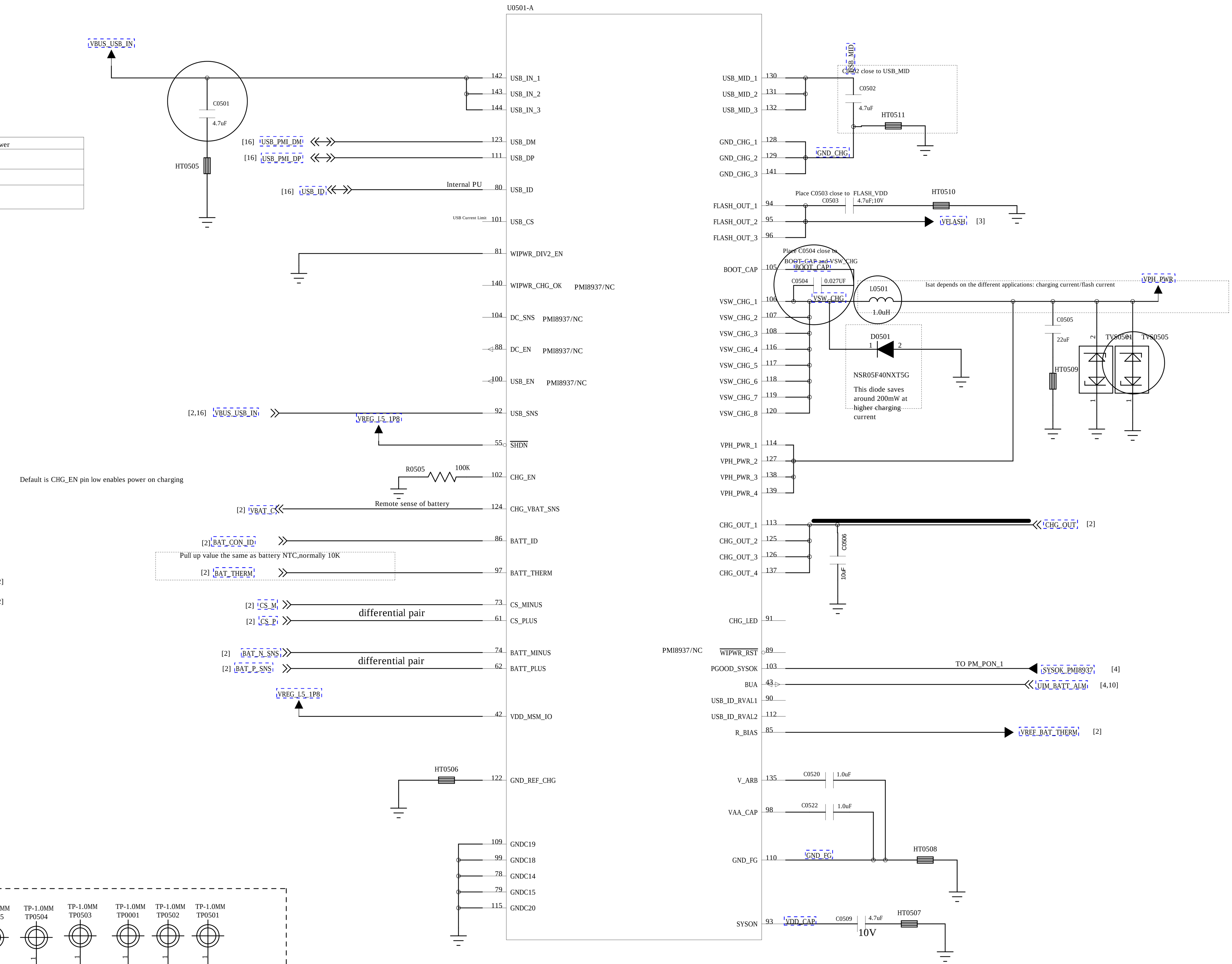
(VIETMOBILE.VN)

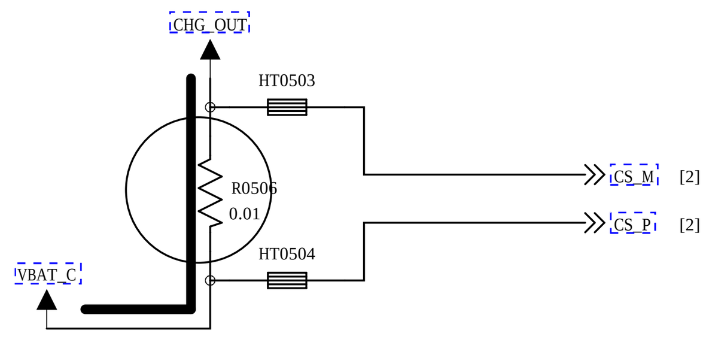




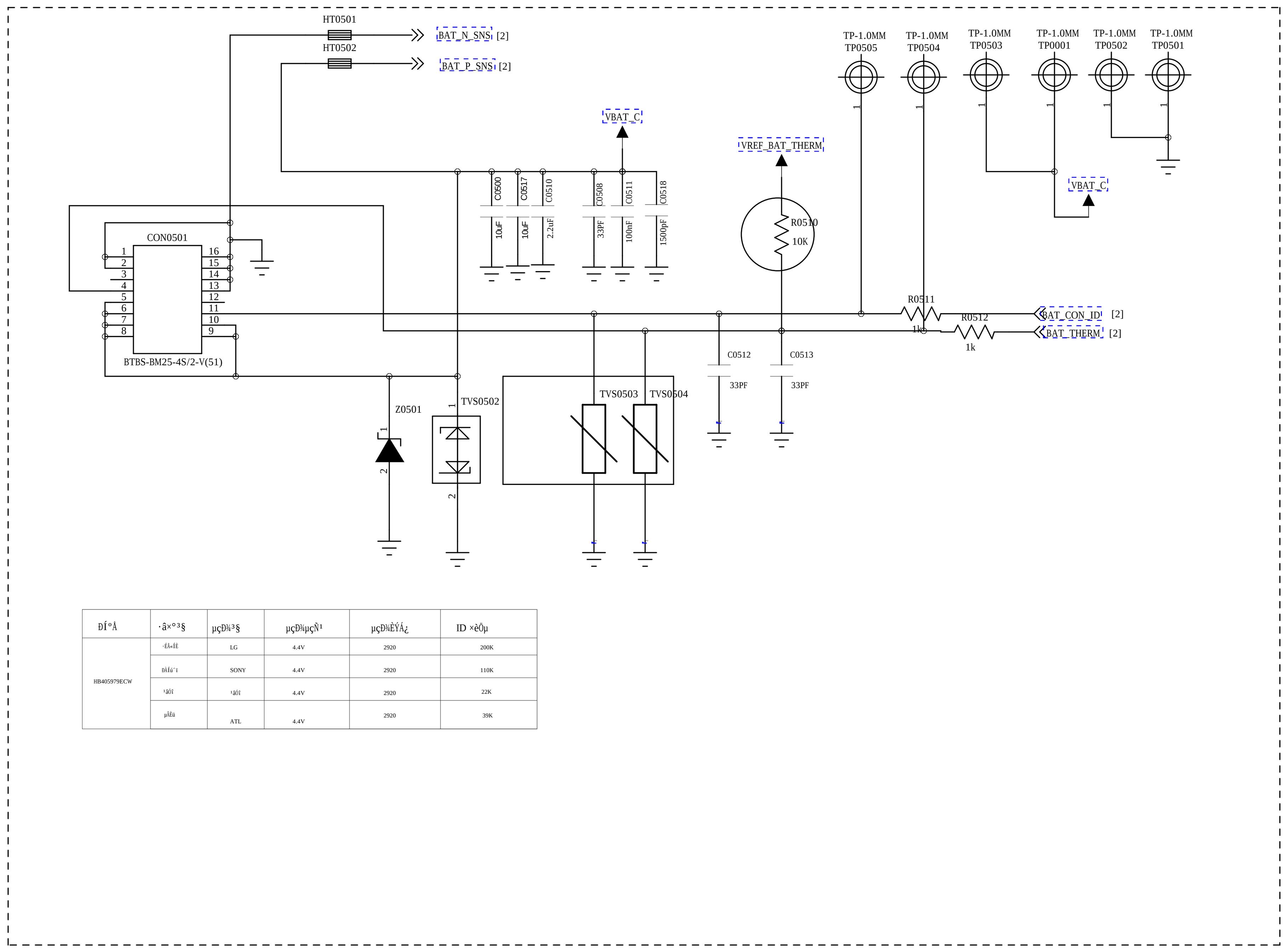
(VIETMOBILE.VN)

PMI PIN	connection on device without Wipower	connection on device with Wipower
CHG_OK	Pull up to VDD_CAP with 51kohm	Stark PRU CHG_OK
DVI2_EN	Pull down to GND with 0ohm	Stark PRU DIV2_EN
GPIO2	No Connect	10Kohm pull down to gnd





PMI_VDD_CAP net is 5VDC,cap is 0603.
Do not use 0402 as may derate to -80%.



(VIETMOBILE.VN)

U0501-B

[4,23] PM_RESIN_N\ — 68 RESIN
[4,8] SPMI_CLK — 38 SPMI_CLK
[4,8] SPMI_DATA — 39 SPMI_DATA
[4,23] XYPD_PWR_N\ — 134 XYPD_PWR
[4,8] PM_PON_RESET_N\ — 60 PS_HOLD
CLK_IN is not used — 50 CLK_IN
40 NC1
41 NC2
44 NC3
18 NC4
19 NC5
85 GPIO_1 PMI8937/NC
83 GPIO_2 PMI8937/NC
[3] CHG_THERM — 82 MPP_1
84 MPP_2
80 MPP_3 PMI8937/NC
[10] FLASH_STROBE_SYNC — 87 MPP_4
VDL_PWR — 57 VDD_ADC_LDO
49 GNDC4
45 GNDC3
87 GNDC17

VREG_ADC_LDO — 46 VREG_ADC_LDO — C0603 0.47UF
DVDD_BYP — 54 DVDD_BYP — C0602 0.1uF
AVDD_BYP — 53 AVDD_BYP — C0601 0.47UF — HT0601
REF_BYP — 58 REF_BYP_PMU — C0604 0.1uF
GND_REF — 59 GND_REF_PMU — HT0602
GNDC6 — 56
GNDC9 — 66
GNDC10 — 67
GNDC12 — 76
GNDC13 — 77
GNDC8 — 65
GNDC16 — 82
GNDC21 — 121
GNDC22 — 133
GNDC23 — 136

U0501-C

VDL_PWR
Depends on if having boost bypass
[2] VFLASH — 60 VDD_TORCH
72 VDD_FLASH_1
84 VDD_FLASH_2
VDL_PWR
[3] PGND_VLED — 7 VDD_WLED
8 GND_WLED
VDL_PWR
28 VDD_DIS_P
15 DIS_N_CAP_REF PMI8937/NC
26 GND_DIS_N_REF
VREG_L5_1P8
VDL_PWR — C0608 0.1uF
25 VDD_1PB_DIS_N
DISplay
3 VDD_DIS_N
Place C0609 close to PIN3 — C0609 1uF — HT0604
[19] LCD_CABC — 30 WLED_CABC
For AMOLED,Not needed in LCD mode. leave float if not used
internal PD — 51 DIS_SCTRL PMI8937/NC
[10] GP_PDM_OUT — R0602 100K — 11 HAP_PWM_IN1
From MSM IO or codec
12 HAP_PWM_IN2
VDL_PWR — C0614 22nF — R0601 1M +/-1%
48 VDD_HAP
C0600 10uF
36 GND_HAP
HT0605
23 GNDC1
37 GNDC2
52 GNDC5
64 GNDC7
70 GNDC11

FLASH_LED1 — 71 — [20]
FLASH_LED2 — 83
VREG_WLED — 62 — C0618 18PF — C0607 4.7uF — HT0606 — 35V
Place C0607 close to PIN8,dedicated trace from PIN8 to C0607 PGND and then a dedicated via to main GND at C0607
PGND_VLED [3]
OVP Progamable MAX 31.7V
D0605
R0604 0
LCD_BL_LED_A [19]
VDL_PWR
VSW_WLED — 9 — L0601 10UH — B6000 — C0611 10uF — C0612 18PF — HT0607 — C0610 1uF — C0630 1uF — HT0608
PMI8937 WLED has the function of output isolation/short circuit protection, need add external FET and diode if this function is needed.
GND_WLED_I — 31
WLED_SINK1 — 21 — LCD_BL_LED_K1 [19]
WLED_SINK2 — 20 — LCD_BL_LED_K2 [19]
PMI8937/NC WLED_SINK3 — 32
PMI8937/NC WLED_SINK4 — 33
PMI8937/NC VDIS_P_FB — 29
PMI8937/NC VDIS_P_OUT — 5
GND_DIS_P — 4
PMI8937/NC VSW_DISP_1 — 16
PMI8937/NC VSW_DISP_2 — 17
PMI8937/NC VDIS_N_FB — 25
PMI8937/NC VDIS_N_OUT_1 — 1
PMI8937/NC VDIS_N_OUT_2 — 13
PMI8937/NC VSW_DIS_N_1 — 7
PMI8937/NC VSW_DIS_N_2 — 14
HAP_OUT_P — 35 — R0601 1000ohm — HAPOUTP [21]
Support LRA/ERM
HAP_OUT_N — 24 — R0602 1000ohm — HAPOUTN [21]

Backup, may change to other MPP as needed
VREG_L16_1P8 [4,6]
R0603 100K +/-1%
LCM_LCD_THERM [4]
NTC0601
1%
100K
C0615 NF_0.1uf

VREG_ADC_LDO
R0007 100K +/-1%
[3] CHG_THERM
NTC0001
1%
100K
Hardware version

NTC0601 placement Ref to 80-VU794-17
Away from heat devices, such as MSM PMU Charger

X0701
XTAL-19.2M-OZ19270001

[4] PM_XO_THERM
NC
GND
XOADC_GND [4]

Note:
XO GND should connect to XOADC_GND pin using thin trace, then via to main ground plane under the XO_THERM cap ground

U0701-B
HK
PM8937

NC_WSP_TST1 85
XTAL19M2_IN 3
XTAL19M2_OUT 2
XYPDPWR_N 102
PON_1 143
PON_RESET_N 182
PS_HOLD 129
RESIN_N 128
CBLPWR_N 115
SPMI_CLK 75
SPMI_DATA 62
RFCLK1 42
RFCLK2 40
LNBBCLK 43
BB_CLK1_EN 26
BBCLK1 6
BBCLK2 44
XO_THERM 119
XOADC_GND 109
XOISO_GND1 1
XOISO_GND2 13
AVDD_BYP 127
VPP 81
VPH_PWR 63
VCOIN 132
OPT_1 87
PA_THERM 122
TEST_IN 76
VREF_LPDDR2 123
SLEEP_CLK1 74
GND_XO 14
GND_RF 15
REF_BYP 59
REF_GND 58

[3,23] XYPD_PWR_N
[2] SYSOK_PMIC
[3,8] PM_PON_RESET_N
[8] MSM_PS_HOLD
[3,23] PM_RESIN_N
[3,8] SPMI_CLK
[3,8] SPMI_DATA
[24] QTR_XO_CLK
[32] WCN_XO_CLK
[8] MSM_BBCLK1_EN
[8] BBCLK1
[3,4,6] QBTC_1P_1P8
[4] PM_XO_THERM
[4] XOADC_GND
[10,22] SD_SIM_DET_N
[2,10] VIM_BATT_ALM
[3,4] GND_XOISO
[8] SLEEP_CLK
[4] PM_XO_THERM
[4] XOADC_GND
[24] QTR_XO_CLK
[32] WCN_XO_CLK
[3,4,6] QBTC_1P_1P8
[27] PA_THERM
[8,15] VREF_LPDDR2
[8] SLEEP_CLK
[4] PM_XO_THERM
[4] XOADC_GND
[10,22] SD_SIM_DET_N
[2,10] VIM_BATT_ALM
[3,4] GND_XOISO
[8] SLEEP_CLK

VPH_PWR
C0701 1.0uF HT0703
Note:
VPP can be left floating in 1N1 design.
VREG_L6_1P8
C0706 NF_33PF
C0707 2.2uF
R0702 100K +/-1%
Internal PD
VREF_LPDDR
C0702 NF_33PF
R0704 0
C0703 0.1uF
HT0704
HT0705
R0706 0
C0711 33PF_NF
R0701 0
C0705 33PF_NF
Note:
Reserve placeholder C0705 for BBCLK signal quality
Place R0701 C0705 near PM8937
R0703 100K +/-1%
C0704 1nF
HT0702
HT0701

Note
GND_REF MUST connect directly to C0703 and then to main GND with a dedicated via.
GND_XO and GND_RF MUST connect directly to C0920 and C0921 respectively and then connect to main GND with dedicated via.

U0701-C
UI
PM8937

GPIO_01 22
GPIO_02 38
GPIO_03 50
GPIO_04 36
GPIO_05 49
GPIO_06 25
GPIO_07 141
GPIO_08 152
MPP_01 137
MPP_02 151
MPP_03 131
MPP_04 89

[10,22] SD_SIM_DET_N
[2,10] VIM_BATT_ALM
R0750 NF
R401 240K
VDD_PX_BIAS_MPP_1 [12]
VREG_L6_1P8
VBIAS_DAC_MPP_3 [11]
QUIET_THERM [3]
R402 0K
Note:
Only even MPP's can be configured as current sinks and odd MPP's as analog output buffers.

R401	R402	ADC_PU	pvpp33
240k	30k	0.2v	MPTHTA61
82.5k	30k	0.48v	MPTHTA61
41.2k	30k	0.75dv	
22k	30k	1.428v	
10k	30k	1.917v	
3.92k	30k	1.59ov	

U0701-F
GND_NC
PM8937

GND1 57
GND2 71
GND3 72
GND4 73
GND5 83
GND6 84
GND7 86
GND8 97
GND9 98
GND10 99
GND11 100
GND12 110
GND13 114
NC1 136
NC2 138
NC3 142

U0701-D

VREG1

PM8937

VDD_PWR

C0800 33nF

C0801 33nF

C0802 22nF

C0803 2.2uF

C0804 2.2uF

C0805 2.2uF

C0806 2.2uF

C0807 2.2uF

C0808 2.2uF

HT18

HT19

HT20

HT21

HT22

HT23

GND_S1

GND_S2

GND_S3

GND_S4

GND_S5

GND_S6

[5] GND_S3

[5] GND_S4 [8]

39 VIN_S1

65 GND_S1_1

66 GND_S1_2

77 VIN_S2_1

78 VIN_S2_2

79 VIN_S2_3

103 GND_S2_1

104 GND_S2_2

105 GND_S2_3

164 VIN_S3_1

176 VIN_S3_2

154 GND_S3_1

166 GND_S3_2

178 GND_S3_3

9 VIN_S4

11 GND_S4_1

24 GND_S4_2

156 VIN_S5_1

170 VIN_S5_2

183 VIN_S5_3

144 GND_S5_1

145 GND_S5_2

171 GND_S5_3

167 VIN_S6_1

179 VIN_S6_2

169 GND_S6_1

181 GND_S6_2

VFB_S1 64

VSW_S1_1 51

VSW_S1_2 52

L0801 1.0uH

Rated for 3A

Power for MSM Modem

Remote sense from MSM side

VREG_S1_1P225_RE [13]

VREG_S1_1P225 [13]

VFB_S2 88

VSW_S2_1 90

VSW_S2_2 91

L0802 1.0uH

Rated for 3A

Power for MSM Core&GBA

Remote sense from MSM side

VREG_S2_1P225_RE [12]

VREG_S2_1P225 [12,13]

Sense node from output caps

Note:
Buck input and Output cap ground of each switch regulator should be
directly connected to their respective GND pins, then connect to main ground with dedicated vias

VSW_S3_1 153

VSW_S3_2 165

VSW_S3_3 177

L0803 2.2uh

Rated for 2.7A

Power for Low-voltage LDOs

C0809 22uF

C0810 22uF

VREG_S3_1P225 [6,20]

GND_S3 [5]

VSW_S4_1 10

VSW_S4_2 23

VSW_S4_3 37

L0804 2.2uh

Rated for 2.5A

Power for High-voltage LDOs

C0811 22uF

C0812 22uF

VREG_S4_1P95 [6,7]

GND_S4 [5]

VFB_S5 116

VSW_S5_1 157

VSW_S5_2 158

L0805 0.47uh

Rated for 3A

Power for MSM APC

VREG_S5_S6_APC_1P225 [12]

VFB_S6 101

L0806 0.47uh

Rated for 3A

VSW_S6_1 155

VSW_S6_2 168

VSW_S6_3 180

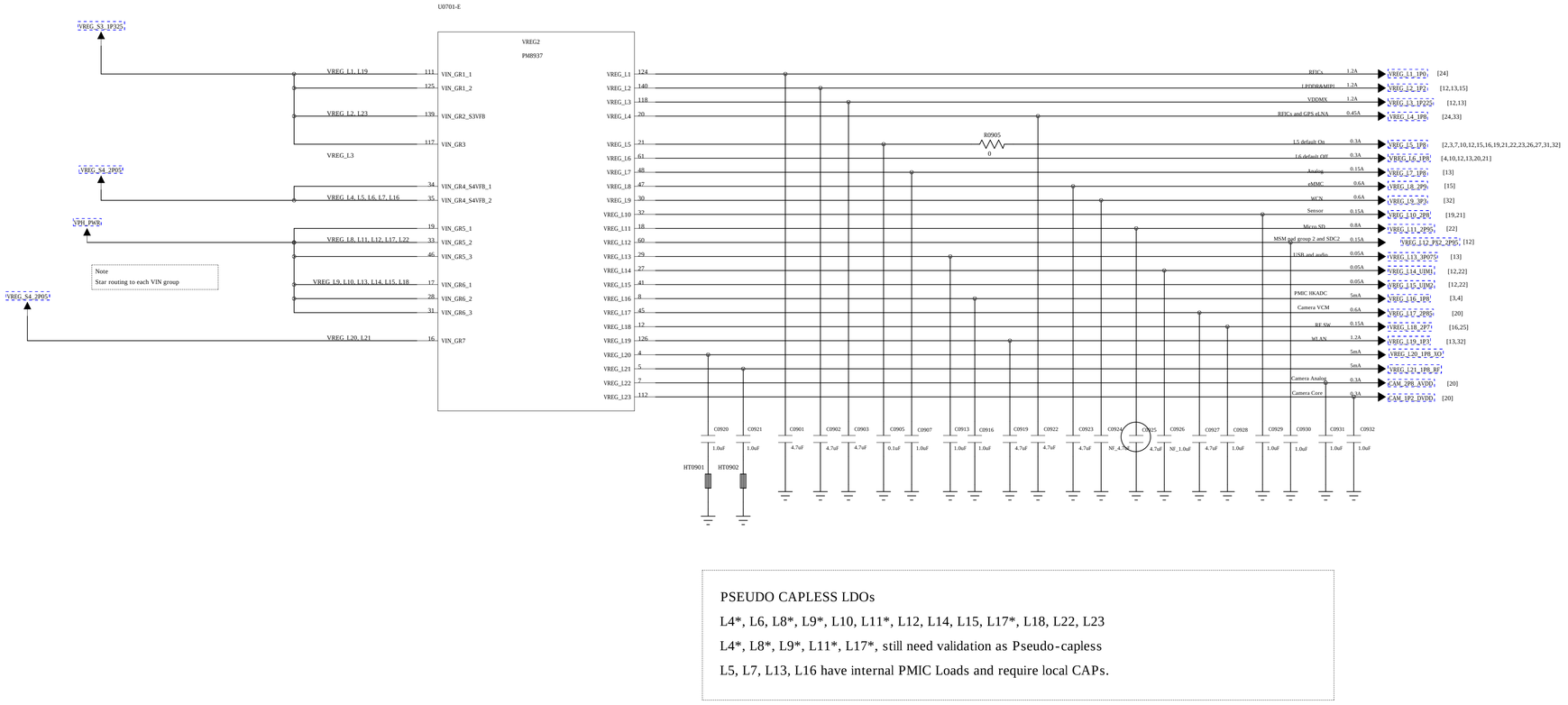
Remote sense from MSM side

VFB_S5_S6_C [12]

VREF_NEG_S5 130

VREF_NEG_S6 113

VFB_S5_S6_A [12]



PSEUDO CAPLESS LDOs

L4*, L6, L8*, L9*, L10, L11*, L12, L14, L15, L17*, L18, L22, L23

L4*, L8*, L9*, L11*, L17*, still need validation as Pseudo-capless

L5, L7, L13, L16 have internal PMIC Loads and require local CAPs.

U0701-A

CDC

PM8937

[17] MIC_IN1_P

[17] MIC_IN1_M

[18] MIC_IN2_P

[17] MIC_IN3_P

[16,17] MIC_BIAS1

MIC_BIAS2

C1011 0.1uF

C1012 NF_0.1uF

C1038 NF_100PF

C1039 NF_100PF

Place near PM8937

106 SPKR_DRV_P

107 SPKR_DRV_M_1

121 SPKR_DVR_M_2

56 MIC1_IN_P

69 MIC1_IN_M

108 MIC2_IN_P

95 MIC3_IN_P

82 MIC_BIAS1

96 MIC_BIAS2

[17] PM_EAR_P

[17] PM_EAR_M

92 EAR_P

93 EAR_M

[10] CDC_PDM_CLK

[10] CDC_PDM_SYNC

[10] CDC_PDM_TX

[10] CDC_PDM_RX0

[10] CDC_PDM_RX1

[10] CDC_PDM_RX2

174 PDM_CLK

175 PDM_SYNC

149 PDM_TX

150 PDM_RX0

173 PDM_RX1

159 PDM_RX2

C1016 2.2uF

CP_C1_P

CP_C1_N

147 NCP_FLY_P

133 NCP_FLY_N

10V

134 NCP_VNEG

B1001 120ohm

CDC_PA_VNEG

68 PA_VNEG

C1018 2.2uF

C1019 1.0uF

GND_CP [7]

VDDIO 163

VDD_PA 67

VDD_CP 148

VDD_SPKDRV 94

VREG_BOOST_5V 162

BOOST_SW 161

BOOST_SNS 135

VREG_L_1P8 [2,3,6,10,12,15,16,19,21,22,23,26,27,31,32]

VREG_S4_2P05 [5,6,7]

C1020 1.0uF

C1005 0.1uF

VREG_S4_2P05 [5,6,7]

C1004 2.2uF

GND_CP [7]

VDD_PA [2,3,4,5,6,17,19,20,21,27,31]

C1024 2.2uF

10V?

GND_SPK [7]

Place C1024 near pin89

HPH_REF 53

HPH_L 54

HPH_R 55

HS_DET 80

GND_CP 146

GND_CFILT 70

GND_SPKDRV 120

GND_BOOST_1 160

GND_BOOST_2 172

CDC_HPH_REF [17,18]

CDC_HPH_L [18]

CDC_HPH_R [17,18]

R1001 20K

CDC_HS_DET [8]

C1009 0.01uF

C1013 4700PF

C1014 680PF

GND_CP [7]

HT1005

GND_CFILT

R1005 0

PM_GND_MIC [17,18]

R1006 NF_0

C1017 NF_33PF

HT1004

GND_SPK [7]

GND_BOOST

HT1001

HT1002

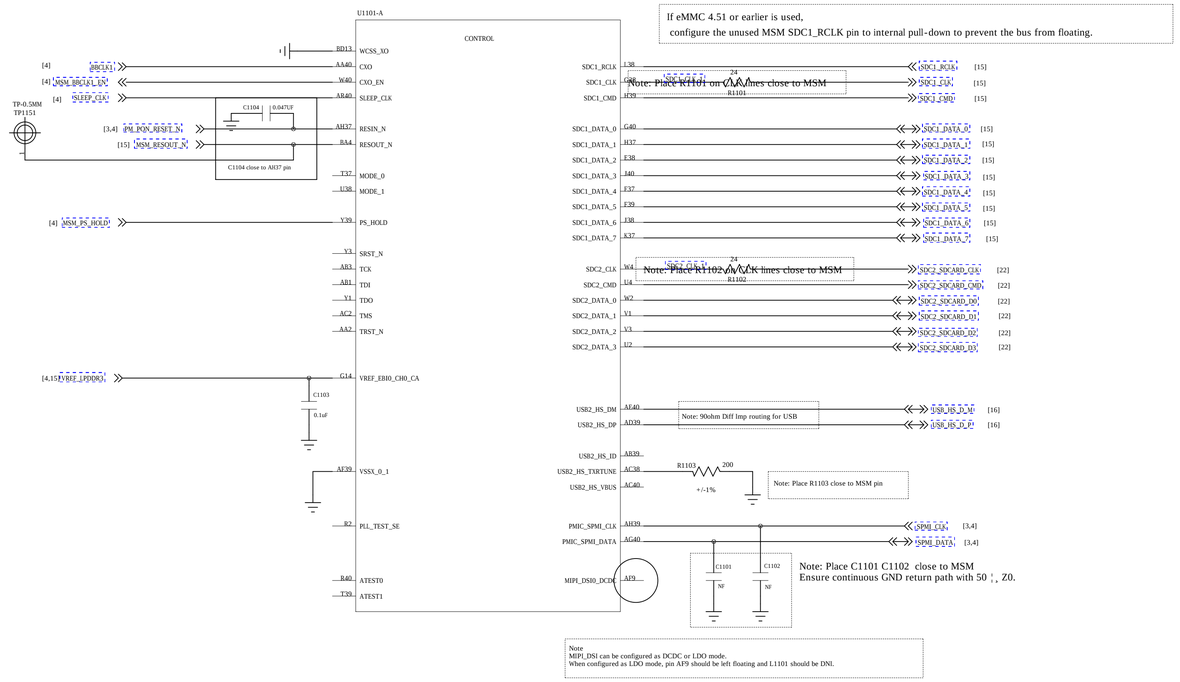
HT1003

1) Please connect GND_CP (pin 146) to C1004 GND.
Then connect to main PCB GND from C1004.

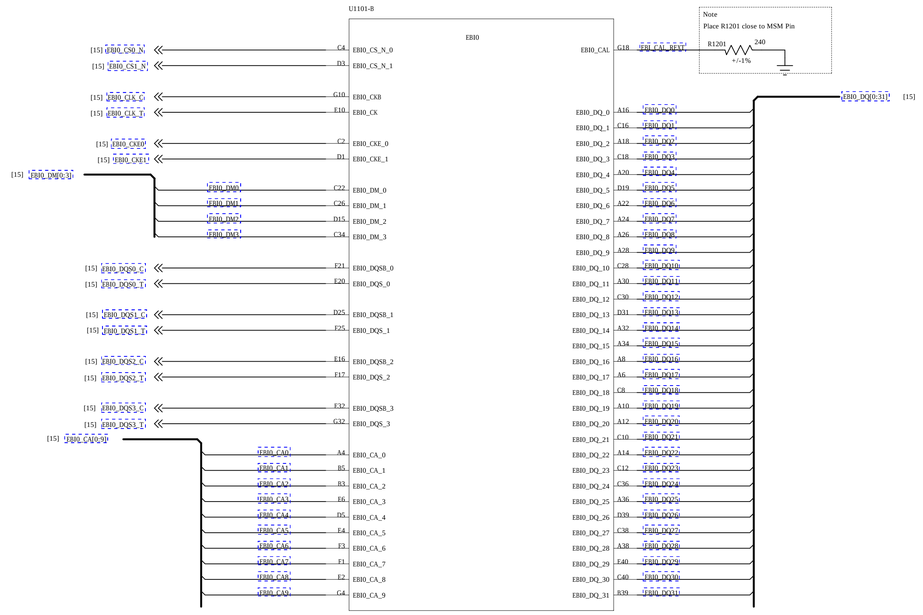
2) Please connect GND_SPKR_PA (pin 120) to C1024 GND.
Then connect to Main PCB GND from C1024.

3) Please connect GND_BOOST (pins 151/152) to C1022/C1023 GND.
Then connect to Main PCB GND from C1022/C1023.

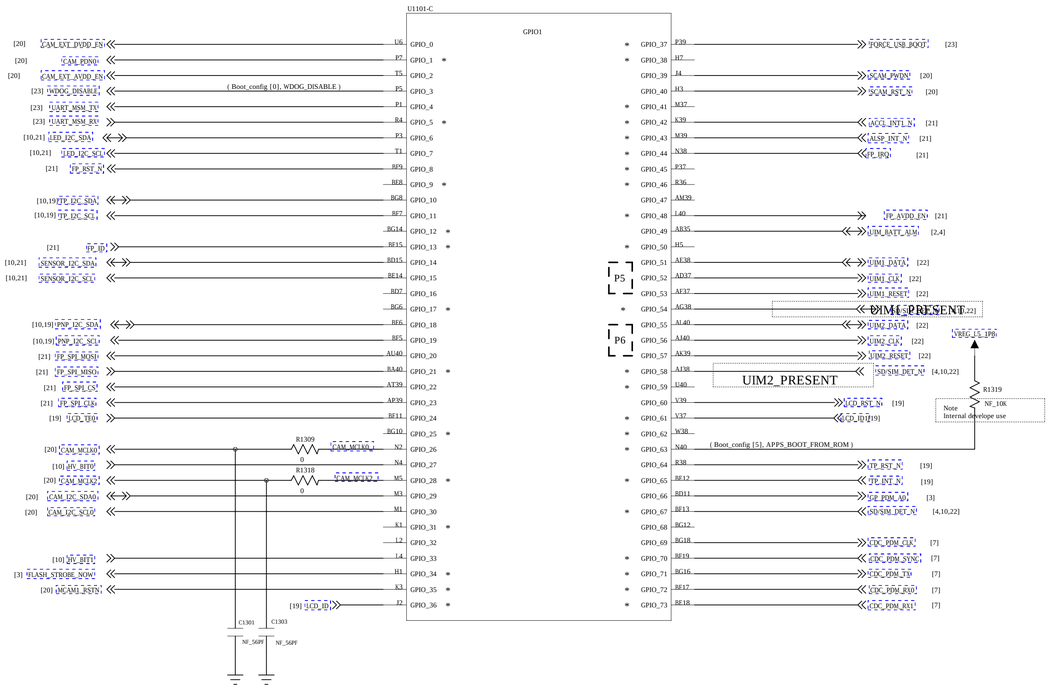
Note: WCSS_XO signal required only for 5GHZ.
When using WCN3615 connect pin BD13 to GND.

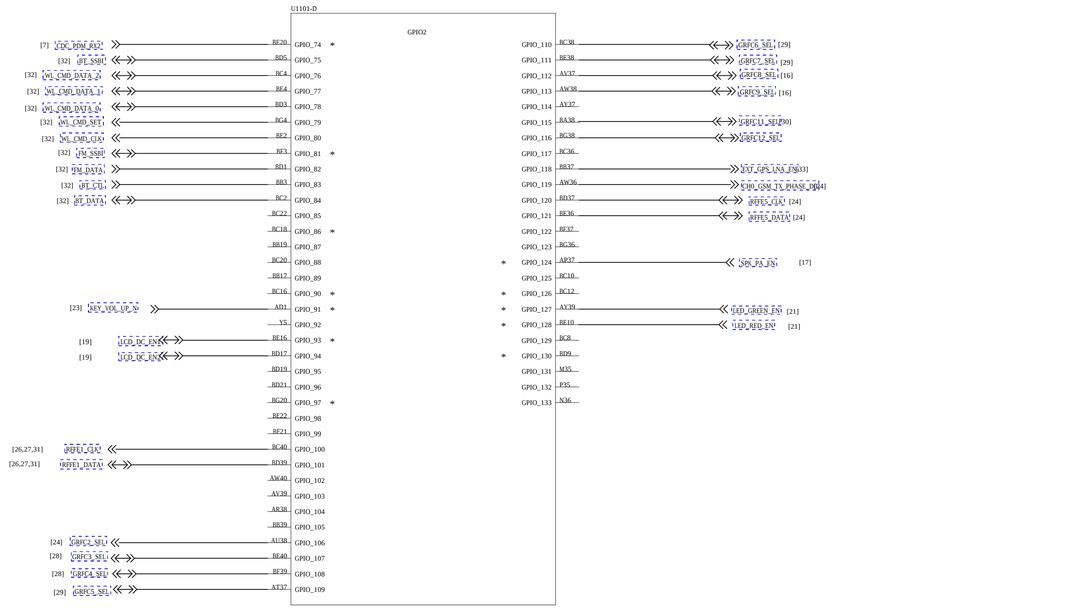


DC-DC mode ¨C For better power ~3 mA lower


U1101-8
EBI0
EBI0_CS_N_0
EBI0_CS_N_1
EBI0_CKB
EBI0_CK
EBI0_CXE_0
EBI0_CXE_1
EBI0_DM_0
EBI0_DM_1
EBI0_DM_2
EBI0_DM_3
EBI0_DQS8_0
EBI0_DQS_0
EBI0_DQS8_1
EBI0_DQS_1
EBI0_DQS8_2
EBI0_DQS_2
EBI0_DQS8_3
EBI0_DQS_3
EBI0_CA_0
EBI0_CA_1
EBI0_CA_2
EBI0_CA_3
EBI0_CA_4
EBI0_CA_5
EBI0_CA_6
EBI0_CA_7
EBI0_CA_8
EBI0_CA_9
EBI0_CAL
EBI0_DQ_0
EBI0_DQ_1
EBI0_DQ_2
EBI0_DQ_3
EBI0_DQ_4
EBI0_DQ_5
EBI0_DQ_6
EBI0_DQ_7
EBI0_DQ_8
EBI0_DQ_9
EBI0_DQ_10
EBI0_DQ_11
EBI0_DQ_12
EBI0_DQ_13
EBI0_DQ_14
EBI0_DQ_15
EBI0_DQ_16
EBI0_DQ_17
EBI0_DQ_18
EBI0_DQ_19
EBI0_DQ_20
EBI0_DQ_21
EBI0_DQ_22
EBI0_DQ_23
EBI0_DQ_24
EBI0_DQ_25
EBI0_DQ_26
EBI0_DQ_27
EBI0_DQ_28
EBI0_DQ_29
EBI0_DQ_30
EBI0_DQ_31
Note
Place R1201 close to MSM Pin
R1201
240
+-1%
[15]

Note: Asterisks (*) indicate modem power management (MPM) wake-up pins





Note: Do not have pull-ups on the following GPIOs unless intend for boot or secure- boot related configurations:
GPIO_91, 107, 109

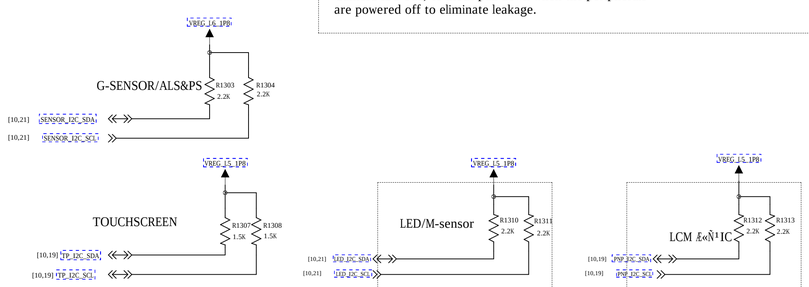
GPIO	BOOT_CONFIG
GPIO_3	BOOT_CONFIG[0]/WDOG_DISABLE
GPIO_111	BOOT_CONFIG[1]
GPIO_112	BOOT_CONFIG[2]
GPIO_88	BOOT_CONFIG[3]

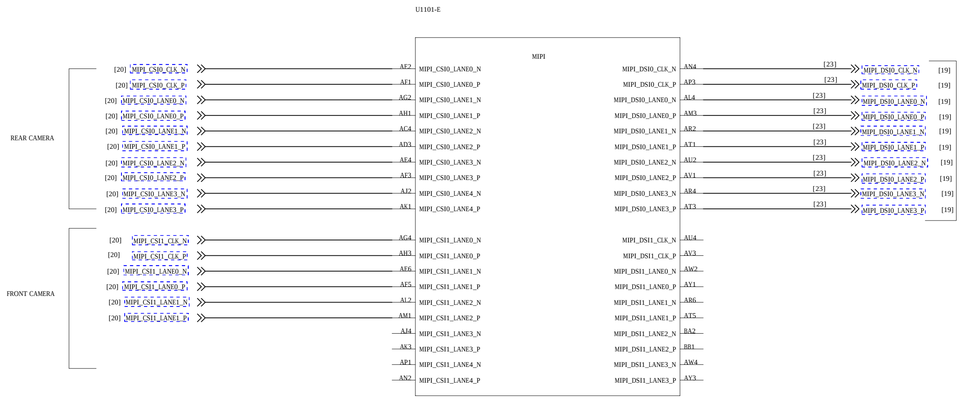
BOOT_CONFIG[3:1]	BOOT_CONFIG
0b000	SDC1 -> SDC2 -> USB2.0
0b010	SDC1
0b100	SDC2-> SDC1

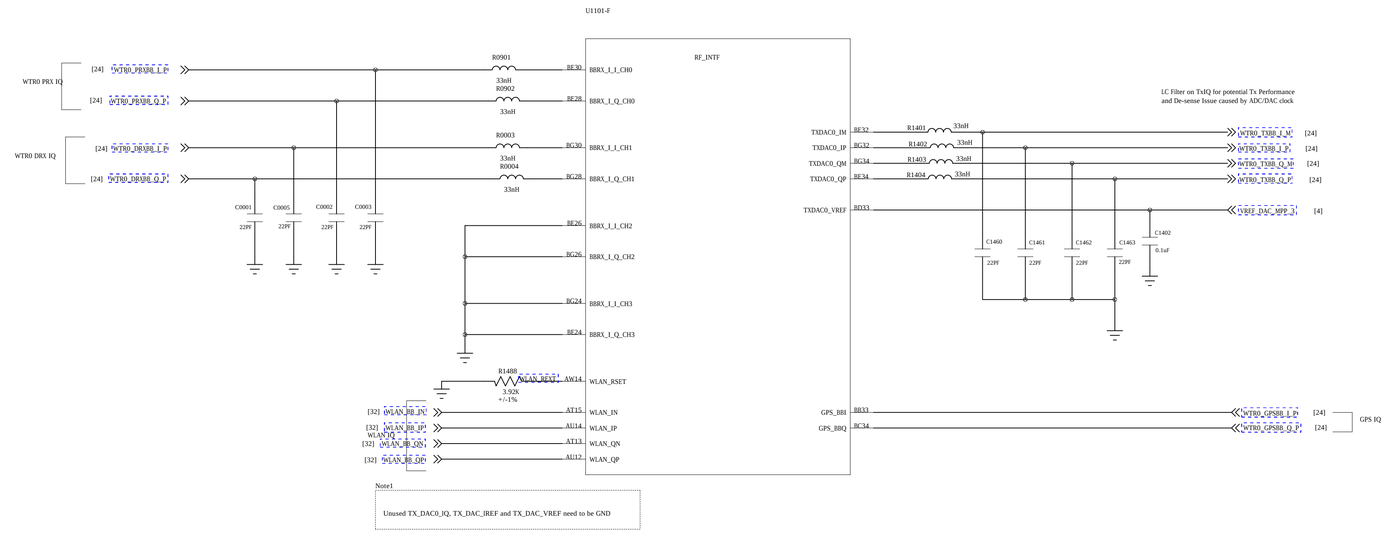
Default Boot Config (0b000) is SDC1(eMMC)

I2C PULL-UP RESISTORS

Note: Ensure SW sets these GPIOs (Sensor, CTP and Camera I2C bus) to inout pull down when the peripherals are powered off to eliminate leakage.







Note: If best EMI practices are followed for MIPI CSI/DSI signals, there is no need for common mode choke filters. You may choose to have placeholders for common mode depending upon your design constraints.
Extreme care must be taken that no stubs are created by doing so.

Power for on-chip memory

U1101-G

PWR1

VBFG_13_1P225_[6,13]

(VDD_MX)

C1501 4.7uF, C1508 1.0uF

AU30 VDDMX_TXDAC0

VDDMX_1_1 J34, VDDMX_1_2 K9, VDDMX_1_3 K33, VDDMX_1_4 M9, VDDMX_1_5 P19, VDDMX_1_6 T11, VDDMX_1_7 T17, VDDMX_1_8 T19, VDDMX_1_9 U36, VDDMX_1_10 V13, VDDMX_1_11 V35, VDDMX_1_12 Y13, VDDMX_1_13 Y15, VDDMX_1_14 AB15, VDDMX_1_15 AD19, VDDMX_1_16 AD21, VDDMX_1_17 AF13, VDDMX_1_18 AF15, VDDMX_1_19 AH33, VDDMX_1_20 AJ32, VDDMX_1_21 AK29, VDDMX_1_22 AK31, VDDMX_1_23 AL30, VDDMX_1_24 AM33, VDDMX_1_25 AN34, VDDMX_1_26 AP9, VDDMX_1_27 AP17, VDDMX_1_28 AP21, VDDMX_1_29 AP25, VDDMX_1_30 AT9, VDDMX_1_31 AT21, VDDMX_1_32 AT33

Cap depend on PDN simulation

C1527 0.1uF, C1528 NF_1.0uF, C1529 1.0uF, C1530 NF_0.1uF

QFPROM_BLOW_VDD Y17

C1502 0.1uF

R1502 0

VBFG_16_1P8 [4,6,10,13,20,21]

VDDPX_VBIAS_SDC V5

VDDPX_VBIAS_UIM AN40

VDD_PX_BIAS_MPP_0 [4]

C1510 0.1uF, C1511 0.1uF

VDD_APC_1 M27, VDD_APC_2 N26, VDD_APC_3 N28, VDD_APC_4 P27, VDD_APC_5 P31, VDD_APC_6 P33, VDD_APC_7 R26, VDD_APC_8 R32, VDD_APC_9 T33, VDD_APC_10 U28, VDD_APC_11 U30, VDD_APC_12 U32, VDD_APC_13 V27, VDD_APC_14 V29, VDD_APC_15 W30, VDD_APC_16 Y29, VDD_APC_17 Y31, VDD_APC_18 AA26, VDD_APC_19 AA30, VDD_APC_20 AB25, VDD_APC_21 AB31, VDD_APC_22 AC26, VDD_APC_23 AC32, VDD_APC_24 AD25, VDD_APC_25 AD31, VDD_APC_26 AE28, VDD_APC_27 AE27, VDD_APC_28 AF29, VDD_APC_29 AG28, VDD_APC_30 AG32, VDD_APC_31 AH27, VDD_APC_32 AH31, VDD_APC_33 AJ26, VDD_APC_34 AJ30, VDD_APC_35 AL34, VDD_APC_36 AM35, VDD_APC_37 AM37, VDD_APC_38 AN36, VDD_APC_39 AN38

(VDD_APC)

Cap depend on PDN simulation

VBFG_S5_SC_APC_1P225 [5]

HT1504, HT1505

VDD_S5_SC_N [5]

C1540 0.1uF, C1541 NF_0.1uF, C1542 NF_2.2uF, C1544 10pF, C1545 10pF, C1570 10pF, C1571 10pF, C1572 10pF, C1573 10pF, C1574 10pF, C1575 10pF, C1576 10pF

Depopulated VIA to MSM GND

C1536 0.1uF, C1537 1.0uF, C1538 1.0uF, C1539 NF_0.1uF

Note:
HTR1501 are used to help show that the sense Bulk caps C1567/C1557/C1558 are close to the MSM and the sense line feeding back to the PMIC should be placed after the caps.

Note:
HTR1504/HTR1505 are used to help show that the sense Bulk caps C1560/C1566/C1544/C1545 are close to the MSM and the sense line feeding back to the PMIC should be placed after the caps.

HT1501

VBFG_S2_1P225_[5,13]

Cap depend on PDN simulation

C1491 NF_30pF, C1502 NF_30pF, C1503 10pF, C1504 10pF, C1506 10pF, C1507 10pF

Depopulated VIA to MSM GND

(VDD_CX)

C1564 2.2uF, C1563 NF_1.0uF, C1514 1.0uF, C1503 NF_0.1uF

C1516 0.1uF, C1517 NF_0.1uF, C1518 NF_0.1uF, C1504 NF_0.1uF, C1519 0.1uF

U1101-H

PWR2

VDDCX_1_1 K35, VDDCX_1_2 P9, VDDCX_1_3 P11, VDDCX_1_4 P15, VDDCX_1_5 P17, VDDCX_1_6 P25, VDDCX_1_7 R34, VDDCX_1_8 T9, VDDCX_1_9 T23, VDDCX_1_10 T25, VDDCX_1_11 V9, VDDCX_1_12 V15, VDDCX_1_13 V17, VDDCX_1_14 V25, VDDCX_1_15 Y9, VDDCX_1_16 Y11, VDDCX_1_17 Y21, VDDCX_1_18 Y23, VDDCX_1_19 Y25, VDDCX_1_20 AA32, VDDCX_1_21 AB13, VDDCX_1_22 AB21, VDDCX_1_23 AB23, VDDCX_1_24 AD13, VDDCX_1_25 AD15, VDDCX_1_26 AD23, VDDCX_1_27 AE26, VDDCX_1_28 AF19, VDDCX_1_29 AF21, VDDCX_1_30 AF23, VDDCX_1_31 AF25, VDDCX_1_32 AG26, VDDCX_1_33 AK11, VDDCX_1_34 AK13, VDDCX_1_35 AM11, VDDCX_1_36 AP11, VDDCX_1_37 AP23, VDDCX_1_38 AP35, VDDCX_1_39 AT23, VDDCX_1_40 AV33

(VDD_PX1)
(LPDDR)

VBFG_13_1P225_[6,13,15]

VDDPX_1_1 H27, VDDPX_1_2 J12, VDDPX_1_3 J14, VDDPX_1_4 J16, VDDPX_1_5 J18, VDDPX_1_6 J20, VDDPX_1_7 J22, VDDPX_1_8 J28, VDDPX_1_9 J30

C1515 0.1uF, C1520 0.1uF, C1521 0.1uF, C1522 0.1uF, C1569 1.0uF, C1568 1.0uF, C1523 2.2uF

VBFG_1_12_P2_2P95_[6]

C1565 1.0uF

VDDPX_2 W6

VBFG_1_1P8

(VDD_PX3(HD))

U1506 0 For current measurement

VDDPX_3_1 AD35, VDDPX_3_2 AH35, VDDPX_3_3 AW10, VDDPX_3_4 BA36, VDDPX_3_5 BR21, VDDPX_3_6 K11, VDDPX_3_7 K31, VDDPX_3_8 T7, VDDPX_3_9 V7

C1531 0.1uF, C1532 0.1uF, C1533 1.0uF, C1534 1.0uF

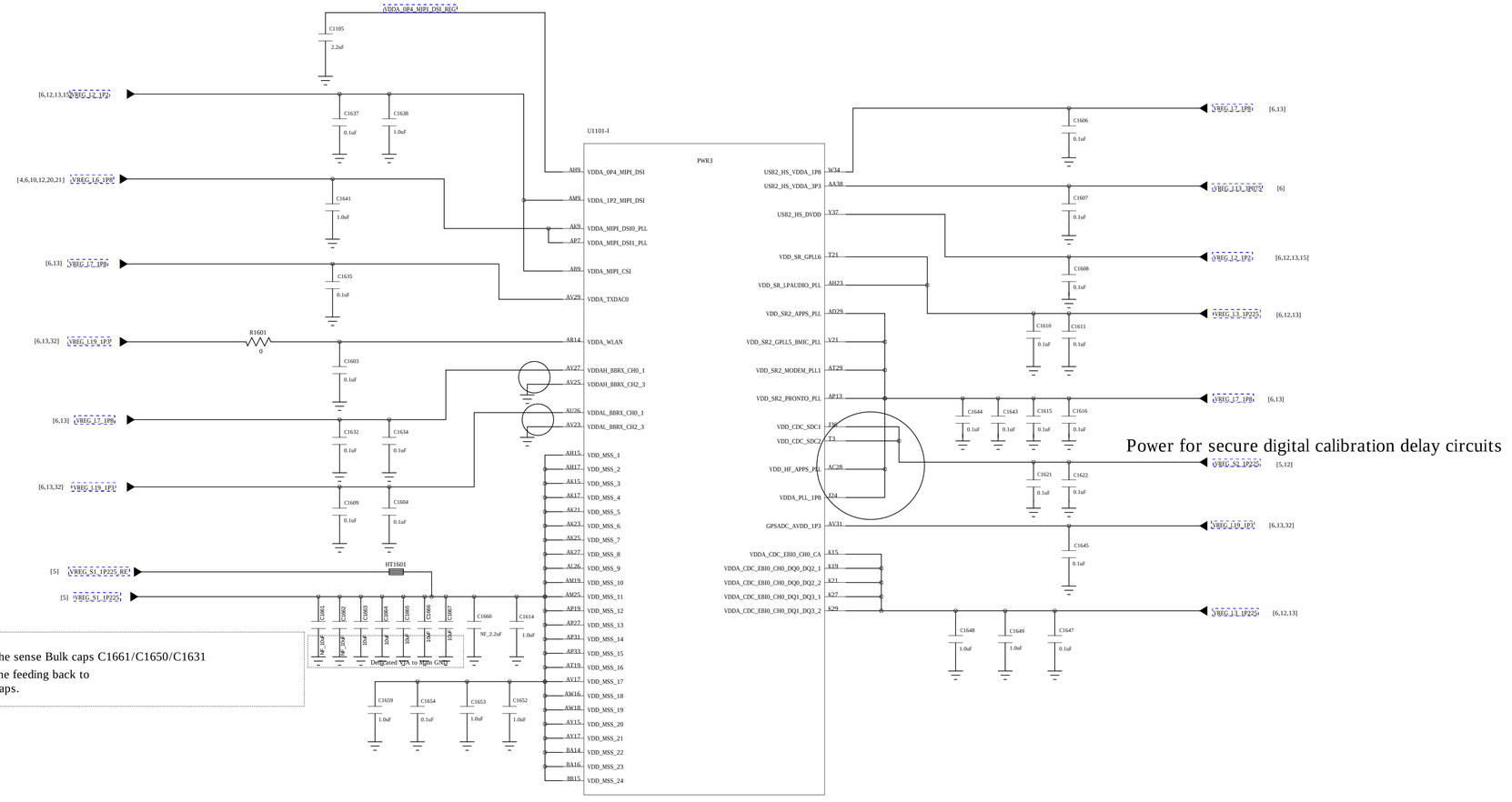
C1546 0.1uF, C1547 0.1uF, C1548 0.1uF, C1549 0.1uF

VDDPX_5 AC36 (UIM1) VBFG_1_14_UIM1 [6,22]

VDDPX_6 AE36 (UIM2) VBFG_1_15_UIM2 [6,22]

VDDPX_7 N34 (eMMC) VBFG_1_1P8 [2,3,6,7,10,12,15,16,19,21,22,23,26,27,31,32]

C1550 0.1uF, C1551 0.1uF, C1552 0.1uF



Note:
HTR1601 are used to help show that the sense Bulk caps C1661/C1650/C1631
are close to the MSM and the sense line feeding back to
the PMIC should be placed after the caps.

Power for secure digital calibration delay circuits

U1101-L

GND3

A85	VSSX_0_154	VSSX_0_204
AB17	VSSX_0_155	VSSX_0_205
AB19	VSSX_0_156	VSSX_0_206
AB33	VSSX_0_157	VSSX_0_207
AC6	VSSX_0_158	VSSX_0_208
AC8	VSSX_0_159	VSSX_0_209
AD5	VSSX_0_160	VSSX_0_210
AD17	VSSX_0_161	VSSX_0_211
AD33	VSSX_0_162	VSSX_0_212
AE30	VSSX_0_163	VSSX_0_213
AE32	VSSX_0_164	VSSX_0_214
AF17	VSSX_0_165	VSSX_0_215
AF31	VSSX_0_166	VSSX_0_216
AF33	VSSX_0_167	VSSX_0_217
AG30	VSSX_0_168	VSSX_0_218
AH5	VSSX_0_169	VSSX_0_219
AH11	VSSX_0_170	VSSX_0_220
AH13	VSSX_0_171	VSSX_0_221
AH19	VSSX_0_172	VSSX_0_222
AH25	VSSX_0_173	VSSX_0_223
AH29	VSSX_0_174	VSSX_0_224
AJ28	VSSX_0_175	VSSX_0_225
AJ34	VSSX_0_176	VSSX_0_226
AJ36	VSSX_0_177	VSSX_0_227
AK19	VSSX_0_178	VSSX_0_228
AK33	VSSX_0_179	VSSX_0_229
AK35	VSSX_0_180	VSSX_0_230
AK37	VSSX_0_181	VSSX_0_231
AL28	VSSX_0_182	VSSX_0_232
AL36	VSSX_0_183	VSSX_0_233
AL38	VSSX_0_184	VSSX_0_234
AM15	VSSX_0_185	VSSX_0_235
AM17	VSSX_0_186	VSSX_0_236
AM21	VSSX_0_187	VSSX_0_237
AM23	VSSX_0_188	
AM27	VSSX_0_189	
AM29	VSSX_0_190	
AP15	VSSX_0_191	
AT7	VSSX_0_192	
AT25	VSSX_0_193	
AT35	VSSX_0_194	
AU6	VSSX_0_195	
AU32	VSSX_0_196	
AV5	VSSX_0_197	
AV7	VSSX_0_198	
AV9	VSSX_0_199	
AV11	VSSX_0_200	
AV19	VSSX_0_201	
AV21	VSSX_0_202	
AV35	VSSX_0_203	
		AW8
		AW12
		AW20
		AW22
		AW34
		AY5
		AY7
		AY9
		AY11
		AY13
		AY19
		AY21
		AY23
		AY33
		AY35
		BA8
		BA10
		BA12
		BA18
		BA20
		BA22
		BB7
		BB9
		BB11
		BB13
		BB35
		BC6
		BC14
		BD23
		BF1
		BF23
		BG2
		BG22
		BG40

U1101-J

GND1

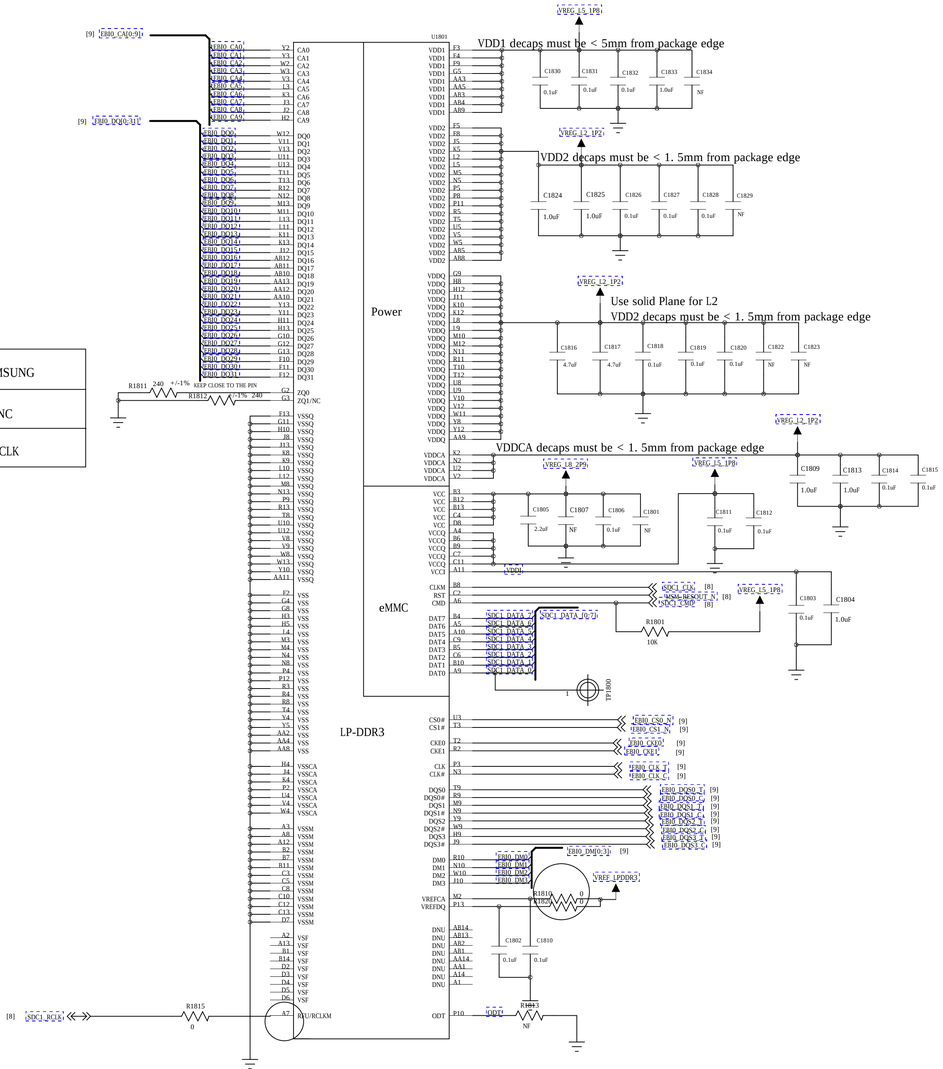
AK7	VSSX_0_2	VSSX_0_32
AN8	VSSX_0_3	VSSX_0_33
AH7	VSSX_0_4	VSSX_0_34
AK5	VSSX_0_5	VSSX_0_35
AM5	VSSX_0_6	
AM7	VSSX_0_7	
AP5	VSSX_0_8	VSSX_0_36
		VSSX_0_37
AW30	VSSX_0_9	VSSX_0_38
AY29	VSSX_0_10	VSSX_0_39
BB31	VSSX_0_11	
BC32	VSSX_0_12	VSSX_0_40
BD31	VSSX_0_13	VSSX_0_41
BF31	VSSX_0_14	
BF33	VSSX_0_15	VSSX_0_42
BF35	VSSX_0_16	VSSX_0_43
AV13	VSSX_0_17	VSSX_0_44
		VSSX_0_45
AW28	VSSX_0_18	VSSX_0_46
AY27	VSSX_0_19	VSSX_0_47
BC28	VSSX_0_20	
BC30	VSSX_0_21	VSSX_0_48
BD27	VSSX_0_22	VSSX_0_49
BD29	VSSX_0_23	
BF27	VSSX_0_24	
BF29	VSSX_0_25	VSSX_0_50
AY25	VSSX_0_26	
BC24	VSSX_0_27	
BC26	VSSX_0_28	
BD25	VSSX_0_29	
BF25	VSSX_0_30	VSSX_0_51
		VSSX_0_52
AT27	VSSX_0_31	VSSX_0_53
		AA34
		AB37
		AD27
		AB27
		U20
		V19
		AJ22
		AH21
		AC30
		AB29
		V23
		U22
		AR28
		AP29
		AN14
		AM13
		K23
		H23
		M23
		AW32
		BD35
		AT31

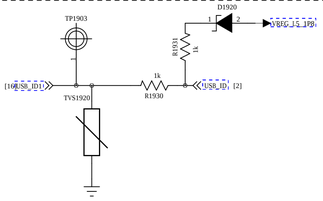
U1101-K

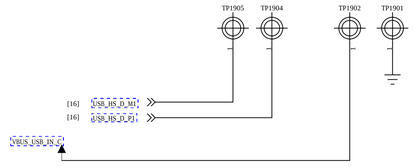
GND2

A2	VSSX_0_54	VSSX_0_104
A40	VSSX_0_55	VSSX_0_105
B1	VSSX_0_56	VSSX_0_106
B7	VSSX_0_57	VSSX_0_107
B9	VSSX_0_58	VSSX_0_108
B11	VSSX_0_59	VSSX_0_109
B13	VSSX_0_60	VSSX_0_110
B15	VSSX_0_61	VSSX_0_111
B17	VSSX_0_62	VSSX_0_112
B19	VSSX_0_63	VSSX_0_113
B21	VSSX_0_64	VSSX_0_114
B23	VSSX_0_65	VSSX_0_115
B25	VSSX_0_66	VSSX_0_116
B27	VSSX_0_67	VSSX_0_117
B29	VSSX_0_68	VSSX_0_118
B31	VSSX_0_69	VSSX_0_119
B33	VSSX_0_70	VSSX_0_120
B35	VSSX_0_71	VSSX_0_121
B37	VSSX_0_72	VSSX_0_122
C6	VSSX_0_73	VSSX_0_123
C14	VSSX_0_74	VSSX_0_124
C20	VSSX_0_75	VSSX_0_125
C24	VSSX_0_76	VSSX_0_126
C32	VSSX_0_77	VSSX_0_127
D7	VSSX_0_78	VSSX_0_128
D9	VSSX_0_79	VSSX_0_129
D11	VSSX_0_80	VSSX_0_130
D13	VSSX_0_81	VSSX_0_131
D17	VSSX_0_82	VSSX_0_132
D21	VSSX_0_83	VSSX_0_133
D23	VSSX_0_84	VSSX_0_134
D27	VSSX_0_85	VSSX_0_135
D29	VSSX_0_86	VSSX_0_136
D33	VSSX_0_87	VSSX_0_137
D35	VSSX_0_88	VSSX_0_138
D37	VSSX_0_89	VSSX_0_139
F8	VSSX_0_90	VSSX_0_140
F18	VSSX_0_91	VSSX_0_141
F22	VSSX_0_92	VSSX_0_142
F24	VSSX_0_93	VSSX_0_143
F26	VSSX_0_94	VSSX_0_144
F28	VSSX_0_95	VSSX_0_145
F30	VSSX_0_96	VSSX_0_146
F34	VSSX_0_97	VSSX_0_147
F36	VSSX_0_98	VSSX_0_148
F7	VSSX_0_99	VSSX_0_149
F13	VSSX_0_100	VSSX_0_150
F23	VSSX_0_101	VSSX_0_151
G2	VSSX_0_102	VSSX_0_152
G6	VSSX_0_103	VSSX_0_153
		G8
		G12
		G28
		G36
		H11
		H13
		H19
		H29
		H31
		H35
		J8
		J10
		J26
		J32
		K5
		K7
		K25
		L36
		M7
		M29
		M33
		N30
		N32
		P13
		P21
		P23
		P29
		R28
		R30
		T13
		T15
		T27
		T29
		T31
		T35
		U26
		U34
		V31
		V33
		W20
		W22
		W26
		W28
		W32
		Y7
		Y19
		Y27
		AA4
		AA6
		AA28

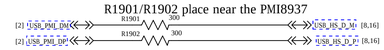
	MICRO/HYNIX	SAMSUNG
U1501.G3	ZQ1	NC
U1501.A7	RFU	RCLK

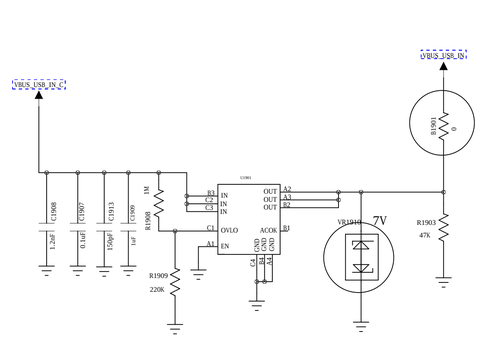


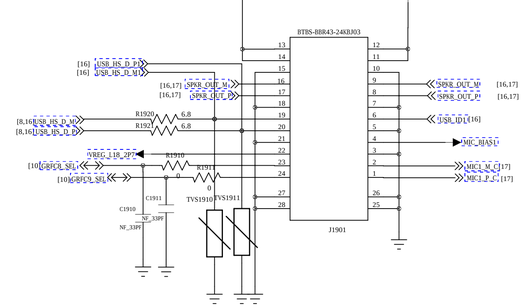




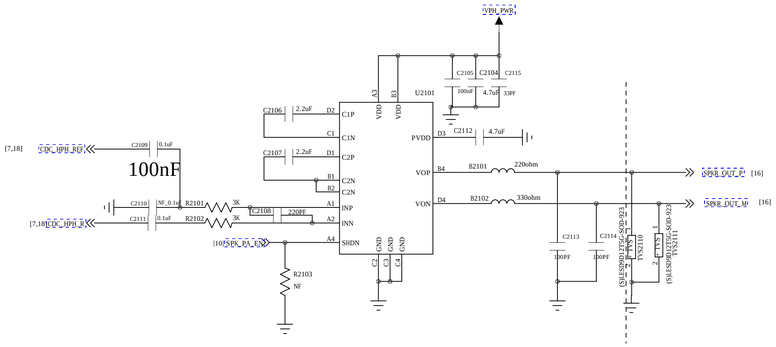
R1901/R1902 place near the PMI8937

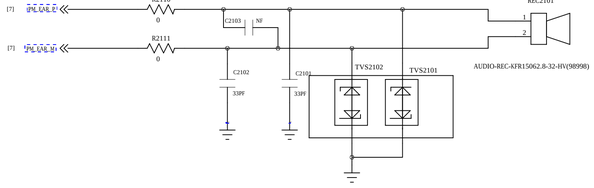






IO

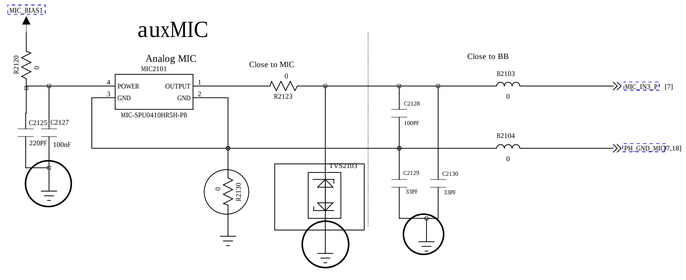




REC

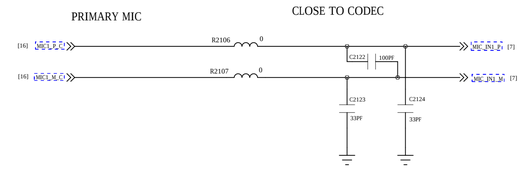
VDD_PWR [2,3,4,5,6,7,17,19,20,21,27,31]

VDD_1V8 [2,3,4,5,6,7,17,19,20,21,27,31]

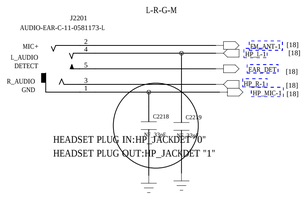


together then single via to main GND

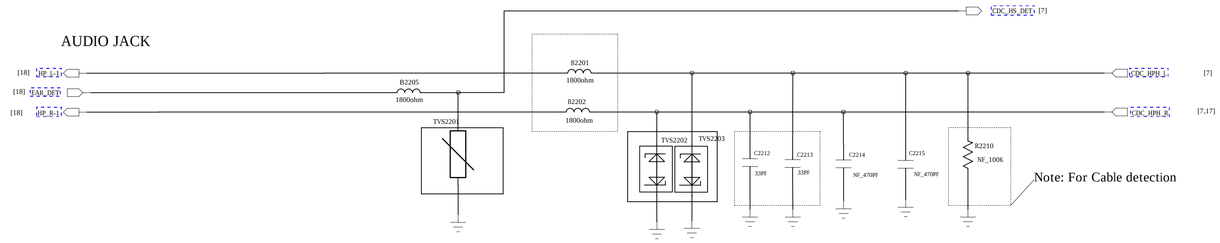
AUX_MIC

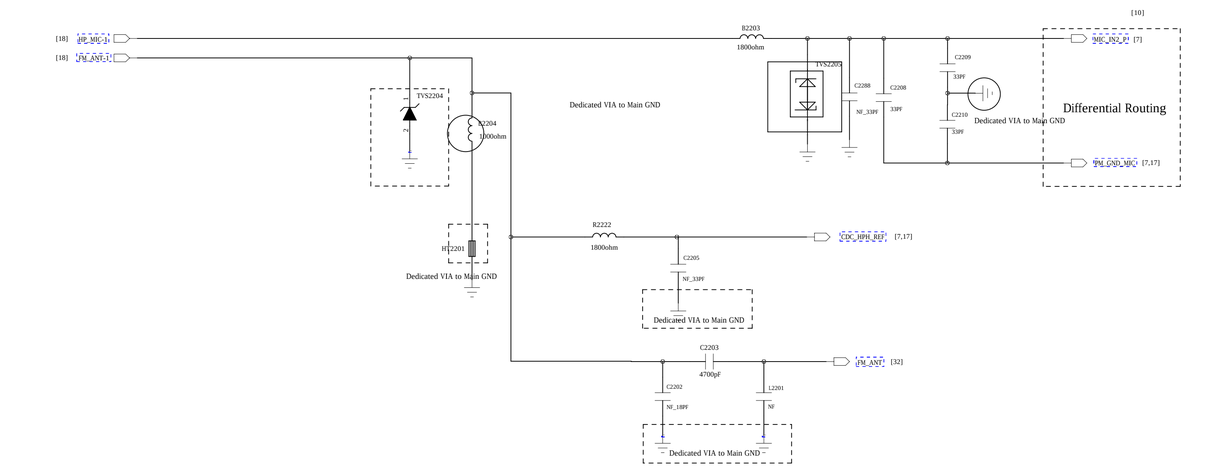


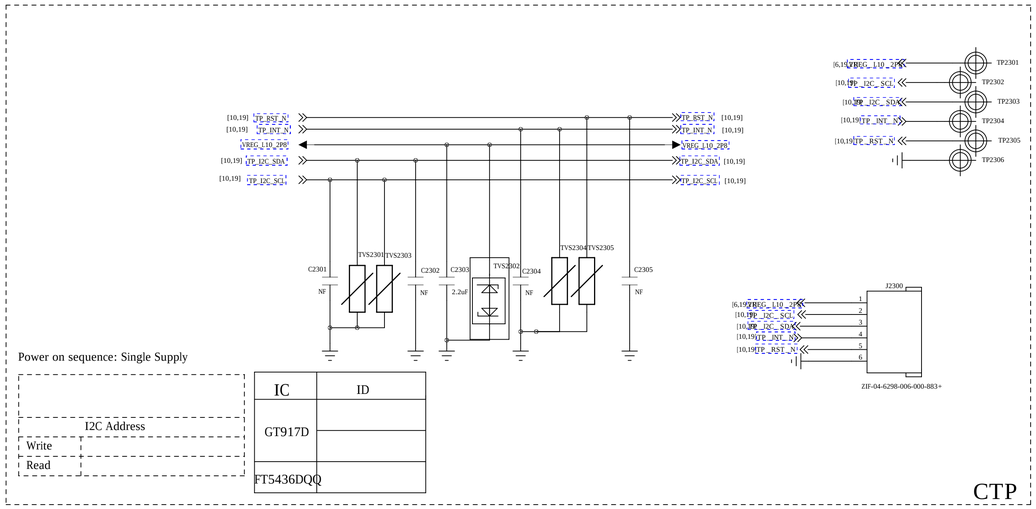
MAIN_MIC



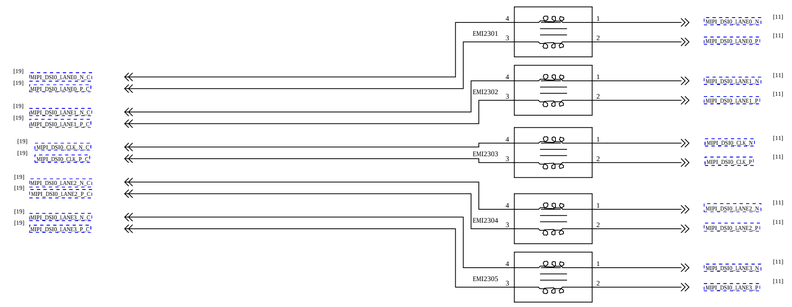
Note: Ferrite beads and their corresponding bypass capacitors on CDC_HPH_L, CDC_HPH_R and CDC_HPH_REF are needed to reduce noise generated by audio/FM concurrency

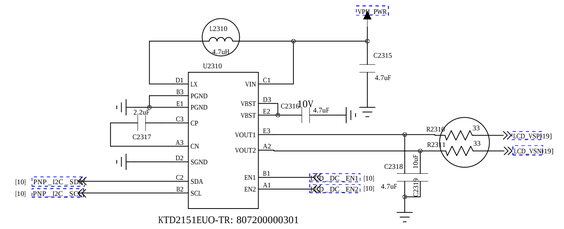






(VIETMOBILE.VN)

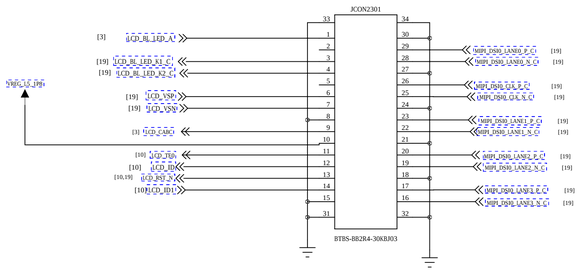


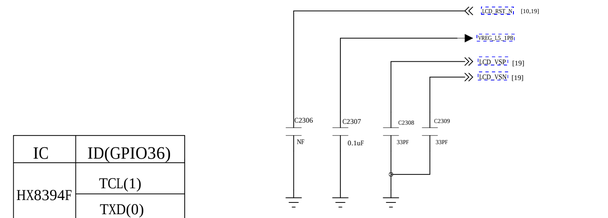


KTD2151EUO-TR: 807200000301

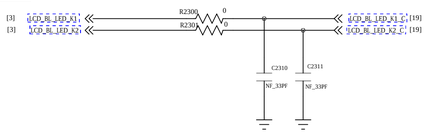
KTD2151& NT50358 powers ON with a default voltage of 5.0V
software can use without I2C

LCD



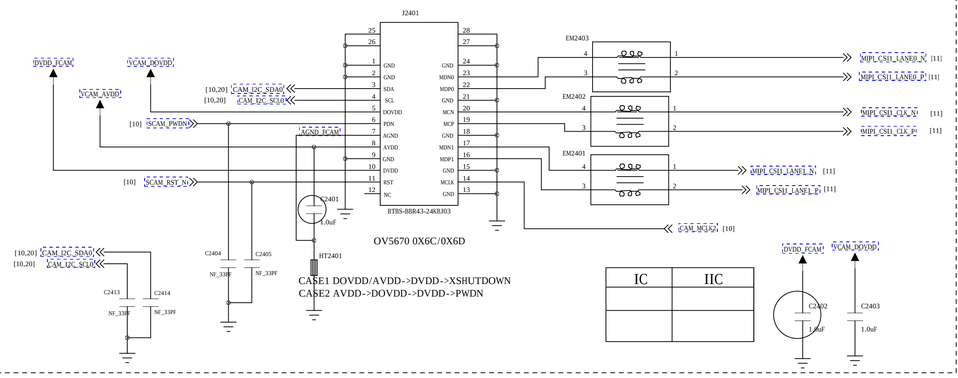


IC	ID(GPIO36)
HX8394F	TCL(1)
	TXD(0)



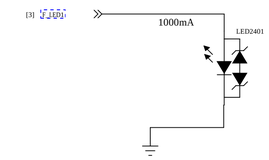
Note: If best EMI practices are followed for MIPI CSI/DSI signals, there is no need for common mode choke filters. You may choose to have placeholders for common mode depending upon your design constraints.
Extreme care must be taken that no stubs are created by doing so.

FRONT_camera

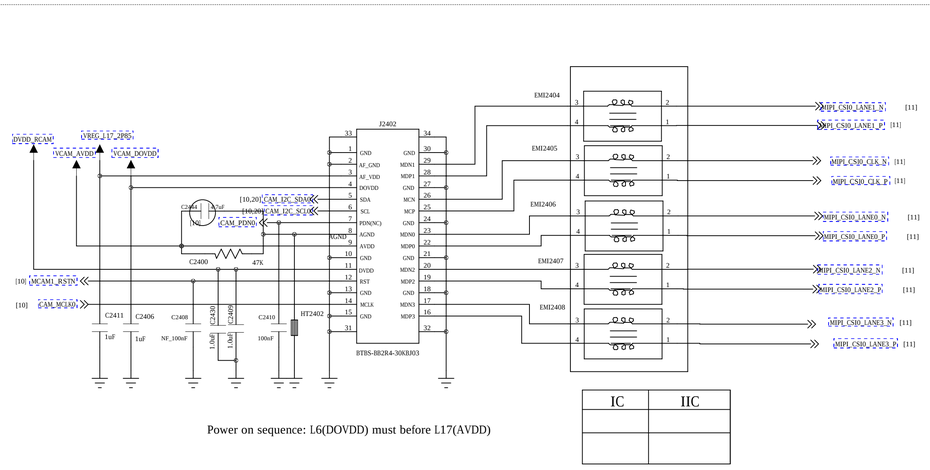


Main Camera / Sub Camera share power domain design
should double check the voltage level is compatible

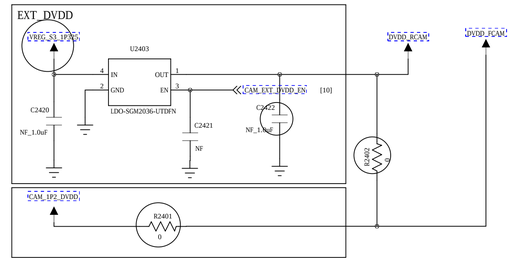
FLASH LED



Main Camera

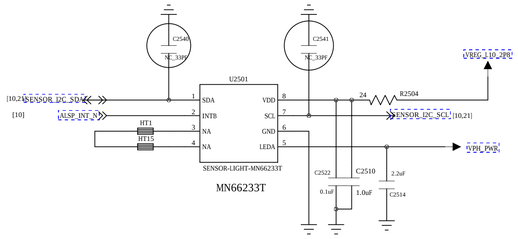


Power on sequence: L6(DOVDD) must before L17(AVDD)



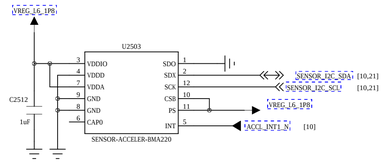
If use CAM_2P8_AVDD as DOVDD, set LDO22's voltage:
0x00015541 LDO22_VOLTAGE_CTL2 0x54- ->0x04

ALS+PS+IR



MN66233T

G-SENSOR

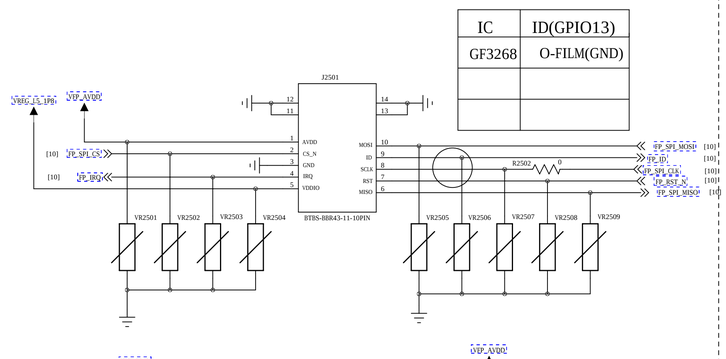


KXTJ2-1009-HQ

W/R:0X92/0X93

FP

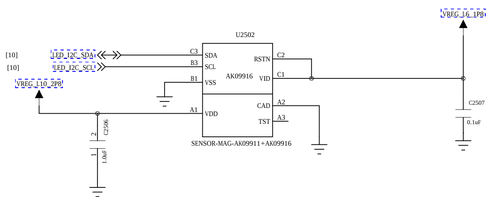
IC	ID(GPIO13)
GF3268	O-FILM(GND)



M-SENSOR

AKM: AK09916

Write	0x18
Read	0x19



AKM: AK09911

I2C Address@CAD=0	
Write	0x18
Read	0x19

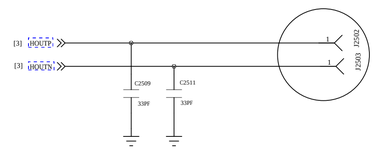
I2C Address@CAD=1	
Write	0x1A
Read	0x1B

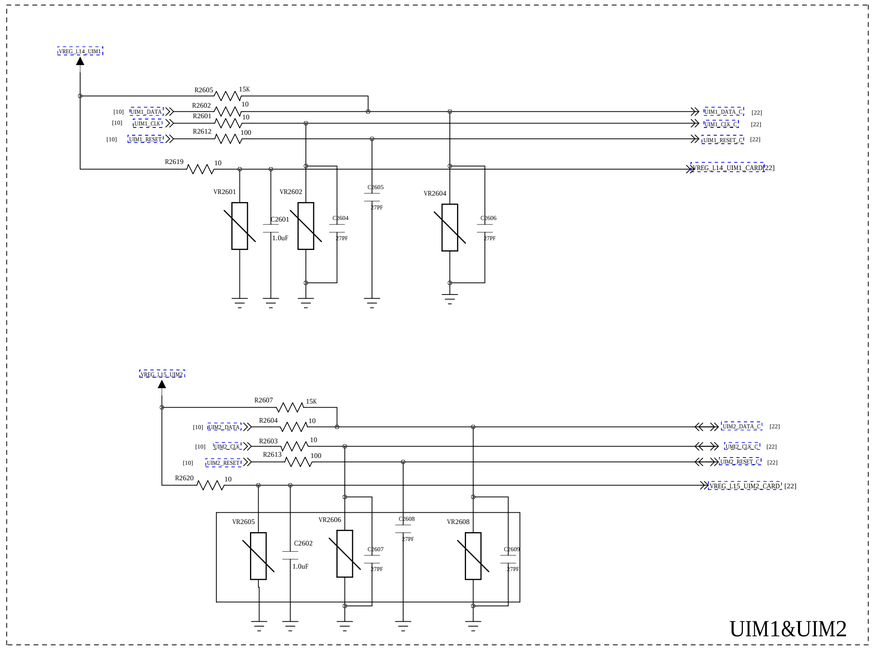
Power on sequence: L6/L17 can be applied in any order

RG

Power on sequence: can be applied in any order

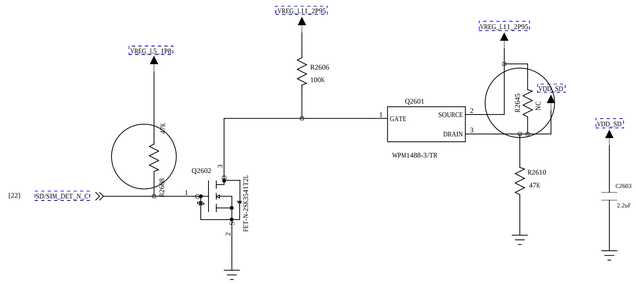
MOTOR



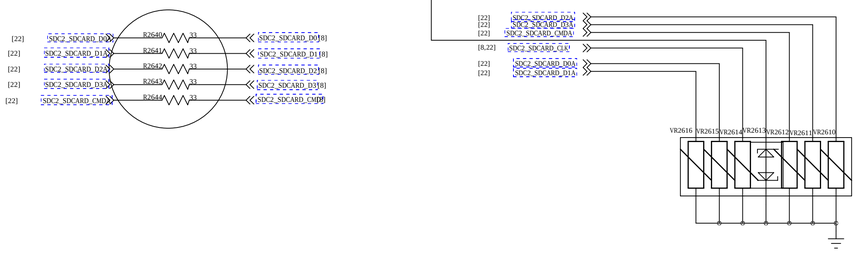


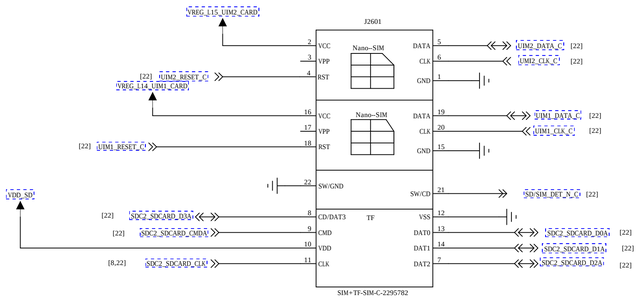
UIM1&UIM2

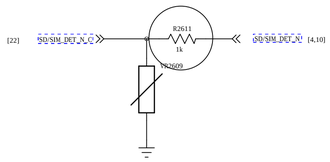
Vout=3.0V,I-lim=1A



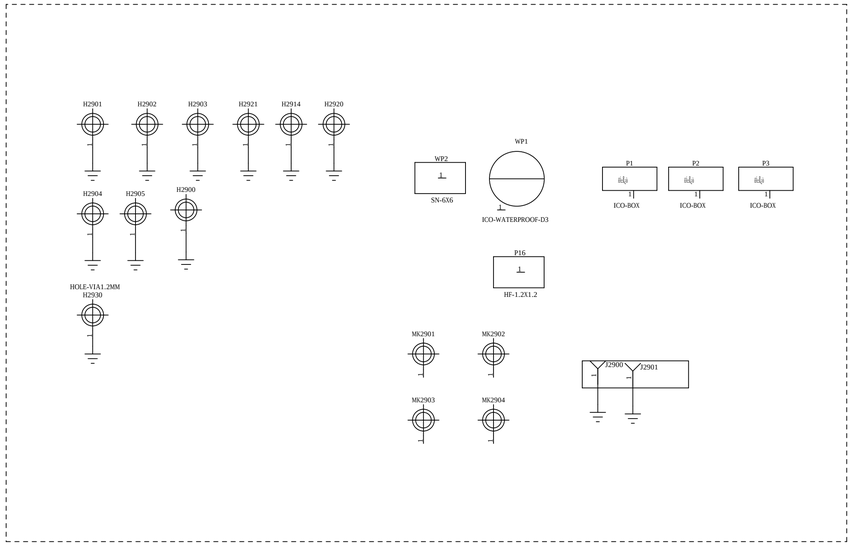
SD CARD

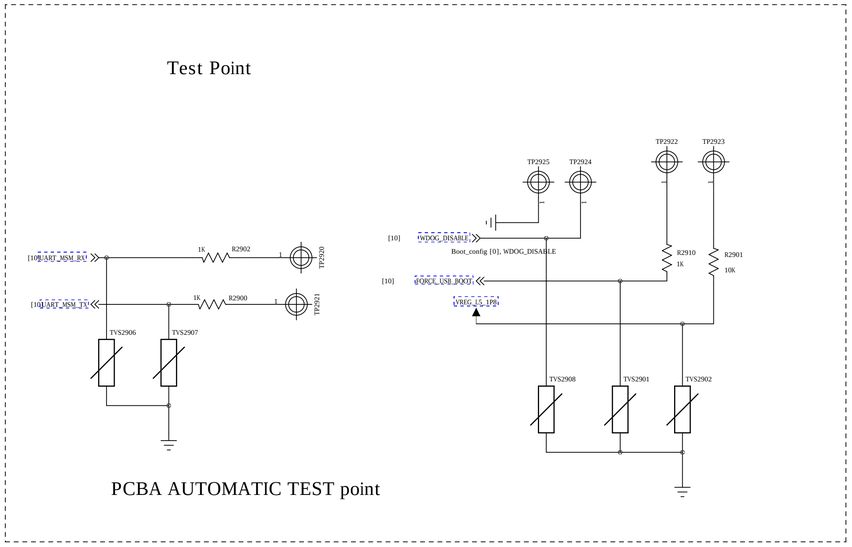




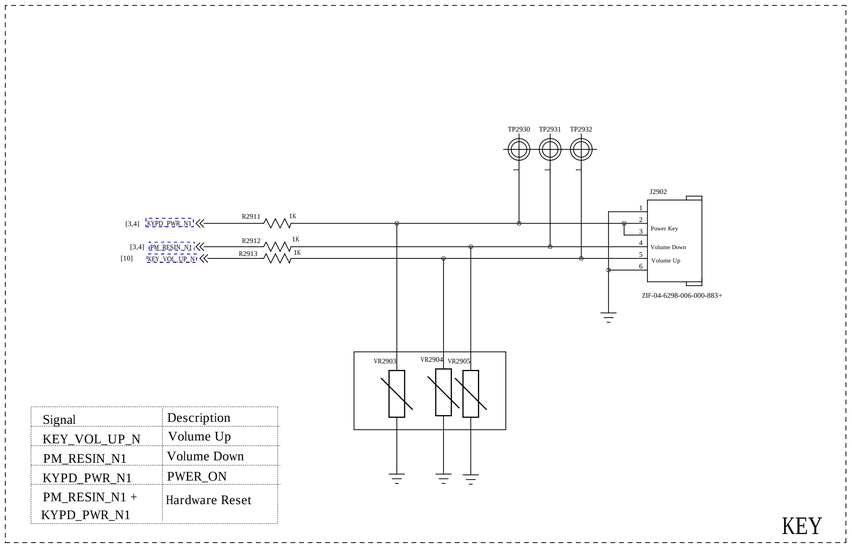


This int should give to GPIO54/GPIO58/GPIO67



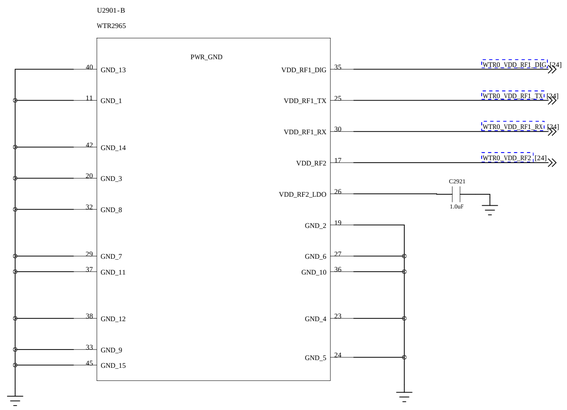


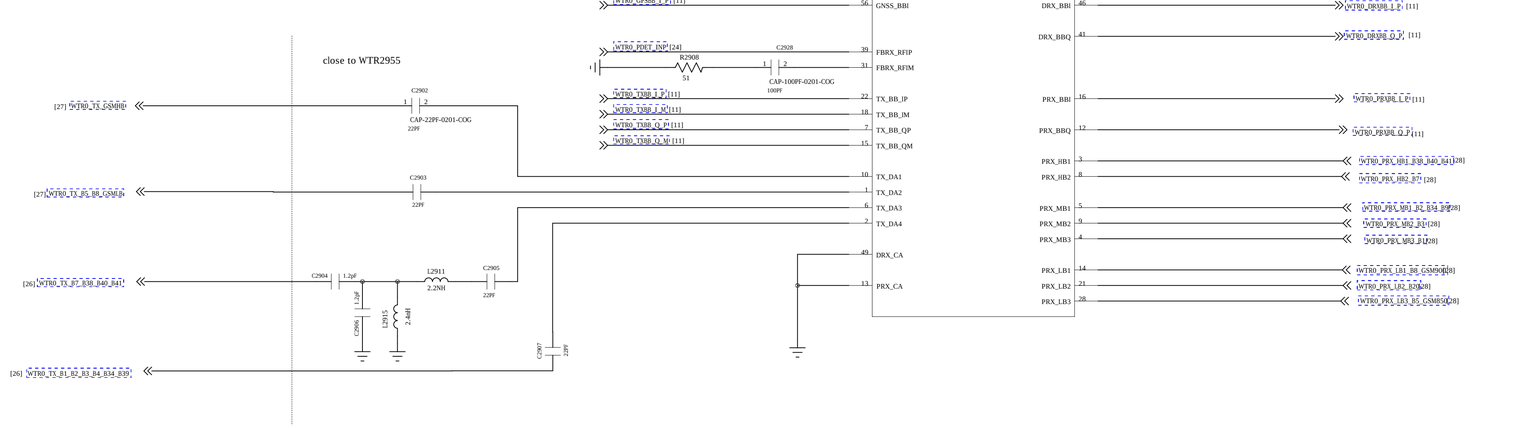
JTAG



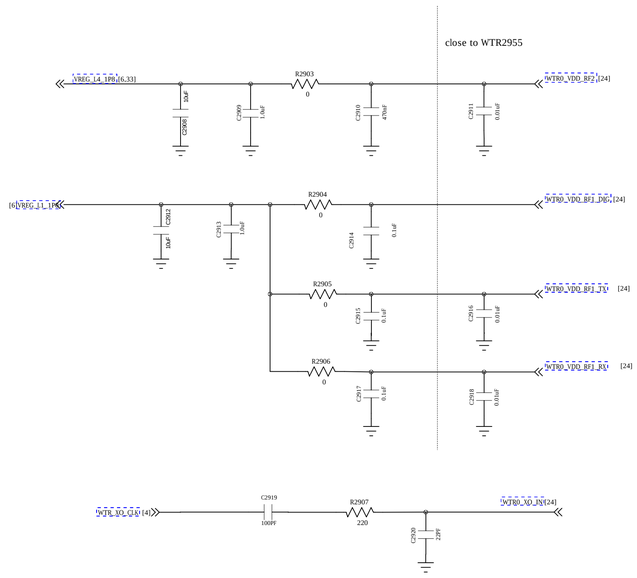
Signal	Description
KEY_VOL_UP_N	Volume Up
PM_RESIN_N1	Volume Down
KYPD_PWR_N1	PWER_ON
PM_RESIN_N1 + KYPD_PWR_N1	Hardware Reset

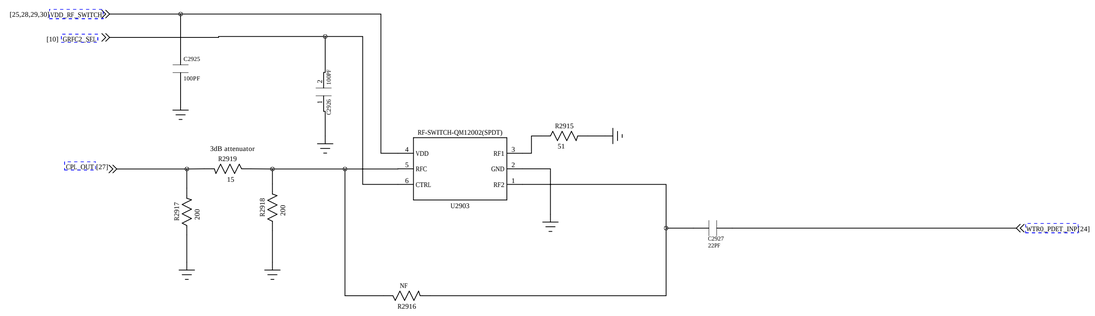
KEY

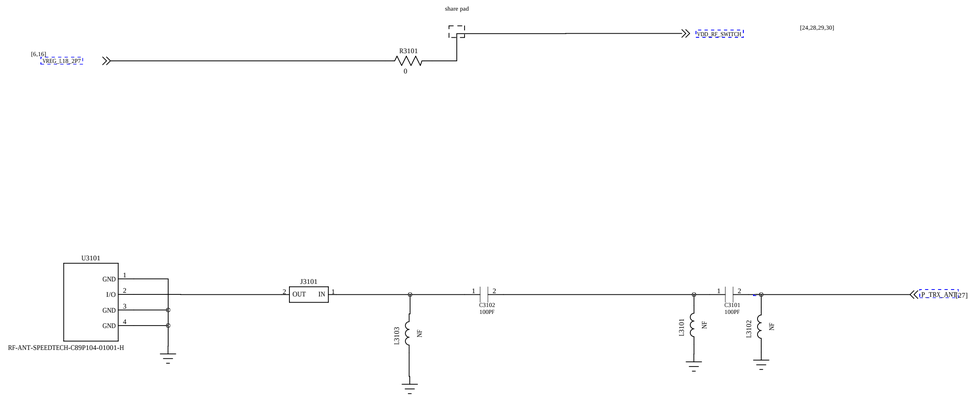




Note:RX ports have DC at the pin, so it need DC block,please make sure there is no DC short to other voltages and GND






share pad
[6,16]
[24,28,29,30]
R3101
0
U3101
GND
I/O
GND
GND
1
2
3
4
RF-ANT-SPEEDTECH-C89P104-01001-H
J3101
2
OUT
IN
1
L3103
NF
1
2
C3102
100PF
L3101
NF
1
2
C3101
100PF
L3102
NF

Band40

Band41

Band7

PRX_B40B41

HB_IN

Band3

MB_IN

Band1

Band39

LB_IN

Band2

Band8

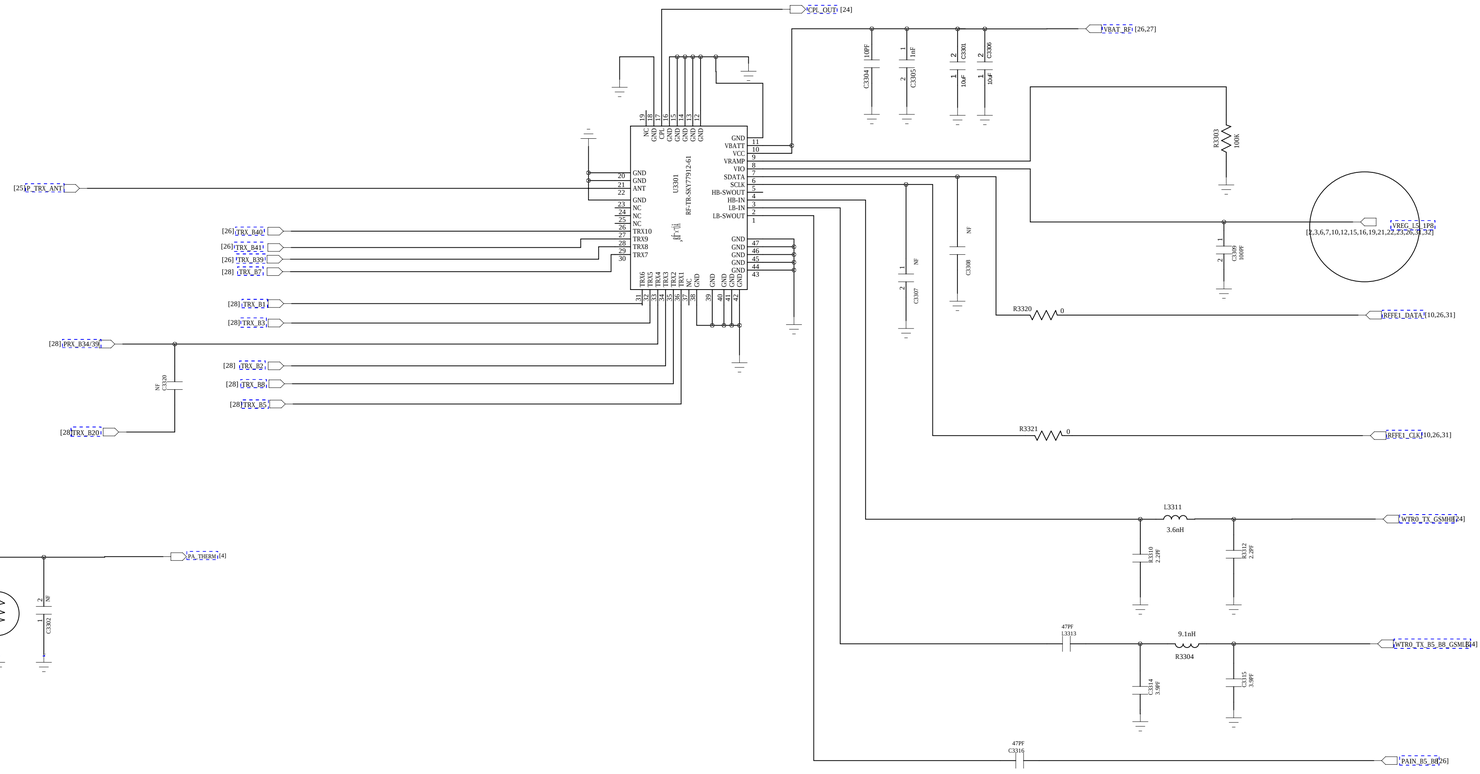
Band20

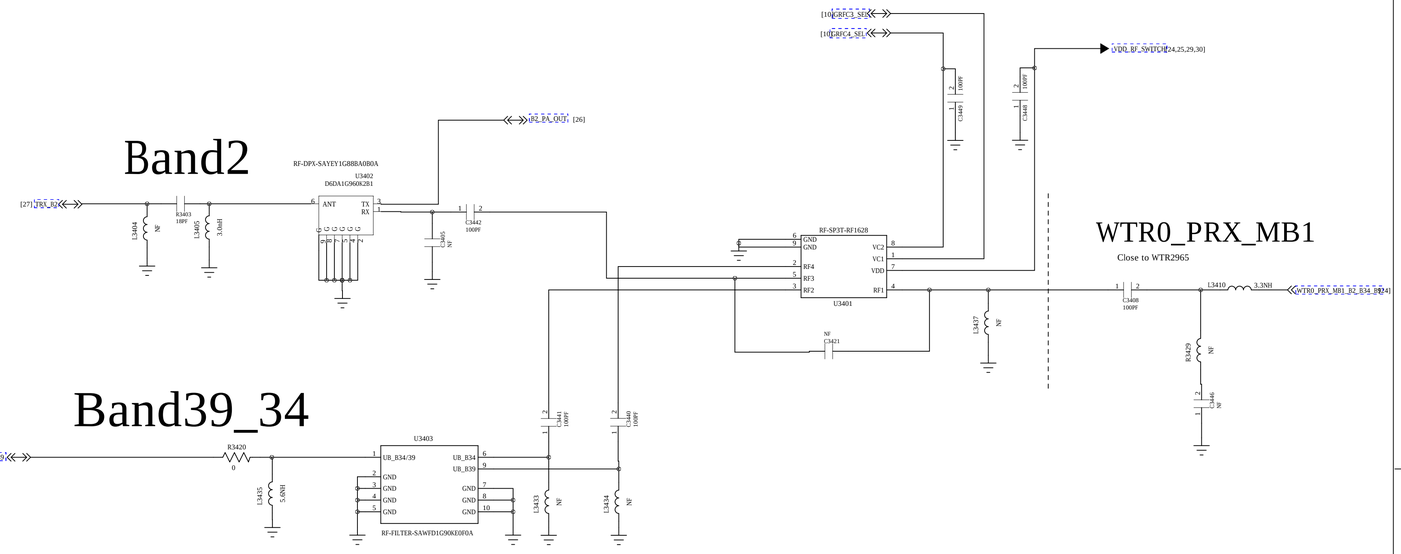
Band5

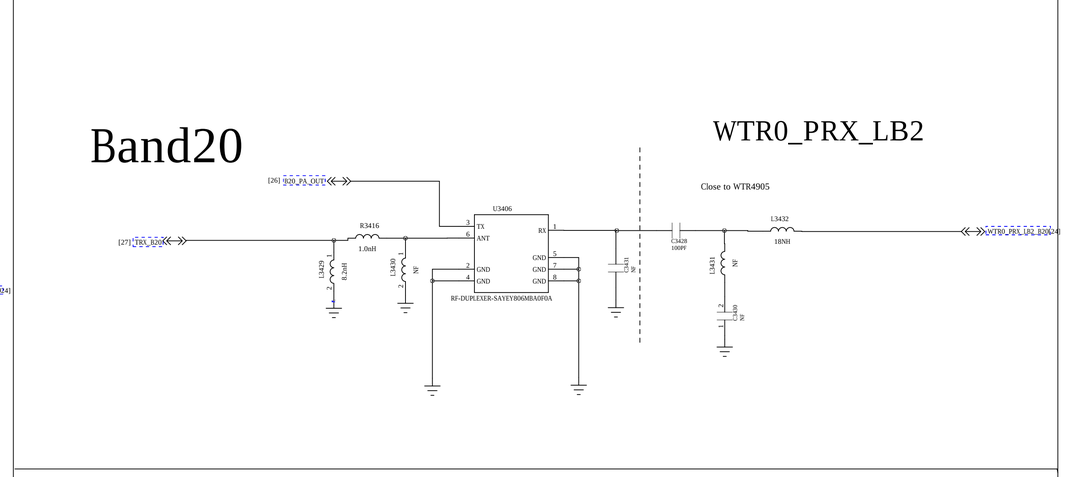
GSM_HB

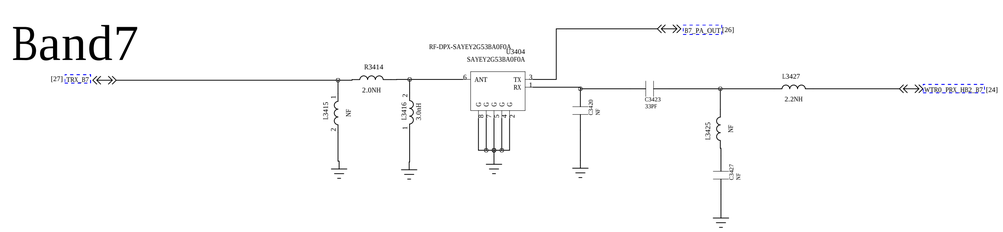
B5_B8_2GLB

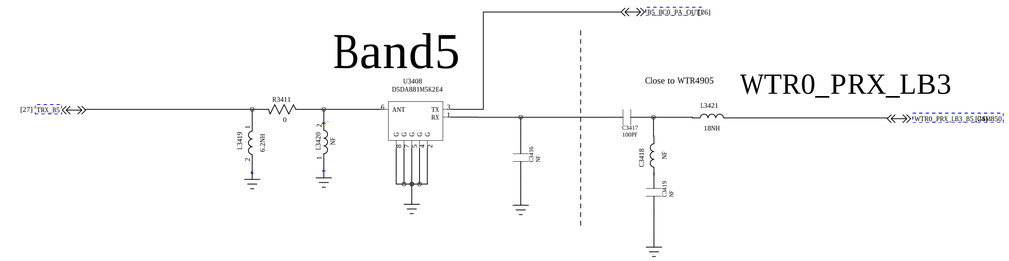
B5_B8

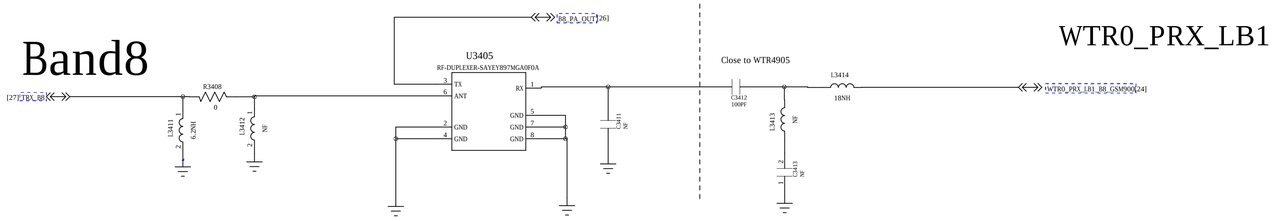


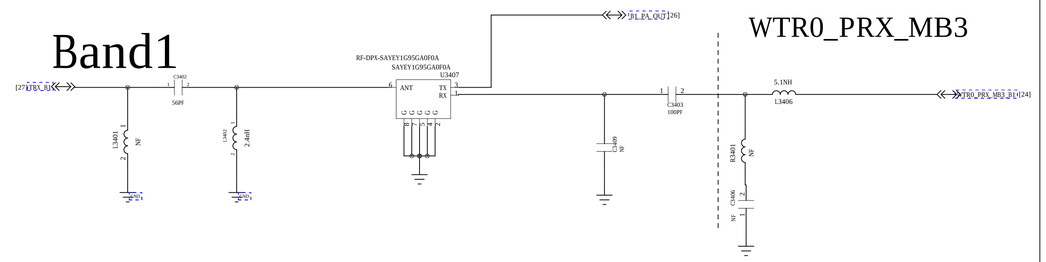


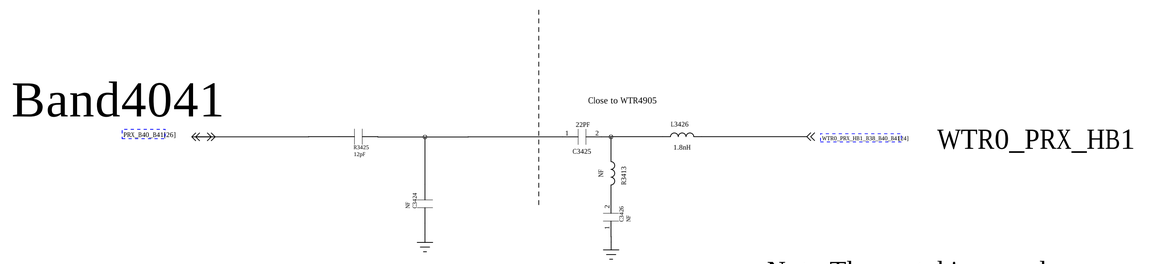




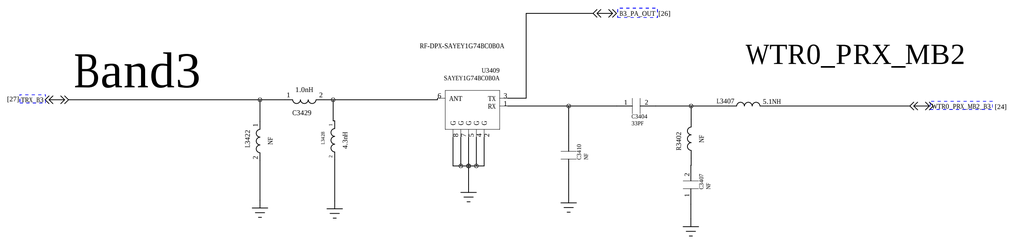




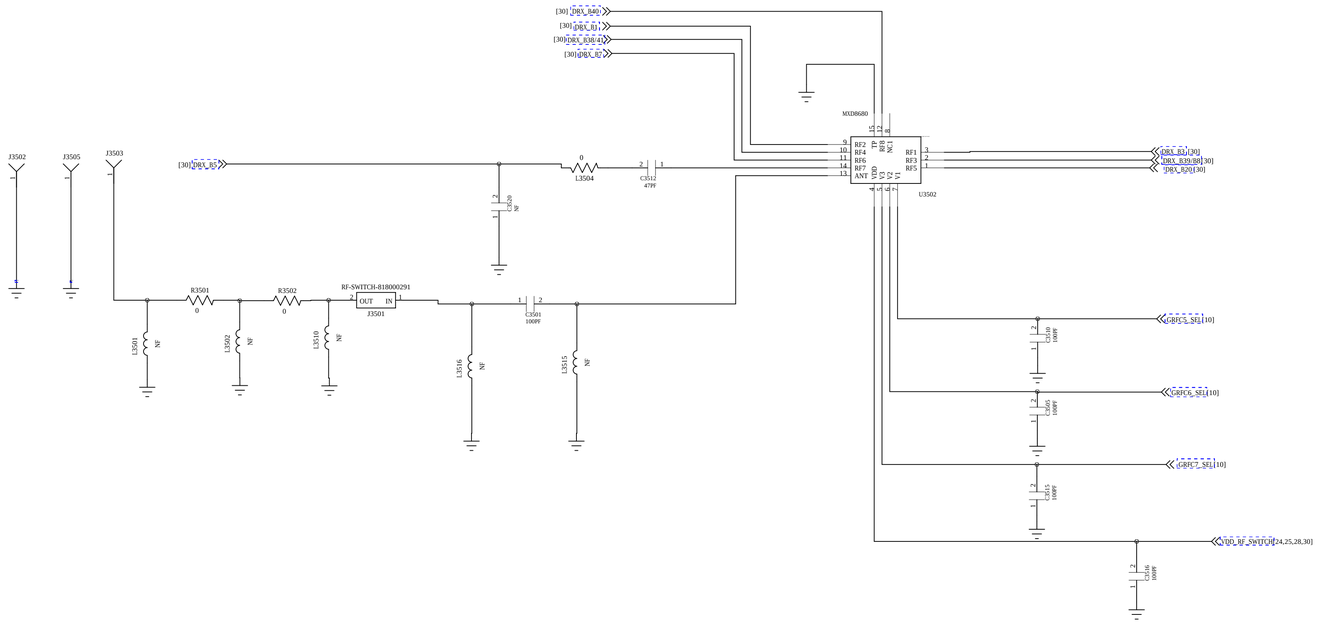




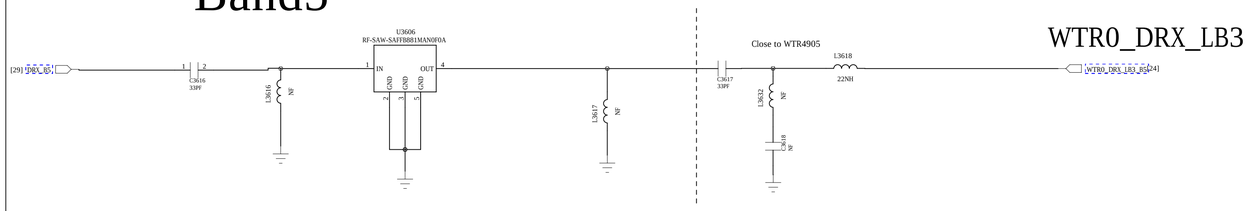
Note:The matching need close to WTR, RX ports have DC at the pin, so it need DC block,



(VIETMOBILE.VN)

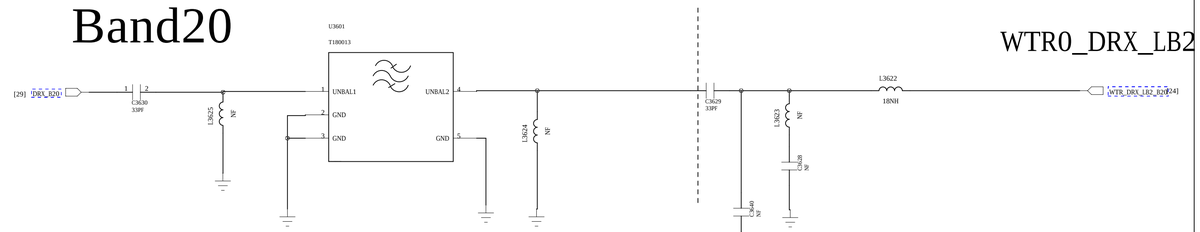


Band5



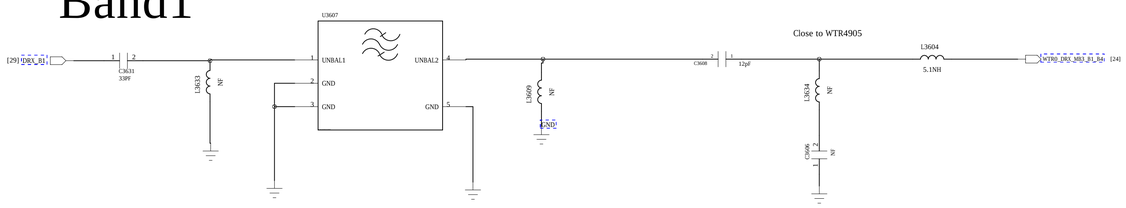
WTR0_DRX_LB3

Band20



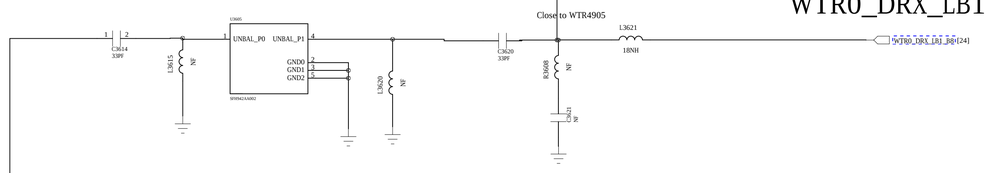
WTR0_DRX_LB2

Band1



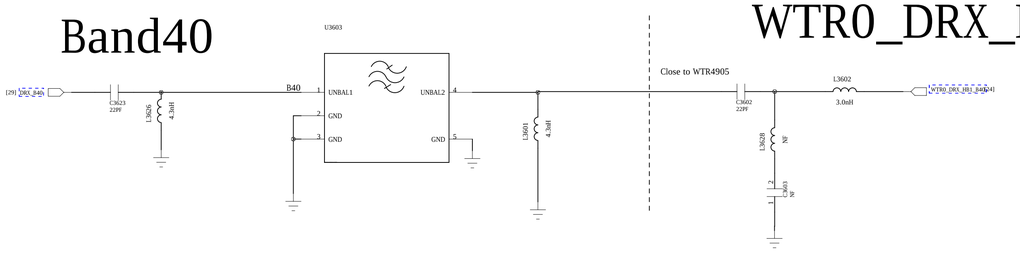
WTR0_DRX_MB3

Band8



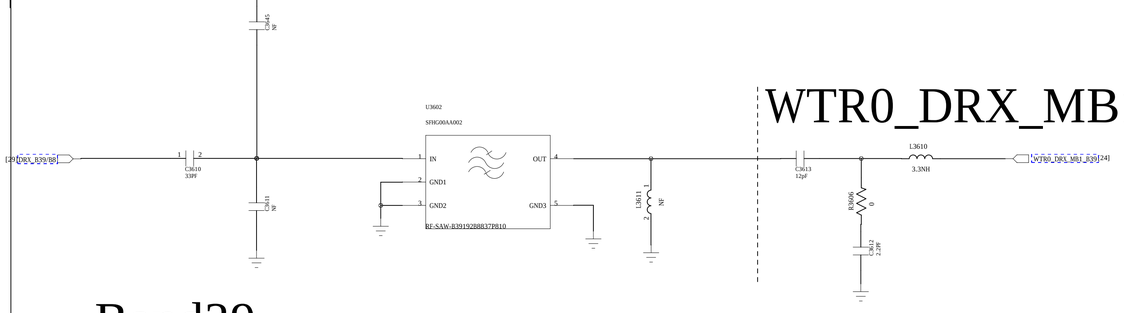
WTR0_DRX_LB1

Band40



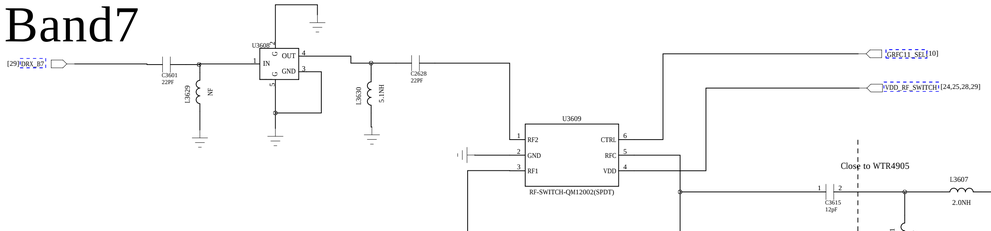
WTR0_DRX_HB1

Band39

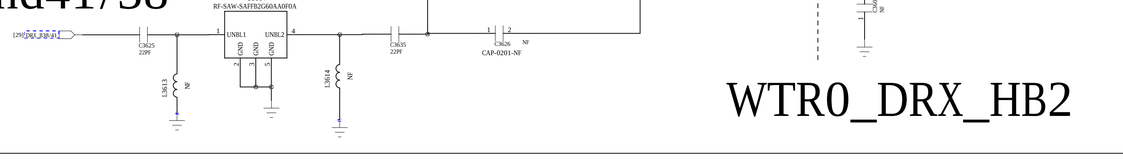


WTR0_DRX_MB1

Band7

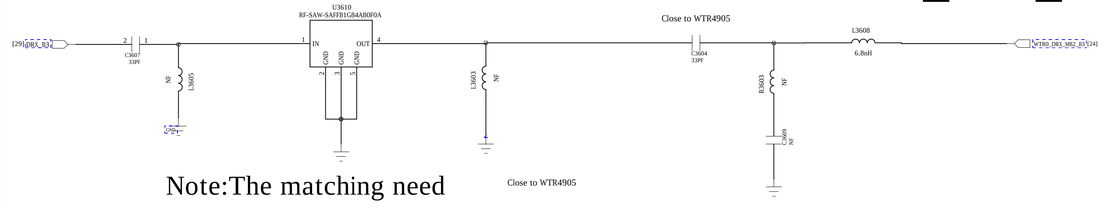


Band41/38



WTR0_DRX_HB2

Band3



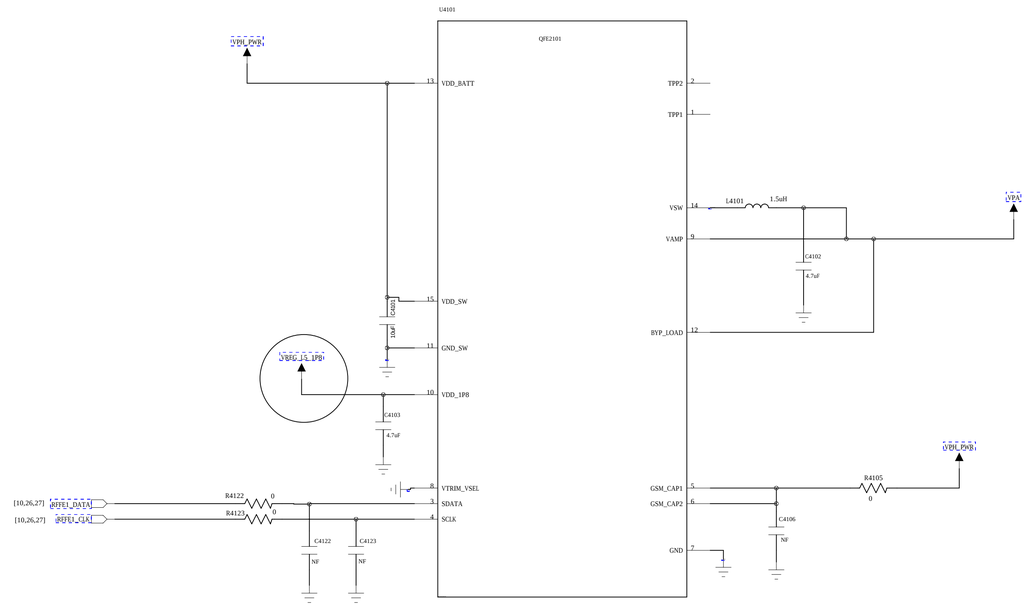
WTR0_DRX_MB2

Note:The matching need close to WTR, RX ports have DC at the pin, so it need DC block,

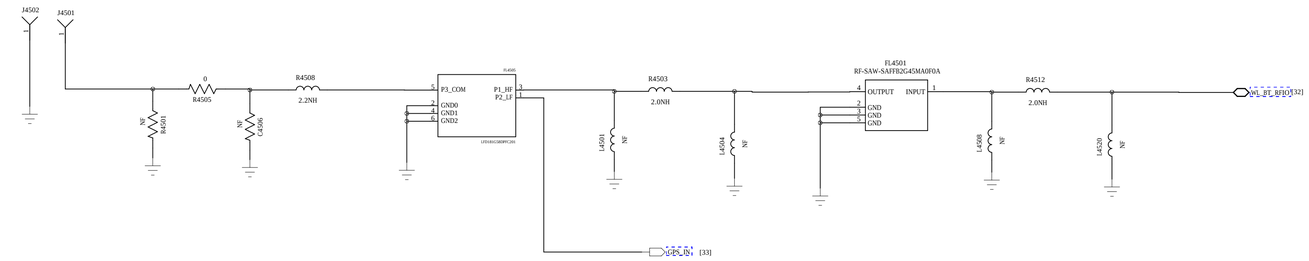
Close to WTR4905

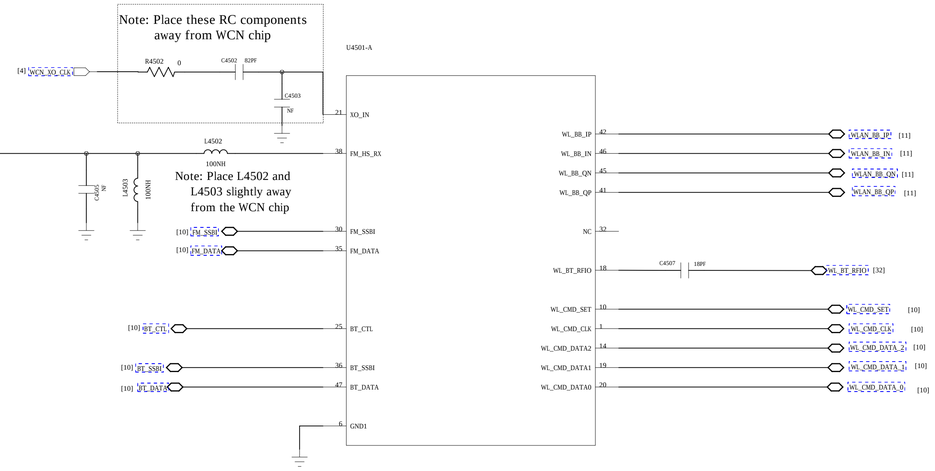
Note: Use a signle low impedance power plane/fill VPA for all ET PA VCC1/VCC2.

Refer to 80-NA681-91 rev.B or later revisions for more layout details.

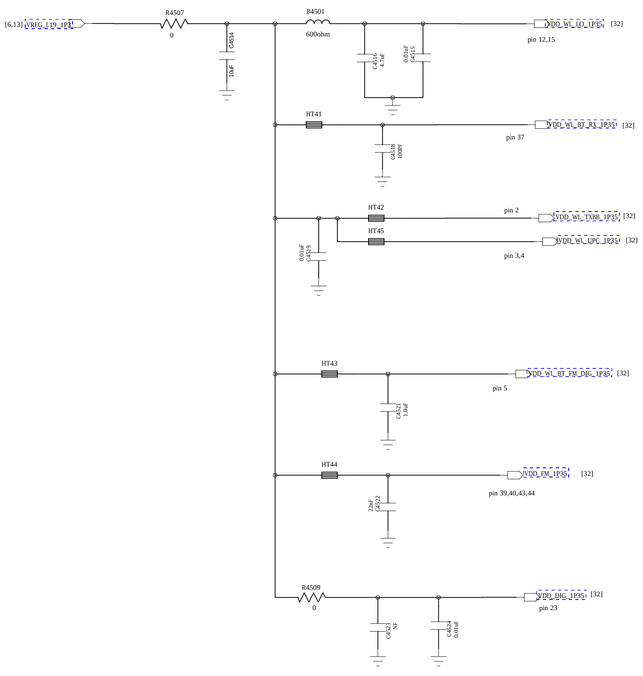


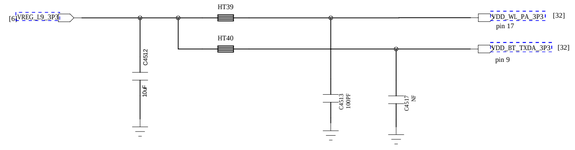
WCN

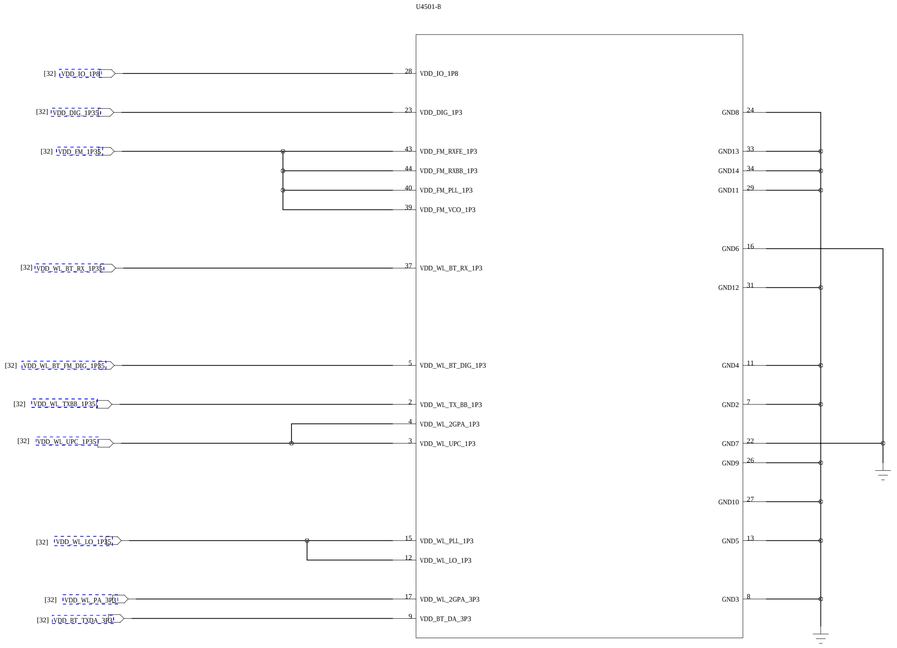




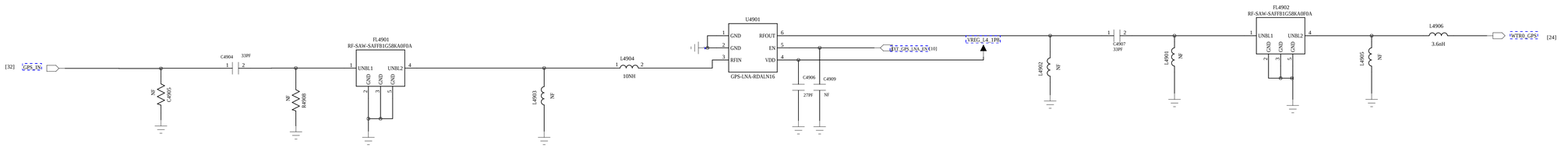
(VIETMOBILE.VN)







GPS


[32]
GPS_IN
C4904
33PF
NF
C4905
NF
R4908
FL4901
RF-SAW-SAFFB1G58KA0F0A
UNBL1
UNBL2
GND
GND
GND
L4903
NF
L4904
10NH
U4901
GND
GND
RFIN
RFOUT
EN
VDD
GPS-LNA-RDALN16
C4906
27PF
C4909
NI
VREG_L4_1P8N
[10]
L4902
NF
C4907
33PF
L4901
NF
FL4902
RF-SAW-SAFFB1G58KA0F0A
UNBL1
UNBL2
GND
GND
GND
L4905
NF
L4906
3.6nH
GNSS_GPS
[24]