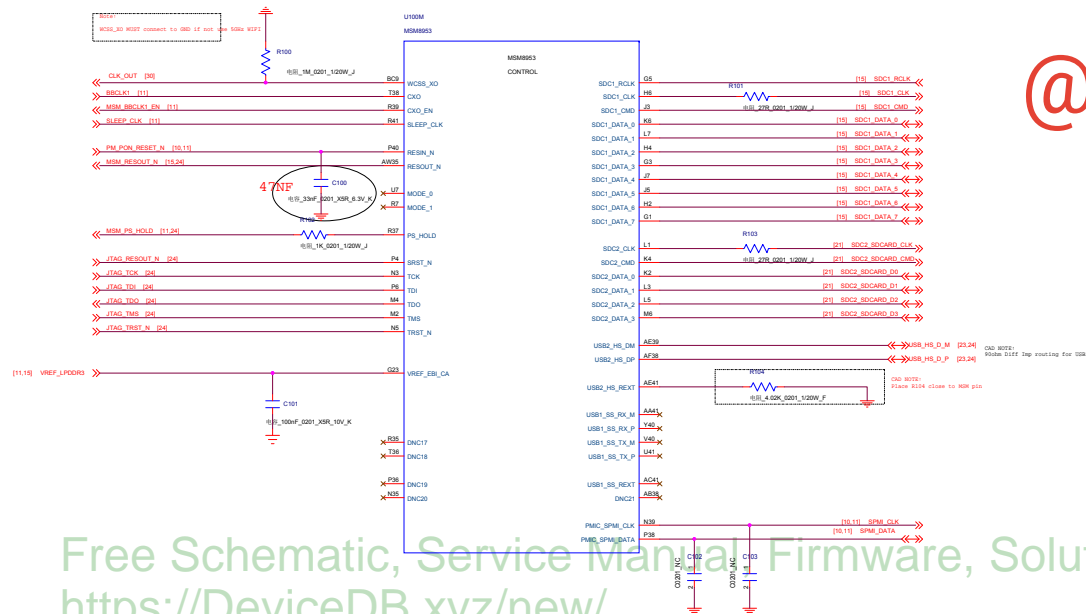
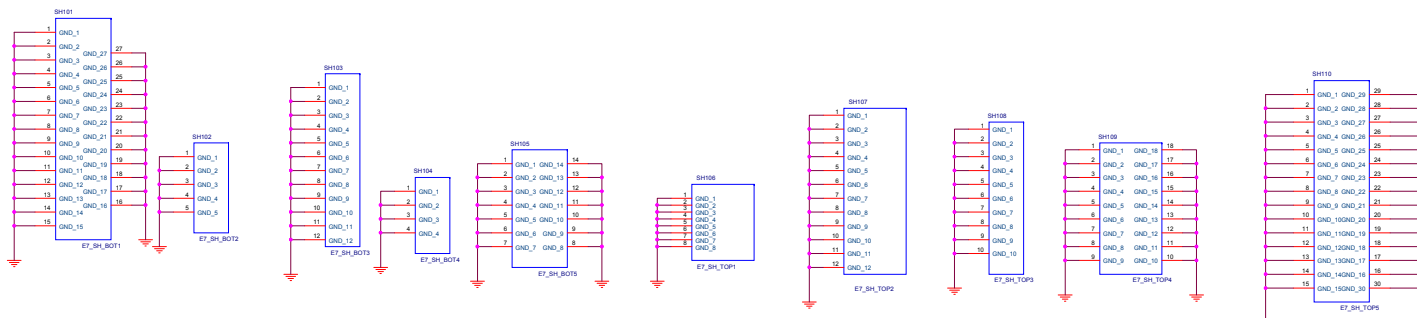


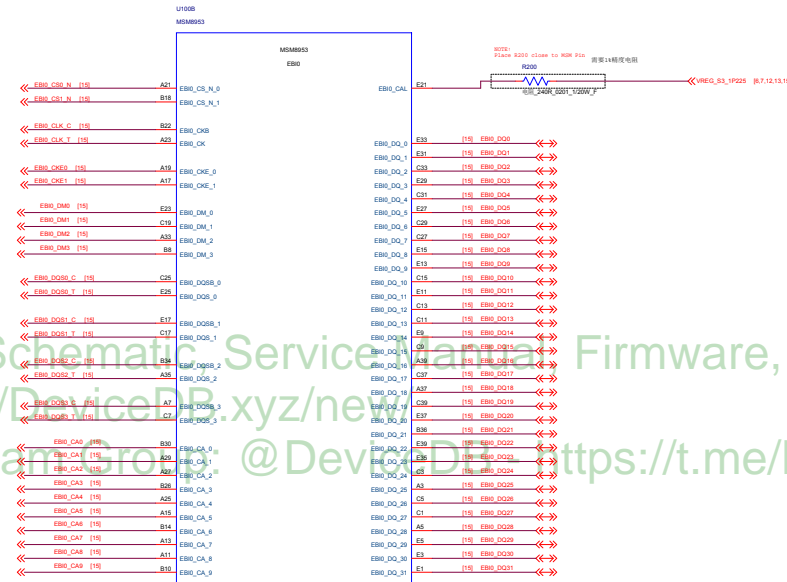
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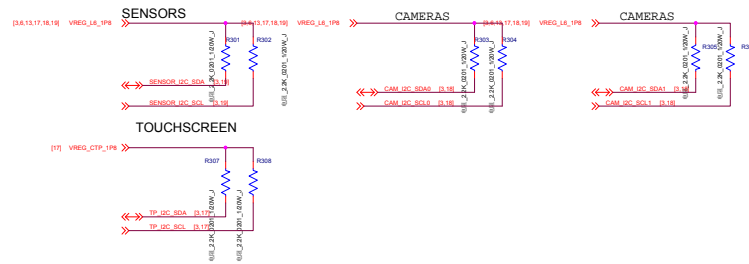
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NOTE:  
Asterisks (\*) indicate modem power management (MPM) wake-up pins



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## I2C PULL-UP RESISTORS



NOTE:  
Ensure SW sets these GPIOs (Sensor, CTP and Camera I2C bus) to inout pull down when the peripherals are powered off to eliminate leakage.

## Breathing LED



GPIO_37	POWER_USB_BOOT
GPIO_154	MODE_DISMABLE
GPIO_158	APPS_BOOT_FROM_ROM

BOOT_CAMP(21:1)	BOOT_CAMP(2)
0B00	00C1 -> 00C2 -> 03B2:0
0B01	00C2 -> 00C3 -> 03B2:0
0B05	00C1 -> 03B2:0
0B11	03B2:0

Default Boot Config (0B00) is 00C1(4MB)

File	E7_M8_V1
Rev	0
Document Number	MSM8993 GPIO
Ver	1.0
Created	2017-01-10
Page	3 of 3

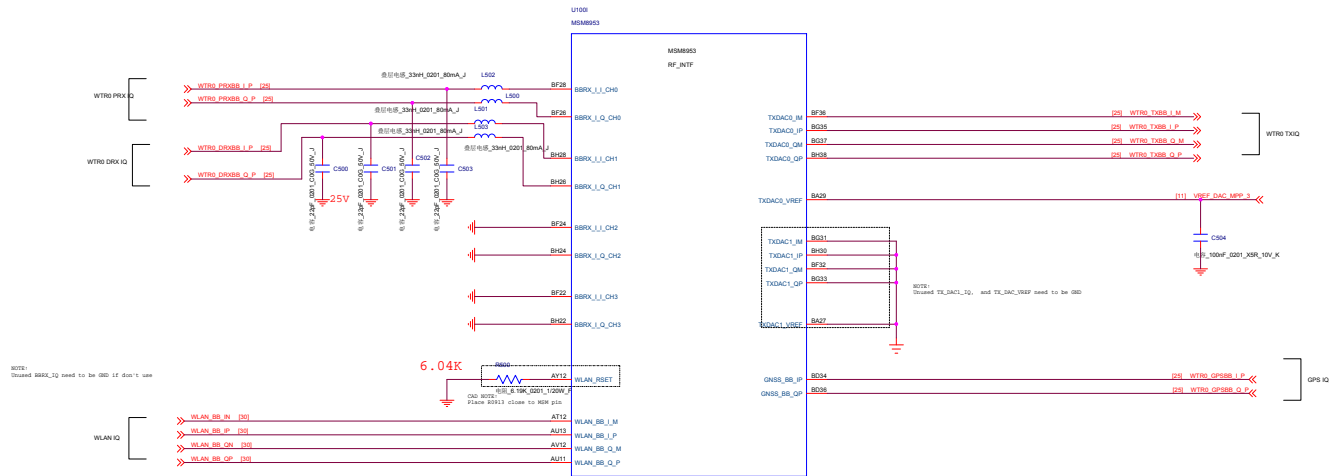
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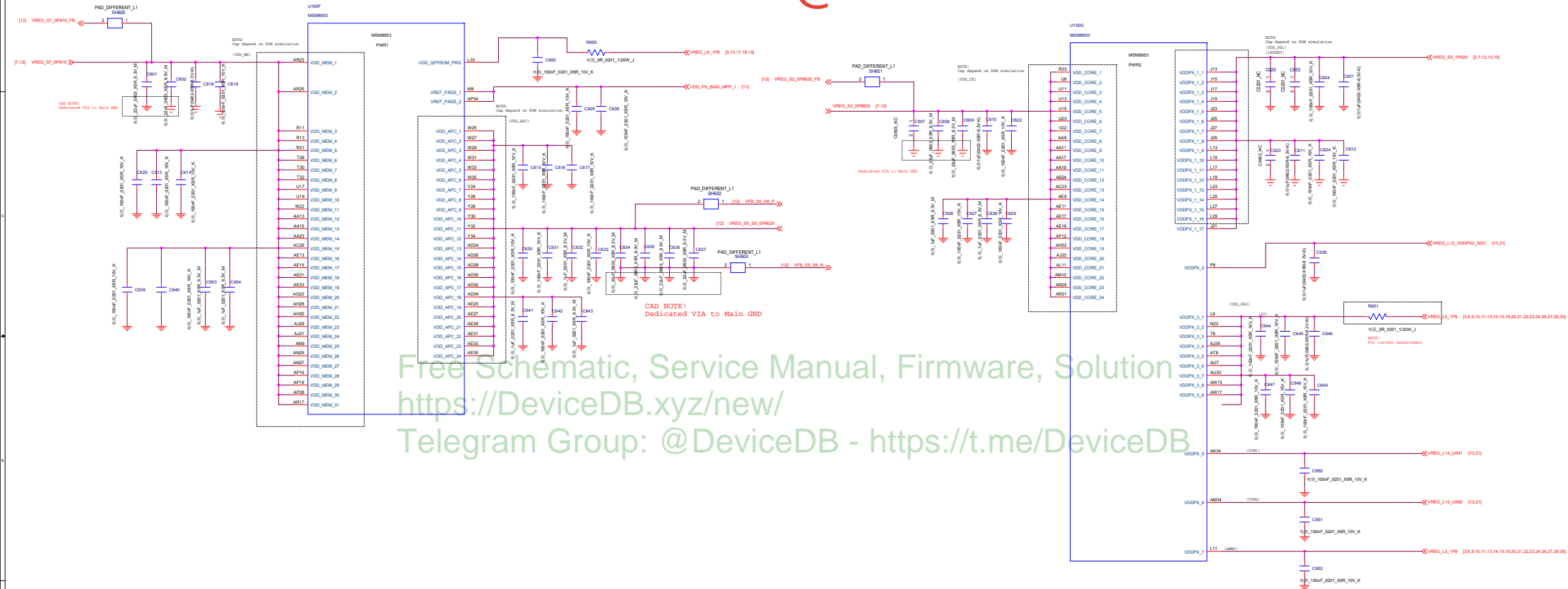
CSI Pin Name	CSI DPHY 4-lane	CSI DPHY 2+1 Mode	CSI CPHY 3Phase Mode
CSI0_3PHASE_PIN0	CSI0_CLKP	CSI0_2LANE_CLKP	NC
CSI0_3PHASE_PIN1	CSI0_CLKN	CSI0_2LANE_CLKN	CSI0_TRI0_A
CSI0_3PHASE_PIN2	CSI0_DP0	CSI0_2LANE_DP0	CSI0_TRI0_B
CSI0_3PHASE_PIN3	CSI0_DN0	CSI0_2LANE_DN0	CSI0_TRI0_C
CSI0_3PHASE_PIN4	CSI0_DP1	CSI0_2LANE_DP1	CSI0_TRI1_A
CSI0_3PHASE_PIN5	CSI0_DN1	CSI0_2LANE_DN1	CSI0_TRI1_B
CSI0_3PHASE_PIN6	CSI0_DP2	CSI0_1LANE_DP0	CSI0_TRI1_C
CSI0_3PHASE_PIN7	CSI0_DN2	CSI0_1LANE_DN0	CSI0_TRI2_A
CSI0_3PHASE_PIN8	CSI0_DP3	CSI0_1LANE_CLKP	CSI0_TRI2_B
CSI0_3PHASE_PIN9	CSI0_DN3	CSI0_1LANE_CLKN	CSI0_TRI2_C
CSI1_3PHASE_PIN0	CSI1_CLKP	CSI1_2LANE_CLKP	NC
CSI1_3PHASE_PIN1	CSI1_CLKN	CSI1_2LANE_CLKN	CSI1_TRI0_A
CSI1_3PHASE_PIN2	CSI1_DP0	CSI1_2LANE_DP0	CSI1_TRI0_B
CSI1_3PHASE_PIN3	CSI1_DN0	CSI1_2LANE_DN0	CSI1_TRI0_C
CSI1_3PHASE_PIN4	CSI1_DP1	CSI1_2LANE_DP1	CSI1_TRI1_A
CSI1_3PHASE_PIN5	CSI1_DN1	CSI1_2LANE_DN1	CSI1_TRI1_B
CSI1_3PHASE_PIN6	CSI1_DP2	CSI1_1LANE_DP0	CSI1_TRI1_C
CSI1_3PHASE_PIN7	CSI1_DN2	CSI1_1LANE_DN0	CSI1_TRI2_A
CSI1_3PHASE_PIN8	CSI1_DP3	CSI1_1LANE_CLKP	CSI1_TRI2_B
CSI1_3PHASE_PIN9	CSI1_DN3	CSI1_1LANE_CLKN	CSI1_TRI2_C
CSI2_3PHASE_PIN0	CSI2_CLKP	CSI2_2LANE_CLKP	NC
CSI2_3PHASE_PIN1	CSI2_CLKN	CSI2_2LANE_CLKN	CSI2_TRI0_A
CSI2_3PHASE_PIN2	CSI2_DP0	CSI2_2LANE_DP0	CSI2_TRI0_B
CSI2_3PHASE_PIN3	CSI2_DN0	CSI2_2LANE_DN0	CSI2_TRI0_C
CSI2_3PHASE_PIN4	CSI2_DP1	CSI2_2LANE_DP1	CSI2_TRI1_A
CSI2_3PHASE_PIN5	CSI2_DN1	CSI2_2LANE_DN1	CSI2_TRI1_B
CSI2_3PHASE_PIN6	CSI2_DP2	CSI2_1LANE_DP0	CSI2_TRI1_C
CSI2_3PHASE_PIN7	CSI2_DN2	CSI2_1LANE_DN0	CSI2_TRI2_A
CSI2_3PHASE_PIN8	CSI2_DP3	CSI2_1LANE_CLKP	CSI2_TRI2_B
CSI2_3PHASE_PIN9	CSI2_DN3	CSI2_1LANE_CLKN	CSI2_TRI2_C

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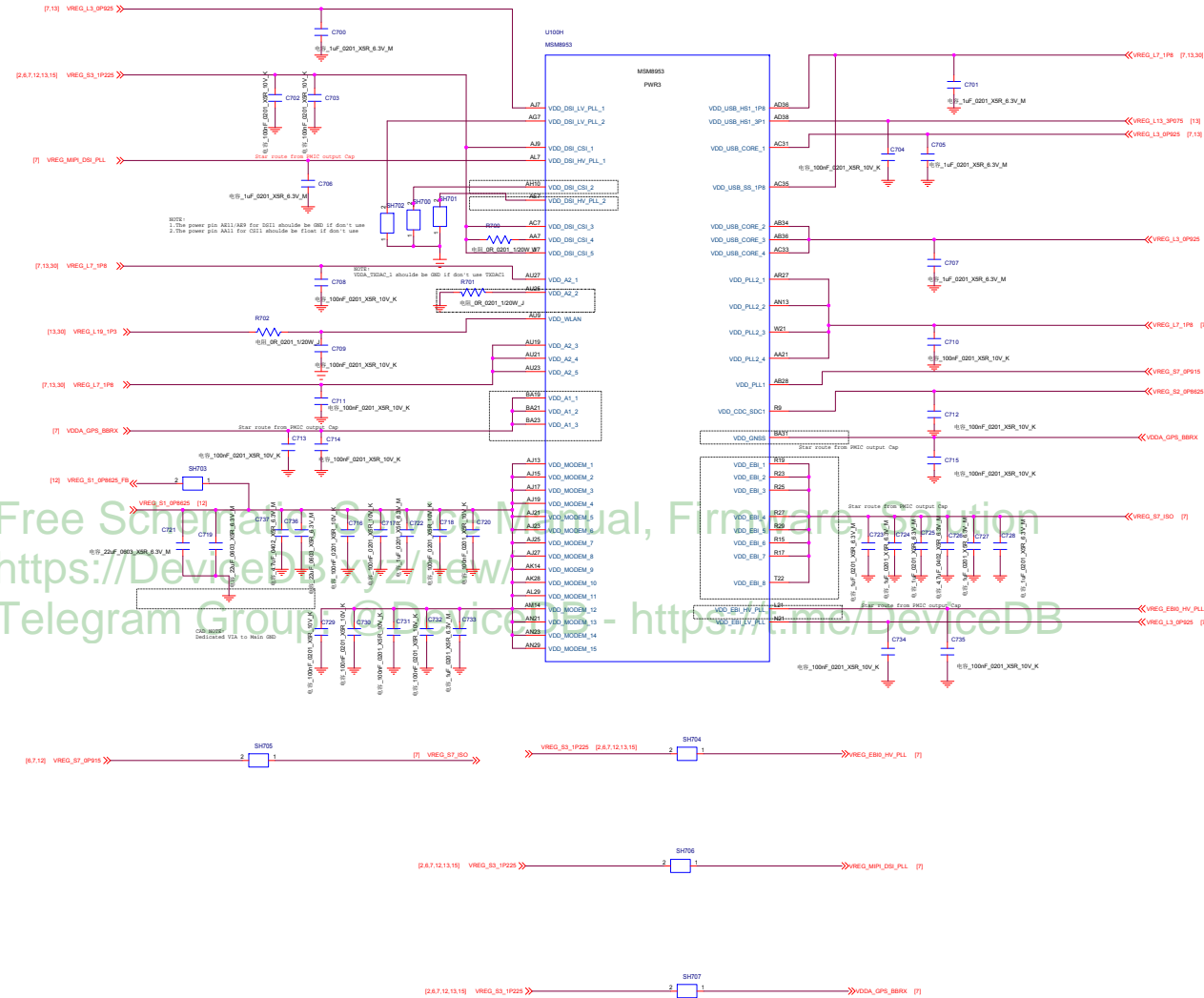
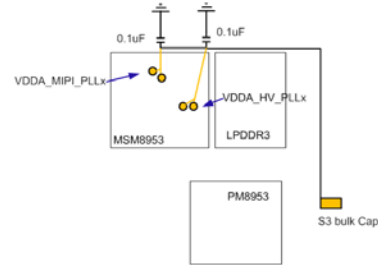
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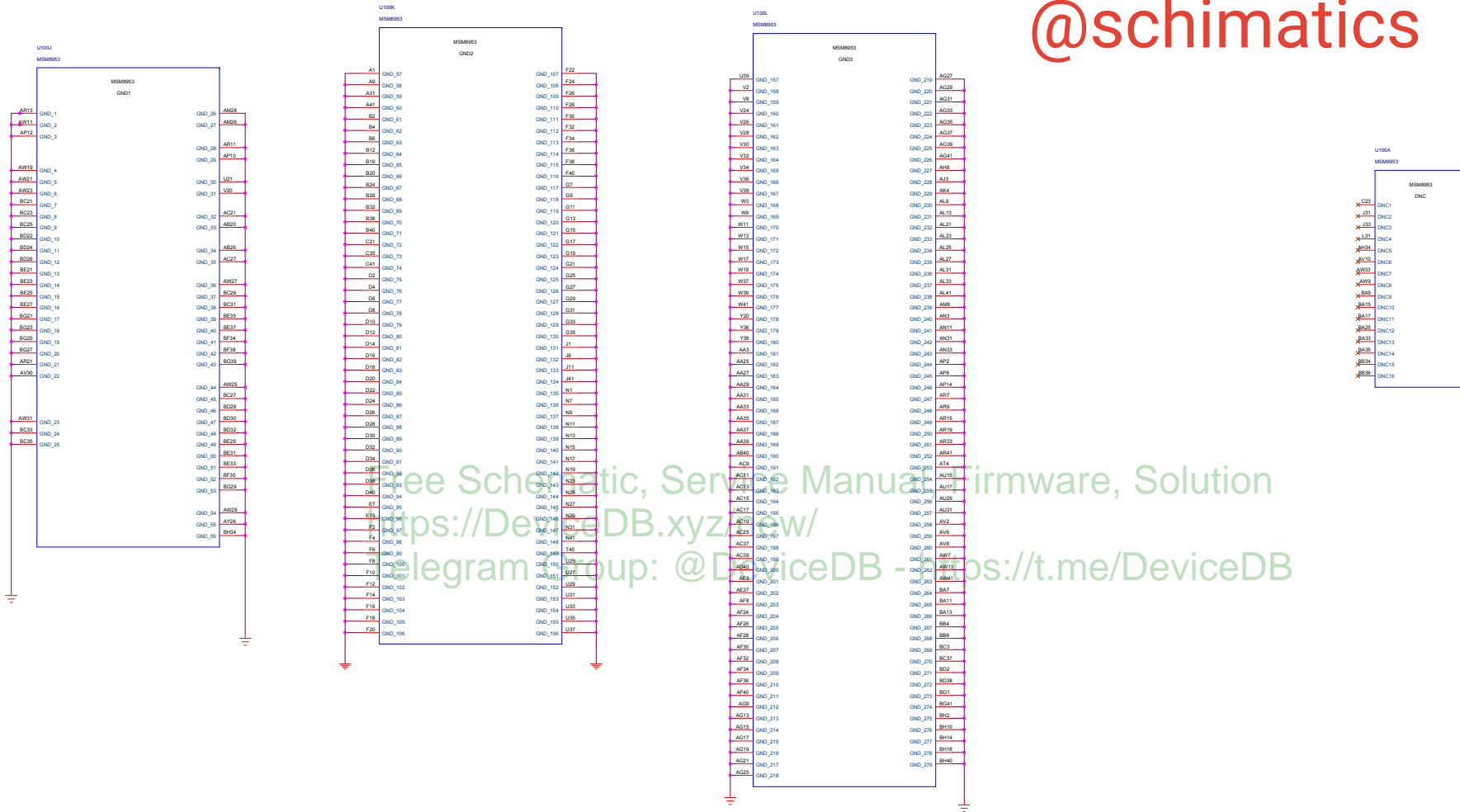


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CAD NOTE:  
About star route from PMIC output Cap:



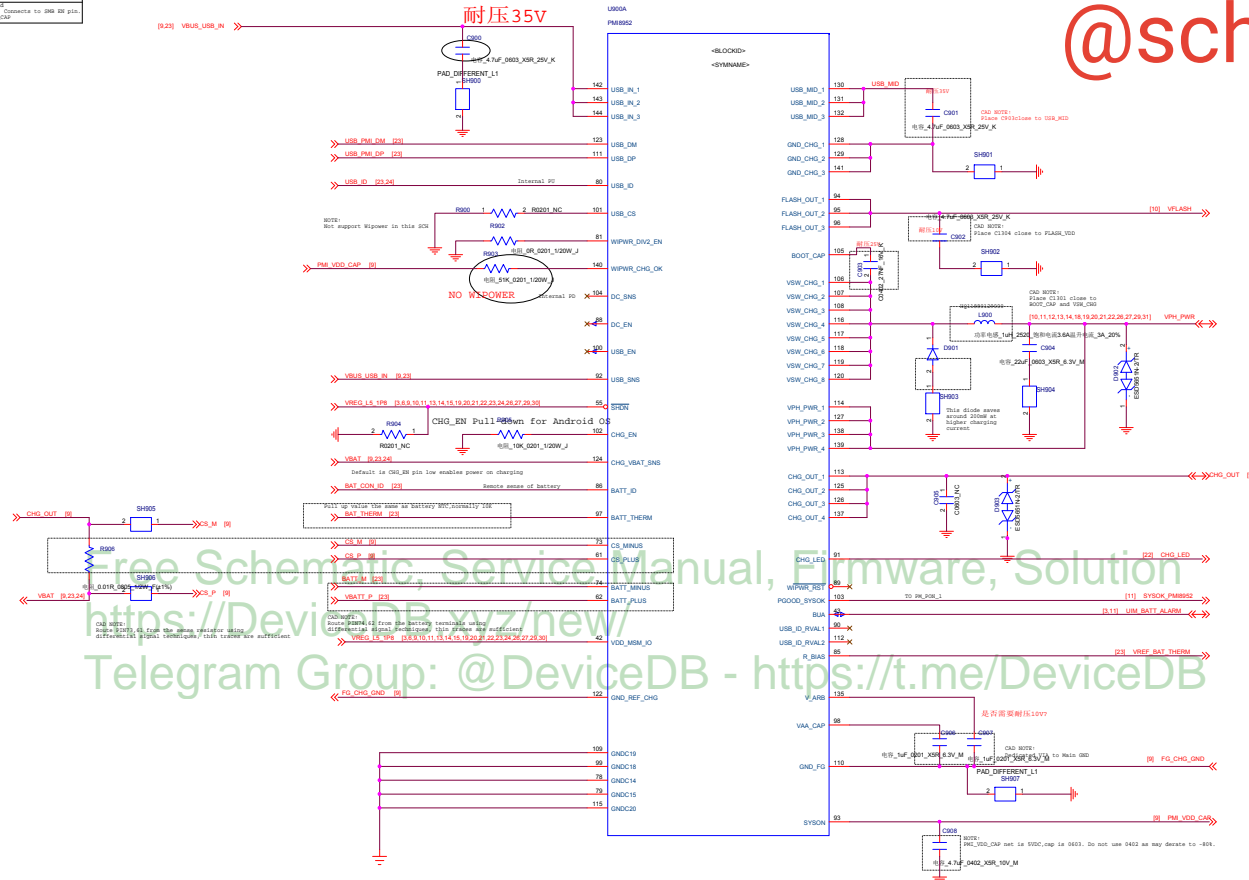
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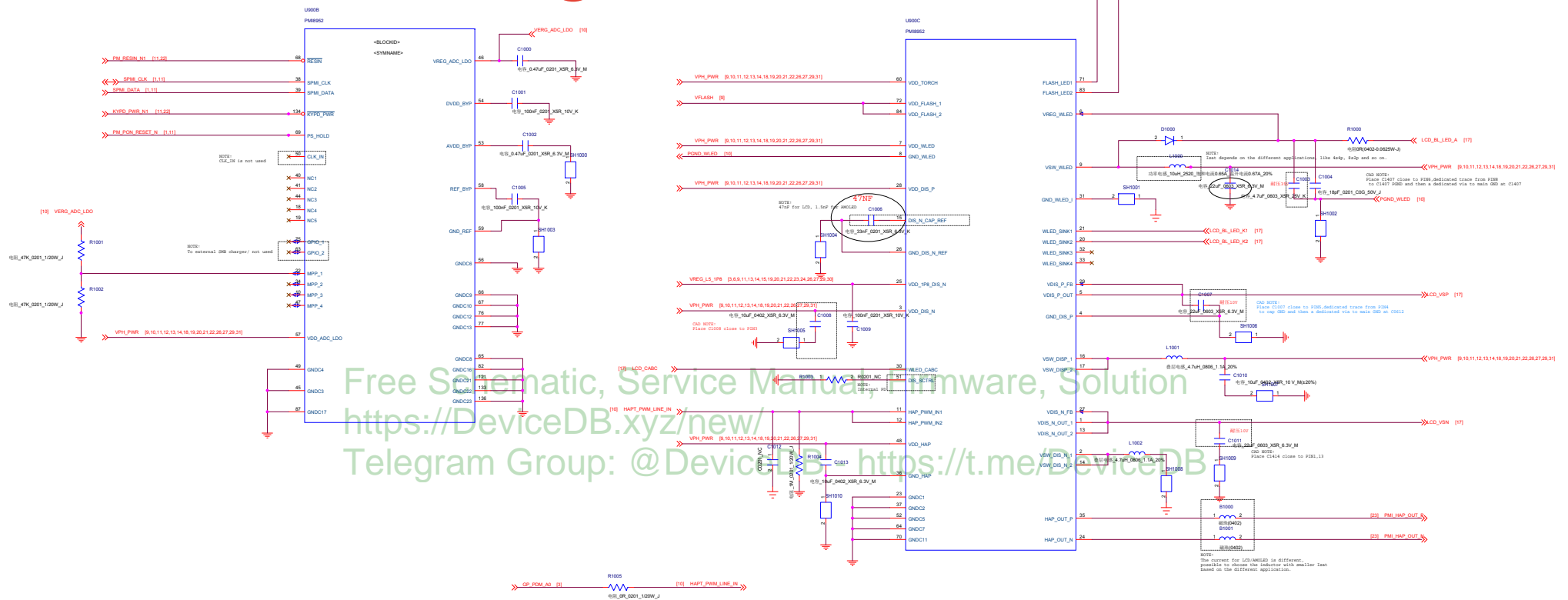


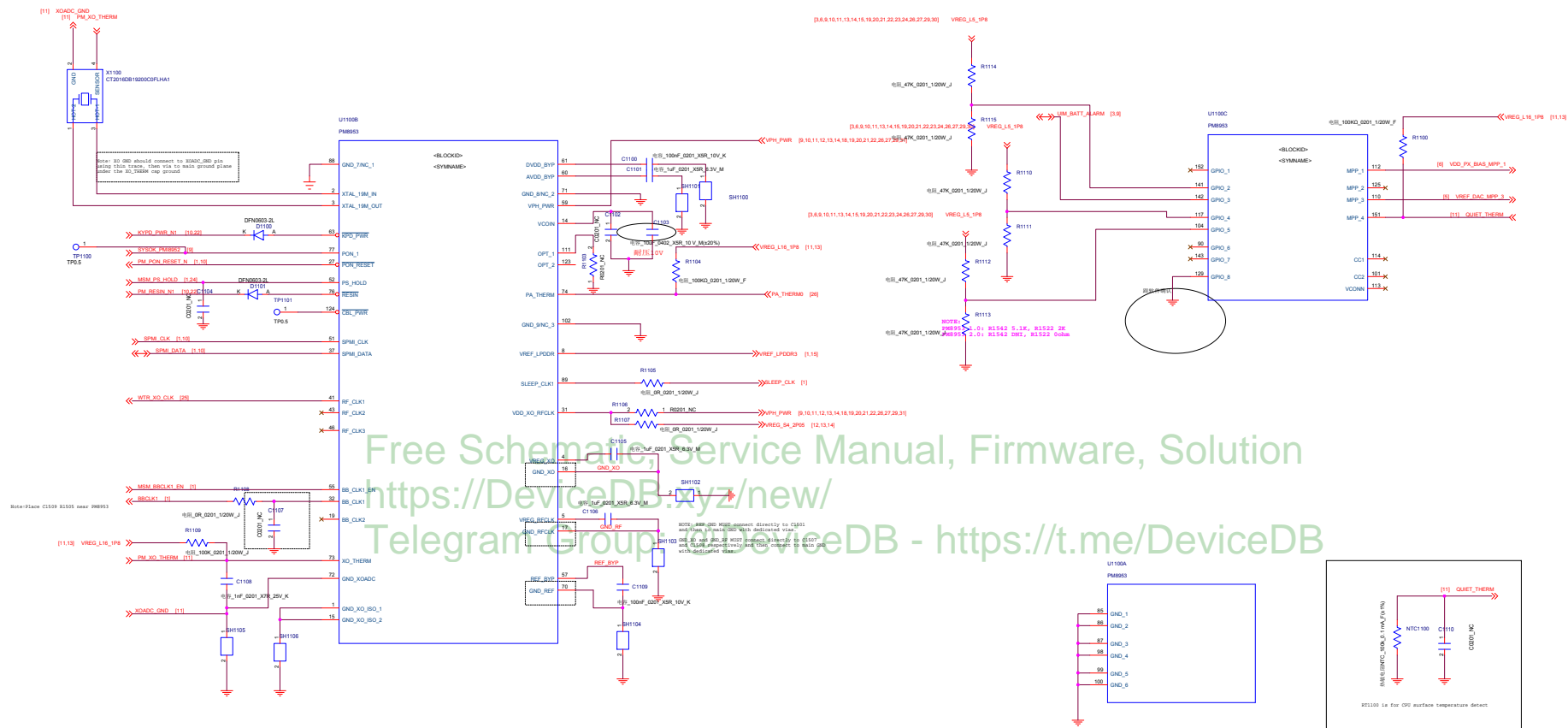
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SWR PIN	connection on device without Wipower	connection on device with Wipower
CHG_OK	Pull up to VDD_CAP with 11kOhm	Stark SWR CHG_OK
DIV2_EN	Pull down to GND with 60ohm	Stark SWR DIV2_EN
GP102	No Connect For parallel charging: Connects to SWR_EN pin. Do NOT pull up to VDD_CAP	10kOhm pull down to gnd For parallel charging: Connects to SWR_EN pin. Do NOT pull up to VDD_CAP

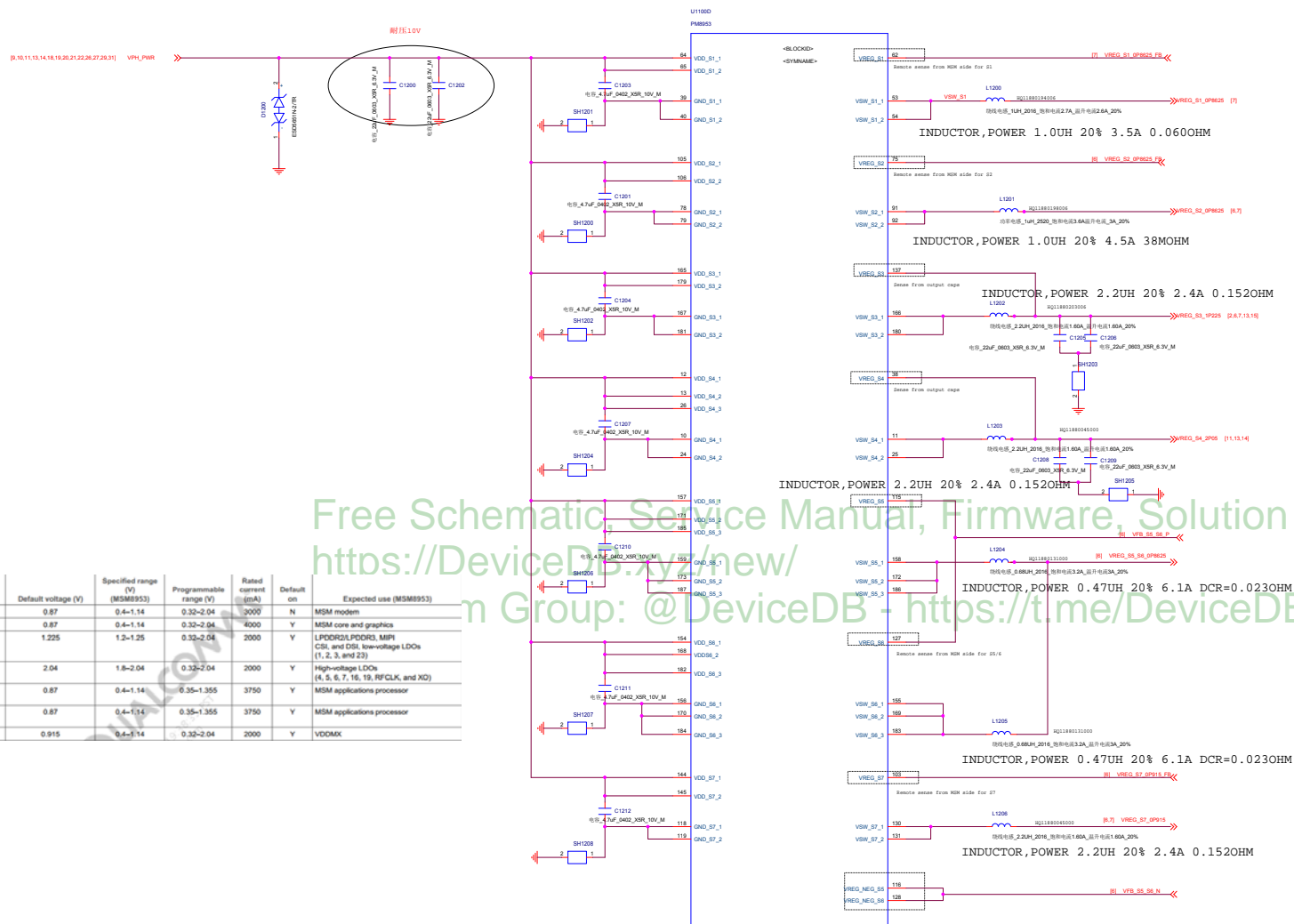


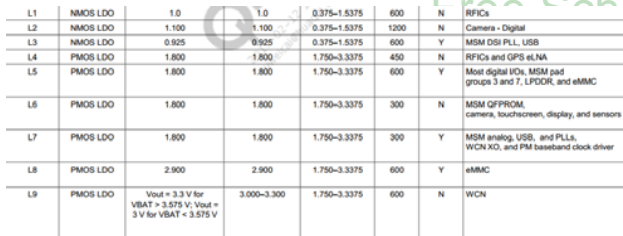
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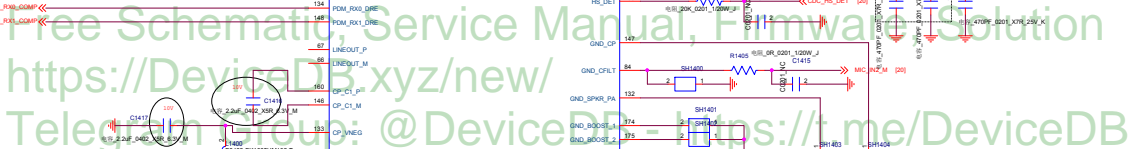


Function	Circuit type	Default voltage (V)	Specified range (V) (MSM8953)	Programmable range (V)	Rated current (mA)	Default on	Expected use (MSM8953)
S1	SMPS	0.87	0.4~1.14	0.32~2.04	3000	N	MSM modem
S2	SMPS	0.87	0.4~1.14	0.32~2.04	4000	Y	MSM core and graphics
S3	SMPS	1.225	1.2~1.25	0.32~2.04	2000	Y	LPODRG/LPODR3, MPI, CSI, and DSI; low-voltage LDOs (1, 2, 3, and 23)
S4	SMPS	2.04	1.8~2.04	0.32~2.04	2000	Y	High-voltage LDOs (4, 5, 6, 7, 16, 19, RFCLK, and XG)
S5	SMPS	0.87	0.4~1.14	0.35~1.355	3750	Y	MSM applications processor
S6	SMPS	0.87	0.4~1.14	0.35~1.355	3750	Y	MSM applications processor
S7	SMPS	0.915	0.4~1.14	0.32~2.04	2000	Y	VDDMX





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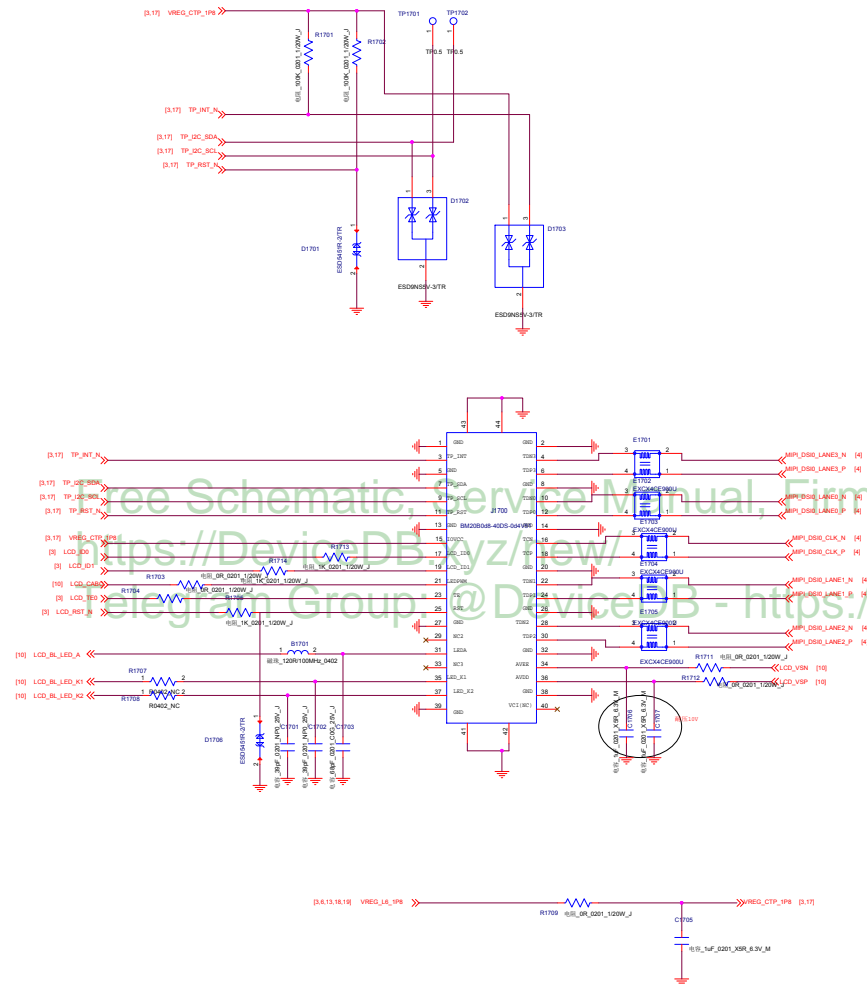




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Note: If best EMI practices are followed for MIPI CSI/DSI signals, there is no need for common mode choke filters. You may choose to have placeholders for common mode depending upon your design constraints. Extreme care must be taken that no stubs are created by doing so.

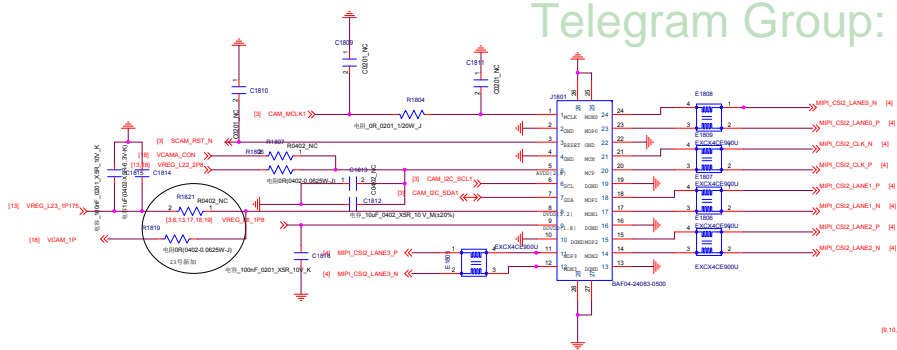


The diagram shows a 2-wire LED driver circuit. Two input lines, labeled F1\_LED1 and F1\_LED2, enter from the left. These lines are connected to a network of components. A 5V supply is connected to the circuit. The circuit includes two LEDs, LED1801 and LED1802, which are connected in series. The circuit also includes two capacitors, C181 and C182, and four resistors, R181, R182, R183, and R184. The components are connected in a way that allows the LEDs to be driven by the 2-wire input. The circuit is powered by a 5V supply and includes a ground connection.

Front Camera

[illegible]

## 待和结构确认方向



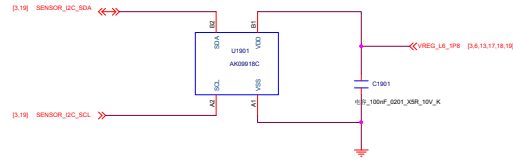
1-wire Pulse Configurable,Max current 200mA,  
12.5mA per step ,Total 16 STEP.

Rev	Rev	Docment Number
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1-wire Pulse Configurable, Max current 200mA.  
12.5mA per step .Total 16 STEP.

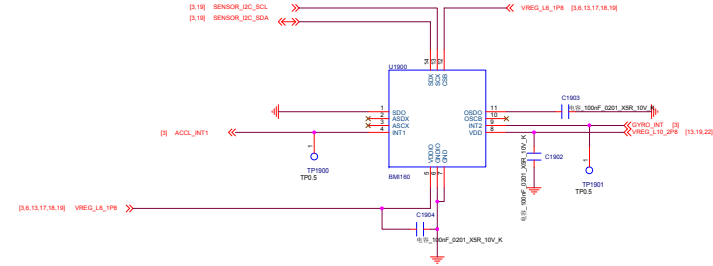
# E-compass

厂家	120 8840	120 88178
IMU110	19	18



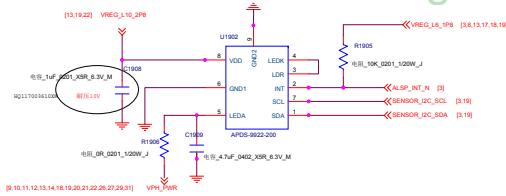
# Gyro+A sensor

厂家	120 8840	120 88178
IMU110	D1	D0

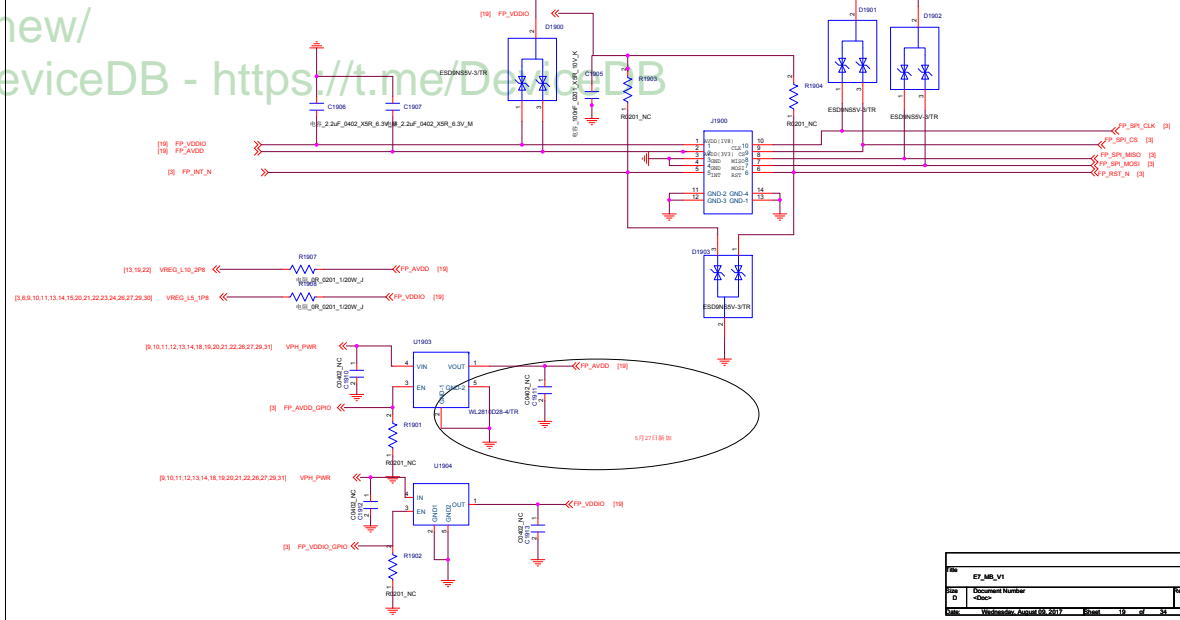


# ALS PS

厂家	120 8840	120 88178
IMU110	91	90

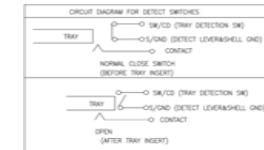


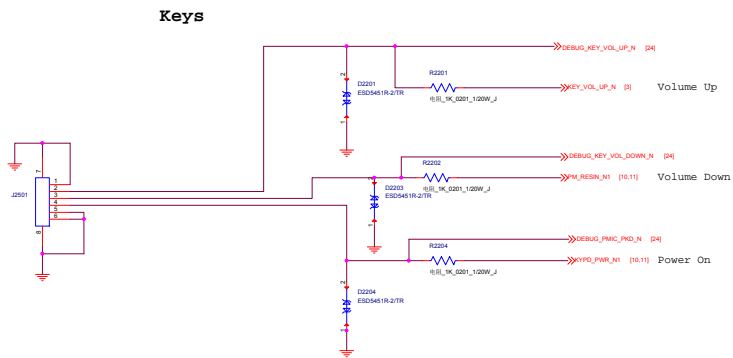
# Finger Print



厂家	120 8840	120 88178
IMU110	91	90

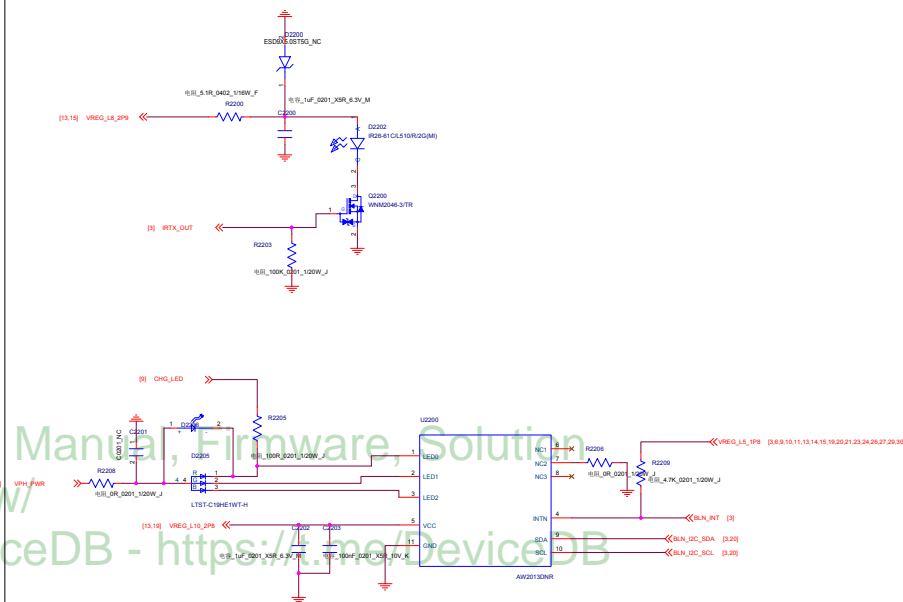




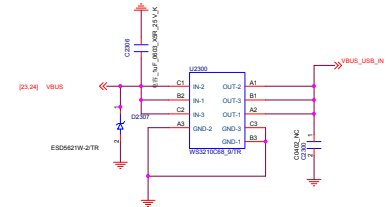
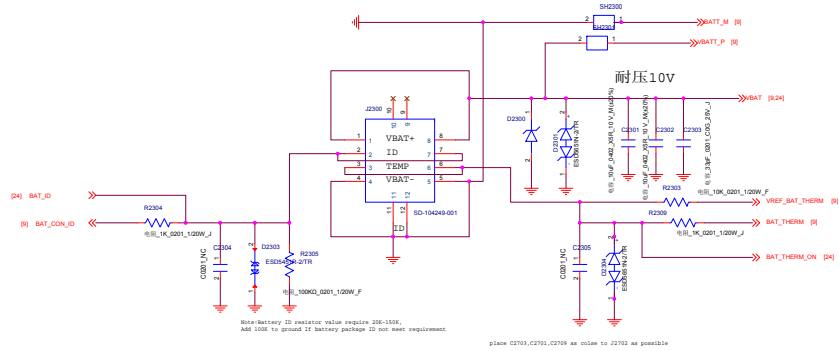


Signal	Description
KPSNS0	Volume Up
PM_RST_N	Volume Down
KYPD_PWR_N	PWR_ON

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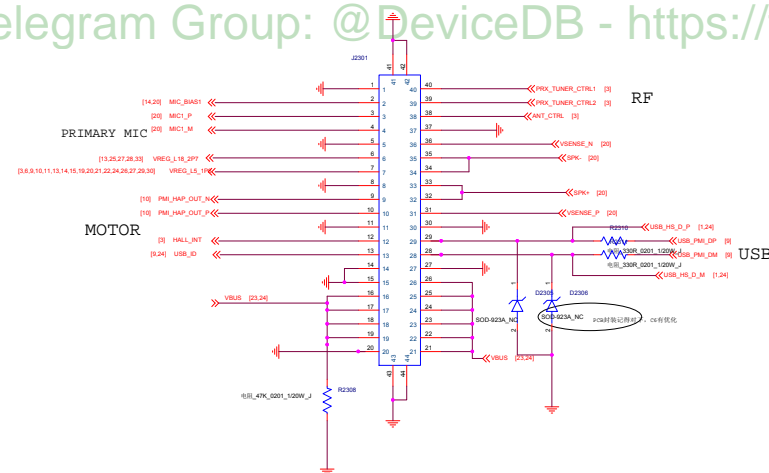


## Battery Connector

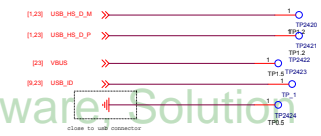
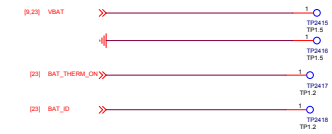
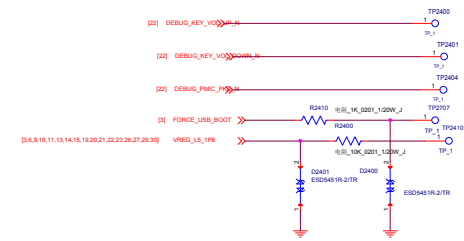


## BTB Connector

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The diagram illustrates the JTAG and BSC interfaces for the TP2402/TP2405. The JTAG interface consists of four lines: JTAG\_TMS, JTAG\_TCK, JTAG\_TDO, and JTAG\_TDI. The BSC interface consists of two lines: MSTRM\_HOLD and MSTRM\_RESET\_N. The MSTRM\_HOLD line is connected to the TP2402/TP2405 pin and has a 10k pull-up resistor. The MSTRM\_RESET\_N line is connected to the TP2402/TP2405 pin and has a 25V voltage rating. The diagram also shows the connection of the TP2402/TP2405 pins to the JTAG and BSC lines.



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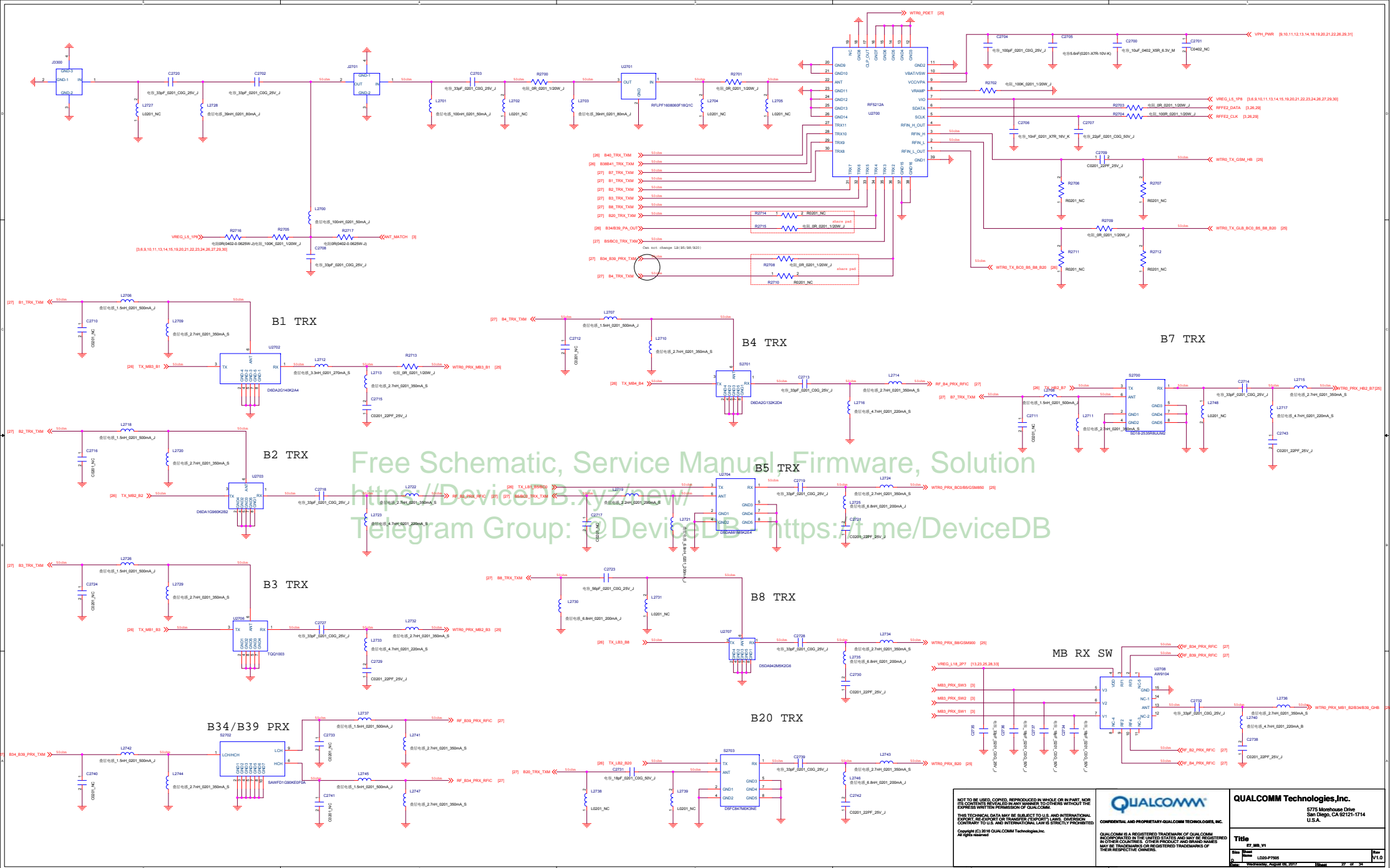
## Grounding

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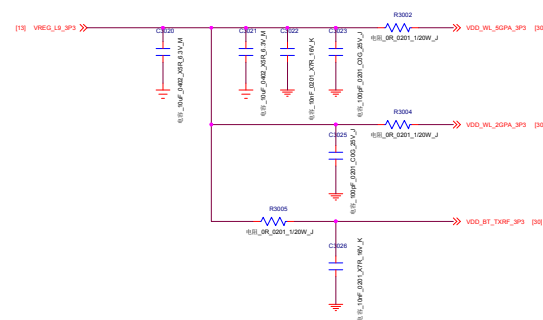
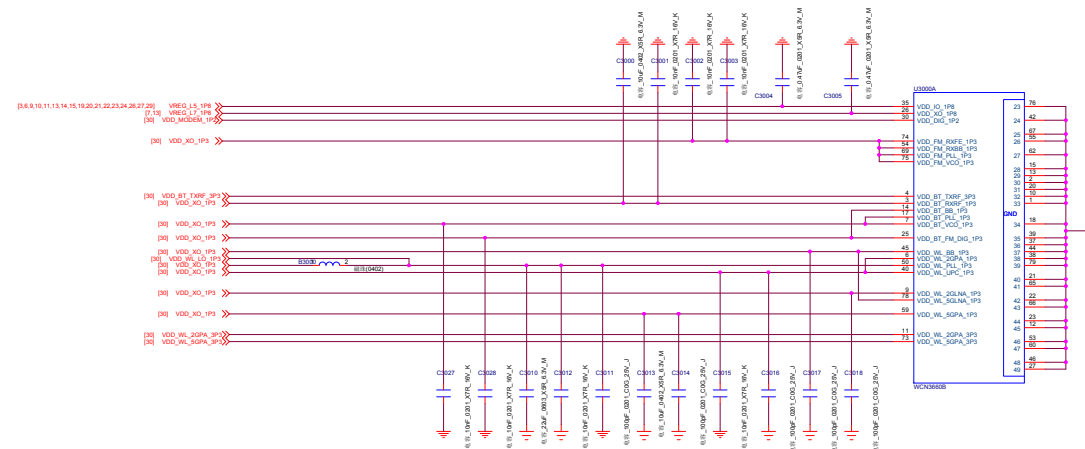
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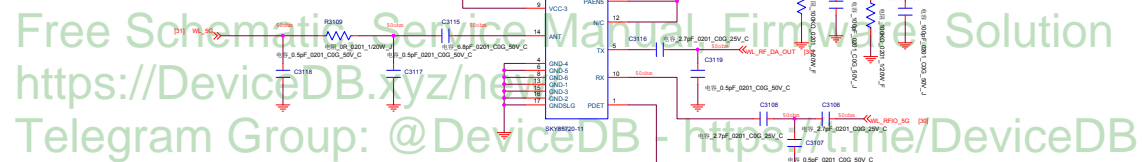
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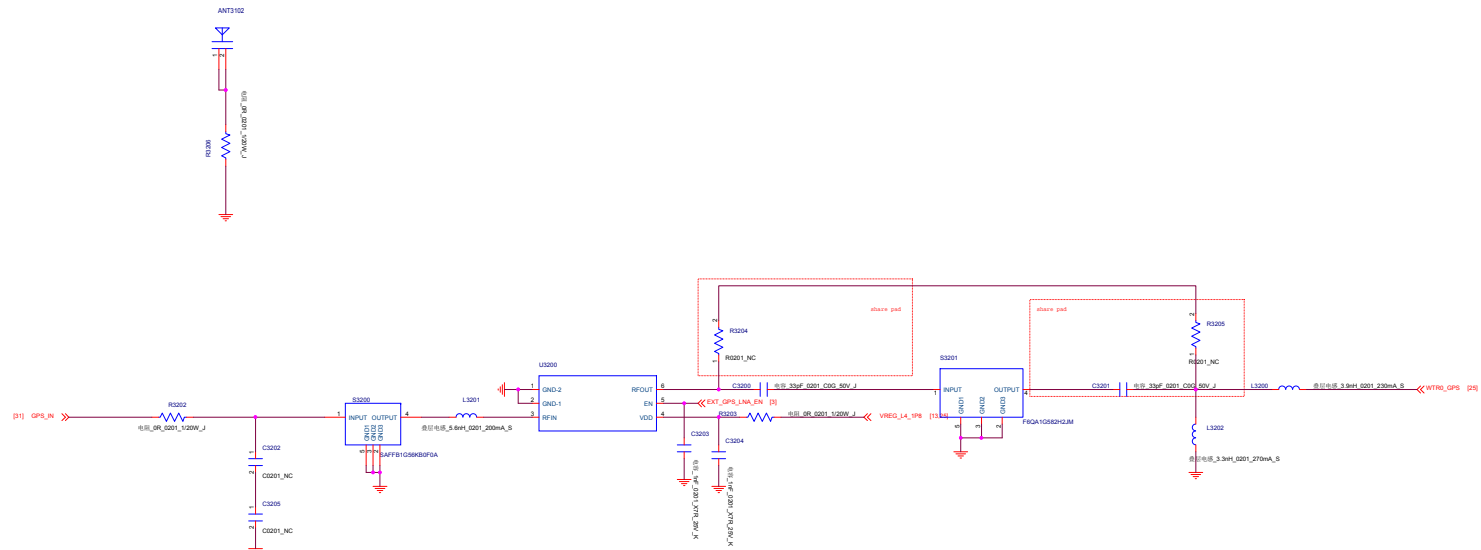
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	extra S3201 option	Non-extra S3201 option
R3200	DNI	0ohm
R3201	DNI	0ohm
C3200	33pF	DNI
C3201	33pF	DNI
S3201	SAFFB1G56KB0F0A	DNI

GPS

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Date	Issue									
Jan	1200-F7936									
Rev										
	V1.0									