1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

REV	ECN	DESCRIPTION OF REVISION	CK APPD / DATE
A	0004536627	PRODUCTION RELEASED	2015-07-21

N71 MLB - PVT OK2FAB

LAST_MODIFICATION=Tue Jul 21 11:39:02 2015

SCH 051-1902
BRD 820-5507
MCO 056-01060

BOM 639-00263 (BETTER,DB30)
BOM 639-00265 (ULTRA,DB30)
BOM 639-00266 (SUPREME,DB30)
BOM 639-01056 (BETTER,B30)
BOM 639-01057 (ULTRA,B30)
BOM 639-01058 (SUPREME,B30)
BOM 639-01098 (BETTER,DB30C)
BOM 639-01100 (ULTRA,DB30C)
BOM 639-01099 (SUPREME,DB30C)
BOM 939-01627 (BETTER,DARWIN)

TABLE OF CONTENTS

DRAWING TITLE: SCHEM,SINGLE,BRD,N71

Apple Inc.

DRAWING NUMBER: 051-1902 | SIZE: D
REVISION: A.0.0
BRANCH:
PAGE: 1 OF 49
SHEET: 1 OF 59

SCHEMATIC & PCB BOM CALLOUTS

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
051-1902	1	SCH,SINGLE_BRD,N71	SCH	CRITICAL	?
820-5507	1	PCBF,SINGLE_BRD,N71	PCB	CRITICAL	?
825-6838	1	EEEE CODE FOR 639-00263	EEEE_G2KM	CRITICAL	EEEE_16G_DB30
825-6838	1	EEEE CODE FOR 639-00265	EEEE_G2KN	CRITICAL	EEEE_64G_DB30
825-6838	1	EEEE CODE FOR 639-00266	EEEE_G2KL	CRITICAL	EEEE_128G_DB30
825-6838	1	EEEE CODE FOR 639-01056	EEEE_GKF9	CRITICAL	EEEE_16G_B30
825-6838	1	EEEE CODE FOR 639-01057	EEEE_GKFC	CRITICAL	EEEE_64G_B30
825-6838	1	EEEE CODE FOR 639-01058	EEEE_GKF8	CRITICAL	EEEE_128G_B30
825-6838	1	EEEE CODE FOR 639-01098	EEEE_GLHL	CRITICAL	EEEE_16G_DB30C
825-6838	1	EEEE CODE FOR 639-01100	EEEE_GLHR	CRITICAL	EEEE_64G_DB30C
825-6838	1	EEEE CODE FOR 639-01099	EEEE_GLHM	CRITICAL	EEEE_128G_DB30C
825-6838	1	EEEE CODE FOR 939-01627	EEEE_GR09	CRITICAL	EEEE_16G_DARWIN

S3E NAND BOM OPTIONS

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
335S00039	1	NAND,1YNM,16GX8,S3E,64G,T,SLGA70	U1500	CRITICAL	NAND_16G
335S00075	1	NAND,1YNM,64GX8,S3E,MLB,64G,H,SLGA70	U1500	CRITICAL	NAND_64G
335S00079	1	NAND,1YNM,128GX8,S3E,TLC,128G,H,SLGA70	U1500	CRITICAL	NAND_128G

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
335S00074	335S00039	NAND_16G	U1500	HYNIX 16G SLGA70 C DIE
335S00078	335S00075	NAND_64G	U1500	HYNIX 64G SLGA70
335S00064	335S00075	NAND_64G	U1500	SANDISK 64G SLGA70 1Z
335S00065	335S00079	NAND_128G	U1500	SANDISK 128G SLGA70

CARBON/ACCEL BOM OPTIONS

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
338S1163	1	IC,ACCEL,3-AXIS,DIG,BMA282,LGA14	U3030	NOSTUFF
117S0202	1	RES,MF,20 OHM,5%,1/32W,01005	R3030	NOSTUFF
117S0202	1	RES,MF,20 OHM,5%,1/32W,01005	R3031	NOSTUFF
117S0202	1	RES,MF,20 OHM,5%,1/32W,01005	R3032	NOSTUFF
138S0831	1	CAP,CER,X5R,2.2UF,20%,6.3V,0201	C3031	NOSTUFF
132S0316	1	CAP,CER,X5R,0.1UF,20%,6.3V,01005	C3032	NOSTUFF
338S00017	1	IC,CARBON,MPU-6700-12,LGA16	U3010	INVENSENSE_CARBON
338S1163	1	IC,ACCEL,3-AXIS,DIG,BMA282,LGA14	U3030	INVENSENSE_CARBON
117S0202	1	RES,MF,20 OHM,5%,1/32W,01005	R3030	INVENSENSE_CARBON
117S0202	1	RES,MF,20 OHM,5%,1/32W,01005	R3031	INVENSENSE_CARBON
117S0202	1	RES,MF,20 OHM,5%,1/32W,01005	R3032	INVENSENSE_CARBON
138S0831	1	CAP,CER,X5R,2.2UF,20%,6.3V,0201	C3031	INVENSENSE_CARBON
132S0316	1	CAP,CER,X5R,0.1UF,20%,6.3V,01005	C3032	INVENSENSE_CARBON
338S00087	1	IC,CARBON 1.1,MPU-6800-00,LGA16	U3010	INVENSENSE_STANDALONE_CARBON

ALTERNATE BOM OPTIONS

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:	
138S00032	138S0831	ALTERNATE	C0610	TY,2.2UF,0201	NOT ALL REFERENCE DESIGNATORS LISTED. USED ~116 TIMES IN DESIGN.
138S00049	138S0831	ALTERNATE	C0610	KYOCERA,2.2UF,0201	USED ~116 TIMES IN DESIGN.
155S0660	155S0513	ALTERNATE	FL3100	MURATA,FERR,22-OHM	USED ~7 TIMES IN DESIGN.
138S00005	138S00003	ALTERNATE	C2000	TY,15UF,0402	USED ~63 TIMES IN DESIGN.
138S00048	138S00003	ALTERNATE	C2000	KYOCERA,15UF,0402	USED ~63 TIMES IN DESIGN.
138S0702	138S0657	ALTERNATE	C2111	MURATA,4.3UF,0610	USED ~3 TIMES IN DESIGN.
118S0764	118S0717	ALTERNATE	R2250	PANASONIC,3.92K-OHM,0201	
138S00006	138S0835	ALTERNATE	C1106	TY,4.3UF,0402	USED ~19 TIMES IN DESIGN.
152S2052	152S1929	ALTERNATE	L2060	CYNTEC,1UH,1608	
155S0773	155S0453	ALTERNATE	FL3110	TY,FERR,120-OHM,01005	USED ~61 TIMES IN DESIGN.
377S0168	377S0140	ALTERNATE	DZ3150	TDK,VARISTOR,6.8V,100PF,01005	USED ~9 TIMES IN DESIGN.
155S00067	155S0581	ALTERNATE	FL4200	TDK,FERR,240-OHM,0201	USED ~8 TIMES IN DESIGN.
155S00012	155S00009	ALTERNATE	L3100	MURATA,CHOKE,65-OHM,0605	USED ~11 TIMES IN DESIGN.
138S0706	138S0739	ALTERNATE	C3302_RF	MURATA,CAP,CER,1UF,20%,10V,X5R,0201	USED ~17 TIMES IN DESIGN.
138S0945	138S0739	ALTERNATE	C3302_RF	KYOCERA,CAP,CER,1UF,20%,10V,X5R,0201	USED ~17 TIMES IN DESIGN.
155S00095	155S00068	ALTERNATE	FL1280	FERR BD,100 OHM,25%,100MA,2 OHM,01005	
138S0648	138S0652	ALTERNATE	C3650	TY,4.7UF,0402	USED ~12 TIMES IN DESIGN.
132S0400	132S0436	ALTERNATE	C1280	CAP,CER,X5R,0.22UF,20%,6.3V,01005	USED ~2 TIMES IN DESIGN.
155S0960	155S0941	ALTERNATE	FL3151	FERR BD,70 OHM,25%,300MA,0.4 DCR,01005	USED ~9 TIMES IN DESIGN.
138S00024	138S0986	ALTERNATE	C1107	CAP,CER,3-TERM,7.5UF,20%,4V,0402	USED ~7 TIMES IN DESIGN.
335S00066	335S0946	ALTERNATE	U0900	IC,EEPROM,16KX8,1.8V,I2C,WLCSP4	
155S0653	155S0511	ALTERNATE	FL4600	FERR BD,33 OHM,25%,750MA,0.09OCR,0201	USED ~4 TIMES IN DESIGN.

POWER INDUCTOR ALTERNATES

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
152S00120	152S00077	ALTERNATE	L2070	TAIYO 2016 1.0UH 0.65MM
152S00118	152S00075	ALTERNATE	L3700	TAIYO 2016 1.2UH

ACTIVE DIODE ALTERNATE

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
376S00106	376S00047	ALTERNATE	Q2300	DIODES INC. ACT DIODE

SHIELD PART NUMBERS

REFERENCE DESIGNATOR(S)	BOM OPTION	PART#	QTY	DESCRIPTION		
		806-02895	1	SHIELD,EMI,UPPER FRONT,WTOP,N71	SH0500	COMMON
		806-04588	1	SHIELD,EMI,LOWER FRONT,CLOSED,NOMU,N71	SH0501	COMMON
		806-03994	1	SHIELD,EMI,SA,OPEN,N71	SH0502	COMMON
		806-02897	1	SHIELD,EMI,UPPER BACK,WTOP,N71	SH0503	COMMON
		806-02898	1	SHIELD,EMI,LOWER BACK,WTOP,N71	SH0504	COMMON

SOC/PMU SUB BOMS

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
685-00069	1	SUBBOM,SINGLE,BRD,MAUI,N71	SUBBOM_SOC	COMMON
338S00120	1	IC,PMU,ANTIGUA,A0,D2255A1,OTP-AL,WLCSP380	U2000	MAUI
118S0631	1	RES,MF,100 OHM,1%,1/32W,01005	R0730	MAUI
131S0307	1	CAP,CER,NP0/C0G,100PF,5%,16V,01005	C0730	MAUI
339S00112	1	PROD FUSED, H DRAM	U0600	MAUI
117S0161	1	RES,MF,0 OHM,1/32W,01005	R0651	MAUI

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
338S00122	1	IC,PMU,ANTIGUA,D2255A1,OTP-2L,WLCSP380	U2000	MALTA
118S00009	1	RES,MF,3.01KOHM,1%,1/32W,01005	R0730	MALTA
131S0307	1	CAP,CER,NP0/C0G,100PF,5%,16V,01005	C0730	NOSTUFF
339S00124	1	M DEV FUSED, M DRAM	U0600	MALTA
118S00025	1	RES,MF,330 OHM,1%,1/32W,01005	R0651	MALTA

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
685-00070	685-00069	ALTERNATE	SUBBOM_SOC	SUBBOM,SINGLE,BRD,MALTA,N71

SOC ALTERNATES

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
339S00113	339S00112	MAUI	U0600	PROD FUSED, M DRAM
339S00114	339S00112	MAUI	U0600	PROD FUSED, S DRAM

339S00125	339S00124	MALTA	U0600	M PROD FUSED, H DRAM, ATK
339S00126	339S00124	MALTA	U0600	M PROD FUSED, S DRAM, ATK
339S00127	339S00124	MALTA	U0600	M PROD FUSED, H DRAM, SCK
339S00128	339S00124	MALTA	U0600	M PROD FUSED, H DRAM, SCK
339S00129	339S00124	MALTA	U0600	M PROD FUSED, S DRAM, SCK

INDUCTOR SUB BOMS

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
685-00081	1	SUBBOM,SINGLE,BRD,CYNTEC,N71	SUBBOM_IND	COMMON
152S00074	6	IND,PWR,SHLD,1.0UH,3.6A,0.060 OHM,2016	L2009,L2002,L2010,L2012,L2029,L2030	CYNTEC
152S00074	5	IND,PWR,SHLD,1.0UH,3.6A,0.060 OHM,2016	L2040,L2050,L2300,L3300,L4021	CYNTEC
152S00081	6	IND,PWR,SHLD,0.47UH,3.8A,0.048 OHM,2012	L2001,L2003,L2011,L2013,L2021,L2041	CYNTEC

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
152S00117	6	IND,PWR,SHLD,1.0UH,3.6A,0.060 OHM,2016	L2009,L2002,L2010,L2012,L2029,L2030	TAIYO
152S00117	5	IND,PWR,SHLD,1.0UH,3.6A,0.060 OHM,2016	L2040,L2050,L2300,L3300,L4021	TAIYO
152S00121	6	IND,PWR,SHLD,0.47UH,3.8A,0.048 OHM,2012	L2001,L2003,L2011,L2013,L2021,L2041	TAIYO

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
685-00080	685-00081	ALTERNATE	SUBBOM_IND	SUBBOM,SINGLE,BRD,TAIYO,N71

PAGE TITLE
SYSTEM:BOM TABLES

Apple Inc.

DRAWING NUMBER 051-1902
SIZE D
REVISION A.0.0
BRANCH
PAGE 3 OF 49
SHEET 2 OF 59

TESTPOINTS

POWER

TP00 — VOLTAGE=0V — TP-P6 — ROOM=TEST — POWER GROUND

TP01 — 31 30 17 PP5V0_USB — TP-P6 — ROOM=TEST — VBUS

TP02 — 18 17 PP_BATT_VCC — TP-P6 — ROOM=TEST — VBATT

TP03 — TP-P6 — ROOM=TEST — VBATT

TP05 — TP-P55 — ROOM=TEST

RESET

33 16 9 5 PMU_TO_SYSTEM_COLD_RESET_L — TP06 — TP-P55 — ROOM=TEST — SOC & BB RESET

DFU

33 8 FORCE_DFU — TP07 — TP-P55 — ROOM=TEST

21 20 17 14 13 12 9 8 7 6 5 3 33 29 PP1V8 — PP07 P4MM-NSM 1 SM PP — ROOM=TEST

33 8 DFU_STATUS — PP08 P4MM-NSM 1 SM PP — ROOM=TEST

FORCE DFU PROCEDURE:

1. FROM OFF MODE SHORT TP07 TO PP07
2. PLUG IN E75 CABLE TO FORCE DFU

E75

31 30 TRISTAR_DP1_CONN_P — TP08 — TP-P55 — ROOM=TEST — TRISTAR USB

31 30 TRISTAR_DP1_CONN_N — TP09 — TP-P55 — ROOM=TEST — TRISTAR USB

31 30 TRISTAR_DP2_CONN_P — TP10 — TP-P55 — ROOM=TEST — TRISTAR DEBUG UART

31 30 TRISTAR_DP2_CONN_N — TP11 — TP-P55 — ROOM=TEST — TRISTAR DEBUG UART

31 30 PP_TRISTAR_ACC1 — TP12 — TP-P55 — ROOM=TEST — TRISTAR ACCESSORY ID

31 30 PP_TRISTAR_ACC2 — TP13 — TP-P55 — ROOM=TEST — TRISTAR ACCESSORY POWER

TP14 — TP-P55 — ROOM=TEST

31 30 TRISTAR_CON_DETECT_L — TP15 — TP-P55 — ROOM=TEST

AMUX

16 PMU_AMUX_AY — TP16 — TP-P55 — ROOM=TEST

16 PMU_AMUX_BY — TP17 — TP-P55 — ROOM=TEST

MOJAVE

28 27 MESA_TO_BOOST_EN — TP18 — TP-P55 — ROOM=TEST

28 27 PP16V5_MESA — TP19 — TP-P55 — ROOM=TEST

LCM

29 PP_LCM_BL_CAT1_CONN — TP20 — TP-P55 — ROOM=TEST

29 PP_LCM_BL_CAT2_CONN — TP21 — TP-P55 — ROOM=TEST

29 PP_LCM_BL_ANODE_CONN — TP22 — TP-P55 — ROOM=TEST

SUPER SCREW

TP23 — TP-P80 — ROOM=TEST

N71 I2C DEVICE MAP

I2C BUS	DEVICE	BINARY	7-BIT HEX	8-BIT HEX
I2C0	ANTIGUA PMU	1110100X	0X74	0XE8
	CHESTNUT	0100111X	0X27	0X4E
	MUON	1100010X	0X62	0XC4
I2C1	TIGRIS	1110101X	0X75	0XEA
	ARC DRIVER	1000001X	0X41	0X82
	SPEAKER AMP	1000000X	0X40	0X80
	TRISTAR	0011010X	0X1A	0X34
I2C2	ALS	0101001X	0X29	0X52
	DISP EEPROM	1010001X	0X51	0XA2
OWL	UNUSED	N/A	N/A	N/A
ISP I2C0	REAR CAM	TBD	TBD	TBD
	LED DRIVER	1100011X	0X63	0XC6
ISP I2C1	FRONT CAM	0010000X	0X10	0X20
TOUCH I2C	MESON	1000000X	0x40	0x80
	MAMBA	1100000X	0x60	0xC0
	DOPPLER	1011000X	0x58	0xB0
SEP I2C	SEP EEPROM	1010001X	0x51	0xA2

BOOTSTRAPPING: BOARD REV
BOARD ID
BOOT CONFIG

8 OUT BOARD_REV3 — R0400 ROOM=SOC 1 2 1.00K 01005 MF 5% 1/32W — PP1V8 3 5 6 7 8 9 12 13 14 17 20 21 29 33

8 OUT BOARD_REV2 — NOSTUFF R0401 ROOM=SOC 1.00K 01005 MF 5% 1/32W

8 OUT BOARD_REV1 — NOSTUFF R0402 ROOM=SOC 1.00K 01005 MF 5% 1/32W

8 OUT BOARD_REV0 — R0403 ROOM=SOC 1.00K 01005 MF 5% 1/32W

8 OUT BOARD_ID4 — NOSTUFF R0404 ROOM=SOC 1.00K 01005 MF 5% 1/32W

8 OUT BOARD_ID3 — NOSTUFF R0405 ROOM=SOC 1.00K 01005 MF 5% 1/32W

8 OUT BOARD_ID2 — R0406 ROOM=SOC 1.00K 01005 MF 5% 1/32W

8 OUT BOARD_ID1 — NOSTUFF R0407 ROOM=SOC 1.00K 01005 MF 5% 1/32W

8 OUT BOARD_ID0 — NOSTUFF R0408 ROOM=SOC 1.00K 01005 MF 5% 1/32W

8 OUT BOOT_CONFIG2 — NOSTUFF R0409 ROOM=SOC 1.00K 01005 MF 5% 1/32W

8 OUT BOOT_CONFIG1 — R0410 ROOM=SOC 1.00K 01005 MF 5% 1/32W

8 OUT BOOT_CONFIG0 — NOSTUFF R0411 ROOM=SOC 1.00K 01005 MF 5% 1/32W

RESISTOR STUFF = HIGH '1'
RESISTOR NOSTUFF = LOW '0'

BOARD_REV[3:0]
FLOAT=LOW, PULLUP=HIGH

	1111	PROTO1
	1110	PROTO2
	1101	EVT
	1100	EVT DOE 3 (MAMBA LDO)
	1011	CARRIER
	1010	CARRIER 2 (I2C0 SCL)
SELECTED -->	1001	DVT

BOARD_ID[4:0]
FLOAT=LOW, PULLUP=HIGH

SELECTED -->	00100	N71 MLB
	00101	N71 DEV
	00110	N66 MLB

BOOT_CONFIG[2:0]
FLOAT=LOW, PULLUP=HIGH

	000	SPI0
	001	SPI0 TEST MODE
SELECTED -->	010	NVME0 x2 MODE
	011	NVME0 x2 TEST MODE
	100	NVME0 x1 MODE
	101	NVME0 x1 TEST MODE
	110	SLOW SPI0 TEST MODE
	111	FAST SPI0 TEST MODE

PAGE TITLE: SYSTEM:N71 SPECIFIC

Apple Inc.

DRAWING NUMBER: 051-1902 — SIZE: D

REVISION: A.0.0

BRANCH:

PAGE: 4 OF 49

SHEET: 3 OF 59

TOP-SIDE

BOTTOM-SIDE

PENINSULA STANDOFFS

BS0506
STDOFF-2.20D0.25H-0.50-1.70
ROOM=ASSEMBLY

BS0507
STDOFF-2.60D0.5H-0.5-1.7-TH
ROOM=ASSEMBLY

860-8396

1 — 50 AP UAT FEED — 33

860-7846 — 50 AP WIFI 5G CONN ANT — 33

NORTH AC GND SCREW — 4

806-02971

BS0508
2.7X1.94X0.25
RING-TH1
ROOM=ASSEMBLY

SHIM WASHER

STOCKHOLM FEED

BS0505
STDOFF-2.56OD1.4ID.99H-SM
ROOM=ASSEMBLY

860-00109

33 AP TO STOCKHOLM ANT

BS0503
STDOFF-2.60D0.81H-TH
ROOM=ASSEMBLY

860-00096

BS0501
STDOFF-2.85OD1.4ID-0.84H
ROOM=ASSEMBLY

860-00111

860-00111

BS0502
STDOFF-2.85OD1.4ID-0.84H
ROOM=ASSEMBLY

PLATED SLOTTED THRU-HOLE
CL0502
TH-NSP
SL-1.20X0.40-1.50X0.70-NSP

SOUTH DC CURRENT BLOCKING CAPS

SOUTH AC GND SCREW — 4 32

C0540	220PF	10%	16V	X7R-CERM 01005
C0541	100PF	5%	16V	NP0-C0G 01005
C0542	56PF	5%	16V	NP0-C0G 01005
C0543	4.7PF	+/-0.1PF	16V	NP0-C0G 01005

ROOM=ASSEMBLY

NORTH DC CURRENT BLOCKING CAPS

NORTH AC GND SCREW — 4

C0550	220PF	10%	16V	X7R-CERM 01005
C0551	100PF	5%	16V	NP0-C0G 01005
C0552	220PF	10%	16V	X7R-CERM 01005
C0553	100PF	5%	16V	NP0-C0G 01005

ROOM=ASSEMBLY

UPPER SHIELD

OMIT_TABLE

SH0500
SM

SHLD-EMI-UPPER-FRONT-N61
ROOM=ASSEMBLY

UPPER SHIELD

OMIT_TABLE

SH0503
SM

SHLD-EMI-UPPER-BACK-N61
ROOM=ASSEMBLY

DUAL RF COAX CLIP

CLIP-RETENTION-COAX-DOUBLE

CL0501
SM

ROOM=ASSEMBLY
806-01802

LOWER SHIELD

OMIT_TABLE

SH0501
SM

SHLD-EMI-LOWER-FRONT-N61
ROOM=ASSEMBLY

LOWER SHIELD

OMIT_TABLE

SH0504
SM

SHLD-EMI-LOWER-BACK-N61
ROOM=ASSEMBLY

SA SHIELD

OMIT_TABLE

SH0502
SM

SHLD-EMI-SA-N71
ROOM=ASSEMBLY

SOUTH TUBE STANDOFF

BS0500
STDOFF-2.70OD1.84ID-0.88H-TH
860-7862
ROOM=ASSEMBLY

TODO:UPDATE REF DES

FIDUCIALS

FD0501	FID	0P5SM1P0SQ-NSP	ROOM=ASSEMBLY
FD0502	FID	0P5SM1P0SQ-NSP	ROOM=ASSEMBLY
FD0503	FID	0P5SM1P0SQ-NSP	ROOM=ASSEMBLY
FD0505	FID	0P5SM1P0SQ-NSP	ROOM=ASSEMBLY
FD0510	FID	0P5SQ-SMP3SQ-NSP	ROOM=ASSEMBLY
FD0511	FID	0P5SQ-SMP3SQ-NSP	ROOM=ASSEMBLY
FD0512	FID	0P5SQ-SMP3SQ-NSP	ROOM=ASSEMBLY
FD0514	FID	0P5SQ-SMP3SQ-NSP	ROOM=ASSEMBLY
FD0515	FID	0P5SQ-SMP3SQ-NSP	ROOM=ASSEMBLY
FD0504	FID	0P5SM1P0SQ-NSP	ROOM=ASSEMBLY
FD0513	FID	0P5SQ-SMP3SQ-NSP	ROOM=ASSEMBLY

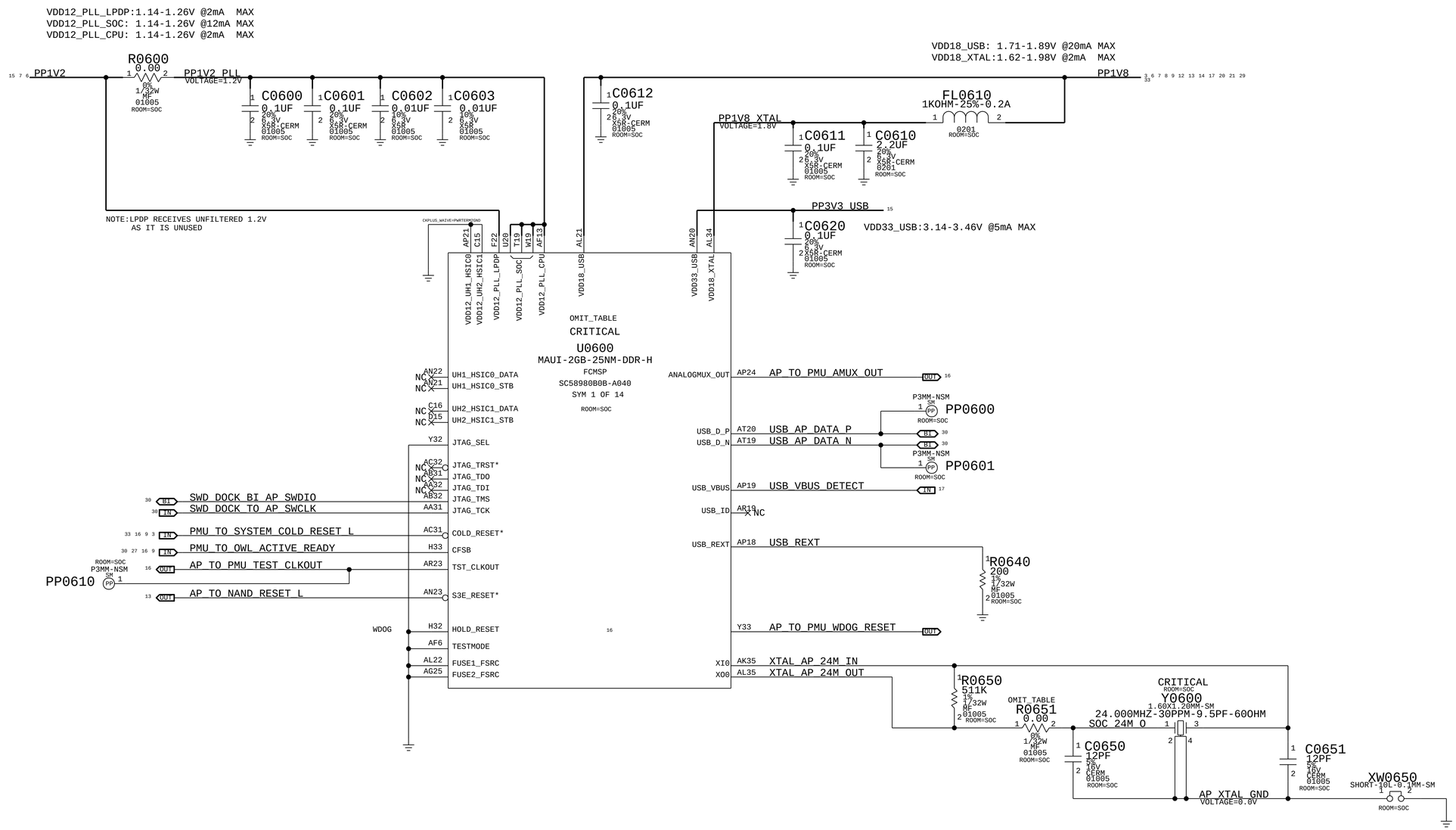
32 4 — SOUTH AC GND SCREW

PAGE TITLE
SYSTEM:MECHANICAL

Apple Inc.

DRAWING NUMBER 051-1902
SIZE D
REVISION A.0.0
BRANCH
PAGE 5 OF 49
SHEET 4 OF 59

MAUI - USB, JTAG, XTAL



SYNC_MASTER=N/A	SYNC_DATE=N/A
PAGE TITLE	SOC:JTAG,USB,XTAL
Apple Inc.	DRAWING NUMBER 051-1902 · SIZE D
	REVISION A.0.0
	BRANCH
	PAGE 6 OF 49
	SHEET 5 OF 59

MAUI - PCIE INTERFACES

VDD12_PCIE_REFBUF:1.08-1.26V @50mA MAX
VDD12_PCIE_TXPLL: 1.08-1.32V @10mA MAX
VDD12_PCIE: 1.14-1.26V @115mA MAX

XW0740 SHORT-10L-0.1MM-SM ROOM=SOC — XW TO ISOLATE C0442,3 FROM C0740,1.

PP1V2 → C0740 2.2UF 20% 6.3V X5R-CERM 0201 ROOM=SOC; C0741 1.0UF 20% 6.3V X5R 0201-1 ROOM=SOC; C0742 0.1UF 20% 6.3V X5R-CERM 01005 ROOM=SOC

PP1V2_XW VOLTAGE=1.2V → C0743 0.1UF 20% 6.3V X5R-CERM 01005 ROOM=SOC; C0731 0.1UF 20% 6.3V X5R-CERM 01005 ROOM=SOC

VDD085_PCIE:0.802-TBDV @TBDmA MAX

PP_FIXED → C0752 0.1UF 20% 6.3V X5R-CERM 01005 ROOM=SOC; C0751 1.0UF 20% 6.3V X5R 0201-1 ROOM=SOC; C0750 2.2UF 20% 6.3V X5R-CERM 0201 ROOM=SOC

VDD12_PCIE: AK28, AK25, AL24, AL27
VDD12_PCIE_TXPLL: AL26
VDD12_PCIE_REFBUF: AJ26
VDD085_PCIE: AH28, AJ25, AL23, AJ29, AL29, AJ24, AK27, AJ27

PCIE EXT C AP29 → PCIE_EXT_C

OMIT_TABLE
CRITICAL
U0600
MAUI-2GB-25NM-DDR-H
FCMSP
SC58980B0B-A040
SYM 2 OF 14
ROOM=SOC

PCIE LINK 0

PCIE NAND TO AP RXD0 P	C0701 0.1UF X5R-CERM 01005	PCIE NAND TO AP RXD0 C P	AM30 PCIE_RX0_P
PCIE NAND TO AP RXD0 N	C0702 0.1UF X5R-CERM 01005	PCIE NAND TO AP RXD0 C N	AN30 PCIE_RX0_N
PCIE AP TO NAND TXD0 P	C0703 0.1UF X5R-CERM 01005	PCIE AP TO NAND TXD0 C P	AT32 PCIE_TX0_P
PCIE AP TO NAND TXD0 N	C0704 0.1UF X5R-CERM 01005	PCIE AP TO NAND TXD0 C N	AR32 PCIE_TX0_N
PCIE NAND TO AP RXD1 P	C0705 0.1UF X5R-CERM 01005	PCIE NAND TO AP RXD1 C P	AM28 PCIE_RX1_P
PCIE NAND TO AP RXD1 N	C0706 0.1UF X5R-CERM 01005	PCIE NAND TO AP RXD1 C N	AN28 PCIE_RX1_N
PCIE AP TO NAND TXD1 P	C0707 0.1UF X5R-CERM 01005	PCIE AP TO NAND TXD1 C P	AT31 PCIE_TX1_P
PCIE AP TO NAND TXD1 N	C0708 0.1UF X5R-CERM 01005	PCIE AP TO NAND TXD1 C N	AR31 PCIE_TX1_N

PCIE LINK 1

PCIE WLAN TO AP RXD P	C0709 0.1UF X5R-CERM 01005	PCIE WLAN TO AP RXD C P	AM27 PCIE_RX2_P
PCIE WLAN TO AP RXD N	C0710 0.1UF X5R-CERM 01005	PCIE WLAN TO AP RXD C N	AN27 PCIE_RX2_N
PCIE AP TO WLAN TXD P	C0711 0.1UF X5R-CERM 01005	PCIE AP TO WLAN TXD C P	AT28 PCIE_TX2_P
PCIE AP TO WLAN TXD N	C0712 0.1UF X5R-CERM 01005	PCIE AP TO WLAN TXD C N	AR28 PCIE_TX2_N

PCIE LINK 2

PCIE BB TO AP RXD P	C0715 0.1UF X5R-CERM 01005	PCIE BB TO AP RXD C P	AM26 PCIE_RX3_P
PCIE BB TO AP RXD N	C0716 0.1UF X5R-CERM 01005	PCIE BB TO AP RXD C N	AN26 PCIE_RX3_N
PCIE AP TO BB TXD P	C0717 0.1UF X5R-CERM 01005	PCIE AP TO BB TXD C P	AT26 PCIE_TX3_P
PCIE AP TO BB TXD N	C0718 0.1UF X5R-CERM 01005	PCIE AP TO BB TXD C N	AR26 PCIE_TX3_N

PCIE_RX_TX_BYPASS_CLK_N

NC AM25 PCIE_RX4_P
NC AN25 PCIE_RX4_N

NC AR24 PCIE_TX4_P
NC AT24 PCIE_TX4_N

PCIE_REF_CLK0_P	AN35	PCIE AP TO NAND REFCLK P (OUT 13)
PCIE_REF_CLK0_N	AP35	PCIE AP TO NAND REFCLK N (OUT 13)
PCIE_REF_CLK1_P	AN34	PCIE AP TO WLAN REFCLK P (OUT 33)
PCIE_REF_CLK1_N	AP34	PCIE AP TO WLAN REFCLK N (OUT 33)
PCIE_REF_CLK2_P	AM32	PCIE AP TO BB REFCLK P (OUT 33)
PCIE_REF_CLK2_N	AN32	PCIE AP TO BB REFCLK N (OUT 33)
PCIE_REF_CLK3_P	AM31	NC
PCIE_REF_CLK3_N	AN31	NC

PP1V8 → R0720 100K 5% 1/32W MF 01005 ROOM=SOC; R0721 100K 5% 1/32W MF 01005 ROOM=SOC; NOSTUFF R0722 100K 5% 1/32W MF 01005 ROOM=SOC

PCIE_CLKREQ0*	AT11	PCIE NAND TO AP CLKREQ L (BI 13)
PCIE_CLKREQ1*	AP12	PCIE WLAN TO AP CLKREQ L (BI 33)
PCIE_CLKREQ2*	AR12	PCIE BB BI AP CLKREQ L (BI 33)
PCIE_CLKREQ3*	AT12	NC

NOTE:CLKREQ_L PULL-UP FOR BB IN RADIO_MLB_MIMO SECTION

PCIE_PERST0*	AR10	PCIE AP TO NAND RESET L (OUT 13)
PCIE_PERST1*	AT10	PCIE AP TO WLAN RESET L (OUT 33)
PCIE_PERST2*	AP11	PCIE AP TO BB RESET L (OUT 33)
PCIE_PERST3*	AR11	NC

R0700 100K 5% 1/32W MF 01005 ROOM=SOC; R0701 100K 5% 1/32W MF 01005 ROOM=SOC; R0702 100K 5% 1/32W MF 01005 ROOM=SOC

PCIE_EXT_REF_CLK_P AR33
PCIE_EXT_REF_CLK_N AT33

PCIE_RX_TX_BYPASS_CLK_P AT29
AR29

PCIE_RCAL_P AT30
PCIE_RCAL_N AR30

PCIE RCAL P → OMIT_TABLE R0730 100 1% 1/32W MF 01005 ROOM=SOC; OMIT_TABLE C0730 100PF 5% 16V NP0-C0G 01005 ROOM=SOC → PCIE RCAL N

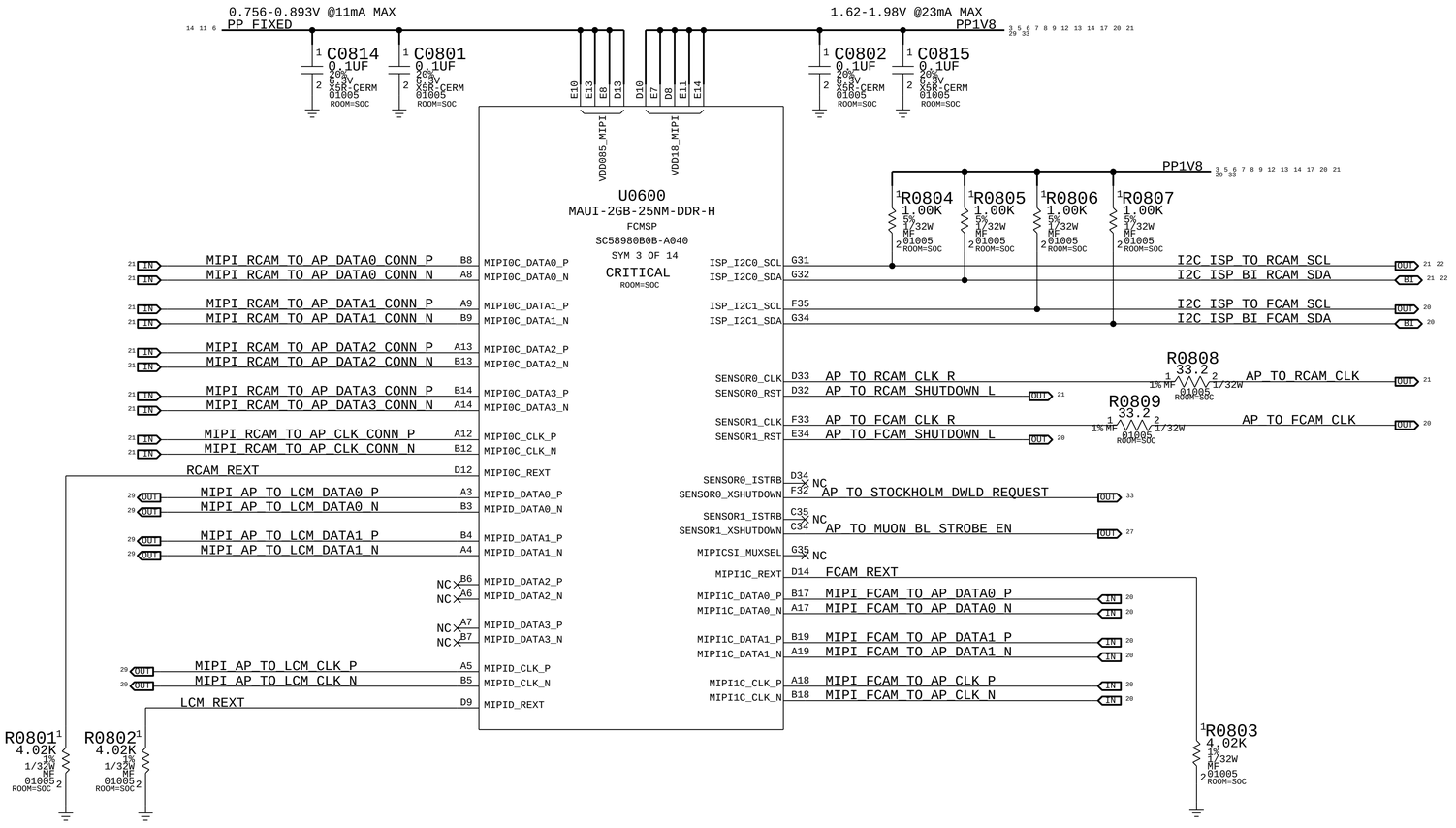
SYNC_MASTER=N/A SYNC_DATE=N/A

PAGE TITLE: SOC:PCIE

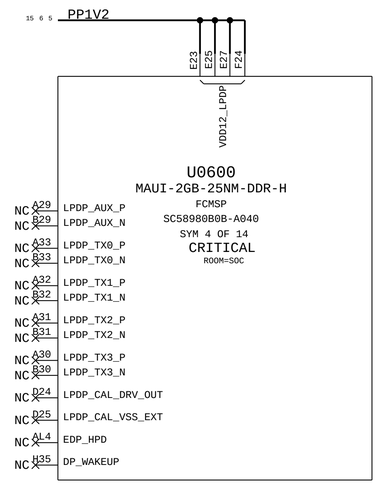
Apple Inc.

DRAWING NUMBER 051-1902 SIZE D
REVISION A.0.0
BRANCH
PAGE 7 OF 49
SHEET 6 OF 59

MAUI - CAMERA & DISPLAY INTERFACES



NOTE:VDD12_LPDP SHOULD BE POWERED
EVEN WHEN LPDP IS NOT USED



SYNC_MASTER=N/A SYNC_DATE=N/A

PAGE TITLE: SOC:CAMERA & DISPLAY

Apple Inc.

DRAWING NUMBER: 051-1902 SIZE: D
REVISION: A.0.0
BRANCH:
PAGE: 8 OF 49
SHEET: 7 OF 59

MAUI - GPIO & SERIAL INTERFACES

U0600
MAUI-2GB-25NM-DDR-H
FCMSP
SC58980B0B-A040
SYM 5 OF 14
CRITICAL
ROOM=SOC
OMIT_TABLE

AP_TO_HP_HS3_CTRL	C1	GPIO_0	
AP_TO_HP_HS4_CTRL	D2	GPIO_1	
BUTTON_VOL_UP_L	D1	GPIO_2	
BUTTON_VOL_DOWN_L	F1	GPIO_3	
SPEAKERAMP_TO_AP_INT_L	E2	GPIO_4	
AP_TO_SPEAKERAMP_STAYIN_ALIVE	F3	GPIO_5	
AP_TO_SPEAKERAMP_RESET_L	F2	GPIO_6	
AP_TO_BT_WAKE	H3	GPIO_7	
AP_TO_BB_RESET_L	G3	GPIO_8	
PCIE_AP_TO_WLAN_DEV_WAKE	J1	GPIO_9	
AP_TO_LED_DRIVER_EN	H4	GPIO_10	
AP_TO_TOUCH_RESET_L	K1	GPIO_11	
AP_TO_LCM_RESET_L	J3	GPIO_12	
PMU_TO_AP_IRQ_L	K2	GPIO_13	
AP_TO_BB_PCIE_DEV_WAKE	J4	GPIO_14	
AP_TO_STOCKHOLM_DEV_WAKE	L2	GPIO_15	
BOARD_ID3	K3	GPIO_16	
NC_AP_TO_STOCKHOLM_SIM_SEL	L3	GPIO_17	
BOOT_CONFIG0	N1	GPIO_18	
AP_TO_ARC_RESET_L	AH2	GPIO_19	
LCM_TO_OWL_BSYNC	AH3	GPIO_20	
ARC_TO_AP_INT_L	AH4	GPIO_21	
BB_TO_AP_GPS_TIME_MARK (AP TO BB)	AJ1	GPIO_22	
AP_TO_ARC_STAYIN_ALIVE	AJ2	GPIO_23	
BB_TO_AP_RESET_DETECT_L	AJ3	GPIO_24	
BOOT_CONFIG1	AJ4	GPIO_25	
FORCE_DFU	AK1	GPIO_26	
DFU_STATUS	AP3	GPIO_27	
BOOT_CONFIG2	AN4	GPIO_28	
BOARD_ID4	AP4	GPIO_29	
CODEC_TO_AP_PMU_INT_L	AP5	GPIO_30	
AP_TO_BB_RADIO_ON_L	AR2	GPIO_31	
AP_TO_NAND_FW_STRAP	AR3	GPIO_32	
TOUCH_TO_AP_INT_L	AR4	GPIO_33	
BOARD_REV3	AP6	GPIO_34	
BOARD_REV2	AT3	GPIO_35	
BOARD_REV1	AT4	GPIO_36	
BOARD_REV0	AR6	GPIO_37	
AP_TO_BB_COREDUMP	AP7	GPIO_38	
BB_IPC_GPIO	AT5	GPIO_39	
BUTTON_RINGER_A	AP8	GPIO_40	
AP_TO_BB_MESA_UP_L	AP9	GPIO_41	
MAMBA_EXT_LDO_EN	AP10	GPIO_42	

TMR32_PWM0	AE1	NC
TMR32_PWM1	AF2	NC
TMR32_PWM2	AF3	NC
UART0_RXD	AE3	UART_AP_DEBUG_RXD
UART0_TXD	AE4	UART_AP_DEBUG_TXD
UART1_CTS*	K31	UART_BT_TO_AP_CTS_L
UART1_RTS*	K32	UART_AP_TO_BT_RTS_L
UART1_RXD	L33	UART_BT_TO_AP_RXD
UART1_TXD	L32	UART_AP_TO_BT_TXD
UART2_CTS*	AT23	NC
UART2_RTS*	AR20	CAM_EXT_LDO_EN
UART2_RXD	AR22	NC
UART2_TXD	AR21	NC
UART3_CTS*	N4	UART_STOCKHOLM_TO_AP_CTS_L
UART3_RTS*	P3	UART_AP_TO_STOCKHOLM_RTS_L
UART3_RXD	R3	UART_STOCKHOLM_TO_AP_RXD
UART3_TXD	R2	UART_AP_TO_STOCKHOLM_TXD
UART4_CTS*	J33	UART_WLAN_TO_AP_CTS_L
UART4_RTS*	J34	UART_AP_TO_WLAN_RTS_L
UART4_RXD	J35	UART_WLAN_TO_AP_RXD
UART4_TXD	K33	UART_AP_TO_WLAN_TXD
UART5_RTXD	T32	SWI_AP_BI_TIGRIS
UART6_RXD	AF1	UART_ACCESSORY_TO_AP_RXD
UART6_TXD	AE2	UART_AP_TO_ACCESSORY_TXD
UART7_RXD	J31	
UART7_TXD	J32	NC

PROX_SELECT

PP1V8
ANALOG_PROX
R0911 1.00K 5% 1/32W MF 01005 ROOM=SOC

PIN J31 (UART7_RXD) SHOULD BE
BRIEFLY SWITCHED TO PD TO CHECK STATE.
STUFF R0911 FOR ANALOG PROX.
NOSTUFF R0911 FOR DOPPLER PROX.

I2S_AP_TO_CODEC_MCLK	R0920 33.2	I2S_AP_TO_CODEC_MCLK_R
I2S_AP_TO_ARC_MCLK	R0921 33.2	I2S_AP_TO_ARC_MCLK_R
I2S_AP_TO_SPEAKERAMP_MCLK	R0922 33.2	I2S_AP_TO_SPEAKERAMP_MCLK_R

	I2S_AP_TO_CODEC_XSP_BCLK	I2S0_MCK
	I2S_AP_OWL_TO_CODEC_XSP_BCLK	I2S0_BCLK
	I2S_AP_OWL_TO_CODEC_XSP_LRCLK	I2S0_LRCK
	I2S_CODEC_TO_AP_OWL_XSP_DIN	I2S0_DIN
	I2S_AP_TO_CODEC_XSP_DOUT	I2S0_DOUT
	I2S_AP_TO_BT_BCLK	I2S1_MCK
	I2S_AP_TO_BT_LRCLK	I2S1_BCLK
	I2S_BT_TO_AP_DIN	I2S1_LRCK
	I2S_AP_TO_BT_DOUT	I2S1_DIN
	I2S_AP_TO_CODEC_ASP_BCLK	I2S1_DOUT
	I2S_AP_TO_CODEC_ASP_LRCLK	I2S2_MCK
	I2S_CODEC_TO_AP_ASP_DIN	I2S2_BCLK
	I2S_AP_TO_CODEC_ASP_DOUT	I2S2_LRCK
ALS_TO_AP_INT_L		I2S2_DIN
	I2S_AP_TO_BB_BCLK	I2S2_DOUT
	I2S_AP_TO_BB_LRCLK	I2S3_MCK
	I2S_BB_TO_AP_DIN	I2S3_BCLK
	I2S_AP_TO_BB_DOUT	I2S3_LRCK
TRISTAR_TO_AP_INT		I2S3_DIN
	I2S_AP_TO_CODEC_MSP_BCLK	I2S3_DOUT
	I2S_AP_TO_CODEC_MSP_LRCLK	I2S4_MCK
	I2S_CODEC_TO_AP_MSP_DIN	I2S4_BCLK
	I2S_AP_TO_CODEC_MSP_DOUT	I2S4_LRCK
		I2S4_DIN
		I2S4_DOUT

U0600
FCMSP
SC58980B0B-A040
SYM 6 OF 14
MAUI-2GB-25NM-DDR-H
CRITICAL
ROOM=SOC

BOARD_ID2	AD4	SPI0_MISO
BOARD_ID1	AC3	SPI0_MOSI
BOARD_ID0	AB2	SPI0_SCLK
	AD3	SPI0_SSIN
SPI_CODEC_TO_AP_MISO	P33	SPI1_MISO
SPI_AP_TO_CODEC_MOSI	V35	SPI1_MOSI
SPI_AP_TO_CODEC_SCLK	N32	SPI1_SCLK
SPI_AP_TO_CODEC_CS_L	M31	SPI1_SSIN
SPI_TOUCH_TO_AP_MISO	E33	SPI2_MISO
SPI_AP_TO_TOUCH_MOSI	E35	SPI2_MOSI
SPI_AP_TO_TOUCH_SCLK_R	F34	SPI2_SCLK
SPI_AP_TO_TOUCH_CS_L	F31	SPI2_SSIN
SPI_MESA_TO_AP_MISO	AA2	SPI3_MISO
SPI_AP_TO_MESA_MOSI	Y2	SPI3_MOSI
SPI_AP_TO_MESA_SCLK_R	AA3	SPI3_SCLK
MESA_TO_AP_INT	AC4	SPI3_SSIN

PP0906 P2MM-NSM SM ROOM=SOC
R0960 0.00 0% 1/32W MF 01005 ROOM=SOC
R0930 0.00 0% 1/32W MF 01005 ROOM=SOC

SPI_AP_TO_TOUCH_SCLK
SPI_AP_TO_MESA_SCLK

PP1V8
R0900 1.00K 1% 1/32W MF 01005 ROOM=SOC
R0901 2.2K 5% 1/32W MF 01005 ROOM=SOC
R0902 2.2K 5% 1/32W MF 01005 ROOM=SOC
R0903 2.2K 5% 1/32W MF 01005 ROOM=SOC
R0904 1.33K 1% 1/32W MF 01005 ROOM=SOC
R0905 1.33K 1% 1/32W MF 01005 ROOM=SOC

I2C0_SCL	E31	I2C0_AP_SCL
I2C0_SDA	D35	I2C0_AP_SDA
I2C1_SCL	AH1	I2C1_AP_SCL
I2C1_SDA	AG4	I2C1_AP_SDA
I2C2_SCL	L31	I2C2_AP_SCL
I2C2_SDA	M32	I2C2_AP_SDA

PP1V8
R0906 2.2K 5% 1/32W MF 01005 ROOM=SOC
R0907 2.2K 5% 1/32W MF 01005 ROOM=SOC

SEP_SPI0_SCLK	W3	NC
SEP_SPI0_MISO	AA4	NC
SEP_SPI0_MOSI	U2	NC
SEP_I2C_SCL	V3	I2C_SEP_TO_EEPROM_SCL
SEP_I2C_SDA	Y4	I2C_SEP_BI_EEPROM_SDA
SEP_GPIO0	Y3	NC
SEP_GPIO1	AR4	NC

PP1V8_ALWAYS
PP1V8
R0941 10K 5% 1/32W MF 01005 ROOM=SOC
NOSTUFF R0910 10K 5% 1/32W MF 01005 ROOM=SOC
R0909 10K 5% 1/32W MF 01005 ROOM=SOC

SOCHOT0	AM1	PMU_TO_AP_SOCHOT0_R_L
		PMU_TO_AP_SOCHOT0_L
SOCHOT1	AM2	AP_TO_PMU_SOCHOT1_L
CPU_ACTIVE_STATUS	H31	NC
CLK32K_OUT	H34	AP_TO_TOUCH_CLK32K_RESET_L
NAND_SYS_CLK	AM24	AP_TO_NAND_SYS_CLK_R

R0940 0.00 0% 1/32W MF 01005 ROOM=SOC
R0945 0.00 0% 1/32W MF 01005 ROOM=SOC

ANTI-ROLLBACK EEPROM

128kbit
APN:335S0946

PP1V8
C0900 1.0UF 20% 6.3V X5R 0201-1 ROOM=SOC
U0900 M34128-FCS6_P/T CRITICAL ROOM=SOC
SCL WLCSP SDA VCC VSS
I2C_SEP_BI_EEPROM_SDA
I2C_SEP_TO_EEPROM_SCL

BUTTON PULL-UP RESISTORS

PP1V8_SDRAM
R0950 191K 1% 1/32W MF 01005 ROOM=SOC
R0951 100K 5% 1/32W MF 01005 ROOM=SOC
PP1V8_ALWAYS
R0952 220K 5% 1/32W MF 01005 ROOM=SOC

BUTTON_MENU_KEY_L
BUTTON_RINGER_A
BUTTON_HOLD_KEY_L

I2C PROBE POINTS

I2C0_AP_SCL	PP0900
I2C0_AP_SDA	PP0901
I2C1_AP_SCL	PP0902
I2C1_AP_SDA	PP0903
I2C2_AP_SCL	PP0904
I2C2_AP_SDA	PP0905

ROOM=SOC P3MM-NSM SM

SYNC_MASTER=N/A SYNC_DATE=N/A
PAGE TITLE: SOC:SERIAL & GPIO

Apple Inc.

DRAWING NUMBER 051-1902 SIZE D
REVISION A.0.0
BRANCH
PAGE 9 OF 49
SHEET 8 OF 59

MAUI - OWL

POWER STATE CONTROL PROBE POINTS

PMU_TO_OWL_ACTIVE_READY — 30 27 16 9 5 — ROOM=SOC, P3MM-NSM, SM, PP — PP1021

PMU_TO_OWL_SLEEP1_READY — 16 11 9 — ROOM=SOC, P3MM-NSM, SM, PP — PP1023

U0600
MAUI-2GB-25NM-DDR-H
FCMSP
SC58980B0B-A040
SYM 7 OF 14
OMIT_TABLE
CRITICAL
ROOM=SOC

OUT	OWL_TO_PMU_SLEEP1_REQUEST	AD30	OWL_DDR_REQ
IN	PMU_TO_OWL_SLEEP1_READY	AB33	OWL_DDR_RESET*
OUT	SPI_OWL_TO_COMPASS_CS_L	AF35	OWL_FUNC_0
IN	COMPASS_TO_OWL_INT	AH32	OWL_FUNC_1
OUT	DISCRETE_ACCEL_TO_OWL_INT2	AG32	OWL_FUNC_2
IN	ACCEL_GYRO_TO_OWL_INT1	AG31	OWL_FUNC_3
OUT	SPI_OWL_TO_ACCEL_GYRO_CS_L	AG30	OWL_FUNC_4
IN	ACCEL_GYRO_TO_OWL_INT2	AF33	OWL_FUNC_5
OUT	SPI_OWL_TO_PHOSPHOROUS_CS_L	AE34	OWL_FUNC_6
IN	LCM_TO_OWL_BSYNC	AF34	OWL_FUNC_7
	OWL_TO_PMU_SHDN_BI_TIGRIS_SWI	AF31	OWL_FUNC_8
IN	PHOSPHORUS_TO_OWL_IRQ	AF32	OWL_FUNC_9
IN	SPI_OWL_TO_DISCRETE_ACCEL_CS_L	AH31	OWL_I2CM_SCL
OUT	DISCRETE_ACCEL_TO_OWL_INT1	AH33	OWL_I2CM_SDA
IN	SPI_IMU_TO_OWL_MISO	AK31	OWL_SPI_MISO
OUT	SPI_OWL_TO_IMU_MOSI	AK32	OWL_SPI_MOSI
OUT	SPI_OWL_TO_IMU_SCLK	AL33	OWL_SPI_SCLK
IN	UART_BB_TO_OWL_RXD	AJ32	OWL_UART0_RXD
OUT	UART_OWL_TO_BB_TXD	AK33	OWL_UART0_TXD
OUT	OWL_TO_WLAN_CONTEXT_B	AH30	OWL_UART1_RXD
OUT	OWL_TO_WLAN_CONTEXT_A	AJ31	OWL_UART1_TXD
IN	TOUCH_TO_OWL_ACCEL_DATA_REQUEST	AJ34	OWL_UART2_RXD
OUT	UART_OWL_TO_TOUCH_TXD	AJ33	OWL_UART2_TXD
OUT	I2S_AP_OWL_TO_CODEC_XSP_BCLK	AD34	OWL_I2S_BCLK
IN	I2S_CODEC_TO_AP_OWL_XSP_DIN	AA34	OWL_I2S_DIN
	NC	AE32	OWL_I2S_MCK
OUT	I2S_AP_OWL_TO_CODEC_XSP_LRCLK	AE31	OWL_I2S_LRCLK

CFSB_AOP	W33	PMU_TO_SYSTEM_COLD_RESET_L	IN 3 5 16 33
AWAKE_REQ	AA33	OWL_TO_PMU_ACTIVE_REQUEST	OUT 16
AWAKE_RESET*	AD32	PMU_TO_OWL_ACTIVE_READY	IN 5 9 16 27 30
PMGR_MISO	AL2	DWI_PMU_TO_PMGR_MISO	IN 16
PMGR_MOSI	AL1	DWI_PMGR_TO_PMU_BACKLIGHT_MOSI	OUT 16 27
PMGR_SCLK0	AK4	DWI_PMGR_TO_PMU_SCLK	OUT 16
PMGR_SSCLK1	AL3	DWI_PMGR_TO_BACKLIGHT_SCLK	OUT 27
RT_CLK32768	AD31	PMU_TO_OWL_CLK32K	IN 16
OWL_SWD_TCK_OUT	AE33	SWD_AP_PERIPHERAL_SWCLK	OUT 13 33
OWL_SWD_TMS0	AD35	NC	
OWL_SWD_TMS1	AC33	SWD_AP_BI_BB_SWDIO	BI 33
SWD_TMS2	U31	SWD_AP_BI_NAND_SWDIO	BI 13
SWD_TMS3	T31	NC	
HOLD_KEY*	U3	BUTTON_HOLD_KEY_L	IN 8 16 32 33
SKEY*	W4	NC	
MENU_KEY*	V4	BUTTON_MENU_KEY_L	IN 8 16 28 33

PP1002 — P2MM-NSM — SM, PP — 1 — OUT 16 27

PP1V8 — 3 5 6 7 8 12 13 14 17 20 21 29 33
NOSTUFF
R1002
1.00K
5% 1/32W MF
01005
ROOM=SOC
1 — 2 — BI 13

OWL SYSTEM SHUTDOWN OPTION

OWL_TO_PMU_SHDN_BI_TIGRIS_SWI — 9

NOSTUFF
R1020
10
1 — 2 1/32W MF 5% 01005
ROOM=SOC
SWI_AP_BI_TIGRIS — BI 8 17

NOSTUFF
R1021
10
1 — 2 1/32W MF 5% 01005
ROOM=SOC
OWL_TO_PMU_SHDN — OUT 16

SYNC_MASTER=N/A — SYNC_DATE=N/A

PAGE TITLE
SOC:OWL

Apple Inc.

DRAWING NUMBER 051-1902 — SIZE D
REVISION A.0.0
BRANCH
PAGE 10 OF 49
SHEET 9 OF 59

MAUI - CPU, GPU & SOC RAILS

PP GPU
0.8V @10.5A MAX

C1100 10UF 20% 6.3V CERM-X5R 0402-9 ROOM=SOC
C1101 10UF 20% 6.3V CERM-X5R 0402-9 ROOM=SOC
C1103 2.2UF 20% 6.3V X5R-CERM 0201 ROOM=SOC
C1104 2.2UF 20% 6.3V X5R-CERM 0201 ROOM=SOC
C1105 2.2UF 20% 6.3V X5R-CERM 0201 ROOM=SOC

XW1110 SHORT-10L-0.1MM-SM ROOM=SOC
BUCK1_PP_GPU_FB OUT 14

TP1120 0.50MM SM
PP 1 PP_GPU 10 14

C1106 4.3UF 20% 4V CERM 0402
C1107 7.5UF 20% 4V CERM 0402
C1108 4.3UF 20% 4V CERM 0402
C1109 7.5UF 20% 4V CERM 0402
C1110 4.3UF 20% 4V CERM 0402
C1111 7.5UF 20% 4V CERM 0402

C1112 1UF 20% 4V CERM 0402
C1113 1UF 20% 4V CERM 0402
C1114 1UF 20% 4V CERM 0402
C1115 1UF 20% 6.3V CERM 0402
C1116 0.47UF 20% 6.3V CERM 0402
C1117 0.47UF 20% 6.3V CERM 0402

PP CPU
0.625V @TBDA MAX
0.9V @10.5A MAX
1.0V @12.5A MAX

C1120 10UF 20% 6.3V CERM-X5R 0402-9 ROOM=SOC
C1121 10UF 20% 6.3V CERM-X5R 0402-9 ROOM=SOC
C1122 2.2UF 20% 6.3V X5R-CERM 0201 ROOM=SOC
C1123 2.2UF 20% 6.3V X5R-CERM 0201 ROOM=SOC
C1124 2.2UF 20% 6.3V X5R-CERM 0201 ROOM=SOC
C1125 2.2UF 20% 6.3V X5R-CERM 0201 ROOM=SOC

TP1100 0.50MM SM
PP 1 PP_CPU 10 14

C1126 7.5UF 20% 4V CERM 0402
C1127 7.5UF 20% 4V CERM 0402
C1128 4.3UF 20% 4V CERM 0402
C1129 7.5UF 20% 4V CERM 0402
C1130 4.3UF 20% 4V CERM 0402
C1131 4.3UF 20% 4V CERM 0402

C1132 4.3UF 20% 4V CERM 0402
C1133 7.5UF 20% 4V CERM 0402
C1134 1UF 20% 4V CERM 0402
C1135 1UF 20% 4V CERM 0402
C1136 1UF 20% 4V CERM 0402
C1137 1UF 20% 4V CERM 0402

C1138 0.47UF 20% 6.3V CERM 0402
C1139 0.47UF 20% 6.3V CERM 0402
C1140 0.47UF 20% 6.3V CERM 0402
C1141 0.47UF 20% 6.3V CERM 0402

XW1100 SHORT-10L-0.1MM-SM ROOM=SOC
14 OUT BUCK0_PP_CPU_FB 2 1

U0600
MAUI-2GB-25NM-DDR-H
FCMSP
SC58980B0B-A040
SYM 8 OF 14
CRITICAL
ROOM=SOC
OMIT_TABLE

VDD_CPU: AA7 AA9 AA11 AB6 AB10 AB12 AC13 AD6 AD8 AD10 AD12 AE7 AE9 AE11 AE13 AF8 AF10 AF12 AH6 AH8 AH10 AH12
VDD_GPU: G15 W13 T12 M6 U9 V12 W9 M12 M18 N15 N21 N9 F10 H14 H16 H20 H22 H6 H8 J11 J13 J17 J19 J23 J7 K10 K14 K16 K20 K22 K6 K8 L11 L13 L15 L17 L19 L21 M24 L7 L9 F8 M8 N11 N13 N17 N19 P10 G11 P14 P16 P20 R15 R19 G13 R9 T10 T14 T16 U11 V14 V16 G7 R23 G9 H10 T24 P22 W17 N23 G17 G21 T18 T20
VSS: AJ5 AJ7 AJ9 AJ11 AJ13 AK6 AK10 AL7 AL9 AL11 AM6 AM8 AM10 AN7 AN11 AL13 Y8 Y10 Y12 AM12 N7 P12

P2MM-NSM SM PP1100 ROOM=SOC
AP_CPU_SENSE_P Y6 VDD_CPU_SENSE
P2MM-NSM SM PP1101 ROOM=SOC
AP_CPU_SENSE_N Y7 VSS_CPU_SENSE
VDD_GPU_SENSE G20
VSS_GPU_SENSE H19
P2MM-NSM SM PP1102 ROOM=SOC
AP_GPU_SENSE_N
16 IN AP_GPU_SENSE_P

NOTE:AP_GPU_SENSE_P PROBE LOCATION @ R2205.2

U0600
MAUI-2GB-25NM-DDR-H
FCMSP
SC58980B0B-A040
SYM 9 OF 14
CRITICAL
ROOM=SOC
OMIT_TABLE

VDD_SOC: AA17 AA19 AA23 AB14 AB16 AB20 AB22 AB24 AB26 AC17 AC19 AC23 AD16 AD20 AD22 AD24 AD26 AE5 AE15 AE17 AE19 AE23 AF14 AF16 AF20 AF22 AF24 AF26 AG17 AG19 AG23 AH16 AH20 AH22 AH24 AH26 AJ15 AJ17 AJ19 AJ23 AK14 J29 G23 AK22 F6 F14 AL15 AM5 G25 G27 H24 H26 H28 J27 K24 K26 K28 L27 L23 M26 M28 AL19 N27 P24 P26 P28 R17 R27 R29 T22 T26 T7 T28 U17 V8 V20 V22 V24 V26 W7 W11 Y28
VSS: W23 Y14 Y16 Y20 Y22 Y24 Y26 G29 AA27 F17 F20 L29 N29 V28 L22 L24 L26 L28 M1 M5 M7 M9 M11 M13 M17 M21 M23 M25 M27 M29 M35 N6 N10 N12 N14 N16 N18 G19 N22 N24 N26 N28 N30 N33 P9 P11 P13 P15 P17 P19 P21 P23 P25 P27 P29 P35 R4 R6 R8 R10 R12 R14 M19 R18 R20 R22 R24 R26 R28 R30 T1 T2 R33 T9 T11 T13 T15 T17 P7 T23 T25 T27 T30 T35 U6 U10 U12

AJ20 VDD_SOC_SENSE
AK21 VSS_SOC_SENSE
P2MM-NSM SM PP1104 ROOM=SOC
AP_SOC_SENSE_N
P2MM-NSM SM PP1105 ROOM=SOC
AP_SOC_SENSE_P

C1150 10UF 20% 6.3V CERM-X5R 0402-9 ROOM=SOC
C1151 10UF 20% 6.3V CERM-X5R 0402-9 ROOM=SOC

PP_SOC 14
0.825V @4.7A MAX
0.725V @TBDA MAX

XW1120 SHORT-10L-0.1MM-SM ROOM=SOC
BUCK2_PP_SOC_FB OUT 14

C1153 4.3UF 20% 4V CERM 0402
C1154 1UF 20% 4V CERM 0402
C1155 1UF 20% 4V CERM 0402
C1156 0.47UF 20% 6.3V CERM 0402
C1157 0.47UF 20% 6.3V CERM 0402

SYNC_MASTER=N/A SYNC_DATE=N/A
PAGE TITLE
SOC:POWER (1/3)

Apple Inc.

DRAWING NUMBER 051-1902
SIZE D
REVISION A.0.0
BRANCH
PAGE 11 OF 49
SHEET 10 OF 59

MAUI - POWER SUPPLIES

1.06 - 1.17V @635mA MAX
INTERNALLY SUPPLIES VDDQ

PP1V1

C1240 10UF 20% 6.3V CERM-X5R 0402-9 ROOM=SOC
C1241 2.2UF 20% 6.3V X5R-CERM 0201 ROOM=SOC
C1242 2.2UF 20% 6.3V X5R-CERM 0201 ROOM=SOC
C1243 2.2UF 20% 6.3V X5R-CERM 0201 ROOM=SOC
C1244 2.2UF 20% 6.3V X5R-CERM 0201 ROOM=SOC
C1248 2.2UF 20% 6.3V X5R-CERM 0201 ROOM=SOC
C1245 4.3UF 20% 4V CERM 0402 ROOM=SOC
C1246 1UF 20% 6.3V CERM 0402 ROOM=SOC
C1247 0.47UF 20% 6.3V CERM 0402 ROOM=SOC

0.802-TBDV @1.1A MAX
PP_FIXED

C1200 10UF 20% 6.3V CERM-X5R 0402-9 ROOM=SOC
C1201 4.3UF 20% 4V CERM 0402 ROOM=SOC
C1202 1UF 20% 6.3V CERM 0402 ROOM=SOC
C1203 0.47UF 20% 6.3V CERM 0402 ROOM=SOC

U0600
MAUI-2GB-25NM-DDR-H
FCMSP
SC58980B0B-A040
SYM 10 OF 14
CRITICAL
ROOM=SOC
OMIT_TABLE

VDD_FIXED: AA15 AA21 AA25 AB18 AC15 AC21 AC25 AD14 AD18 AE21 AE25 AF18 AG15 AG21 AH25 AH14 AH18 AJ21 AK16 F12 G10 V18 AL17 J25 L25 N25 R25 R7 AN6 U25 W15 W21 W25 Y18 F21 F26 AB28 AC27 G18 AK20 F16 R16 T8 V7 U19 W27 U27 AF4 AF27 U21

VDD_CPU_SRAM: AC11 AC7 AC9 AA13 AG11 AG7 AG9 AK12

VDD_GPU_SRAM: H12 H18 R21 U15 J15 J21 J9 K12 K18 M10 M14 M16 M20 P18 R11 R13 U13 V10 M22

W2

0.8V @TBDA MAX
0.9V @TBDA MAX
1.0V @1.0A MAX
PP_CPU_SRAM

C1220 0.47UF 20% 6.3V CERM 0402
C1221 1UF 20% 6.3V CERM 0402
C1222 4.3UF 20% 4V CERM 0402
C1223 2.2UF 20% 6.3V X5R-CERM 0201 ROOM=SOC

0.8V @0.5A MAX
PP_GPU_SRAM

C1224 4.3UF 20% 4V CERM 0402
C1225 1UF 20% 6.3V CERM 0402
C1226 4.3UF 20% 4V CERM 0402
C1227 2.2UF 20% 6.3V X5R-CERM 0201 ROOM=SOC

0.756-TBDV @44mA MAX
PP0V8_OWL

C1250 1.0UF 20% 6.3V X5R 0201-1 ROOM=SOC

VDD_LOW: AH29 AD29 AF29

U0600
MAUI-2GB-25NM-DDR-H
FCMSP
SC58980B0B-A040
SYM 11 OF 14
CRITICAL
ROOM=SOC
OMIT_TABLE

VDDIO11_DDR0: A20 A22 B11 B15 B23 B25 D16 D20 D22 E15 E17 E19 E21
VDDIO11_DDR1: AN19 AR18 AR21 AR8 AT13 AT16 AM14 AM16 AM18 AM20 AR15 AN13 AN15
VDDIO11_DDR2: AB29 V29 Y29 Y35 AB35 AG34 M34 R35 T29 T34 AA30 U30 AC30
VDDIO11_DDR3: AA1 AC2 V6 H2 M2 U5 P6 T6 U1 N5 R5 W5

DDR IMPEDANCE CONTROL

PP1V1

R1200 240 1% 1/32W MF 01005 ROOM=SOC
R1201 240 1% 1/32W MF 01005 ROOM=SOC
R1202 240 1% 1/32W MF 01005 ROOM=SOC
R1203 240 1% 1/32W MF 01005 ROOM=SOC
R1204 240 1% 1/32W MF 01005 ROOM=SOC
R1205 240 1% 1/32W MF 01005 ROOM=SOC

DDR0_RREF: C21 DDR0 RREF
DDR1_RREF: AP17 DDR1 RREF
DDR2_RREF: V31 DDR2 RREF
DDR3_RREF: P5 DDR3 RREF
DDR0_ZQ: B21 DDR0 ZQ
DDR3_ZQ: P2 DDR3 ZQ
DDR0_RET*: C18 PMU_TO_OWL_SLEEP1_READY
DDR1_RET*: AP15
DDR2_RET*: Y31
DDR3_RET*: U4

PMU_TO_OWL_SLEEP1_READY → IN 9 16

1.1V @7mA MAX
PP1V1_DDR_PLL
VOLTAGE=1.1V

FL1280 100OHM-25%-0.12A 01005 ROOM=SOC

VDDIO11_PLL_DDR: AK18 W26 P8

C1280 0.22UF 20% 6.3V X5R 01005-1 ROOM=SOC

VDDIO11_RET_DDR: AN17 W31 T4

PP1V1_SDRAM
1.06 - 1.17V

DDR0_SYS_ALIVE: C19
DDR1_SYS_ALIVE: AP16
DDR2_SYS_ALIVE: W32
DDR3_SYS_ALIVE: T3

SYSTEM_ALIVE → IN 13 16 17

SYNC_MASTER=N/A	SYNC_DATE=N/A
PAGE TITLE	SOC:POWER (2/3)
Apple Inc.	DRAWING NUMBER 051-1902
	SIZE D
	REVISION A.0.0
	BRANCH
	PAGE 12 OF 49
	SHEET 11 OF 59

MAUI - POWER SUPPLIES

U0600
MAUI-2GB-25NM-DDR-H
FCMSP
SC58980B0B-A040
SYM 13 OF 14
CRITICAL
ROOM=SOC

OMIT_TABLE

A1		AF23	
A2		AF25	
A11		AF30	
A16		AG1	
A21		AG2	
A24		AG3	
A25		AG6	
A27		AG8	
A34		AG10	
A35		AG14	
AA6		AG16	
AA8		AG18	
AA10		AG20	
AA12		AG22	
AA14		AG24	
AA16		U7	
AA18		AG29	
AA20		AG33	
AA22		AG35	
AA24		AH5	
AA26		AH7	
N8		AH9	
AA28		AH11	
AA35		AH13	
AB1		AH15	
C17		AH17	
AB3		AH19	
AB5		AH21	
AB7		AH23	
AB9		AH27	
AB11		AJ6	
AB13		AJ8	
AB15		AJ10	
AB17		AJ12	
AB19		AJ14	
AB21		AJ16	
AB23		AJ18	
AB25		W8	
AB27		AJ22	
AB30		AG12	
AC1		AK24	
AC6		AJ28	
AC8		AK2	
AC10		AK3	
AC12		AK5	
AC14	VSS	AK7	VSS
AC16		AK9	
AC18		AK11	
AC20		AK13	
AC22		AK15	
AC24		B28	
AC26		AK17	
T5		M15	
AC28		AP28	
AC34		AK26	
AC35		AK30	
AD5		AK34	
AD7		AK29	
AD9		AL6	
AD11		AL8	
AD15		AL10	
AD17		AL12	
AD19		AF28	
AD21		AL14	
AD23		AM29	
AD25		AL16	
AD27		AR27	
AD33		AL18	
AE6		Y30	
AE8		AL20	
AE10		AL25	
AE12		AL28	
AE14		AL30	
AE16		AL31	
AE18		AM7	
AE20		AM9	
AE22		AM11	
AE24		AM13	
AE26		AM15	
AE29		AM17	
AE30		AM19	
AE35		AM21	
AF5		AM33	
AF7		AM34	
AF9		AM35	
AF11		AN3	
AF15		AN5	
AF17		AN8	
AF19		AN16	
AF21		AN10	

U0600
MAUI-2GB-25NM-DDR-H
FCMSP
SC58980B0B-A040
SYM 14 OF 14
CRITICAL
ROOM=SOC

OMIT_TABLE

AN12		E12	
AN14		E16	
AN18		E18	
AN29		E20	
AN33		E22	
AP2		E24	
AP13		E26	
AP14		E29	
AP20		E32	
AP25		F4	
AP26		F5	
AP27		F7	
AP30		F9	
AP31		F11	
AP32		F13	
AP33		F15	
AR1		F18	
AR5		D18	
AR9		F23	
AR14		E30	
AR16		F25	
AR25		F27	
AR34		F28	
AR35		F29	
AT1		G4	
AT2		G5	
AT6		G6	
AT8		G8	
AT9		G12	
AT14		G14	
AT17		G16	
AT18		E6	
AT21		G22	
AT25		G24	
AT34		G26	
AT35		G28	
B1		G33	
B2		H1	
B16		H7	
B20		H9	
B22		H11	
B24		H13	
B27		H15	
B34		H17	
B35		E28	
C2		H21	
C3	VSS	H23	VSS
C4		H25	
C5		H27	
C6		H29	
C7		J2	
C8		J5	
C9		J6	
C10		J30	
C11		J8	
C12		J10	
C13		J12	
C14		J14	
C20		J16	
C22		J18	
C23		J20	
C24		J22	
C25		J24	
C26		J26	
C27		J28	
C28		K7	
C29		K9	
C30		K11	
C31		K13	
C32		K15	
C33		K17	
D3		K19	
D4		K21	
D5		K23	
D6		K25	
D11		K27	
D17		K29	
D21		K34	
D23		K35	
D26		L1	
D27		L5	
D28		L6	
D29		K4	
D30		L8	
E1		L10	
E3		L12	
E4		L14	
E5		L16	
D7		L18	
E9		L20	

1.70-1.95V @100mA(TBD) MAX
PP1V8_SDRAM
33 31 30 27 24 16 15 14 8

C1300 2.2UF 20% 6.3V X5R-CERM 0201 ROOM=SOC
C1301 2.2UF 20% 6.3V X5R-CERM 0201 ROOM=SOC
C1302 2.2UF 20% 6.3V X5R-CERM 0201 ROOM=SOC

1.06-1.17V @1.3A(TBD) MAX
PP1V1_SDRAM
15 14 11

C1310 10UF 20% 6.3V CERM-X5R 0402-9 ROOM=SOC
C1312 2.2UF 20% 6.3V X5R-CERM 0201 ROOM=SOC
C1313 2.2UF 20% 6.3V X5R-CERM 0201 ROOM=SOC
C1314 2.2UF 20% 6.3V X5R-CERM 0201 ROOM=SOC

C1311 (2.2UF) MOVED TO PP1V1
TO HELP WITH DDR PI (SAME AS N66).

C1316 1UF 20% 4V CERM 0402 ROOM=SOC
C1317 1UF 20% 4V CERM 0402 ROOM=SOC

1.62-1.98V @41mA MAX
PP1V8
21 20 17 14 13 12 9 8 7 6 5 3 33 29

C1320 10UF 20% 6.3V CERM-X5R 0402-9 ROOM=SOC
C1321 2.2UF 20% 6.3V X5R-CERM 0201 ROOM=SOC
C1322 2.2UF 20% 6.3V X5R-CERM 0201 ROOM=SOC
C1323 2.2UF 20% 6.3V X5R-CERM 0201 ROOM=SOC

VDDIO18_GRP10:1.62-1.98V @8mA MAX
VDDIO18_LPOSC:1.62-1.98V @1mA MAX
PP1V8_IMU_OWL
19 14

PP1V8_ALWAYS 1.62-1.98V @1mA MAX
17 15 8

PP1V8
21 20 17 14 13 12 9 8 7 6 5 3 33 29

VDD18_FMON :1.62-1.98V @1mA MAX
VDD18_UVD :1.62-1.98V @5mA MAX
VDD18_AMUX :1.62-1.98V @1mA MAX
VDD18_TSADC:1.645-1.89V @2mA MAX

C1330 2.2UF 20% 6.3V X5R-CERM 0201 ROOM=SOC

U0600
MAUI-2GB-25NM-DDR-H
FCMSP
SC58980B0B-A040
SYM 12 OF 14
CRITICAL
ROOM=SOC

OMIT_TABLE

A10		U14	
A26		U16	
AD1		U18	
AH35		U22	
AT22	VDD1	U24	
AT7		U26	
G1		U28	
L35		U35	
A15		V1	
A23		V5	
AB34		AA29	
AD2		U29	
AH34		V9	
AR13		V11	
AR17		V13	
AR22		V15	
AR7		V17	
AT15	VDD2	V19	
B10		V21	
B26		V23	
G2		V25	
L34		V27	
N2		W30	
R1		W1	
U34		W6	
V2		W10	
W35		W12	
		W14	
		W16	
		W18	
		W20	
		W22	
		W24	VSS
		W28	
		W29	
		W34	
F30		Y1	
H30		Y9	
K30		Y11	
M30	VDDIO18_GRP1	Y13	
N31		Y15	
P30		Y17	
H5		Y19	
K5	VDDIO18_GRP2	Y21	
AN9		Y23	
AA5		Y25	
AC5	VDDIO18_GRP3	Y27	
AG5		Y34	
AL5		AC29	
AM23	VDDIO18_GRP4	AD28	
AE28		AE27	
AG28	VDDIO18_GRP10 (OWL)	AG27	
Y5	VDDIO18_GRP11 (AON)	AJ30	
AG26	VDD18_LPOSC	AJ35	
AM22	VDD18_FMON	AK19	
AD13	VDD18_UVD	AT27	
AN24	VDD18_AMUX	D31	
AG13		G30	
AK8		L30	
AB8		P4	
N20	VDD18_TSADC	U8	
U23		V30	
AK23		A28	
		AL32	
		T21	

SYNC_MASTER=N/A SYNC_DATE=N/A

PAGE TITLE
SOC:POWER (3/3)

Apple Inc.

DRAWING NUMBER 051-1902
SIZE D
REVISION A.0.0
BRANCH
PAGE 13 OF 49
SHEET 12 OF 59

S3E NAND

PP1V8
R1530 24.9 1% 1/32W MF 01005 ROOM=NAND
PP1V8_NAND_AVDD VOLTAGE=1.8V
C1530 2.2UF 20% 6.3V X5R-CERM 0201 ROOM=NAND
C1531 0.1UF 20% 6.3V X5R-CERM 01005 ROOM=NAND
NAND_AGND VOLTAGE=0V
C1534 10UF 20% 6.3V CERM-X5R 0402-9 ROOM=NAND
C1520 15UF 20% 6.3V X5R 0402-1 ROOM=NAND
C1521 15UF 20% 6.3V X5R 0402-1 ROOM=NAND
C1522 10UF 20% 6.3V CERM-X5R 0402-9 ROOM=NAND
C1524 0.1UF 20% 6.3V X5R-CERM 01005 ROOM=NAND
C1525 100PF 5% 16V NP0-C0G 01005 ROOM=NAND
C1523 10UF 20% 6.3V CERM-X5R 0402-9 ROOM=NAND
C1532 1.0UF 20% 6.3V X6S 0201-1 ROOM=NAND
C1526 0.1UF 20% 6.3V X5R-CERM 01005 ROOM=NAND
C1527 1.0UF 20% 6.3V X6S 0201-1 ROOM=NAND
C1528 220PF 10% 16V X7R-CERM 01005 ROOM=NAND
C1529 33PF 5% 16V NP0-C0G-CERM 01005 ROOM=NAND
C1533 8.2PF +/-0.5PF 16V NP0-C0G-CERM 01005 ROOM=NAND
EXTRA CAPS ADDED FOR UF BLOCKING AND DESENSE MITIGATION.

PP0V9_NAND
C1548 10UF 20% 6.3V CERM-X5R 0402-9 ROOM=NAND
C1540 15UF 20% 6.3V X6S 0402-1 ROOM=NAND
C1541 15UF 20% 6.3V X6S 0402-1 ROOM=NAND
C1542 10UF 20% 6.3V CERM-X5R 0402-9 ROOM=NAND
C1543 10UF 20% 6.3V CERM-X5R 0402-9 ROOM=NAND
C1546 1.0UF 20% 6.3V X6S 0201-1 ROOM=NAND
C1547 1.0UF 20% 6.3V X6S 0201-1 ROOM=NAND
C1550 0.1UF 20% 6.3V X5R-CERM 01005 ROOM=NAND
C1551 0.1UF 20% 6.3V X5R-CERM 01005 ROOM=NAND
C1554 1000PF 10% 6.3V X5R-CERM 01005 ROOM=NAND

PP1V8
C1560 0.01UF 10% 6.3V X5R 01005 ROOM=NAND
NOSTUFF R1560 10K 1% 1/32W MF 01005 ROOM=NAND
NAND_VREF
C1561 0.01UF 10% 6.3V X5R 01005 ROOM=NAND
NOSTUFF R1561 10K 1% 1/32W MF 01005 ROOM=NAND
R1501 3.01K 1% 1/20W MF 0201 ROOM=NAND

U1500
VLGA
VER-1
BOMOPTION=OMIT_TABLE
ROOM=NAND
CRITICAL

PCI_AVDD_CLK1	M4		
PCI_AVDD_CLK2	J5		
PCI_AVDD_H	J7		
PCI_VDD1	K4		
PCI_VDD2	K6		
AVDD1	C3		
VREF	E5		
VDD	A3		
VDD	A7		
VDD	F2		
VDD	J1		
VDD	J9		
VDD	R3		
VDD	R7		
VDDIO	A5		
VDDIO	OB0		
VDDIO	OB10		
VDDIO	OF0		
VDDIO	OF10		
VDDIO	R5		
VCC	OA0		
VCC	OA10		
VCC	OD0		
VCC	OD10		
VCC	OG0		
VCC	OG10		
CLK_IN	D2	IN	AP_TO_NAND_SYS_CLK
PINUSE=BI PCIE_REFCLK_P	H8	IN	PCIE_AP_TO_NAND_REFCLK_P
PINUSE=BI PCIE_REFCLK_M	H6	IN	PCIE_AP_TO_NAND_REFCLK_N
PCIE_CLKREQ*	G9	OUT	PCIE_NAND_TO_AP_CLKREQ_L
PCI_RESREF	M6		PCIE_NAND_RESREF
PINUSE=BI PCIE_RX0_P	M8	IN	PCIE_AP_TO_NAND_TXD0_P
PINUSE=BI PCIE_RX0_M	K8	IN	PCIE_AP_TO_NAND_TXD0_N
PINUSE=BI PCIE_RX1_P	N5	IN	PCIE_AP_TO_NAND_TXD1_P
PINUSE=BI PCIE_RX1_M	N3	IN	PCIE_AP_TO_NAND_TXD1_N
PINUSE=BI PCIE_TX0_P	P8	OUT	PCIE_NAND_TO_AP_RXD0_P
PINUSE=BI PCIE_TX0_M	N7	OUT	PCIE_NAND_TO_AP_RXD0_N
PCIE_TX1_P	M2	OUT	PCIE_NAND_TO_AP_RXD1_P
PINUSE=BI PCIE_TX1_M	K2	OUT	PCIE_NAND_TO_AP_RXD1_N
RESET*	F8	IN	AP_TO_NAND_RESET_L
TRST*	D8	NC	
ZQ	D6		NAND_ZQ
VSSA	B2		
VSS	B4		
VSS	B6		
VSS	OE10		
VSS	G7		
VSS	L3		
VSS	L5		
VSS	L7		
VSS	P2		
VSS	P4		
VSS	P6		
VSS	OC0		
VSS	OC10		
VSS	OE0		

R1500 34.8 0.5% 1/32W MF 01005 ROOM=NAND
NAND_AGND

PP3V0_NAND
C1500 15UF 20% 6.3V X5R 0402-1 ROOM=NAND
C1501 15UF 20% 6.3V X5R 0402-1 ROOM=NAND
C1502 15UF 20% 6.3V X5R 0402-1 ROOM=NAND
C1503 15UF 20% 6.3V X5R 0402-1 ROOM=NAND
C1504 1.0UF 20% 6.3V X6S 0201-1 ROOM=NAND
C1506 1.0UF 20% 6.3V X6S 0201-1 ROOM=NAND
C1510 220PF 10% 16V X7R-CERM 01005 ROOM=NAND
C1511 0.1UF 20% 6.3V X5R-CERM 01005 ROOM=NAND
C1512 33PF 5% 16V NP0-C0G-CERM 01005 ROOM=NAND
C1513 8.2PF +/-0.5PF 16V NP0-C0G-CERM 01005 ROOM=NAND
C1516 100PF 5% 16V NP0-C0G 01005 ROOM=NAND
C1514 56PF 2% 50V NP0-C0G 0201 ROOM=NAND
C1515 1UF 20% 6.3V X5R 0201 ROOM=NAND
EXTRA CAPS ADDED FOR UF BLOCKING AND DESENSE MITIGATION.
DEFAULT_CAPACITOR_56.000000pF_2_1
C1517 1.0UF 20% 6.3V X6S 0201-1 ROOM=NAND
C1507 100PF 5% 16V NP0-C0G 01005 ROOM=NAND
C1508 100PF 5% 16V NP0-C0G 01005 ROOM=NAND
C1505 10UF 20% 6.3V CERM-X5R 0402-9 ROOM=NAND

EXT_D0	G3		PMU_TO_NAND_LOW_BATT_BOOT_L
EXT_D1	J3		AP_TO_NAND_FW_STRAP
EXT_D2	H2	NC	
EXT_D3	E2	NC	
EXT_D4	E1	NC	
EXT_D5	F6	NC	
EXT_D6	C1	NC	
EXT_D7	B8		SYSTEM_ALIVE
EXT_NCE	G1		PCIE_AP_TO_NAND_RESET_L
EXT_NRE	F4		SWD_AP_BI_NAND_SWDIO_R
EXT_NWE	C5		SWD_AP_NAND_SWCLK_R
EXT_RNB	G5	NC	
EXT_CLE	H4	NC	
EXT_ALE	D4		

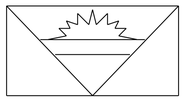
PP1520 R1520 0.00 0% MF 1/32W 01005 ROOM=NAND SWD_AP_BI_NAND_SWDIO
PP1521 R1521 0.00 0% MF 1/32W 01005 ROOM=NAND SWD_AP_PERIPHERAL_SWCLK
P3MM-NSM ROOM=NAND

PCIE RECEIVE-SIDE PROBE POINTS

PCIE_AP_TO_NAND_REFCLK_P → PP1500
PCIE_AP_TO_NAND_REFCLK_N → PP1501
PCIE_AP_TO_NAND_TXD0_P → PP1502
PCIE_AP_TO_NAND_TXD0_N → PP1503
PCIE_AP_TO_NAND_TXD1_P → PP1504
PCIE_AP_TO_NAND_TXD1_N → PP1505
P3MM-NSM ROOM=NAND

SYNC_MASTER=N/A SYNC_DATE=N/A
PAGE TITLE: NAND
Apple Inc.
DRAWING NUMBER 051-1902 SIZE D
REVISION A.0.0
BRANCH
PAGE 15 OF 49
SHEET 13 OF 59

ANTIGUA PMU - Buck Supplies



PP_VCC_MAIN
VCC_MAIN_SNS
U2000 D2255A080UXUVAI2 CSP SYM 2 OF 5 ROOM=PMU
CRITICAL OMIT_TABLE
VDD_MAIN_SNS V3
VDD_MAIN R6 F10 L13 L5 R8 L4
BAT/USB
VDD_BUCK0_01 A4 B4 C4
VDD_BUCK0_23 A8 B8 C8
VDD_BUCK1_01 A16 B16 C16
VDD_BUCK1_23 A12 B12 C12
VDD_BUCK2 J17 J18 J19
VDD_BUCK3 T18 T19
VDD_BUCK4 V12 Y12 Z12
VDD_BUCK5 N17 N18 N19
VDD_BUCK6 J1 J2
VDD_BUCK7 E1 E2
VDD_BUCK8 E17 E18 E19
BUCK INPUT
C2085 10UF 20% 6.3V CERM-X5R 0402-9 ROOM=PMU
C2086 10UF 20% 6.3V CERM-X5R 0402-9 ROOM=PMU
C2087 10UF 20% 6.3V CERM-X5R 0402-9 ROOM=PMU
C2088 10UF 20% 6.3V CERM-X5R 0402-9 ROOM=PMU
C2089 2.2UF 20% 6.3V X5R-CERM 0201 ROOM=PMU
C2090 2.2UF 20% 6.3V X5R-CERM 0201 ROOM=PMU
C2091 2.2UF 20% 6.3V X5R-CERM 0201 ROOM=PMU
C2092 2.2UF 20% 6.3V X5R-CERM 0201 ROOM=PMU
C2093 2.2UF 20% 6.3V X5R-CERM 0201 ROOM=PMU
C2094 2.2UF 20% 6.3V X5R-CERM 0201 ROOM=PMU
C2095 2.2UF 20% 6.3V X5R-CERM 0201 ROOM=PMU
C2096 2.2UF 20% 6.3V X5R-CERM 0201 ROOM=PMU
C2097 2.2UF 20% 6.3V X5R-CERM 0201 ROOM=PMU
C2098 2.2UF 20% 6.3V X5R-CERM 0201 ROOM=PMU
C2099 100PF 5% 16V NP0-C0G 01005 ROOM=PMU
PP1V8
PP1V8_TOUCH VOLTAGE=1.8V
PP1V8_TMU_OWL VOLTAGE=1.8V
PP1V1 VOLTAGE=1.1V
BUCK3_SW1 U18 V18 Y18 Z18
BUCK3_SW2 U16
BUCK3_SW3 U15
BUCK4_SW1 V16 Y16 Z16
L2050 1.0UH-20%-3.6A-0.060OHM PIQA20161T-SM CRITICAL OMIT_TABLE ROOM=PMU
BUCK5_LX0 M17 M18 M19
XW2050 SHORT-10L-0.1MM-SM ROOM=PMU
BUCK5_FB M13
BUCK5 1.1A MAX
PP_FIXED VOLTAGE=0.85V
C2050 15UF 20% 6.3V X5R 0402-1 ROOM=PMU
C2051 15UF 20% 6.3V X5R 0402-1 ROOM=PMU
L2060 1UH-20%-1.2A-0.320OHM 0603 ROOM=PMU
BUCK6_LX0 H1 H2
BUCK6_FB J5
BUCK6 400mA MAX
PP1V2_CAMERA VOLTAGE=1.2V
C2060 15UF 20% 6.3V X5R 0402-1 ROOM=PMU
C2061 15UF 20% 6.3V X5R 0402-1 ROOM=PMU
C2062 100PF 5% 16V NP0-C0G 01005 ROOM=PMU
L2070 1.0UH-20%-2.25A-0.150HM PIXB2016FE-SM ROOM=PMU
BUCK7_LX0 F1 F2
XW2070 SHORT-10L-0.1MM-SM ROOM=PMU
BUCK7_FB C1
BUCK7 1.1A MAX
PP_CPU_SRAM VOLTAGE=1.0V 0.80V/0.90V/1.0V
C2070 15UF 20% 6.3V X5R 0402-1 ROOM=PMU
C2071 15UF 20% 6.3V X5R 0402-1 ROOM=PMU
L2080 1.0UH-20%-2.25A-0.150HM PIXB2016FE-SM ROOM=PMU CRITICAL
BUCK8_LX0 F17 F18 F19
XW2080 SHORT-10L-0.1MM-SM ROOM=PMU
BUCK8_FB C19
BUCK8 1.1A MAX
PP_GPU_SRAM VOLTAGE=1.0V 0.80V/0.90V/1.0V
C2080 15UF 20% 6.3V X5R 0402-1 ROOM=PMU
C2081 15UF 20% 6.3V X5R 0402-1 ROOM=PMU

L2000 1.0UH-20%-3.6A-0.060OHM PIQA20161T-SM CRITICAL OMIT_TABLE ROOM=PMU
BUCK0_LX0 A3 B3 C3
L2001 0.47UH-20%-3.8A-0.048OHM PIQA20121T-SM CRITICAL OMIT_TABLE ROOM=PMU
BUCK0_LX1 A5 B5 C5
L2002 1.0UH-20%-3.6A-0.060OHM PIQA20161T-SM CRITICAL OMIT_TABLE ROOM=PMU
BUCK0_LX2 A7 B7 C7
L2003 0.47UH-20%-3.8A-0.048OHM PIQA20121T-SM CRITICAL OMIT_TABLE ROOM=PMU
BUCK0_LX3 A9 B9 C9
BUCK0_FB F8 BUCK0_PP_CPU_FB
C2000 15UF 20% 6.3V X5R 0402-1 ROOM=PMU
C2001 15UF 20% 6.3V X5R 0402-1 ROOM=PMU
C2002 15UF 20% 6.3V X5R 0402-1 ROOM=PMU
C2003 15UF 20% 6.3V X5R 0402-1 ROOM=PMU
C2004 15UF 20% 6.3V X5R 0402-1 ROOM=PMU
C2005 15UF 20% 6.3V X5R 0402-1 ROOM=PMU
C2006 15UF 20% 6.3V X5R 0402-1 ROOM=PMU
C2007 15UF 20% 6.3V X5R 0402-1 ROOM=PMU
C2008 15UF 20% 6.3V X5R 0402-1 ROOM=PMU
C2009 15UF 20% 6.3V X5R 0402-1 ROOM=PMU
C2010 15UF 20% 6.3V X5R 0402-1 ROOM=PMU
PP_CPU VOLTAGE=1.03V 0.625V/0.9V/1.03V
BUCK0 12.5A MAX

L2010 1.0UH-20%-3.6A-0.060OHM PIQA20161T-SM CRITICAL OMIT_TABLE ROOM=PMU
BUCK1_LX0 A17 B17 C17
L2011 0.47UH-20%-3.8A-0.048OHM PIQA20121T-SM CRITICAL OMIT_TABLE ROOM=PMU
BUCK1_LX1 A15 B15 C15
L2012 1.0UH-20%-3.6A-0.060OHM PIQA20161T-SM CRITICAL OMIT_TABLE ROOM=PMU
BUCK1_LX2 A13 B13 C13
L2013 0.47UH-20%-3.8A-0.048OHM PIQA20121T-SM CRITICAL OMIT_TABLE ROOM=PMU
BUCK1_LX3 A11 B11 C11
BUCK1_FB F12 BUCK1_PP_GPU_FB
C2012 15UF 20% 6.3V X5R 0402-1 ROOM=PMU
C2013 15UF 20% 6.3V X5R 0402-1 ROOM=PMU
C2014 15UF 20% 6.3V X5R 0402-1 ROOM=PMU
C2015 15UF 20% 6.3V X5R 0402-1 ROOM=PMU
C2016 15UF 20% 6.3V X5R 0402-1 ROOM=PMU
C2017 15UF 20% 6.3V X5R 0402-1 ROOM=PMU
C2018 15UF 20% 6.3V X5R 0402-1 ROOM=PMU
C2019 15UF 20% 6.3V X5R 0402-1 ROOM=PMU
C2020 15UF 20% 6.3V X5R 0402-1 ROOM=PMU
C2021 15UF 20% 6.3V X5R 0402-1 ROOM=PMU
C2011 15UF 20% 6.3V X5R 0402-1 ROOM=PMU
PP_GPU VOLTAGE=0.9V 0.70V/0.80V/0.9V
BUCK1 10.5A MAX

L2020 1.0UH-20%-3.6A-0.060OHM PIQA20161T-SM CRITICAL OMIT_TABLE ROOM=PMU
BUCK2_LX0 H17 H18 H19
L2021 0.47UH-20%-3.8A-0.048OHM PIQA20121T-SM CRITICAL OMIT_TABLE ROOM=PMU
BUCK2_LX1 K17 K18 K19
BUCK2_FB J14 BUCK2_PP_SOC_FB
C2022 15UF 20% 6.3V X5R 0402-1 ROOM=PMU
C2023 15UF 20% 6.3V X5R 0402-1 ROOM=PMU
C2024 15UF 20% 6.3V X5R 0402-1 ROOM=PMU
C2025 15UF 20% 6.3V X5R 0402-1 ROOM=PMU
C2026 15UF 20% 6.3V X5R 0402-1 ROOM=PMU
PP_SOC VOLTAGE=0.825V 0.725V/0.825V
BUCK2 4.7A MAX

L2030 1.0UH-20%-3.6A-0.060OHM PIQA20161T-SM CRITICAL OMIT_TABLE ROOM=PMU
BUCK3_LX0 R18 R19
XW2030 SHORT-10L-0.1MM-SM ROOM=PMU
BUCK3_FB V19
VBUCK3_SW U17 V17 Y17 Z17
C2030 15UF 20% 6.3V X5R 0402-1 ROOM=PMU
C2031 15UF 20% 6.3V X5R 0402-1 ROOM=PMU
C2032 100PF 5% 16V NP0-C0G 01005 ROOM=PMU
PP1V8_SDRAM VOLTAGE=1.8V
BUCK3 1.5A MAX

L2040 1.0UH-20%-3.6A-0.060OHM PIQA20161T-SM CRITICAL OMIT_TABLE ROOM=PMU
BUCK4_LX0 V11 Y11 Z11
L2041 0.47UH-20%-3.8A-0.048OHM PIQA20121T-SM CRITICAL OMIT_TABLE ROOM=PMU
BUCK4_LX1 V13 Y13 Z13
XW2040 SHORT-10L-0.1MM-SM ROOM=PMU
BUCK4_FB T9
VBUCK4_SW V15 Y15 Z15
C2040 15UF 20% 6.3V X5R 0402-1 ROOM=PMU
C2041 15UF 20% 6.3V X5R 0402-1 ROOM=PMU
C2042 15UF 20% 6.3V X5R 0402-1 ROOM=PMU
C2043 15UF 20% 6.3V X5R 0402-1 ROOM=PMU
C2044 100PF 5% 16V NP0-C0G 01005 ROOM=PMU
PP1V1_SDRAM VOLTAGE=1.1V
BUCK4 4.7A MAX

SYNC_MASTER=N/A SYNC_DATE=N/A
PAGE TITLE: SYSTEM POWER:PMU (1/3)
Apple Inc.
DRAWING NUMBER 051-1902 SIZE D
REVISION A.0.0
BRANCH
PAGE 20 OF 49
SHEET 14 OF 59

ANTIGUA PMU - LDOs

ANTIGUA LDO SPECS

LDO#	ADJ.RANGE	ACCURACY	MAX.CURRENT
LDO1 (A)	2.5-3.3V	+/-1.4%	50mA
LDO2 (B)	1.2-2.0V	+/-2.5%	50mA
LDO3 (A)	2.5-3.3V	+/-1.4%	50mA
LDO4 (D)	0.7-1.2V	+/-2.5%	100mA
LDO5 (F)	2.5-3.3V	+/-2.5%	1000mA
LDO6 (C1)	1.2-3.6V	+/-2.5%	150mA
LDO7 (C)	2.5-3.3V	+/-25mV	250mA
LDO8 (C)	2.5-3.3V	+/-25mV	250mA
LDO9 (C)	2.5-3.3V	+/-25mV	250mA
LDO10 (G)	0.7-1.2V	+/-5.5%	1335mA
LDO11 (C)	2.5-3.3V	+/-25mV	250mA
LDO12 (E)	1.8V	+/-5%	10mA
LDO13 (C)	2.5-3.3V	+/-25mV	250mA
LDO14 (H)	0.8-1.5V	+/-2.5%	250mA
LDO15 (B)	1.2-2.0V	+/-2.5%	50mA

PP VCC MAIN — C2120 10UF, C2121 10UF, C2122 10UF — 20% 6.3V CERM-X5R 0402-9 ROOM=PMU

XW2105 SHORT-10L-0.1MM-SM

VCC MAIN SNS — OUT 14 — ROOM=PMU — PLACE_NEAR=U2000.U1:2mm

C2123 10UF, C2124 10UF, C2125 10UF — 20% 6.3V CERM-X5R 0402-9 ROOM=PMU

C2126 10UF, C2127 10UF — 20% 6.3V CERM-X5R 0402-9 ROOM=PMU

PP1V1 SDRAM — C2130 2.2UF, C2131 2.2UF — 20% 6.3V X5R-CERM 0201 ROOM=PMU

PP1V8 SDRAM — C2132 2.2UF — 20% 6.3V X5R-CERM 0201 ROOM=PMU

U2000
D2255A080UXUVAI2
CSP
SYM 1 OF 5
ROOM=PMU
CRITICAL
OMIT_TABLE

M3	VDD_LDO1_3
V2	VDD_LDO2
M2	VDD_LDO4
U1	
U2	VDD_LDO5
L2	VDD_LDO6
Y6	VDD_LDO7
Y4	VDD_LDO8
Y3	VDD_LDO9
Y9	
Z9	VDD_LDO10
R3	VDD_LDO11
Y5	VDD_LDO13
Y7	VDD_LDO14
N2	VDD_LDO15
K3	VDD_BYPASS
P12	VPP_OTP

LDO INPUT / LDO

VLDO1	M1	
VLDO2	V1	
VLDO3	L1	
VLDO4	N1	
	T1	
VLDO5	T2	
VLDO6	K1	
VBYPASS	K2	
VLDO7	Z6	
VLDO8	Z4	
VLDO9	Z3	
VLDO9_FB	Y2	CAM_AVDD_FB — PLACE_NEAR=U2000.Y2:2mm — 1 2 XW2100 ROOM=PMU SHORT-10L-0.1MM-SM
	Y8	
VLDO10	Z8	
VLDO11	R2	
VLDO12	K6	
VLDO13	Z5	
VLDO14	Z7	
VLDO15	P2	
VPUMP	U19	PMU_VPUMP

VPUMP:10nF min. @ 4.6V

C2100 47NF 20% 6.3V X5R-CERM 01005 ROOM=PMU

C2101 2.2UF, C2102 2.2UF, C2103 2.2UF, C2104 2.2UF, C2105 2.2UF, C2106 2.2UF, C2107 4.3UF, NOSTUFF C2108 2.2UF, C2109 2.2UF, C2110 2.2UF, C2111 4.3UF, C2112 2.2UF, C2113 2.2UF, C2114 2.2UF, C2115 4.3UF — 20% 6.3V X5R-CERM 0201 ROOM=PMU (4.3UF: 4V X5R-CERM 0610 ROOM=PMU)

VOLTAGE=3.3V	PP3V3_USB	5	LDO1
VOLTAGE=1.8V	PP1V8_VA	24 25 26	LDO2
	PP3V0_TRISTAR	19 27 30 31 33	LDO3
VOLTAGE=0.8V	PP0V8_OWL	11	LDO4
VOLTAGE=3.0V	PP3V0_NAND	13	LDO5
VOLTAGE=3.3V	PP3V3_ACC	30	LDO6
VOLTAGE=3.0V	PP3V0_PROX_ALS	20	LDO7
VOLTAGE=2.775V	PMU_LDO8		LDO8
VOLTAGE=2.85V	PP2V85_CAM_AVDD_PMU	20	LDO9
VOLTAGE=0.9V	PP0V9_NAND	13	LDO10
VOLTAGE=3.0V	PP3V0_PROX_IRLED	20	LDO11
VOLTAGE=1.8V	PP1V8_ALWAYS	8 12 17	LDO12
VOLTAGE=3.0V	PP3V0_MESA	28	LDO13
VOLTAGE=1.2V	PP1V2	5 6 7	LDO14
VOLTAGE=1.8V	PP1V8_MESA	28	LDO15

U2000
D2255A080UXUVAI2
CSP
SYM 5 OF 5
ROOM=PMU
CRITICAL
OMIT_TABLE

D10		J15	
D11		J16	
D12		J3	
D13		J4	
D14		K15	
D15		K16	
D16		L15	
D17		L16	
D18		M14	
D2		M15	
D5		M16	
D6		N14	
D7		N15	
D8		N16	
D9		P13	
D3		P14	
E10		P15	
E11		P16	
E12		P17	
E13		R13	
D4	NC	R14	NC
E15		R15	
E16		R16	
E3		R17	
E4		T10	
E5		T11	
E7		T12	
E8		T13	
E9		T14	
F14		T15	
F15		T17	
F16		U10	
F3		U11	
F4		U12	
G14		U13	
G15		U14	
G16		U4	
G3		U5	
G4		U6	
H15		V4	
H16		V5	
H3		V6	
H4			

U2000
D2255A080UXUVAI2
CSP
SYM 4 OF 5
ROOM=PMU
CRITICAL
OMIT_TABLE

A1		L9	
A10		M8	
A14		M9	
A18		N10	
A19		N12	
A2		N13	
A6		N9	
B1		P10	
B10		P11	
B14		P18	
B18		P19	
B19		P5	
B2		R10	
B6		R11	
C10		R12	
C14		R9	
C18		T16	
C2	VSS	T3	PMU_VSS_RTC — 16
C6		T6	NOTE: T3 IS XTAL REF GND
D1		T8	
D19		U3	
E14		U9	
G1		V10	
G17		V14	
G18		V8	
G19		V9	
G2		Y1	
H7		Y10	
J6		Y14	
K12		Y19	
K7		Z1	
L17		Z10	
L18		Z14	
L19		Z19	
L6		Z2	
L7			

SYNC_MASTER=N/A — SYNC_DATE=N/A

PAGE TITLE: SYSTEM POWER:PMU (2/3)

Apple Inc.

DRAWING NUMBER: 051-1902 — SIZE: D

REVISION: A.0.0

BRANCH:

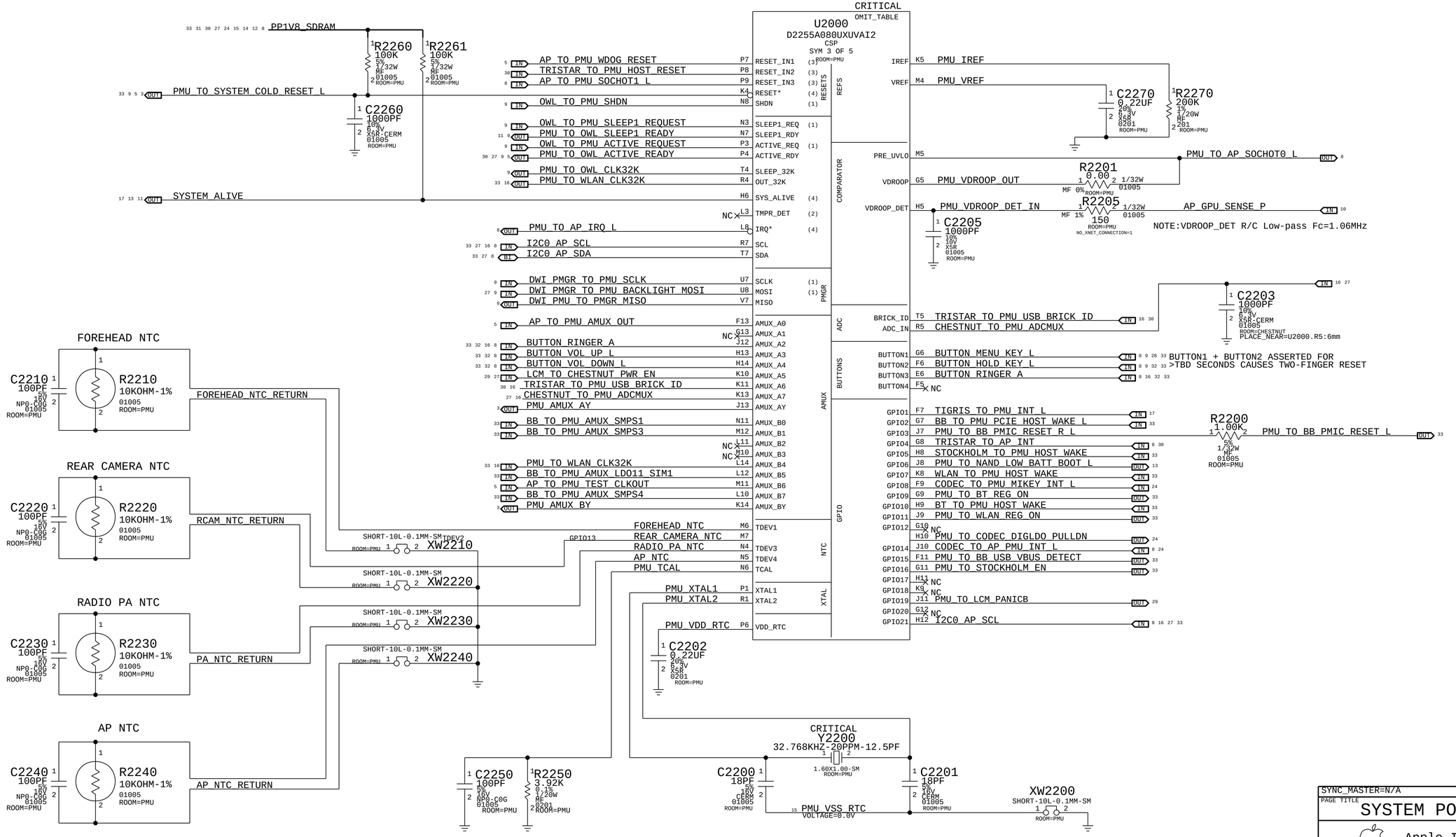
PAGE: 21 OF 49

SHEET: 15 OF 59

ANTIGUA PMU - GPIOs, NTCs

CONTROL PIN NOTES:

NOTE (1):INPUT PULL-DOWN 100-300k
NOTE (2):INPUT PULL-DOWN 1M
NOTE (3):INPUT PULL-UP OR DOWN 100k-300k
NOTE (4):OUTPUT OPEN-DRAIN, REQUIRES PULL-UP



NOTE:100PF CAPS ARE THE SAMPLING CAPS FOR PMU ADC

SYNC_MASTER=N/A SYNC_DATE=N/A

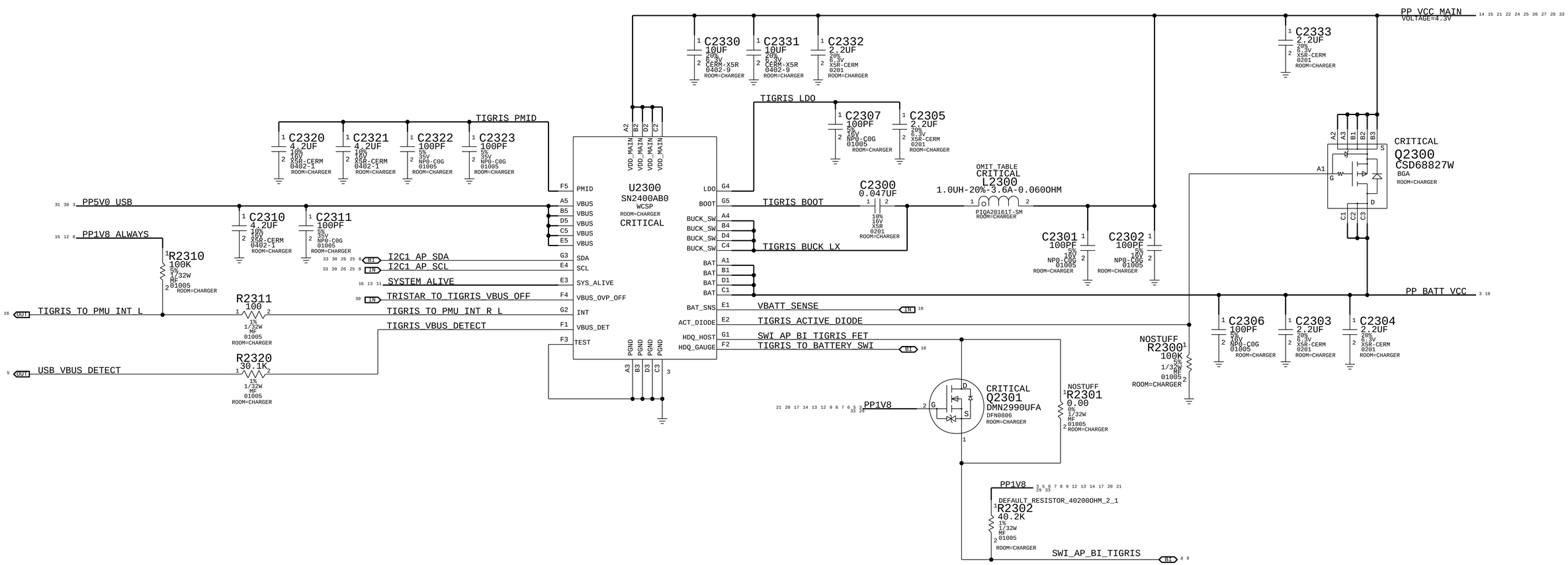
PAGE TITLE
SYSTEM POWER:PMU (3/3)

Apple Inc.

DRAWING NUMBER 051-1902 SIZE D
REVISION A.0.0
BRANCH
PAGE 22 OF 49
SHEET 16 OF 59

TIGRIS CHARGER

APN:343S00033



SYNC_MASTER=N/A SYNC_DATE=N/A

PAGE TITLE

SYSTEM POWER:CHARGER

Apple Inc.

DRAWING NUMBER 051-1902 SIZE D

REVISION A.0.0

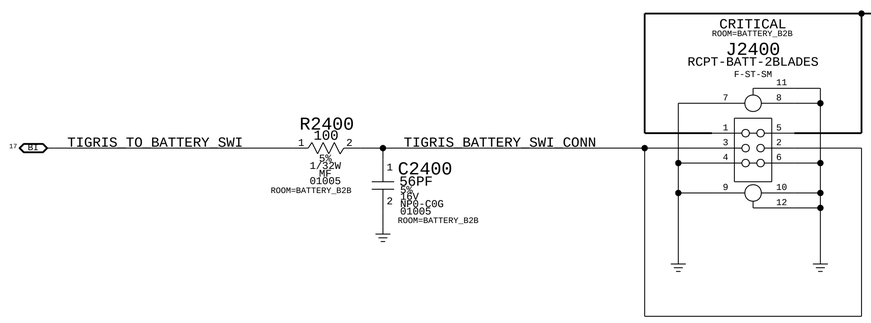
BRANCH

PAGE 23 OF 49

SHEET 17 OF 59

BATTERY CONNECTOR

THIS ONE ON MLB ---> 516S00104 (RCPT)
516S00105 (PLUG)



SYNC_MASTER=N/A SYNC_DATE=N/A

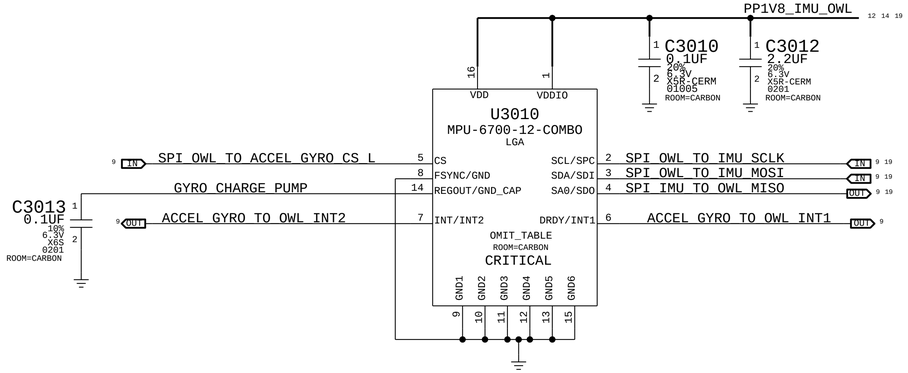
PAGE TITLE
SYSTEM POWER:BATTERY CONN

Apple Inc.

DRAWING NUMBER 051-1902 SIZE D
REVISION A.0.0
BRANCH
PAGE 24 OF 49
SHEET 18 OF 59

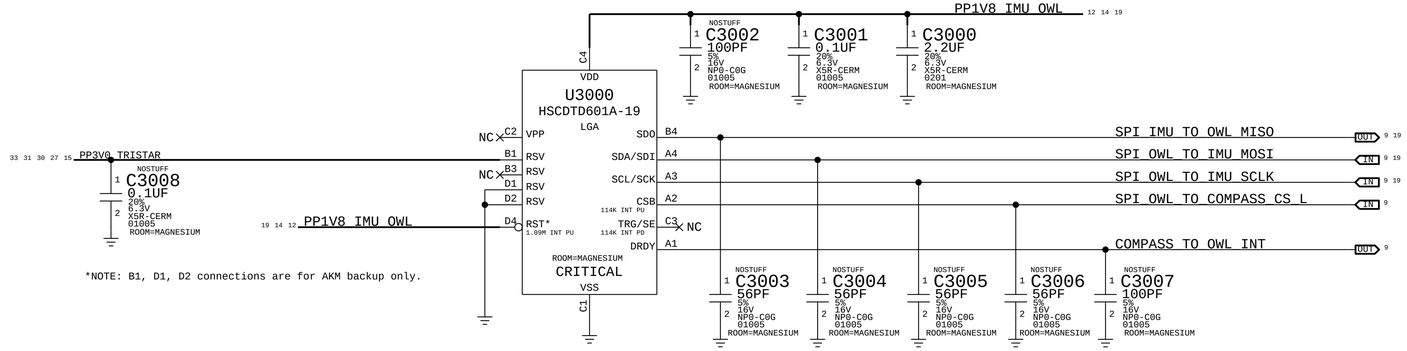
CARBON - ACCEL & GYRO

INVENSENSE (APN: 338S00017, 338S00087)



MAGNESIUM - COMPASS

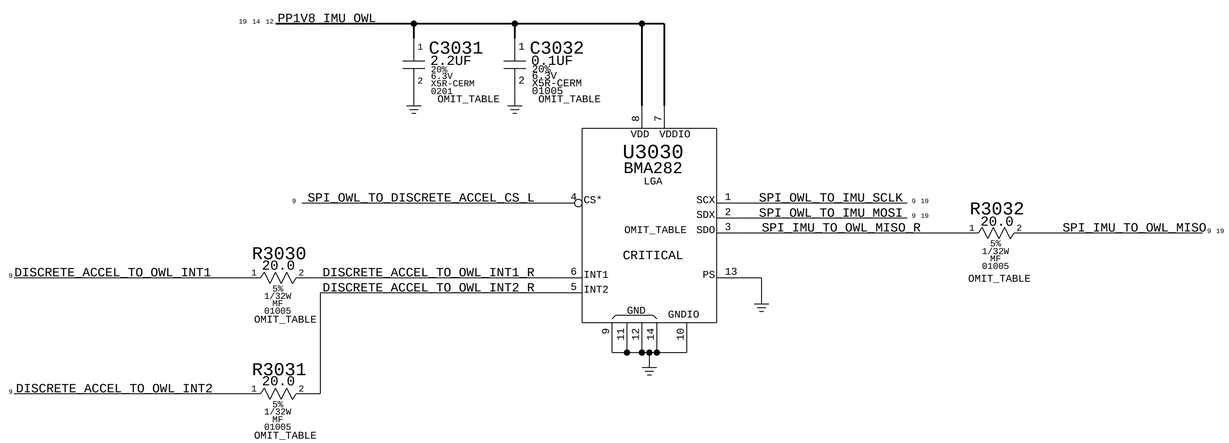
ALPS (APN:338S00084)



*NOTE: B1, D1, D2 connections are for AKM backup only.

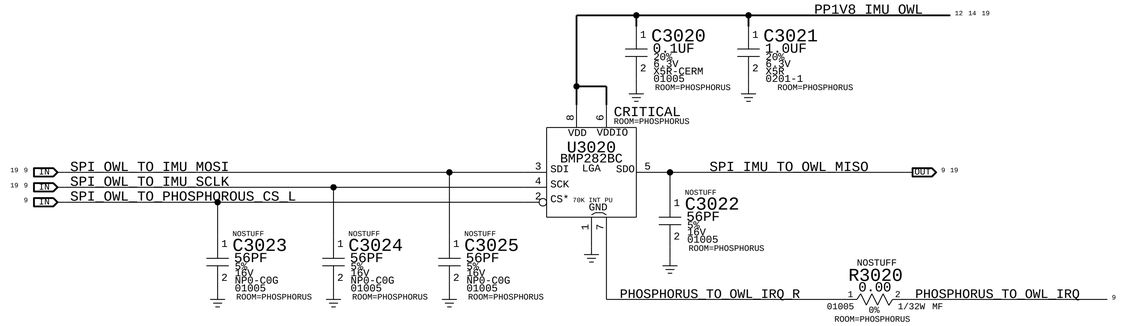
DISCRETE ACCEL

BOSCH (APN: 338S1163)



PHOSPHOROUS

BOSCH (APN:338S00044)



R3020 SHOULD BE STUFFED FOR ST PHOSPHORUS ONLY.
FOR BOSCH PHOSPHORUS, PINS 1 AND 7 ARE SHORTED INTERNALLY,
SO NO NEED FOR 0-OHM TO GROUND OPTION ON PIN 7.

SYNC_MASTER=N/A SYNC_DATE=N/A

PAGE TITLE: SENSORS:MOTION SENSORS

Apple Inc.

DRAWING NUMBER: 051-1902 SIZE: D

REVISION: A.0.0

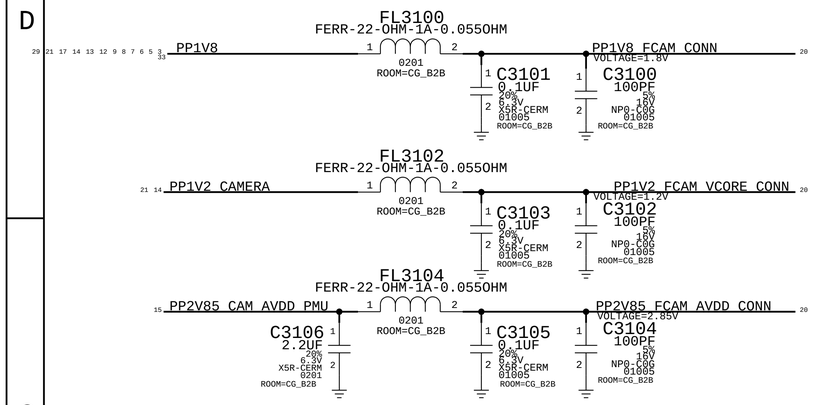
BRANCH:

PAGE: 30 OF 49

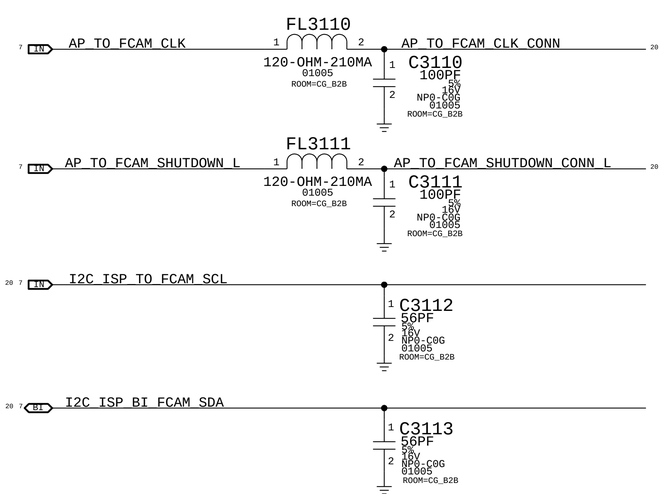
SHEET: 19 OF 59

FOREHEAD FLEX (FCAM)

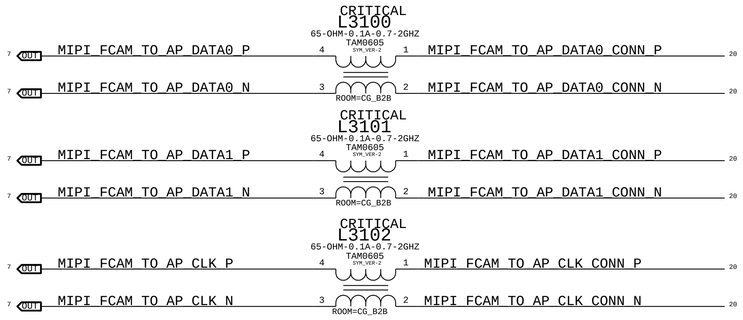
CAMERA POWER



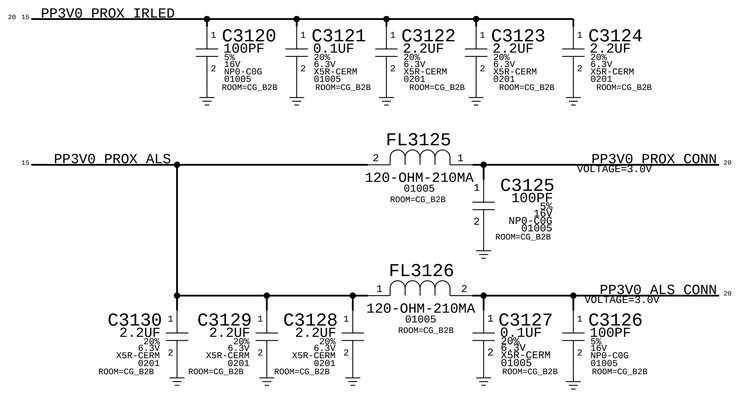
CAMERA I/O



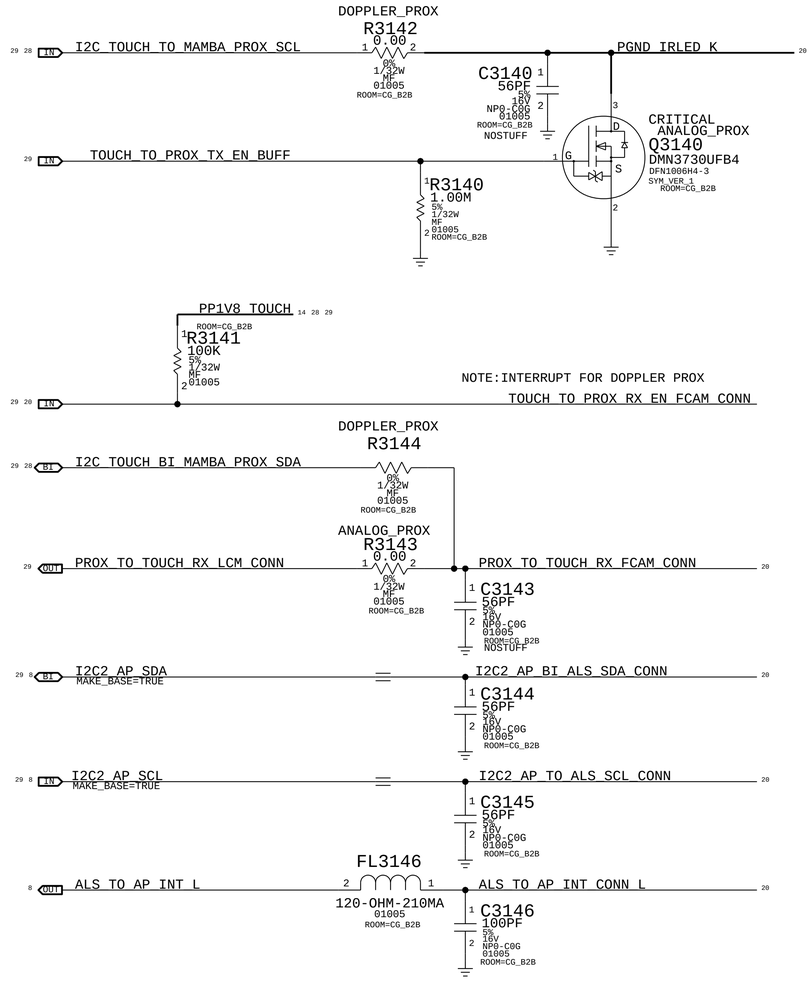
CAMERA MIPI



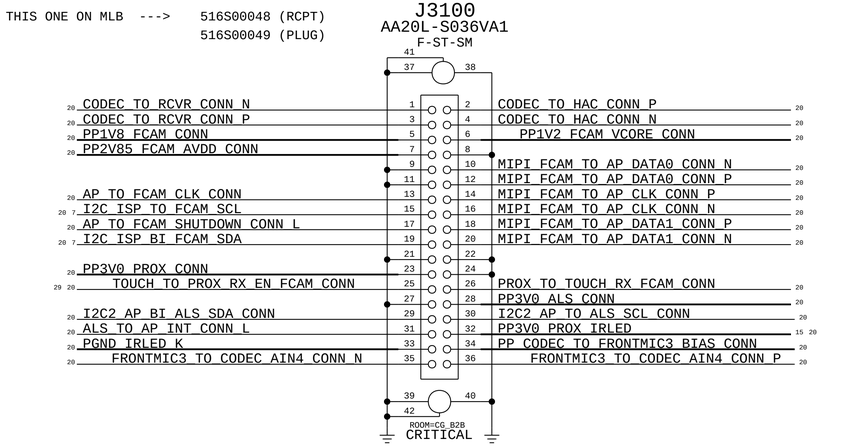
PROX & ALS POWER

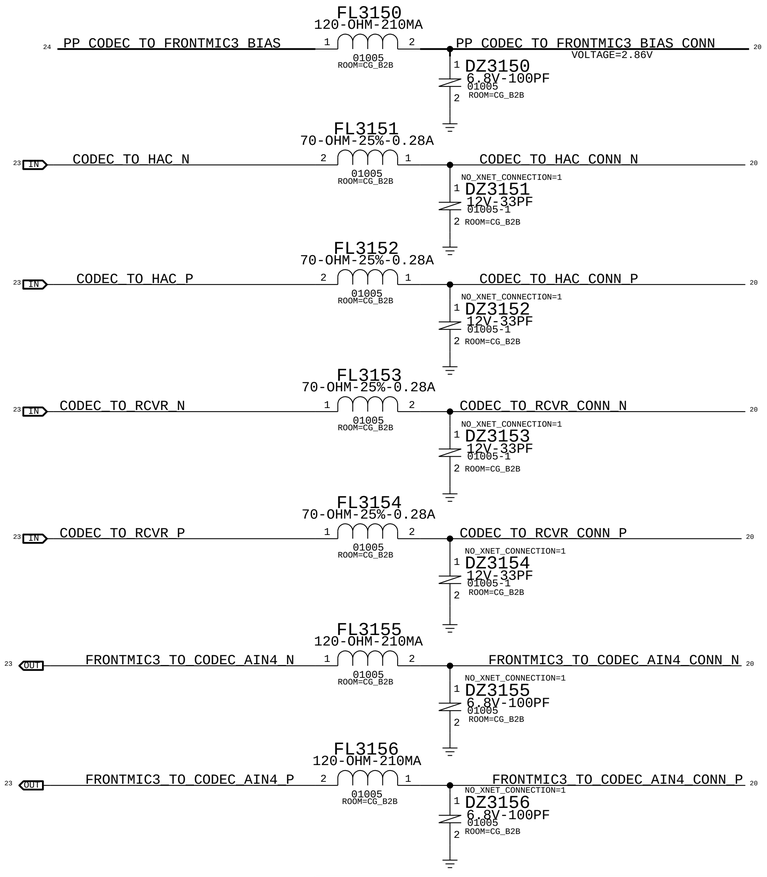


PROX & ALS INTERFACE



FOREHEAD CONNECTOR





SYNC_MASTER=N/A SYNC_DATE=N/A

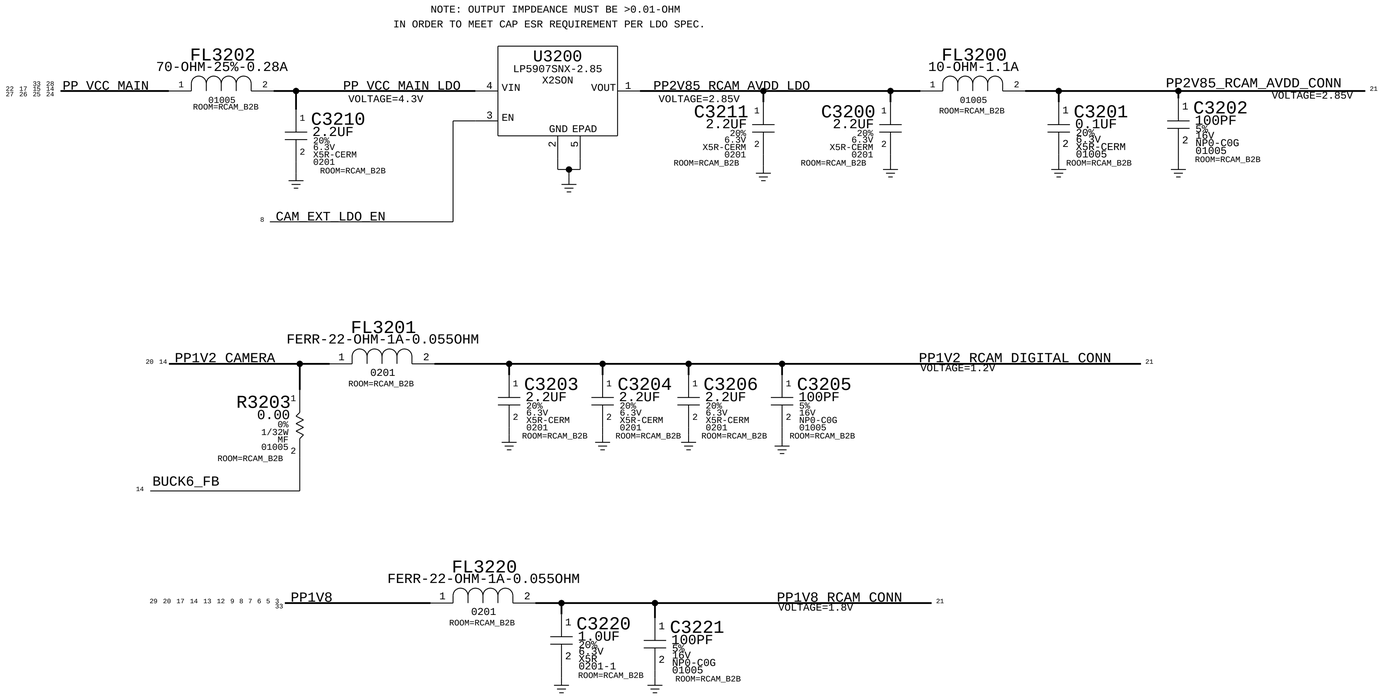
PAGE TITLE
CAMERA:FOREHEAD FLEX B2B

Apple Inc.

DRAWING NUMBER 051-1902 SIZE D
REVISION A.0.0
BRANCH
PAGE 31 OF 49
SHEET 20 OF 59

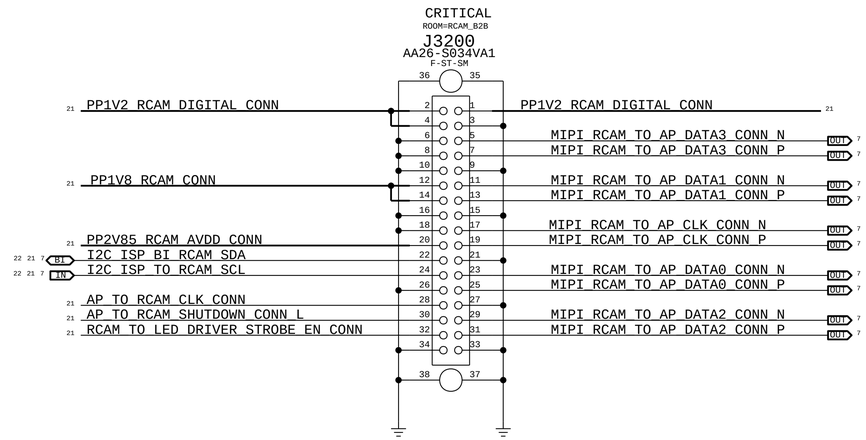
REAR CAMERA FLEX

CAMERA POWER

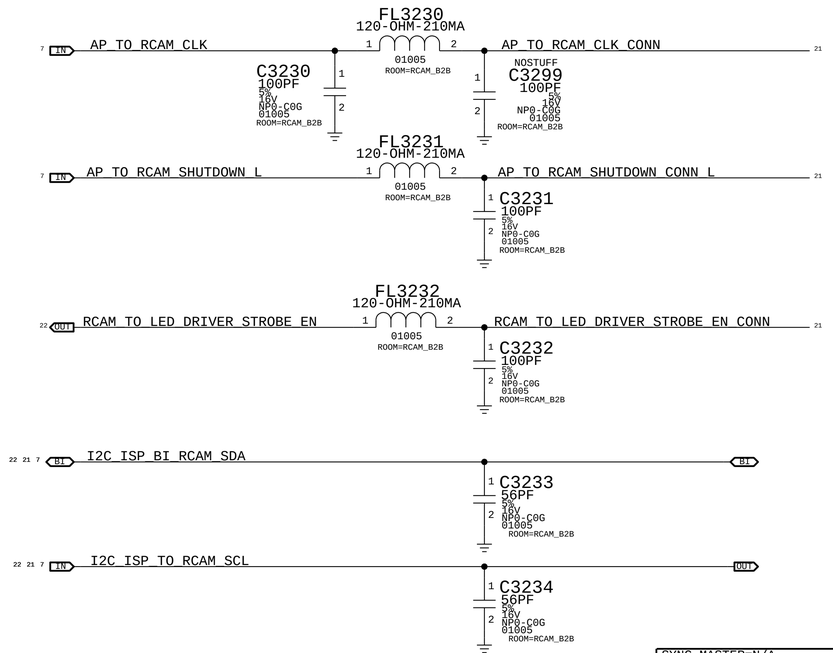


RCAM CONNECTOR

THIS ONE ON MLB ---> 516S00043 (RCPT)
516S00042 (PLUG)



DIGITAL I/O



SYNC_MASTER=N/A	SYNC_DATE=N/A
PAGE TITLE: CAMERA:REAR CAMERA B2B	
Apple Inc.	DRAWING NUMBER: 051-1902 SIZE: D
	REVISION: A.0.0
	BRANCH:
	PAGE: 32 OF 49
	SHEET: 21 OF 59

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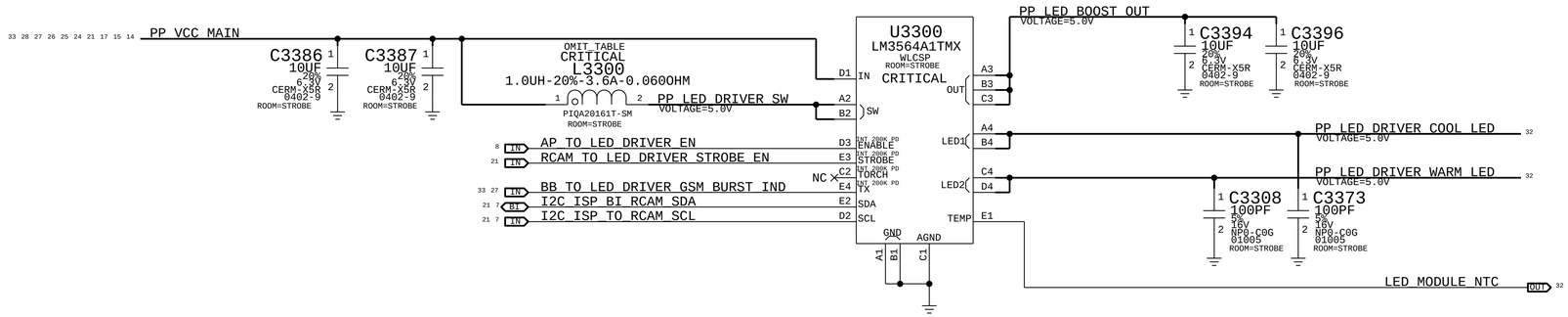
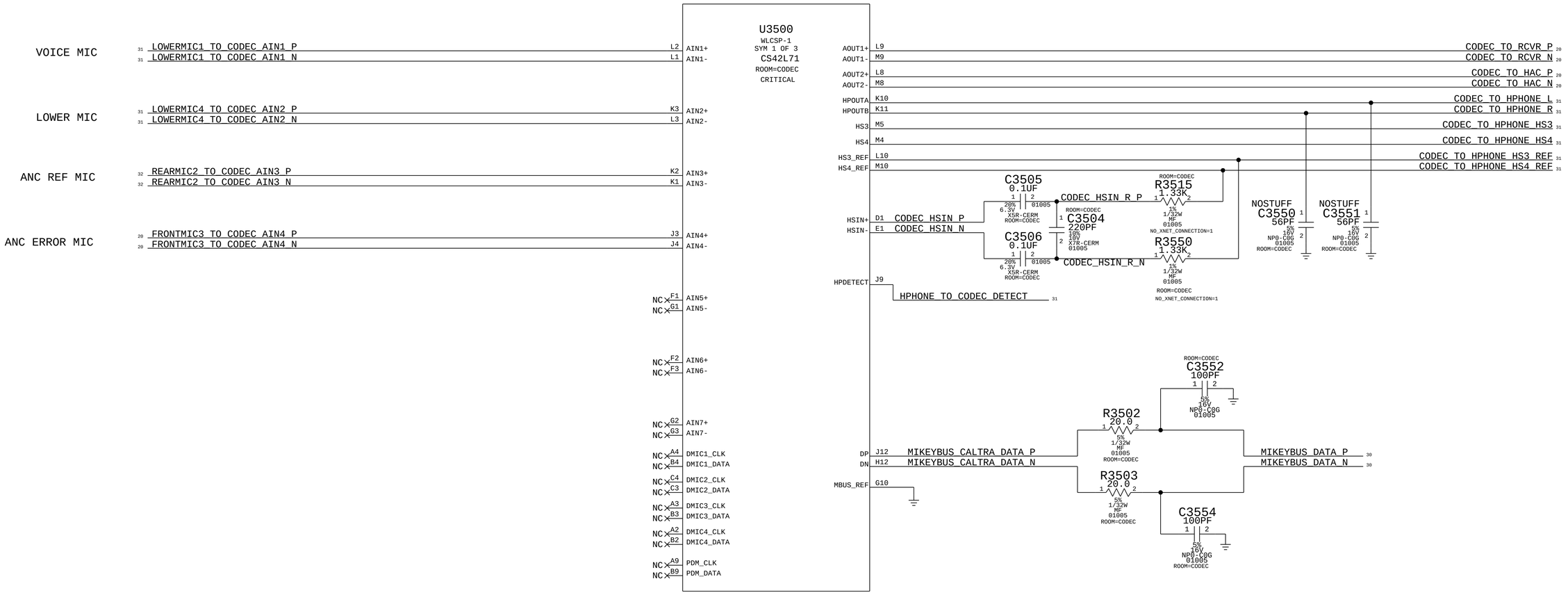
DUAL LED STROBE DRIVER

APN:353S3899



SYNC_MASTER=N/A	SYNC_DATE=N/A
PAGE TITLE	CAMERA:STROBE DRIVER
Apple Inc.	DRAWING NUMBER 051-1902 · SIZE D
	REVISION A.0.0
	BRANCH
	PAGE 33 OF 49
	SHEET 22 OF 59

CALTRA AUDIO CODEC (ANALOG INPUTS & OUTPUTS)



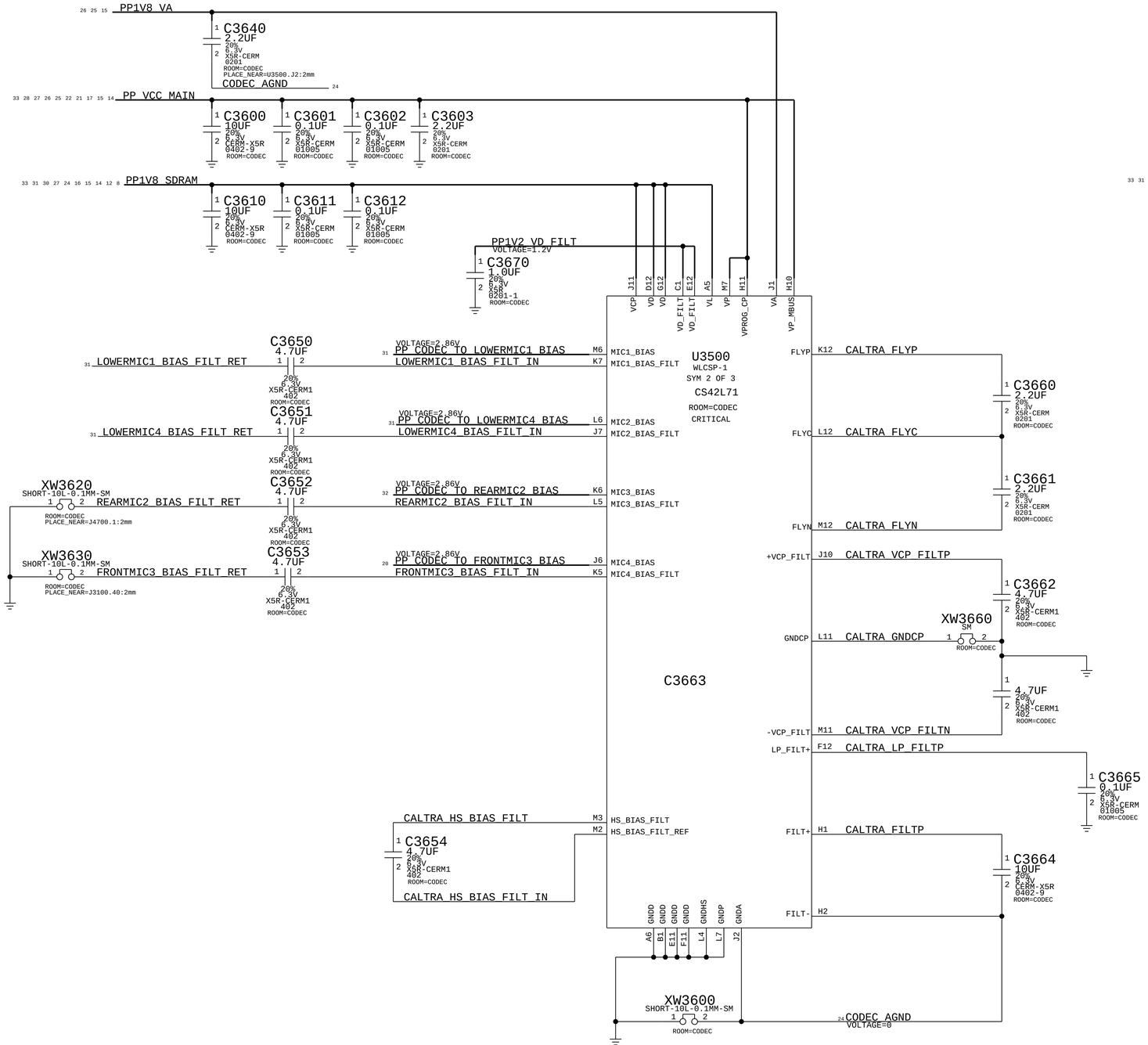
SYNC_MASTER=N71_SINGLE_BRD
SYNC_DATE=05/29/2014

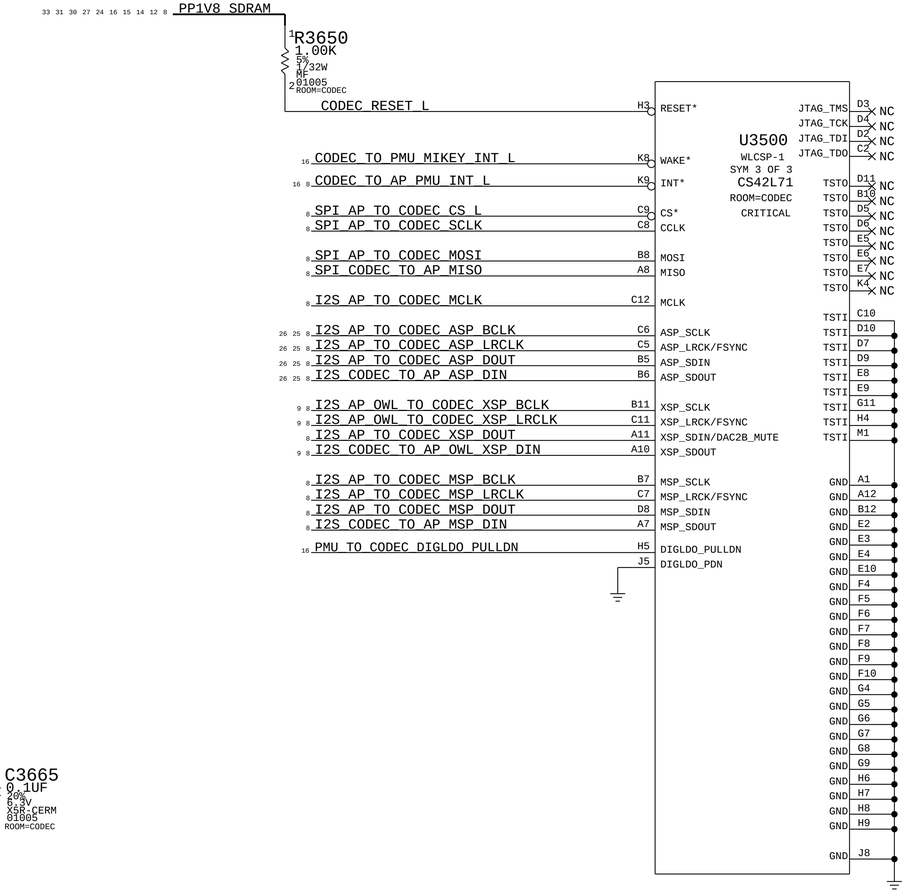
PAGE TITLE
AUDIO:CALTRA CODEC (1/2)

Apple Inc.

DRAWING NUMBER 051-1902
SIZE D
REVISION A.0.0
BRANCH
PAGE 35 OF 49
SHEET 23 OF 59

CALTRA AUDIO CODEC (POWER & I/O)





SYNC_MASTER=N71_SINGLE_BRD SYNC_DATE=05/29/2014

PAGE TITLE: AUDIO:CALTRA CODEC (2/2)

Apple Inc.

DRAWING NUMBER: 051-1902 SIZE: D

REVISION: A.0.0

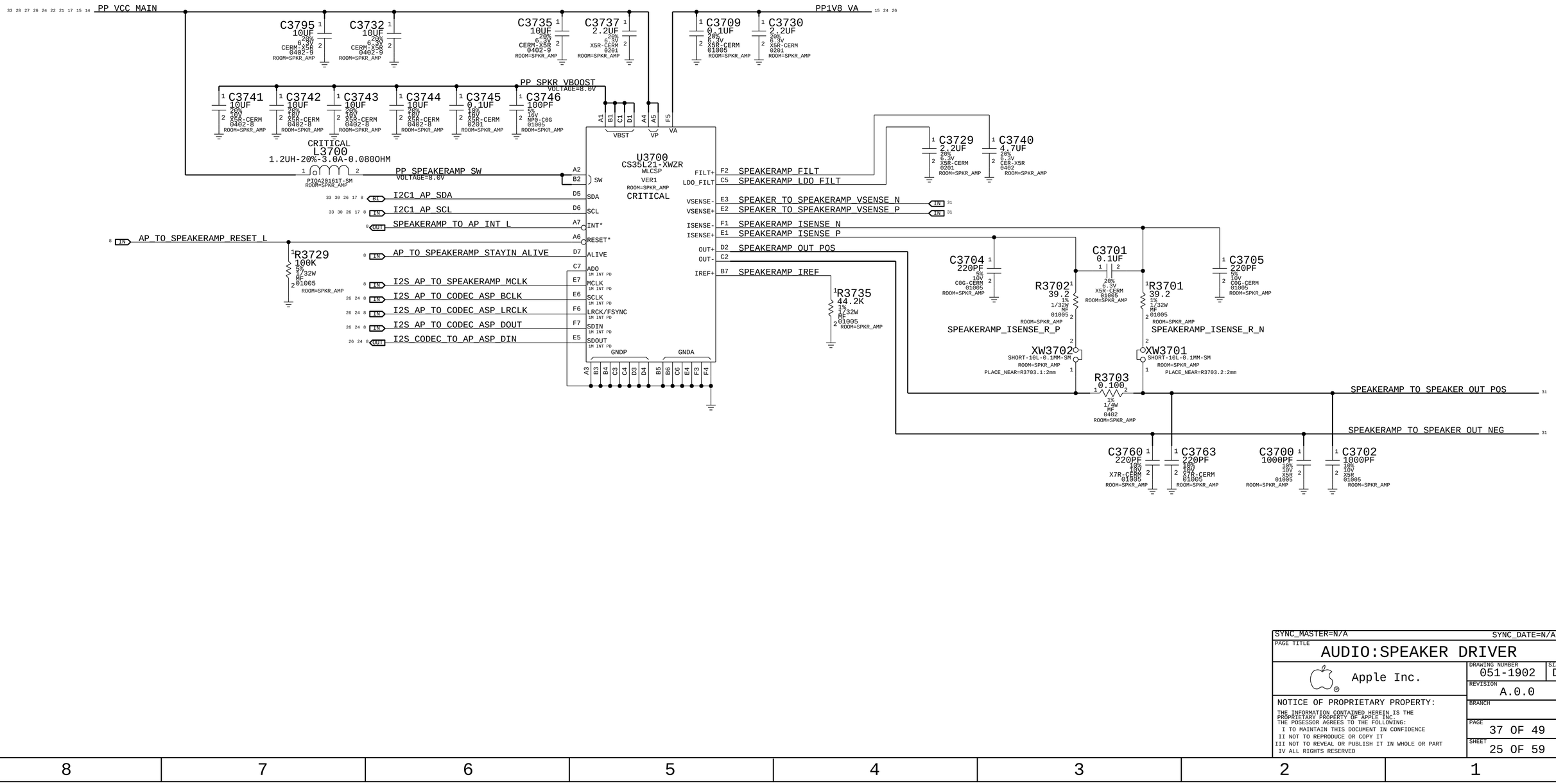
BRANCH:

PAGE: 36 OF 49

SHEET: 24 OF 59

SPEAKER AMPLIFIER

APN: 338S1285



SYNC_MASTER=N/A SYNC_DATE=N/A

PAGE TITLE: AUDIO:SPEAKER DRIVER

Apple Inc.

DRAWING NUMBER: 051-1902 SIZE: D

REVISION: A.0.0

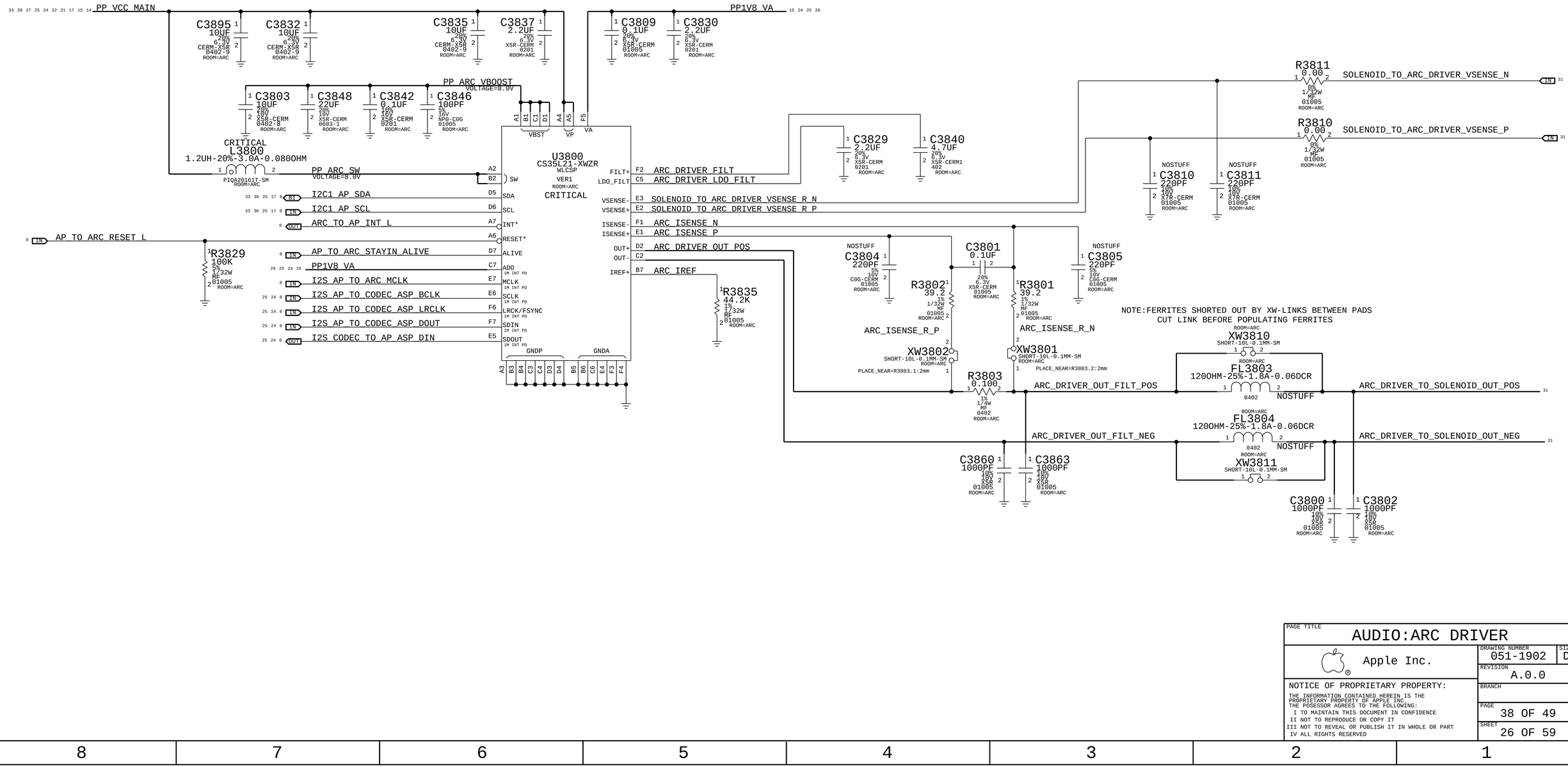
BRANCH:

PAGE: 37 OF 49

SHEET: 25 OF 59

ARC DRIVER

APN: 338S1285



PAGE TITLE

AUDIO:ARC DRIVER

Apple Inc.

DRAWING NUMBER 051-1902

SIZE D

REVISION A.0.0

BRANCH

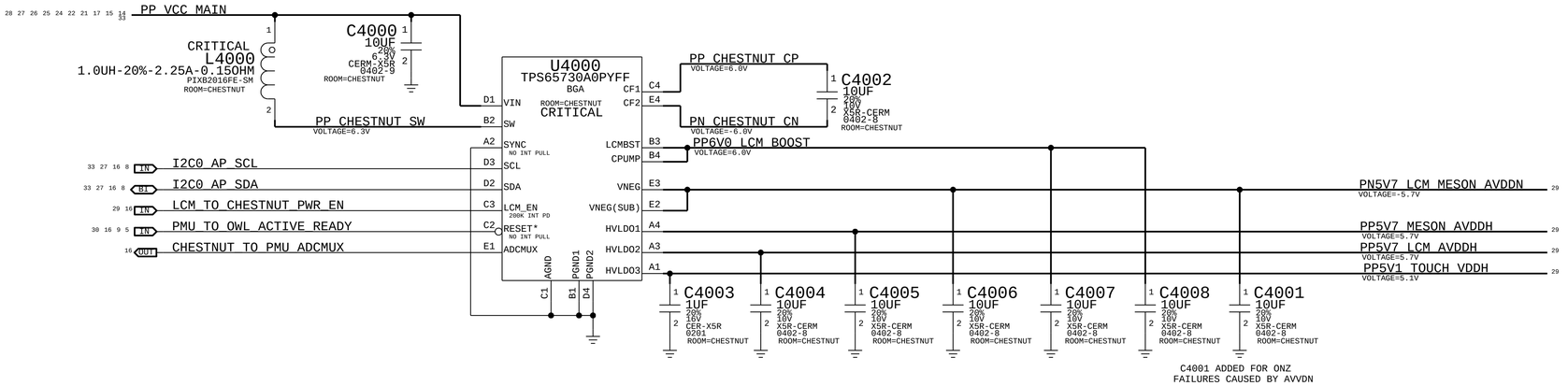
PAGE 38 OF 49

SHEET 26 OF 59

DISPLAY & TOUCH - POWER SUPPLIES

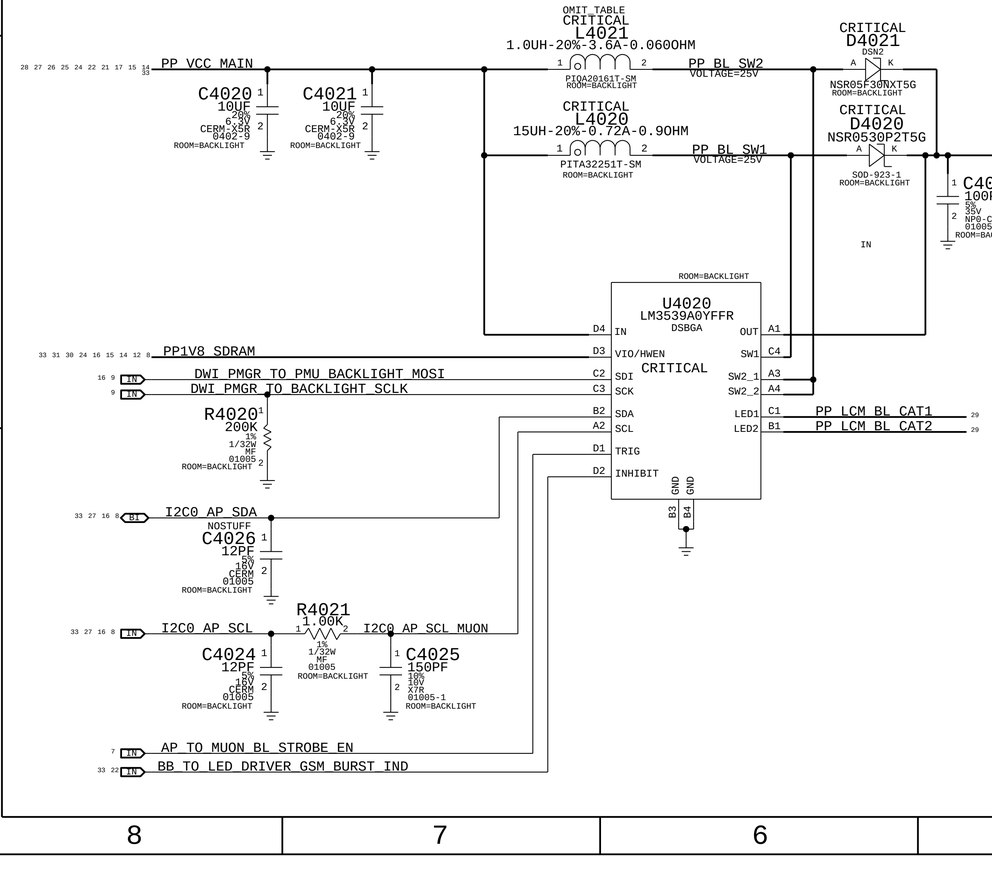
CHESTNUT DISPLAY PMU

APN:338S1172



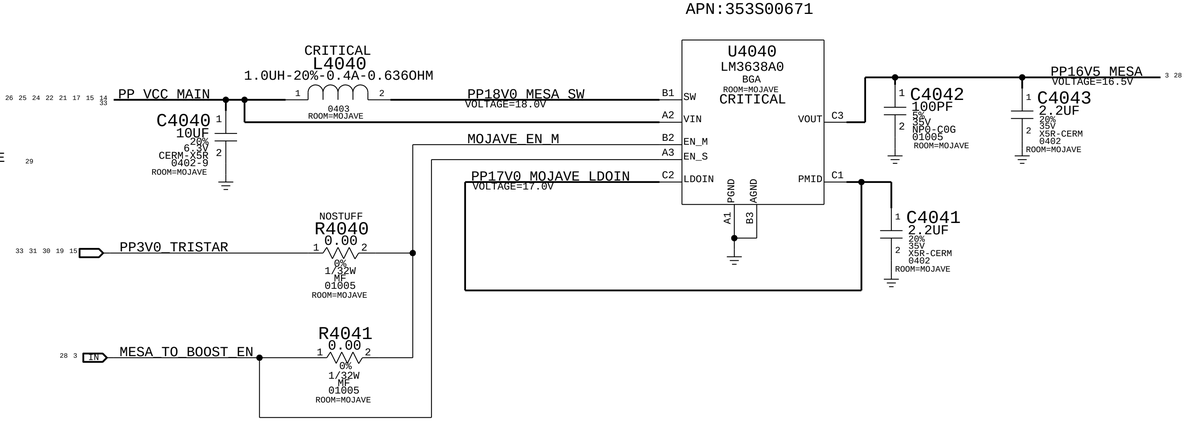
LED BACKLIGHT DRIVER

APN:353S00407



MOJAVE MESA BOOST

APN:353S00671



SYNC_MASTER=N/A SYNC_DATE=N/A

PAGE TITLE

DISPLAY:POWER

Apple Inc.

DRAWING NUMBER 051-1902 SIZE D

REVISION A.0.0

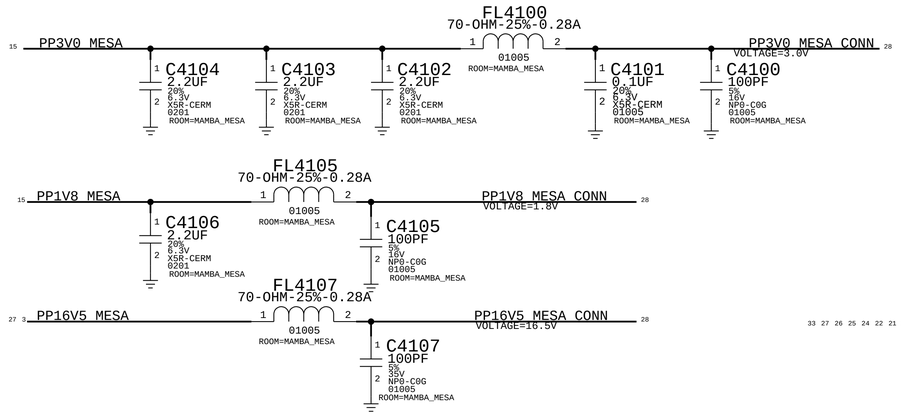
BRANCH

PAGE 40 OF 49

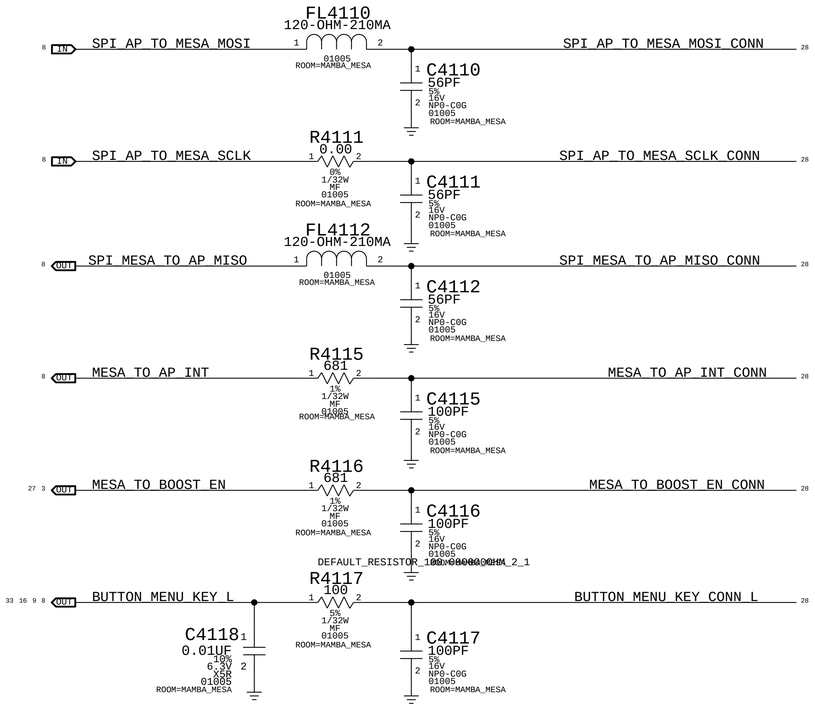
SHEET 27 OF 59

MAMBA & MESA (M&M) FLEX

MESA POWER

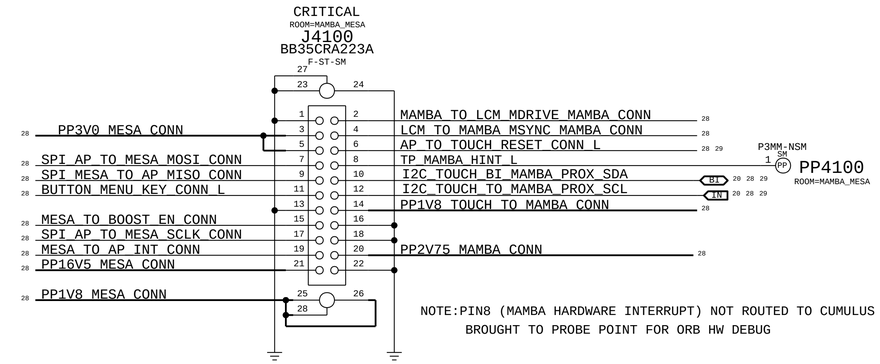


MESA DIGITAL I/O



MAMBA & MESA CONNECTOR

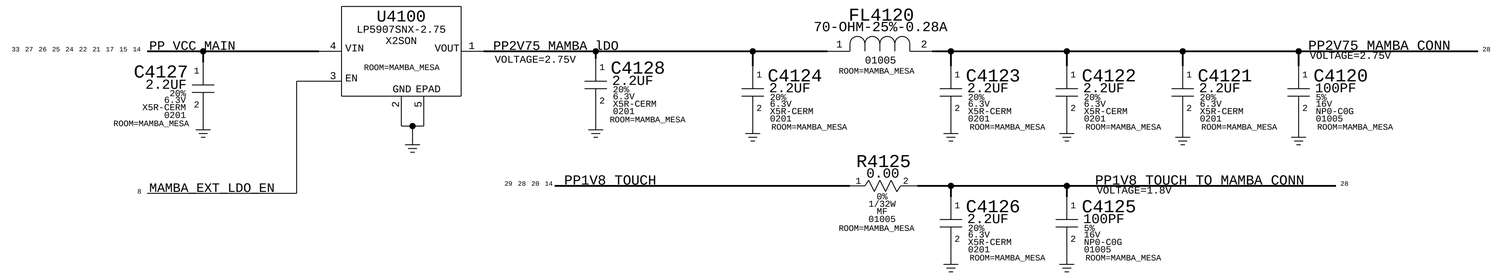
THIS ONE ON MLB ---> 516S00056 (RCPT)
516S00057 (PLUG)



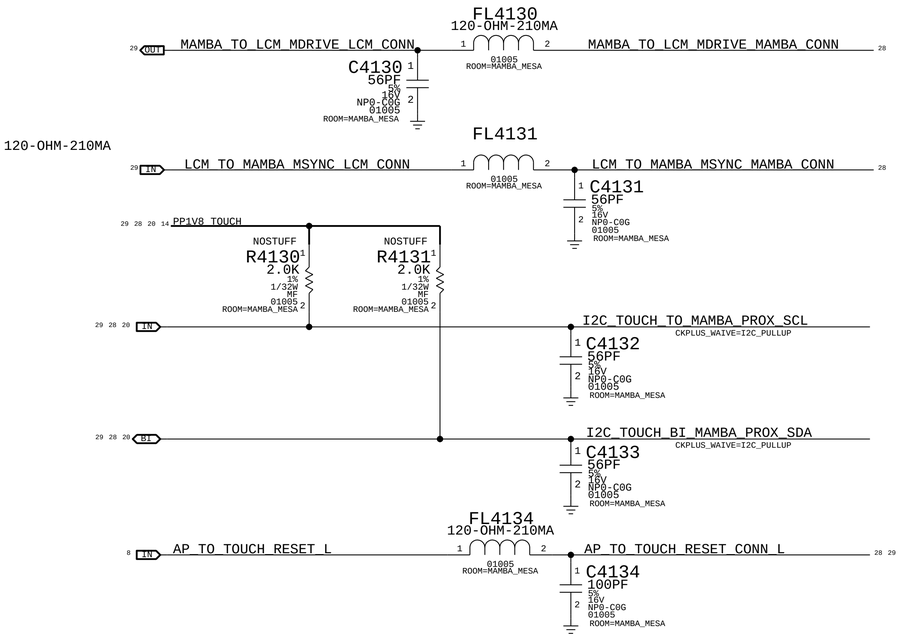
NOTE:PIN8 (MAMBA HARDWARE INTERRUPT) NOT ROUTED TO CUMULUS
BROUGHT TO PROBE POINT FOR ORB HW DEBUG

MAMBA POWER

NOTE: OUTPUT IMPDEANCE MUST BE >0.01-OHM
IN ORDER TO MEET CAP ESR REQUIREMENT PER LDO SPEC.



MAMBA DIGITAL I/O



NOTE:TOUCH I2C PULL-UPS TO PP1V8_TOUCH INSIDE KEPLER
ADDING R4130, R4131 AS OPTION FOR TWEAKING VALUES.

SYNC_MASTER=N/A SYNC_DATE=N/A

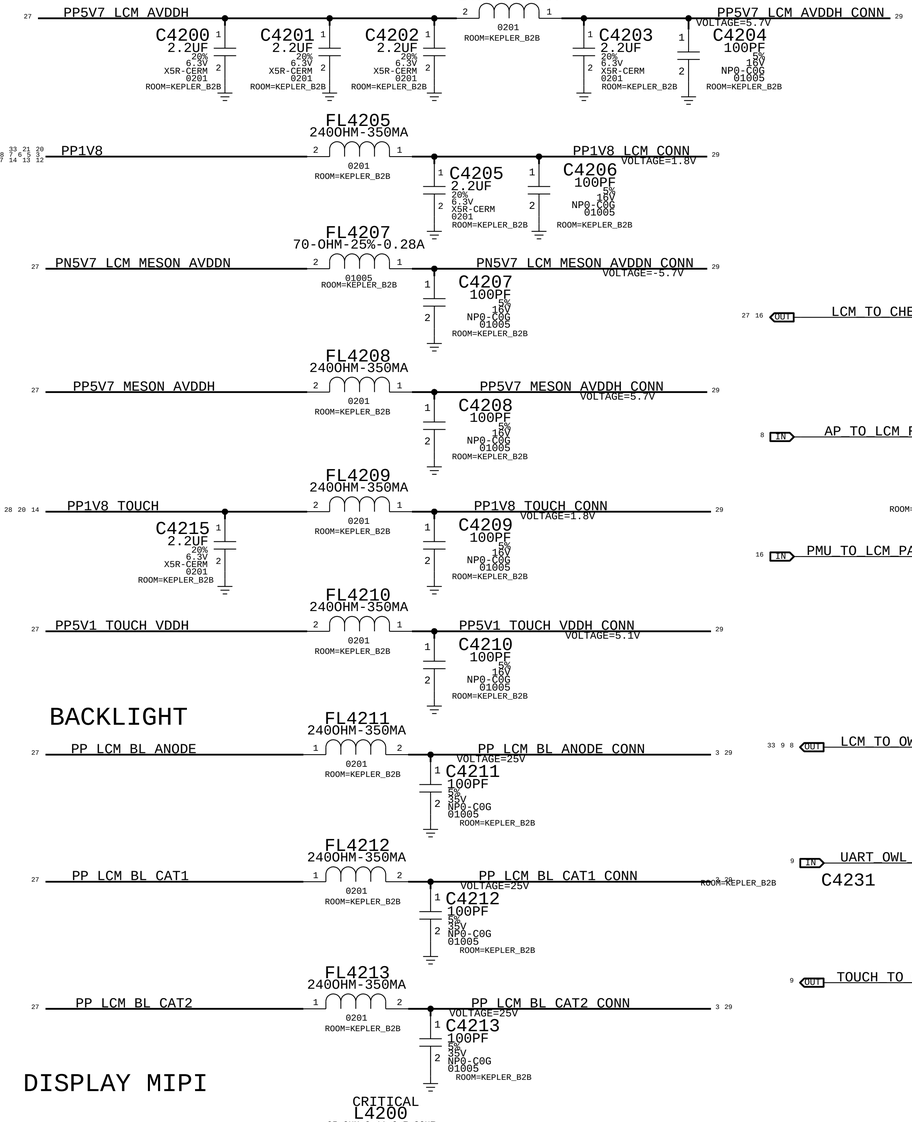
PAGE TITLE
TOUCH:ORB & MESA B2B

Apple Inc.

DRAWING NUMBER 051-1902 SIZE D
REVISION A.0.0
BRANCH
PAGE 41 OF 49
SHEET 28 OF 59

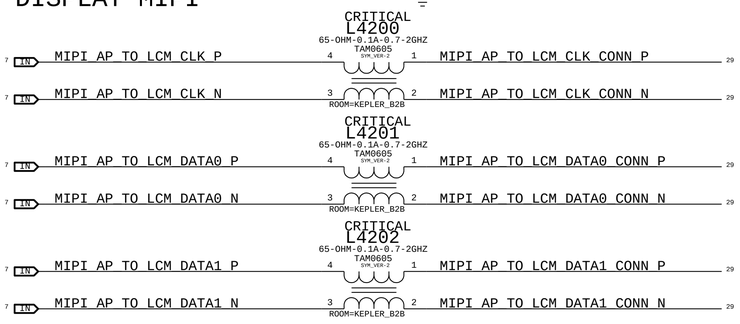
DISPLAY & TOUCH FLEX

DISPLAY POWER

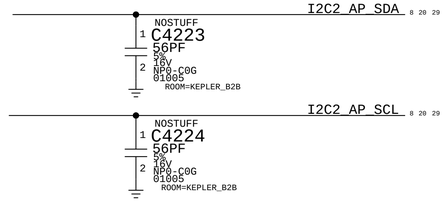


BACKLIGHT

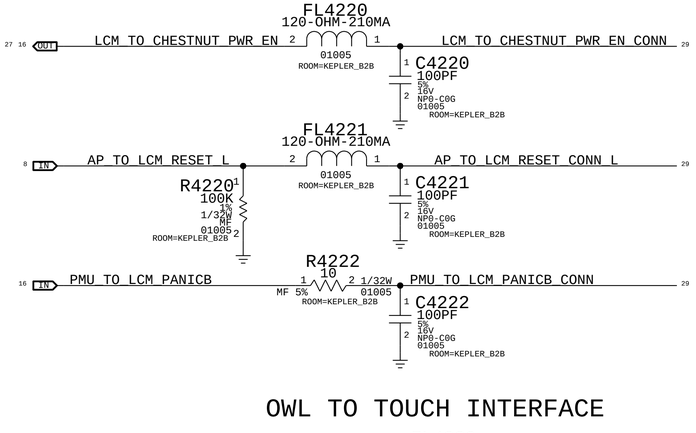
DISPLAY MIPI



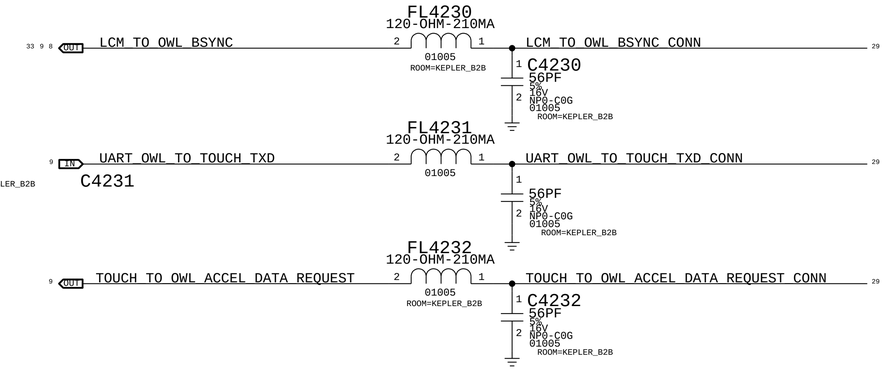
DISPLAY EEPROM I2C



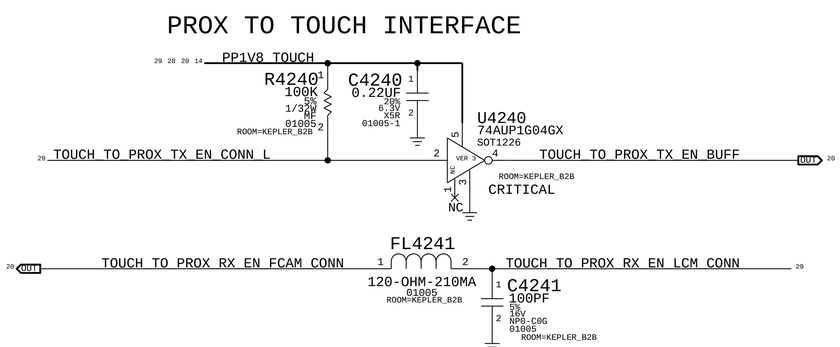
DISPLAY CONTROL SIGNALS



OWL TO TOUCH INTERFACE



PROX TO TOUCH INTERFACE



DISPLAY CONNECTOR

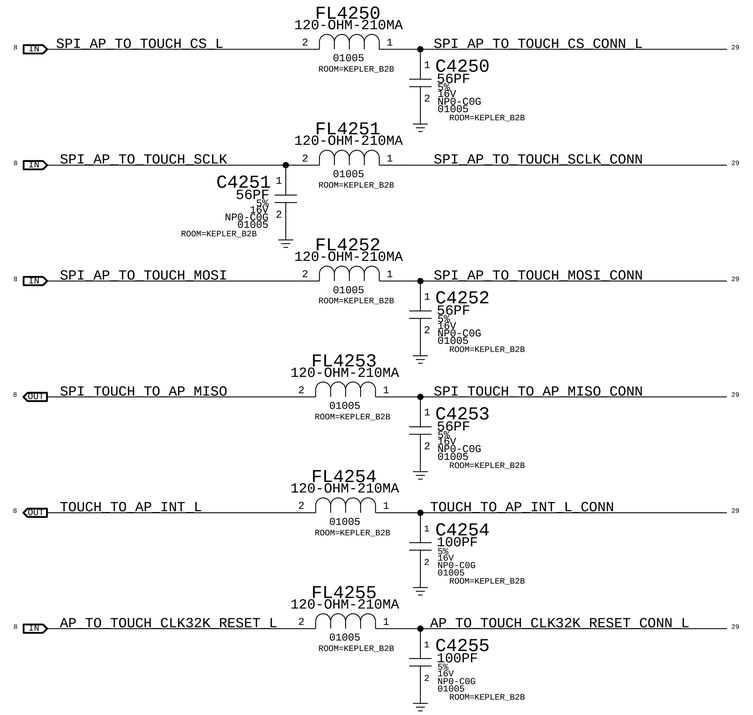
THIS ONE ON MLB ---> 516S00038 (RCPT)
516S00037 (PLUG)

CRITICAL
J4200
BM28P0.6-44DS-0.35V
F-ST-SM

	PP_LCM_BL_CAT1_CONN	1	2	MAMBA_TO_LCM_MDRIVE_LCM_CONN
	PP_LCM_BL_ANODE_CONN	3	4	NC_KEPLER_MESON_TEST_MUX2_CONN
	PP_LCM_BL_CAT2_CONN	5	6	NC_KEPLER_MESON_TEST_MUX0_CONN
		7	8	SPI_AP_TO_TOUCH_SCLK_CONN
	MIPI_AP_TO_LCM_CLK_CONN_N	9	10	TOUCH_TO_PROX_RX_EN_LCM_CONN
	MIPI_AP_TO_LCM_CLK_CONN_P	11	12	PROX_TO_TOUCH_RX_LCM_CONN
		13	14	SPI_AP_TO_TOUCH_CS_CONN_L
	MIPI_AP_TO_LCM_DATA1_CONN_N	15	16	TOUCH_TO_OWL_ACCEL_DATA_REQUEST_CONN
	MIPI_AP_TO_LCM_DATA1_CONN_P	17	18	I2C2_AP_SDA
		19	20	I2C_TOUCH_BI_MAMBA_PROX_SDA
	MIPI_AP_TO_LCM_DATA0_CONN_N	21	22	SPI_TOUCH_TO_AP_MISO_CONN
	MIPI_AP_TO_LCM_DATA0_CONN_P	23	24	SPI_AP_TO_TOUCH_MOSI_CONN
		25	26	LCM_TO_OWL_BSYNC_CONN
	NC_KEPLER_PHOTON_PIFA_CONN	27	28	LCM_TO_CHESTNUT_PWR_EN_CONN
	LCM_TO_MAMBA_MSYNC_LCM_CONN	29	30	PP5V1_TOUCH_VDDH_CONN
	PMU_TO_LCM_PANICB_CONN	31	32	AP_TO_TOUCH_RESET_CONN_L
	AP_TO_LCM_RESET_CONN_L	33	34	TOUCH_TO_PROX_TX_EN_CONN_L
	PP5V7_MESON_AVDDH_CONN	35	36	I2C2_AP_SCL
	PP1V8_LCM_CONN	37	38	I2C_TOUCH_TO_MAMBA_PROX_SCL
	PN5V7_LCM_MESON_AVDDN_CONN	39	40	UART_OWL_TO_TOUCH_TXD_CONN
	PP5V7_LCM_AVDDH_CONN	41	42	TOUCH_TO_AP_INT_L_CONN
	PP1V8_TOUCH_CONN	43	44	AP_TO_TOUCH_CLK32K_RESET_CONN_L

ROOM=KEPLER_B2B

AP TO TOUCH INTERFACE



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Apple Inc.	DRAWING NUMBER 051-1902 · SIZE D
	REVISION A.0.0
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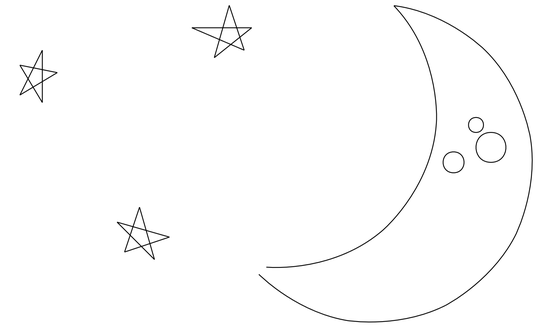
	PAGE 42 OF 49
	SHEET 29 OF 59

TRISTAR 2 (A3)

APN:343S0695



PP3V0_TRISTAR
C4500 1.0UF 20% 6.3V X5R 0201-1 ROOM=TRISTAR
C4501 0.1UF 20% 6.3V X5R-CERM 01005 ROOM=TRISTAR
PP1V8_SDRAM
C4502 0.01UF 10% 6.3V X5R 01005 ROOM=TRISTAR
PP3V3_ACC
PP5V0_USB
REVERSE_GATE
R4500 10K 5% 1/32W MF 01005 ROOM=TRISTAR
Q4500 CSD68822F4 0402 ROOM=TRISTAR CRITICAL
PLACE_NEAR=U2000.T5:8mm
R4510 6.34K 1% 1/32W MF 01005 ROOM=PMU
TRISTAR_TO_PMU_USB_BRICK_ID
C4510 0.01UF 10% 6.3V X5R 01005 ROOM=PMU PLACE_NEAR=U2000.T5:8mm
C4503 1UF 20% 16V CER-X5R 0201 ROOM=TRISTAR
L4521 15NH-250MA 0201 ROOM=TRISTAR
L4522 15NH-250MA 0201 ROOM=TRISTAR
USB_AP_DATA_P
USB_AP_DATA_N
U4500 CBTL1610A3UK WLCSP
CRITICAL ROOM=TRISTAR
MIKEYBUS_DATA_P
MIKEYBUS_DATA_N
USB_BB_DATA_P
USB_BB_DATA_N
TRISTAR_USB_BRICK_ID_R
USB_AP_TRISTAR_DATA_P
USB_AP_TRISTAR_DATA_N
UART_AP_TO_ACCESSORY_TXD
UART_ACCESSORY_TO_AP_RXD
UART_AP_DEBUG_TXD
UART_AP_DEBUG_RXD
SWD_DOCK_TO_AP_SWCLK
SWD_DOCK_BI_AP_SWDIO
PP_TRISTAR_PIN VOLTAGE=5.0V
PP_TRISTAR_ACC1 VOLTAGE=4.3V
PP_TRISTAR_ACC2 VOLTAGE=4.3V
TRISTAR_DP1_CONN_P
TRISTAR_DP1_CONN_N
TRISTAR_DP2_CONN_P
TRISTAR_DP2_CONN_N
TRISTAR_CON_DETECT_L
TRISTAR_TO_TIGRIS_VBUS_OFF
PMU_TO_OWL_ACTIVE_READY
TRISTAR_TO_PMU_HOST_RESET
I2C1_AP_SDA
I2C1_AP_SCL
TRISTAR_TO_AP_INT
TRISTAR_BYPASS
NC
1.0UF
C4504 20% 6.3V X5R 0201-1 ROOM=TRISTAR
TRISTAR_TO_TIGRIS_VBUS_OFF
PP4500 ROOM=TRISTAR P3MM-NSM SM

SYNC_MASTER=N/A	SYNC_DATE=N/A
PAGE TITLE	I/O:TRISTAR 2
Apple Inc.	DRAWING NUMBER 051-1902 SIZE D
	REVISION A.0.0
	BRANCH
	PAGE 45 OF 49
	SHEET 30 OF 59

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DOCK FLEX CONNECTOR

AUDIO JACK

23 OUT HPHONE_TO_CODEC_DETECT → HPHONE_TO_CODEC_DETECT_CONN 31
R4600 3.3K 5% 1/32W MF 01005 ROOM=DOCK_B2B
C4600 56PF 5% 16V NP0-C0G 01005 ROOM=DOCK_B2B

FL4600 FERR-33-OHM-0.8A-0.09-OHM
23 BI CODEC_TO_HPHONE_HS3 → CODEC_TO_HPHONE_HS3_CONN 31
0201 ROOM=DOCK_B2B
DZ4600 6.8V-100PF 01005 ROOM=DOCK_B2B NO_XNET_CONNECTION=1
C4699 220PF 10% 16V X7R-CERM 01005 ROOM=DOCK_B2B

FL4601 FERR-33-OHM-0.8A-0.09-OHM
23 BI CODEC_TO_HPHONE_HS4 → CODEC_TO_HPHONE_HS4_CONN 31
0201 ROOM=DOCK_B2B
DZ4601 6.8V-100PF 01005 ROOM=DOCK_B2B NO_XNET_CONNECTION=1
C4698 220PF 10% 16V X7R-CERM 01005 ROOM=DOCK_B2B

FL4602 600-OHM-25%-0.28A-0.750HM
23 OUT CODEC_TO_HPHONE_HS4_REF → CODEC_TO_HPHONE_HS4_REF_CONN 31
0201 ROOM=DOCK_B2B
DZ4602 6.8V-100PF 01005 ROOM=DOCK_B2B NO_XNET_CONNECTION=1

FL4603 600-OHM-25%-0.28A-0.750HM
23 OUT CODEC_TO_HPHONE_HS3_REF → CODEC_TO_HPHONE_HS3_REF_CONN 31
0201 ROOM=DOCK_B2B
DZ4603 6.8V-100PF 01005 ROOM=DOCK_B2B NO_XNET_CONNECTION=1

FL4604 FERR-33-OHM-0.8A-0.09-OHM
23 IN CODEC_TO_HPHONE_L → CODEC_TO_HPHONE_L_CONN 31
0201 ROOM=DOCK_B2B
DZ4604 6.8V-100PF 01005 ROOM=DOCK_B2B NO_XNET_CONNECTION=1
C4697 220PF 10% 16V X7R-CERM 01005 ROOM=DOCK_B2B

FL4605 FERR-33-OHM-0.8A-0.09-OHM
23 IN CODEC_TO_HPHONE_R → CODEC_TO_HPHONE_R_CONN 31
0201 ROOM=DOCK_B2B
DZ4610 6.8V-100PF 01005 ROOM=DOCK_B2B NO_XNET_CONNECTION=1
C4696 220PF 10% 16V X7R-CERM 01005 ROOM=DOCK_B2B

LOWER MIC1/4

FL4610 120-OHM-210MA
23 OUT LOWERMIC1_TO_CODEC_AIN1_P → LOWERMIC1_TO_CODEC_AIN1_CONN_P 31
01005 ROOM=DOCK_B2B
C4610 56PF 5% 16V NP0-C0G 01005 ROOM=DOCK_B2B

FL4611 120-OHM-210MA
23 OUT LOWERMIC1_TO_CODEC_AIN1_N → LOWERMIC1_TO_CODEC_AIN1_CONN_N 31
01005 ROOM=DOCK_B2B
C4611 56PF 5% 16V NP0-C0G 01005 ROOM=DOCK_B2B

FL4612 120-OHM-210MA
24 PP_CODEC_TO_LOWERMIC1_BIAS → PP_CODEC_TO_LOWERMIC1_BIAS_CONN 31 VOLTAGE=2.86V
01005 ROOM=DOCK_B2B
C4612 100PF 5% 16V NP0-C0G 01005 ROOM=DOCK_B2B

FL4613 120-OHM-210MA
23 OUT LOWERMIC4_TO_CODEC_AIN2_P → LOWERMIC4_TO_CODEC_AIN2_CONN_P 31
01005 ROOM=DOCK_B2B
C4613 56PF 5% 16V NP0-C0G 01005 ROOM=DOCK_B2B

FL4614 120-OHM-210MA
23 OUT LOWERMIC4_TO_CODEC_AIN2_N → LOWERMIC4_TO_CODEC_AIN2_CONN_N 31
01005 ROOM=DOCK_B2B
C4614 56PF 5% 16V NP0-C0G 01005 ROOM=DOCK_B2B

FL4615 120-OHM-210MA
24 PP_CODEC_TO_LOWERMIC4_BIAS → PP_CODEC_TO_LOWERMIC4_BIAS_CONN 31 VOLTAGE=2.86V
01005 ROOM=DOCK_B2B
C4615 100PF 5% 16V NP0-C0G 01005 ROOM=DOCK_B2B

ANTENNA

FL4620 120-OHM-210MA
33 30 27 19 16 PP3V0_TRISTAR → PP3V0_LAT_CONN 31 VOLTAGE=3.0V
01005 ROOM=DOCK_B2B
C4620 100PF 5% 16V NP0-C0G 01005 ROOM=DOCK_B2B

FL4621 120-OHM-210MA
33 30 27 24 16 15 14 12 8 PP1V8_SDRAM VOLTAGE=1.8V → PP1V8_LAT_CONN 31 VOLTAGE=1.8V
01005 ROOM=DOCK_B2B
C4621 100PF 5% 16V NP0-C0G 01005 ROOM=DOCK_B2B

R4622 0.00 0% MF 01005 1/32W ROOM=DOCK_B2B
33 IN RFFE5_BB_TO_ANT_SCLK → RFFE5_BB_TO_ANT_SCLK_CONN 31
C4622 56PF 5% 16V NP0-C0G 01005 ROOM=DOCK_B2B

R4623 0.00 0% MF 01005 1/32W ROOM=DOCK_B2B
33 BI RFFE5_BB_TO_ANT_DATA → RFFE5_BB_TO_ANT_DATA_CONN 31
C4623 56PF 5% 16V NP0-C0G 01005 ROOM=DOCK_B2B

FL4624 120-OHM-210MA
33 IN BB_LAT_GPIO1 → BB_LAT_GPIO1_CONN 31
01005 ROOM=DOCK_B2B
C4624 56PF 5% 16V NP0-C0G 01005 ROOM=DOCK_B2B

FL4606 120-OHM-210MA
8 BI AP_TO_HP_HS3_CTRL → AP_TO_HP_HS3_CTRL_CONN 31
01005 ROOM=DOCK_B2B
C4606 100PF 5% 16V NP0-C0G 01005 ROOM=DOCK_B2B

FL4607 120-OHM-210MA
8 IN AP_TO_HP_HS4_CTRL → AP_TO_HP_HS4_CTRL_CONN 31
01005 ROOM=DOCK_B2B
C4607 100PF 5% 16V NP0-C0G 01005 ROOM=DOCK_B2B

SPEAKER/ARC

FL4630 120-OHM-210MA
25 OUT SPEAKER_TO_SPEAKERAMP_VSENSE_P → SPEAKER_TO_SPEAKERAMP_VSENSE_CONN_P 31
01005 ROOM=DOCK_B2B
C4630 100PF 5% 16V NP0-C0G ROOM=DOCK_B2B

FL4631 120-OHM-210MA
25 OUT SPEAKER_TO_SPEAKERAMP_VSENSE_N → SPEAKER_TO_SPEAKERAMP_VSENSE_CONN_N 31
01005 ROOM=DOCK_B2B
C4631 100PF 5% 16V NP0-C0G 01005 ROOM=DOCK_B2B

FL4632 120-OHM-210MA
26 OUT SOLENOID_TO_ARC_DRIVER_VSENSE_P → SOLENOID_TO_ARC_DRIVER_VSENSE_CONN_P 31
01005 ROOM=DOCK_B2B
C4632 100PF 5% 16V NP0-C0G 01005 ROOM=DOCK_B2B

FL4633 120-OHM-210MA
26 OUT SOLENOID_TO_ARC_DRIVER_VSENSE_N → SOLENOID_TO_ARC_DRIVER_VSENSE_CONN_N 31
01005 ROOM=DOCK_B2B
C4633 100PF 5% 16V NP0-C0G 01005 ROOM=DOCK_B2B

31 25 SPEAKERAMP_TO_SPEAKER_OUT_POS
C4634 220PF 10% 16V X7R-CERM 01005 ROOM=DOCK_B2B

31 25 SPEAKERAMP_TO_SPEAKER_OUT_NEG
C4635 220PF 10% 16V X7R-CERM 01005 ROOM=DOCK_B2B

DOCK FLEX CONNECTOR

THIS ONE ON MLB ---> 516S00033 (RCPT)
516S00034 (PLUG)

CRITICAL ROOM=DOCK_B2B
J4600 24-5859-040-XXX-829 F-ST-SM

31 25	SPEAKERAMP_TO_SPEAKER_OUT_POS	1	2	SPEAKERAMP_TO_SPEAKER_OUT_NEG	25 31
31	SPEAKER_TO_SPEAKERAMP_VSENSE_CONN_P	3	4	SPEAKER_TO_SPEAKERAMP_VSENSE_CONN_N	31
31 26	ARC_DRIVER_TO_SOLENOID_OUT_POS	5	6	ARC_DRIVER_TO_SOLENOID_OUT_NEG	26 31
31	SOLENOID_TO_ARC_DRIVER_VSENSE_CONN_P	7	8	SOLENOID_TO_ARC_DRIVER_VSENSE_CONN_N	31
31	AP_TO_HP_HS4_CTRL_CONN	9	10	CODEC_TO_HPHONE_L_CONN	31
31	HPHONE_TO_CODEC_DETECT_CONN	11	12	CODEC_TO_HPHONE_R_CONN	31
31	CODEC_TO_HPHONE_HS4_REF_CONN	13	14	CODEC_TO_HPHONE_HS4_CONN	31
31	AP_TO_HP_HS3_CTRL_CONN	15	16		
31	CODEC_TO_HPHONE_HS3_REF_CONN	17	18	CODEC_TO_HPHONE_HS3_CONN	31
31	LOWERMIC1_TO_CODEC_AIN1_CONN_N	19	20	LOWERMIC1_TO_CODEC_AIN1_CONN_P	31
31	PP_CODEC_TO_LOWERMIC1_BIAS_CONN	21	22	PP_TRISTAR_ACC1_CONN	31
24 OUT	LOWERMIC1_BIAS_FILT_RET	23	24		
31	RFFE5_BB_TO_ANT_DATA_CONN	25	26	TRISTAR_DP1_CONN_P	BI 3 30
31	PP1V8_LAT_CONN	27	28	TRISTAR_DP1_CONN_N	BI 3 30
31	TRISTAR_CON_DETECT_CONN_L	29	30		
31	RFFE5_BB_TO_ANT_SCLK_CONN	31	32	TRISTAR_DP2_CONN_N	BI 3 30
31	BB_LAT_GPIO1_CONN	33	34	TRISTAR_DP2_CONN_P	BI 3 30
31	PP3V0_LAT_CONN	35	36	PP_TRISTAR_ACC2_CONN	31
24 OUT	LOWERMIC4_BIAS_FILT_RET	37	38	PP_CODEC_TO_LOWERMIC4_BIAS_CONN	31
31	LOWERMIC4_TO_CODEC_AIN2_CONN_N	39	40	LOWERMIC4_TO_CODEC_AIN2_CONN_P	31

45 41 42 43 44 46

30 17 7 PP5V0_USB VOLTAGE=5.0V
C4650 0.1UF 10% 25V X5R 0201 ROOM=DOCK_B2B
C4651 0.1UF 10% 25V X5R 0201 ROOM=DOCK_B2B
C4652 0.1UF 10% 25V X5R 0201 ROOM=DOCK_B2B
NOSTUFF
C4654 100PF 5% 35V NP0-C0G 01005 ROOM=DOCK_B2B
C4653 56PF 5% 25V NP0-C0G-CERM 01005 ROOM=DOCK_B2B
C4655 220PF 10% 25V X7R-CERM 0201 ROOM=DOCK_B2B
DEFAULT_CAPACITOR_220.000000pF_2_1
C4656 100PF 5% 25V NP0-C0G 01005 ROOM=DOCK_B2B

TRISTAR

30 3 OUT TRISTAR_CON_DETECT_L → TRISTAR_CON_DETECT_CONN_L 31
R4640 1.00K 5% 1/32W MF 01005 ROOM=DOCK_B2B
C4640 27PF 5% 16V NP0-C0G 01005 ROOM=DOCK_B2B

FL4641 10-OHM-1.1A
30 3 PP_TRISTAR_ACC1 → PP_TRISTAR_ACC1_CONN 31 VOLTAGE=4.3V
01005 ROOM=DOCK_B2B
C4641 100PF 5% 16V NP0-C0G 01005 ROOM=DOCK_B2B

FL4642 10-OHM-1.1A
30 3 PP_TRISTAR_ACC2 → PP_TRISTAR_ACC2_CONN 31 VOLTAGE=4.3V
01005 ROOM=DOCK_B2B
C4642 100PF 5% 16V NP0-C0G 01005 ROOM=DOCK_B2B

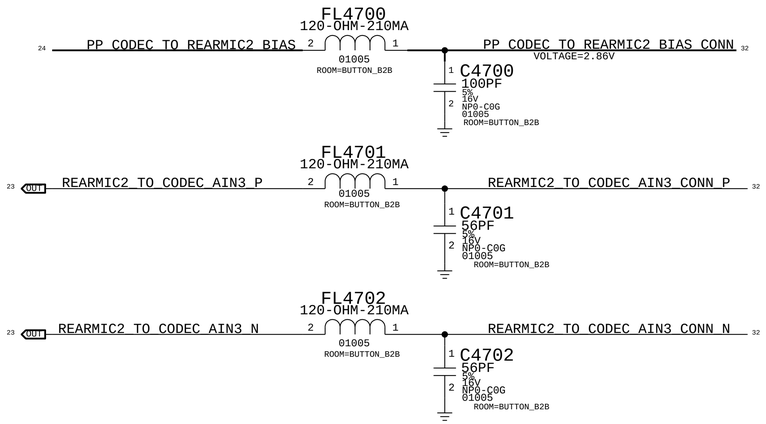
31 26 ARC_DRIVER_TO_SOLENOID_OUT_POS
C4636 100PF 5% 16V NP0-C0G 01005 ROOM=DOCK_B2B

31 26 ARC_DRIVER_TO_SOLENOID_OUT_NEG
C4637 100PF 5% 16V NP0-C0G 01005 ROOM=DOCK_B2B

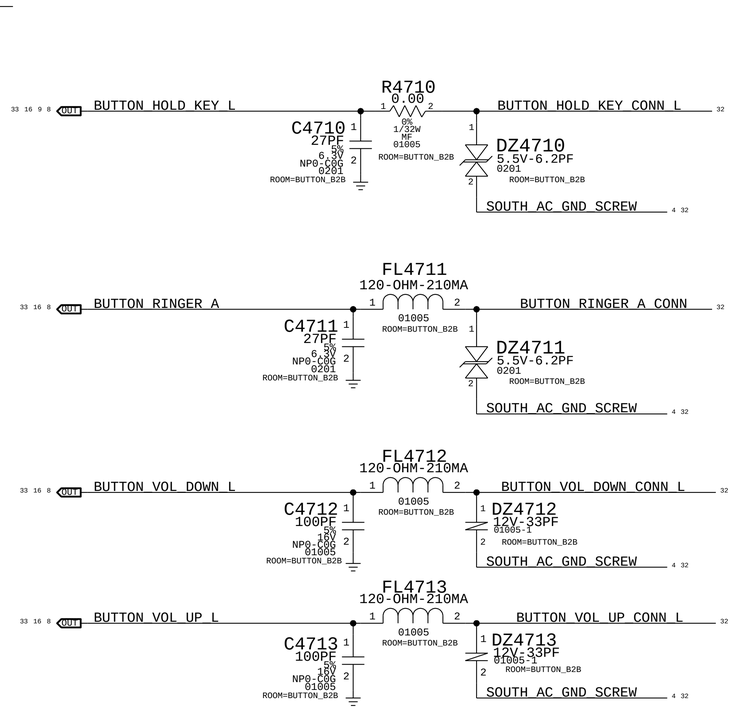
SYNC_MASTER=N/A SYNC_DATE=N/A
PAGE TITLE
I/O:DOCK FLEX B2B
Apple Inc.
DRAWING NUMBER 051-1902 SIZE D
REVISION A.0.0
BRANCH
PAGE 46 OF 49
SHEET 31 OF 59

BUTTON FLEX

MIC2
ANC REF MIC

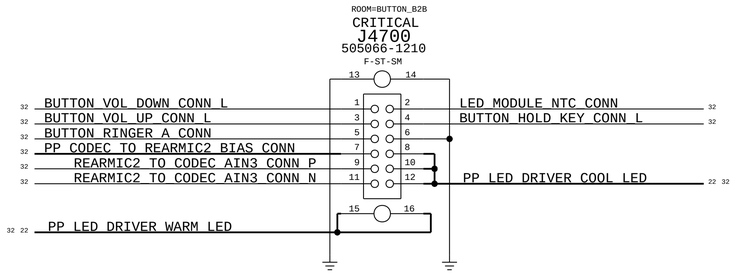


BUTTONS:
HOLD
RINGER
VOL UP/DOWN

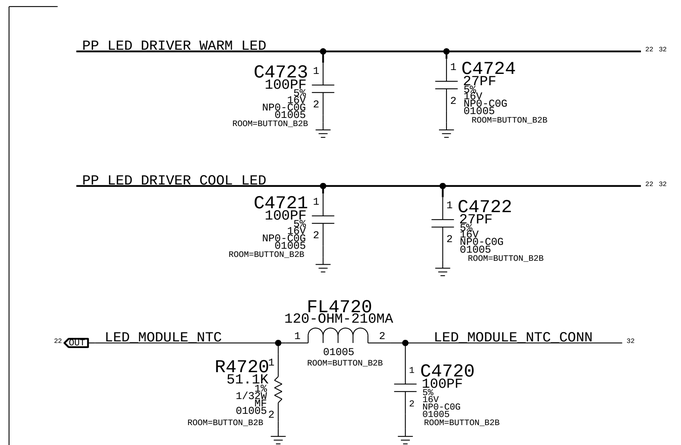


BUTTON FLEX CONNECTOR

THIS ONE ON MLB ---> 516S00058 (RCPT)
516S00059 (PLUG)



STROBE:
WARM LED
COOL LED
MODULE NTC



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PAGE TITLE
I/O:BUTTON FLEX B2B
Apple Inc.
DRAWING NUMBER 051-1902
SIZE D
REVISION A.0.0
BRANCH
PAGE 47 OF 49
SHEET 32 OF 59

BASEBAND, WLAN, BT & STOCKHOLM

I456

RADIO_MLB_MIMO

SHARED POWER

PP_VCC_MAIN
PP3V0_TRISTAR
PP1V8_SDRAM

SUBDESIGN_SUFFIX=RF

28 27 26 25 24 22 21 17 15 14 — PP_VCC_MAIN
31 30 27 19 15 — PP3V0_TRISTAR
31 30 27 24 16 15 14 12 8 — PP1V8_SDRAM

BASEBAND

6 IN	PCIE_AP_TO_BB_TXD_P	PCIE0_AP_TO_BB_TX_P
6 IN	PCIE_AP_TO_BB_TXD_N	PCIE0_AP_TO_BB_TX_N
6 OUT	PCIE_BB_TO_AP_RXD_P	PCIE0_BB_TO_AP_TX_P
6 OUT	PCIE_BB_TO_AP_RXD_N	PCIE0_BB_TO_AP_TX_N
6 IN	PCIE_AP_TO_BB_REFCLK_P	PCIE0_AP_TO_BB_REFCLK_P
6 IN	PCIE_AP_TO_BB_REFCLK_N	PCIE0_AP_TO_BB_REFCLK_N
6 IN	PCIE_AP_TO_BB_RESET_L	PCIE0_AP_TO_BB_PERST_L
6 BI	PCIE_BB_BI_AP_CLKREQ_L	PCIE0_AP_TO_BB_CLKREQ_L
16 OUT	BB_TO_PMU_PCIE_HOST_WAKE_L	PCIE0_BB_TO_PMU_HOST_WAKE_L
9 IN	AP_TO_BB_PCIE_DEV_WAKE	PCIE0_AP_TO_BB_DEV_WAKE
8 IN	I2S_AP_TO_BB_LRCLK	I2S_AP_TO_BB_WS
8 IN	I2S_AP_TO_BB_BCLK	I2S_AP_TO_BB_CLK
8 IN	I2S_AP_TO_BB_DOUT	I2S_AP_TO_BB_TX
8 OUT	I2S_BB_TO_AP_DIN	I2S_BB_TO_AP_TX
8 IN	AP_TO_BB_RADIO_ON_L	AP_TO_BBPMU_RADIO_ON_L
16 IN	PMU_TO_BB_PMIC_RESET_L	PMU_TO_BBPMU_RESET_L
8 IN	AP_TO_BB_RESET_L	AP_TO_BB_RST_L
8 OUT	BB_TO_AP_RESET_DETECT_L	BB_TO_AP_RESET_DET_L
27 22 OUT	BB_TO_LED_DRIVER_GSM_BURST_IND	BB_TO_AP_GSM_TXBURST_IND
8 IN	AP_TO_BB_MESA_UP_L	AP_TO_BB_MESA_ON_L
8 IN	BB_TO_AP_GPS_TIME_MARK	BB_TO_AP_GPS_TIME_MARK
8 IN	AP_TO_BB_COREDUMP	AP_TO_BB_COREDUMP_TRIG
8 IN	BB_IPC_GPIO	AP_TO_BB_IPC_GPIO
29 9 8 IN	LCM_TO_OWL_BSYNC	TOUCH_TO_BBPMU_FORCE_PWM
9 IN	UART_OWL_TO_BB_TXD	UART0_OWL_TO_BB_TX
9 OUT	UART_BB_TO_OWL_RXD	UART0_BB_TO_OWL_TX
30 BI	USB_BB_DATA_P	USB_BB_P
30 BI	USB_BB_DATA_N	USB_BB_N
16 IN	PMU_TO_BB_USB_VBUS_DETECT	USB_BB_VBUS_DETECT
13 9 IN	SWD_AP_PERIPHERAL_SWCLK	SWD_CLK_BB_JTAG_TCK
9 BI	SWD_AP_BI_BB_SWDIO	SWD_IO_BB_JTAG_TMS
31 OUT	RFFE5_BB_TO_ANT_SCLK	75_RFFE5_SCLK_BB
31 BI	RFFE5_BB_TO_ANT_DATA	75_RFFE5_SDATA_BB
31 OUT	BB_LAT_GPIO1	RFFE_BUFFER_LAT_GPIO1
16 OUT	BB_TO_PMU_AMUX_LDO11_SIM1	BB_TO_PMU_AMUX_LDO11_SIM1
16 OUT	BB_TO_PMU_AMUX_SMPS1	BB_TO_PMU_AMUX_SMPS1
16 OUT	BB_TO_PMU_AMUX_SMPS3	BB_TO_PMU_AMUX_SMPS3
16 OUT	BB_TO_PMU_AMUX_SMPS4	BB_TO_PMU_AMUX_SMPS4

MIS-NAMED NET. GPS_TIME_MARK ACTUALLY GOES FROM AP TO BB.

ANT

4 OUT	50_AP_UAT_FEED	50_UPPER_ANT_FEED
4 OUT	50_AP_WIFI_5G_CONN_ANT	50_WIFI_5G_CONN_ANT
4 OUT	AP_TO_STOCKHOLM_ANT	STOCKHOLM_ANT

AP DEBUG

21 20 17 14 13 12 9 8 7 6 5 3 29 IN	PP1V8	PP1V8
8 3 IN	DFU_STATUS	DFU_STATUS
8 3 OUT	FORCE_DFU	FORCE_DFU
	NC_PMU_AMUX_AY	PMU_AMUX_AY
	NC_PMU_AMUX_BY	PMU_AMUX_BY
16 9 5 3 OUT	PMU_TO_SYSTEM_COLD_RESET_L	PMU_TO_SYSTEM_COLD_RESET_L
27 16 9 BI	I2C0_AP_SCL	I2C0_AP_SCL
27 16 9 BI	I2C0_AP_SDA	I2C0_AP_SDA
30 26 25 17 9 BI	I2C1_AP_SCL	I2C1_AP_SCL
30 26 25 17 9 BI	I2C1_AP_SDA	I2C1_AP_SDA
32 16 9 8 OUT	BUTTON_HOLD_KEY_L	BUTTON_HOLD_KEY_L
28 16 9 8 OUT	BUTTON_MENU_KEY_L	BUTTON_MENU_KEY_L
32 16 8 OUT	BUTTON_RINGER_A	BUTTON_RINGER_A
32 16 8 OUT	BUTTON_VOL_DOWN_L	BUTTON_VOL_DOWN_L
32 16 8 OUT	BUTTON_VOL_UP_L	BUTTON_VOL_UP_L
	NC_PMU_GPIO20	PMU_GPIO20
	NC_PMU_GPIO21	PMU_GPIO21
30 8 IN	UART_AP_DEBUG_TXD	AP_RESERVED0
30 8 OUT	UART_AP_DEBUG_RXD	AP_RESERVED1
	NC_AP_RESERVED2	AP_RESERVED2

WLAN

PCIE_AP_TO_WLAN_TX_P	PCIE_AP_TO_WLAN_TXD_P	IN 6
PCIE_AP_TO_WLAN_TX_N	PCIE_AP_TO_WLAN_TXD_N	IN 6
PCIE_WLAN_TO_AP_TX_P	PCIE_WLAN_TO_AP_RXD_P	OUT 6
PCIE_WLAN_TO_AP_TX_N	PCIE_WLAN_TO_AP_RXD_N	OUT 6
PCIE_AP_TO_WLAN_REFCLK_P	PCIE_AP_TO_WLAN_REFCLK_P	IN 6
PCIE_AP_TO_WLAN_REFCLK_N	PCIE_AP_TO_WLAN_REFCLK_N	IN 6
PCIE_AP_TO_WLAN_PERST_L	PCIE_AP_TO_WLAN_RESET_L	IN 6
PCIE_AP_TO_WLAN_DEV_WAKE	PCIE_AP_TO_WLAN_DEV_WAKE	IN 8
PCIE_WLAN_TO_AP_CLKREQ_L	PCIE_WLAN_TO_AP_CLKREQ_L	BI 6
UART4_AP_TO_WLAN_TX	UART_AP_TO_WLAN_TXD	IN 8
UART4_AP_TO_WLAN_RTS_L	UART_AP_TO_WLAN_RTS_L	IN 8
UART4_WLAN_TO_AP_TX	UART_WLAN_TO_AP_RXD	OUT 8
UART4_WLAN_TO_AP_RTS_L	UART_WLAN_TO_AP_CTS_L	OUT 8
PMU_TO_WLAN_32K_CLK	PMU_TO_WLAN_CLK32K	IN 16
PMU_TO_WLAN_REG_ON	PMU_TO_WLAN_REG_ON	IN 16
WLAN_TO_PMU_HOST_WAKE	WLAN_TO_PMU_HOST_WAKE	OUT 16
OWL_TO_WLAN_CONTEXT_A	OWL_TO_WLAN_CONTEXT_A	IN 9
OWL_TO_WLAN_CONTEXT_B	OWL_TO_WLAN_CONTEXT_B	IN 9

BLUETOOTH

I2S_AP_TO_BT_LRCK	I2S_AP_TO_BT_LRCLK	IN 8
I2S_AP_TO_BT_BCLK	I2S_AP_TO_BT_BCLK	IN 8
I2S_AP_TO_BT_DOUT	I2S_AP_TO_BT_DOUT	IN 8
I2S_BT_TO_AP_DOUT	I2S_BT_TO_AP_DIN	OUT 8
UART1_AP_TO_BT_TX	UART_AP_TO_BT_TXD	IN 8
UART1_AP_TO_BT_RTS_L	UART_AP_TO_BT_RTS_L	IN 8
UART1_BT_TO_AP_TX	UART_BT_TO_AP_RXD	OUT 8
UART1_BT_TO_AP_RTS_L	UART_BT_TO_AP_CTS_L	OUT 8
PMU_TO_BT_REG_ON	PMU_TO_BT_REG_ON	IN 16
BT_TO_PMU_HOST_WAKE	BT_TO_PMU_HOST_WAKE	OUT 16
AP_TO_BT_WAKE	AP_TO_BT_WAKE	IN 8

STOCKHOLM

UART3_AP_TO_STOCKHOLM_TXD	UART_AP_TO_STOCKHOLM_TXD	IN 8
UART3_AP_TO_STOCKHOLM_RTS_L	UART_AP_TO_STOCKHOLM_RTS_L	IN 8
UART3_STOCKHOLM_TO_AP_TXD	UART_STOCKHOLM_TO_AP_RXD	OUT 8
UART3_STOCKHOLM_TO_AP_RTS_L	UART_STOCKHOLM_TO_AP_CTS_L	OUT 8
PMU_TO_STOCKHOLM_EN	PMU_TO_STOCKHOLM_EN	IN 16
STOCKHOLM_TO_PMU_HOST_WAKE	STOCKHOLM_TO_PMU_HOST_WAKE	OUT 16
AP_TO_STOCKHOLM_DEV_WAKE	AP_TO_STOCKHOLM_DEV_WAKE	IN 8
AP_TO_STOCKHOLM_FW_DWLD_REQ	AP_TO_STOCKHOLM_DWLD_REQUEST	IN 7

PAGE TITLE
BASEBAND:RADIO SYMBOL

Apple Inc.

DRAWING NUMBER 051-1902
SIZE D
REVISION A.0.0
BRANCH
PAGE 49 OF 49
SHEET 33 OF 59

1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

REV	ECN	DESCRIPTION OF REVISION	CK APPD / DATE
A	0004536627	PRODUCTION RELEASED	2015-07-21

N71 RADIO_MLB_MIMO - PVT
JULY 07, 2015

PDF PAGE	CSA PAGE	CONTENTS
2	2	ELNA & UAT ANT FEED
3	3	FE: ANT CONNECTORS AND UAT TUNER
4	30	DEBUG CONN & TEST POINTS
5	31	CELLULAR BASEBAND: POWER1
6	32	CELLULAR BASEBAND: POWER2
7	33	CELLULAR BASEBAND: CONTROL AND INTERFACES
8	34	CELLULAR BASEBAND: GPIOS
9	35	CELLULAR PMU: CONTROL AND CLOCKS
10	36	CELLULAR PMU: SWITCHERS AND LDOS
11	37	CELLULAR PMU: ET MODULATOR
12	38	CELLULAR TRANSCEIVER: POWER
13	39	CELLULAR TRANSCEIVER: PRX PORTS
14	40	CELLULAR TRANSCEIVER: DRX/GPS PORTS
15	41	CELLULAR TRANSCEIVER: TX PORTS
16	42	CELLULAR FRONT END: LB PAD
17	43	CELLULAR FRONT END: MB PAD
18	44	CELLULAR FRONT END: HB PAD
19	45	CELLULAR FRONT END: 2G PA
20	46	CELLULAR FRONT END: LB ASM
21	47	CELLULAR FRONT END: MB-HB ASM
22	48	CELLULAR FRONT END: DIVERSITY
23	49	SIM
24	50	WIFI/BT: WIFI/BT MODULE
25	51	STOCKHOLM

ROW/RF2 HB PAD MATCHING BOM OPTIONS

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
152S1907	1	3.3NH, INDUCTOR	L4105_RF	ROW
152S1990	1	3.0NH, INDUCTOR	L4105_RF	RF2
131S0377	1	1.2PF, CAPACITOR	C4108_RF	RF2
152S2007	1	8.2NH, INDUCTOR	L4401_RF	ROW
131S0426	1	22PF, CAPACITOR	C4405_RF	ROW
152S2001	1	2.4NH, INDUCTOR	C4405_RF	RF2
131S0631	1	0.3PF, CAPACITOR	L4406_RF	RF2
152S2044	1	2.2NH, INDUCTOR	C4406_RF	ROW
152S2021	1	1.5NH, INDUCTOR	C4406_RF	RF2
131S0631	1	0.3PF, CAPACITOR	L4407_RF	ROW
152S2056	1	5.6NH, INDUCTOR	L4403_RF	ROW
131S0429	1	8.2PF, CAPACITOR	C4407_RF	ROW
152S2036	1	2.5NH, INDUCTOR	C4407_RF	RF2
131S0631	1	0.3PF, CAPACITOR	L4408_RF	RF2
152S00143	1	15NH, INDUCTOR	L4404_RF	ROW
131S0823	1	33PF, CAPACITOR	C4408_RF	ROW
152S2051	1	1.3NH, INDUCTOR	L4408_RF	RF2
152S2042	1	1.8NH, INDUCTOR	C4409_RF	RF2
117S0108	1	51 OHM, RESISTOR	L4410_RF	ROW
131S0363	1	0.6PF, CAPACITOR	L4410_RF	RF2
152S00052	1	3.4NH, INDUCTOR	L3910_RF	ROW
152S00026	1	3.5NH, INDUCTOR	L3910_RF	RF2
152S2039	1	3.8NH, INDUCTOR	L3911_RF	ROW
117S0201	1	0 OHM, RESISTOR	L3911_RF	RF2
131S0279	1	1.3PF, CAPACITOR	L3919_RF	ROW
152S2045	1	3.0NH, INDUCTOR	L3919_RF	RF2
152S00052	1	3.4NH, INDUCTOR	L3912_RF	RF2
131S0599	1	1.5PF, CAPACITOR	C3922_RF	RF2
131S0630	1	27PF, CAPACITOR	C3911_RF	RF2

LB PAD

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
353S00461	1	IC,PWR AMP,LB_PAD,SKWS	ULBPA_RF	ROW
353S00461	1	IC,PWR AMP,LB_PAD,SKWS	ULBPA_RF	RF2
353S00461	1	IC,PWR AMP,LB_PAD,SKWS	ULBPA_RF	RFC
353S00541	1	IC,PWR AMP,LB_PAD,PT	ULBPA_RF	DARWIN

MB PAD

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
353S4495	1	IC,PWR AMP,MB_PAD	UMBPA_RF	ROW
353S4495	1	IC,PWR AMP,MB_PAD	UMBPA_RF	RF2
353S4495	1	IC,PWR AMP,MB_PAD	UMBPA_RF	RFC
353S00477	1	IC,PWR AMP,MB_PAD, PT	UMBPA_RF	DARWIN

RFC HB PAD MATCHING BOM OPTIONS

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
152S1907	1	3.3NH, INDUCTOR	L4105_RF	RFC
152S2007	1	8.2NH, INDUCTOR	L4401_RF	RFC
131S0426	1	22PF, CAPACITOR	C4405_RF	RFC
152S2044	1	2.2NH, INDUCTOR	C4406_RF	RFC
131S0631	1	0.3PF, CAPACITOR	L4407_RF	RFC
152S2056	1	5.6NH, INDUCTOR	L4403_RF	RFC
131S0429	1	8.2PF, CAPACITOR	C4407_RF	RFC
152S00143	1	15NH, INDUCTOR	L4404_RF	RFC
131S0823	1	33PF, CAPACITOR	C4408_RF	RFC
117S0108	1	51 OHM, RESISTOR	L4410_RF	RFC
152S00052	1	3.4NH, INDUCTOR	L3910_RF	RFC
152S2039	1	3.8NH, INDUCTOR	L3911_RF	RFC
131S0279	1	1.3PF, CAPACITOR	L3919_RF	RFC

DARWIN HB PAD MATCHING BOM OPTIONS

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
152S1907	1	3.3NH, INDUCTOR	L4105_RF	DARWIN
152S2007	1	8.2NH, INDUCTOR	L4401_RF	DARWIN
131S0426	1	22PF, CAPACITOR	C4405_RF	DARWIN
152S2044	1	2.2NH, INDUCTOR	C4406_RF	DARWIN
131S0631	1	0.3PF, CAPACITOR	L4407_RF	DARWIN
152S2056	1	5.6NH, INDUCTOR	L4403_RF	DARWIN
131S0429	1	8.2PF, CAPACITOR	C4407_RF	DARWIN
152S00143	1	15NH, INDUCTOR	L4404_RF	DARWIN
131S0823	1	33PF, CAPACITOR	C4408_RF	DARWIN
117S0108	1	51 OHM, RESISTOR	L4410_RF	DARWIN
152S00052	1	3.4NH, INDUCTOR	L3910_RF	DARWIN
152S2039	1	3.8NH, INDUCTOR	L3911_RF	DARWIN
131S0279	1	1.3PF, CAPACITOR	L3919_RF	DARWIN

LAT DIPLEXER1

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
155S0971	1	LAT CELL DIPLEXER1,TDK	FLDIP_RF	ROW
155S0971	1	LAT CELL DIPLEXER1,TDK	FLDIP_RF	RF2
155S0971	1	LAT CELL DIPLEXER1,TDK	FLDIP_RF	RFC
155S0971	1	LAT CELL DIPLEXER1,TDK	FLDIP_RF	DARWIN

HB PAD

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
353S00376	1	IC,PWR AMP,HB_PAD,TQS	UHBPA_RF	ROW
353S4494	1	IC,PWR AMP,HB_PAD,AVAGO	UHBPA_RF	RF2
353S00376	1	IC,PWR AMP,HB_PAD,TQS	UHBPA_RF	RFC
353S00478	1	IC,PWR AMP,HB_PAD,PT	UHBPA_RF	DARWIN

19.2MHZ XTAL ALTERNATE

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
197S0565	197S0593	ALTERNATE	Y_XO_RF	XTAL, 19.2MHZ
197S0598	197S0593	ALTERNATE	Y_XO_RF	XTAL, 19.2MHZ

VINYL

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
337S00176	1	IC, VINYL	U5101_RF	ROW
337S00176	1	IC, VINYL	U5101_RF	RF2

VINYL RESISTOR

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
117S0161	1	0 OHM, RESISTOR	R3402_RF	RFC
117S0161	1	0 OHM, RESISTOR	R3402_RF	DARWIN

HW_REV1_ID RESISTOR

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
118S0646	1	51.1 KOHM, RESISTOR	R3503_RF	DARWIN

SIM ESD DIODE ALTERNATE

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
377S00042	377S0163	ALTERNATE	VR301_RF	ON SEMI ESD DIODE

?

DRAWING TITLE: SCHEM,SINGLE,BRD,N71

Apple Inc.

DRAWING NUMBER: 051-1902 | SIZE: D

REVISION: A.0.0

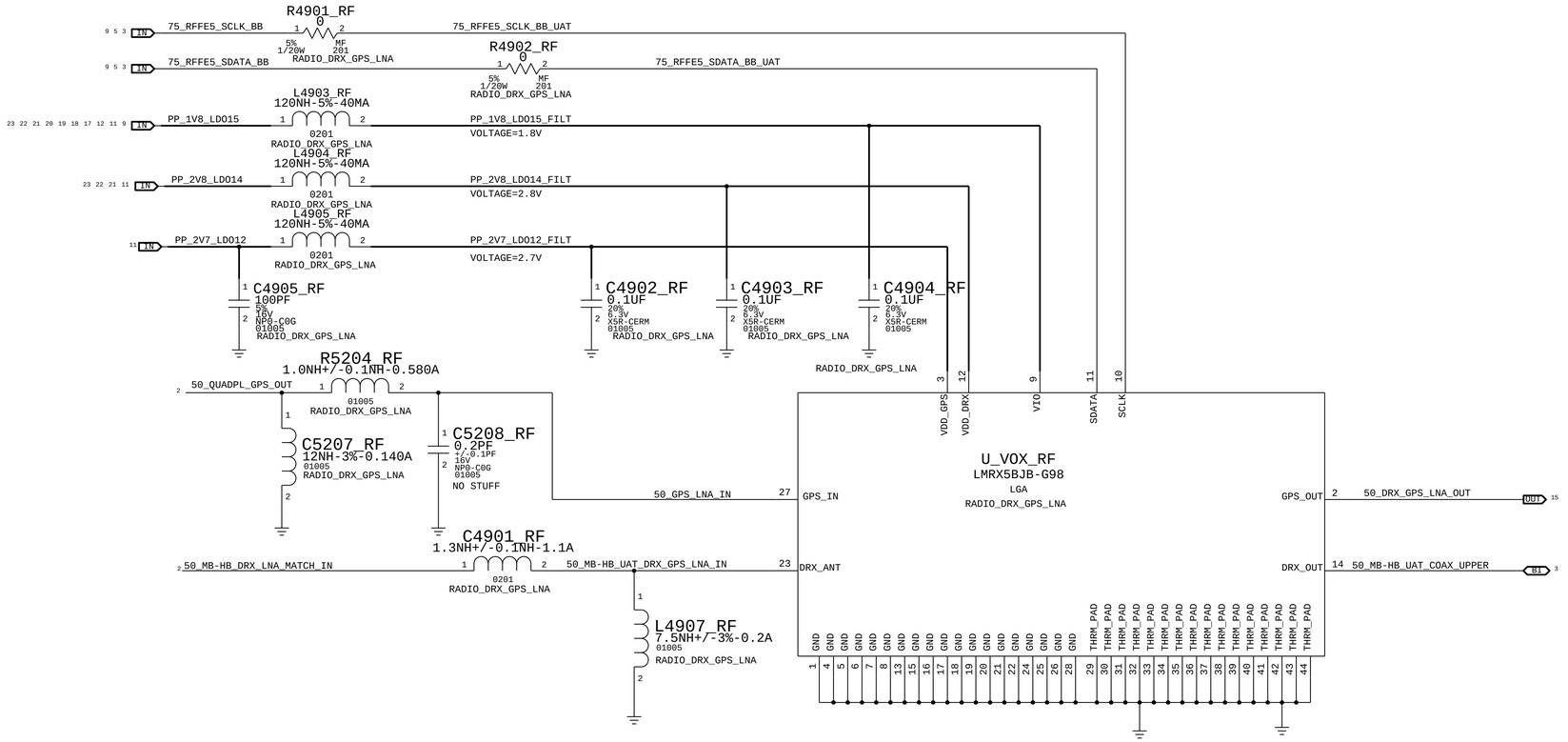
BRANCH:

PAGE: 1 OF 51

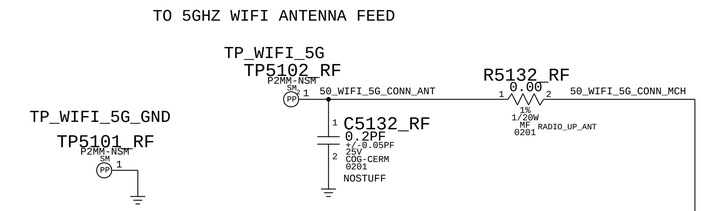
SHEET: 34 OF 59

N71-SPECIFIC RADIO PAGE 2

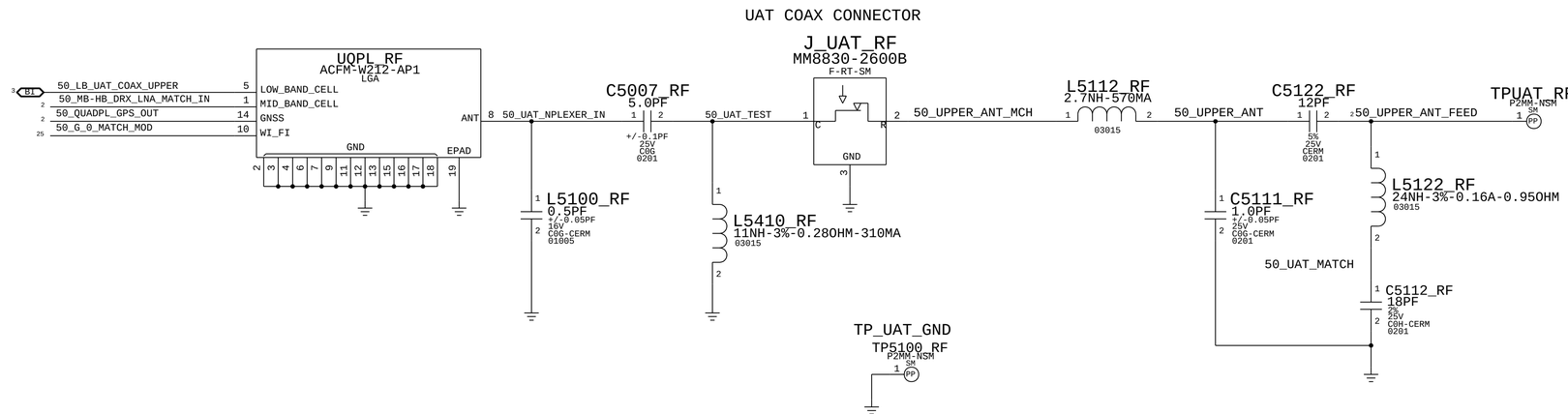
DIVERSITY LNA



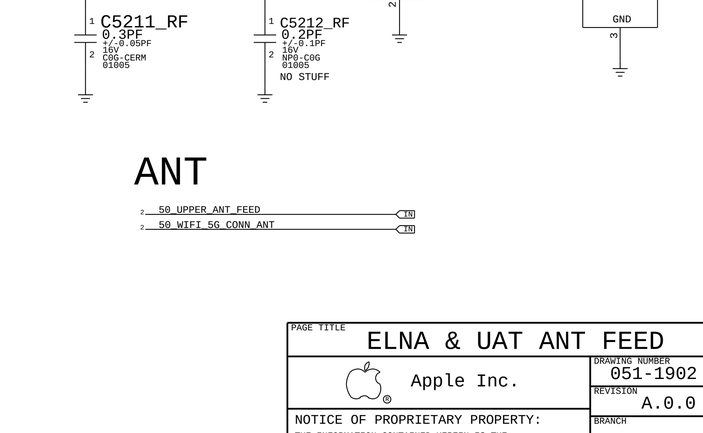
WIFI ANT FEED



UAT ANT FEED



ANT



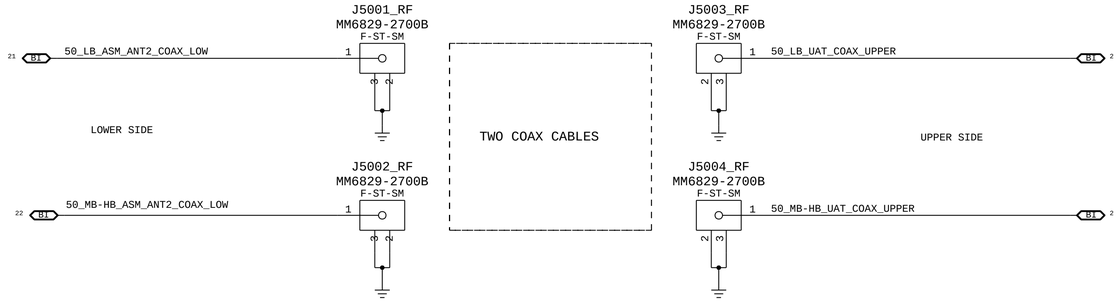
PAGE TITLE
ELNA & UAT ANT FEED

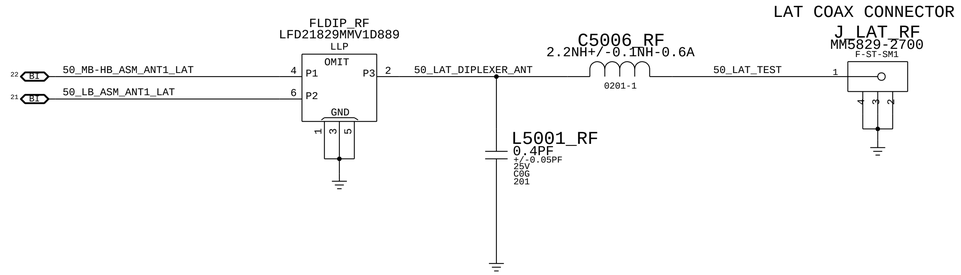
Apple Inc.

DRAWING NUMBER 051-1902 | SIZE D
REVISION A.0.0
BRANCH
PAGE 2 OF 51
SHEET 35 OF 59

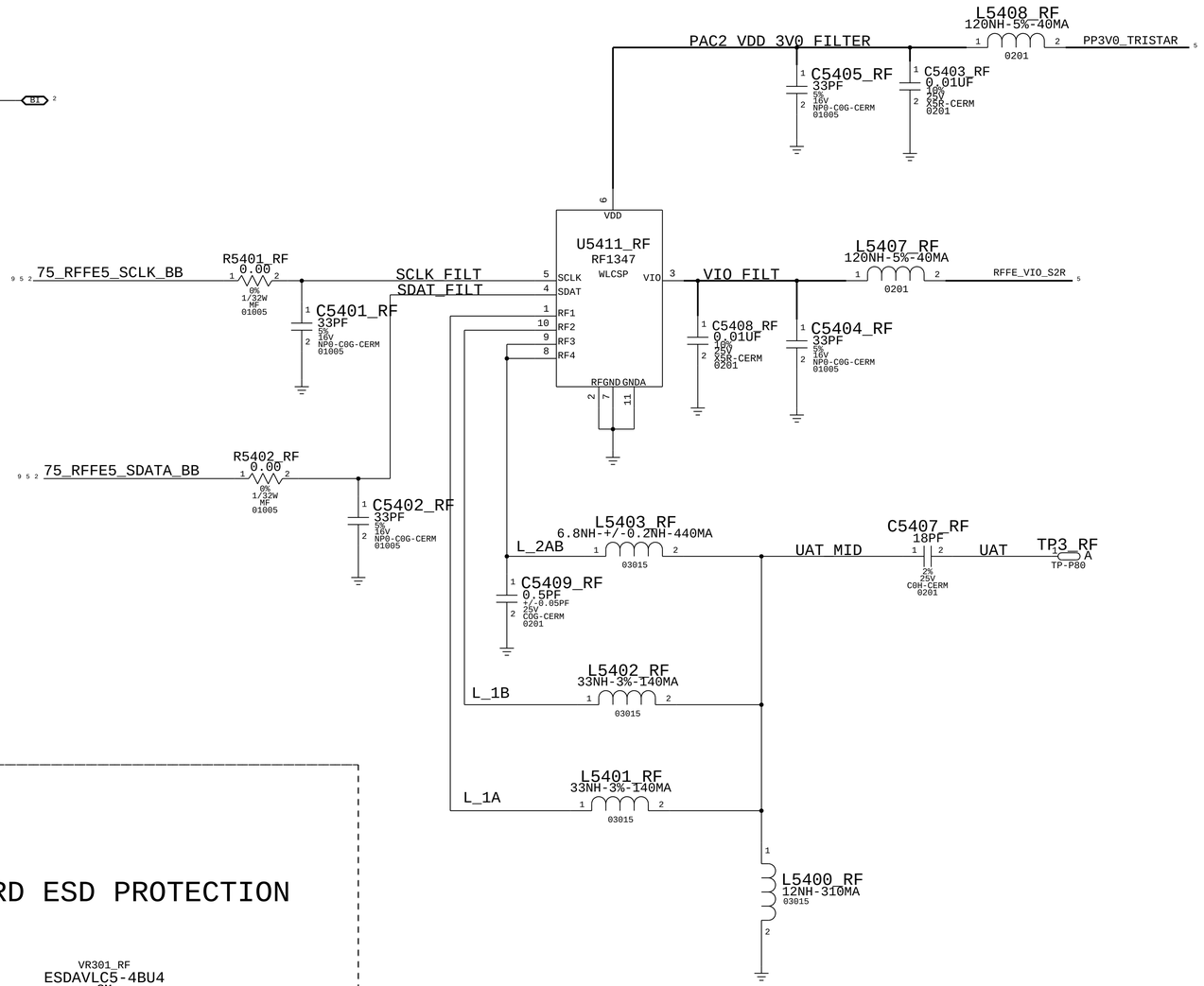
N71-SPECIFIC RADIO PAGE 3

ANTENNA FEEDS AND CONNECTORS

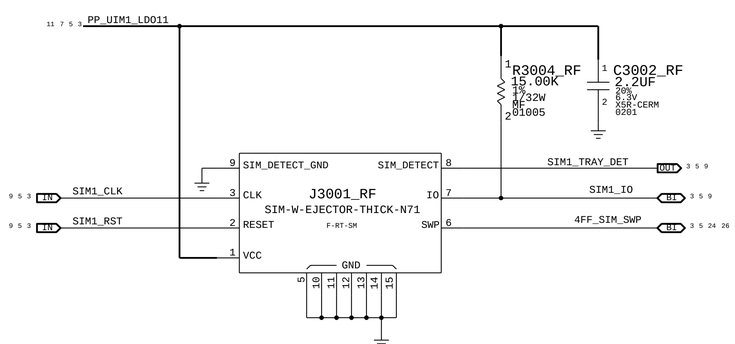




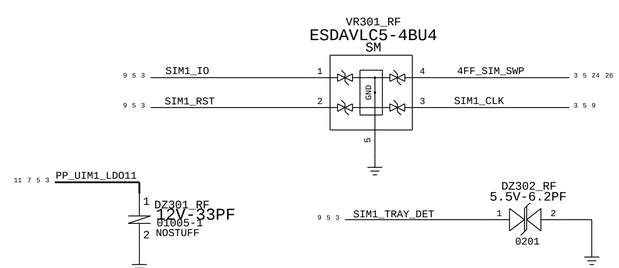
UAT TUNER



SIM CARD CONNECTOR



SIM CARD ESD PROTECTION



PAGE TITLE
FE: ANT CONNECTORS AND UAT TUNER

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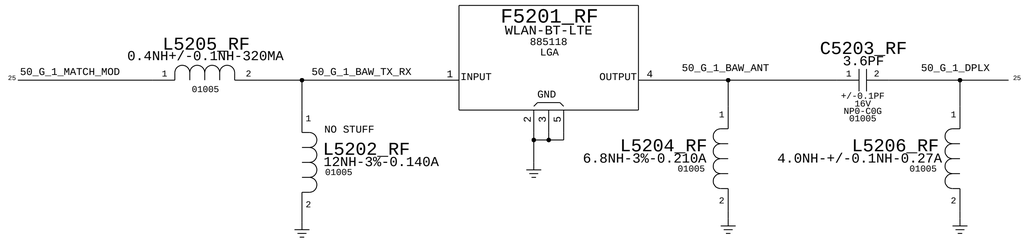
DRAWING NUMBER 051-1902 | SIZE D
REVISION A.0.0
BRANCH
PAGE 3 OF 51
SHEET 36 OF 59

N71-SPECIFIC RADIO PAGE 4

WLAN LAT 2.4GHZ BAW BPF



PAGE TITLE: WLAN LAT 2.4GHZ BAW BPF

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DRAWING NUMBER: 051-1902 | SIZE: D

REVISION: A.0.0

BRANCH:

PAGE: 4 OF 51

SHEET: 37 OF 59

AP TO BB/WLAN/BT/SH CONNECTIONS

BASEBAND

PP_VCC_MAIN
AP_TO_BBPMU_RADIO_ON_L
PMU_TO_BBPMU_RESET_L
AP_TO_BB_RST_L
BB_TO_AP_RESET_DET_L
BB_TO_AP_GSM_TXBURST_IND
AP_TO_BB_MESA_ON_L
BB_TO_AP_GPS_TIME_MARK
AP_TO_BB_COREDUMP_TRIG
AP_TO_BB_IPC_GPIO
TOUCH_TO_BBPMU_FORCE_PWM

UART0_BB_TO_OWL_TX
UART0_OWL_TO_BB_TX

PCIE0_AP_TO_BB_REFCLK_P
PCIE0_AP_TO_BB_REFCLK_N

PCIE0_AP_TO_BB_TX_P
PCIE0_AP_TO_BB_TX_N

PCIE0_BB_TO_AP_TX_P
PCIE0_BB_TO_AP_TX_N

PCIE0_AP_TO_BB_PERST_L
PCIE0_AP_TO_BB_CLKREQ_L
PCIE0_BB_TO_PMU_HOST_WAKE_L
PCIE0_AP_TO_BB_DEV_WAKE

I2S_AP_TO_BB_WS
I2S_AP_TO_BB_CLK
I2S_AP_TO_BB_TX
I2S_BB_TO_AP_TX

USB_BB_P
USB_BB_N
USB_BB_VBUS_DETECT

SWD_CLK_BB_JTAG_TCK
SWD_IO_BB_JTAG_TMS

RFFE_BUFFER_LAT_GPIO1
75_RFFE5_SDATA_BB
75_RFFE5_SCLK_BB
PP3V0_TRISTAR

BB_TO_PMU_AMUX_SMPS1
BB_TO_PMU_AMUX_SMPS3
BB_TO_PMU_AMUX_SMPS4
BB_TO_PMU_AMUX_LDO11_SIM1

SINGLE_NODENET

WLAN/BT

PMU_TO_WLAN_32K_CLK
PMU_TO_WLAN_REG_ON
PMU_TO_BT_REG_ON
WLAN_TO_PMU_HOST_WAKE
BT_TO_PMU_HOST_WAKE
AP_TO_BT_WAKE

UART1_AP_TO_BT_TX
UART1_BT_TO_AP_TX
UART1_AP_TO_BT_RTS_L
UART1_BT_TO_AP_RTS_L

I2S_AP_TO_BT_BCLK
I2S_AP_TO_BT_LRCK
I2S_BT_TO_AP_DOUT
I2S_AP_TO_BT_DOUT

UART4_AP_TO_WLAN_TX
UART4_WLAN_TO_AP_TX
UART4_WLAN_TO_AP_RTS_L
UART4_AP_TO_WLAN_RTS_L

PCIE_WLAN_TO_AP_CLKREQ_L
PCIE_AP_TO_WLAN_PERST_L
PCIE_AP_TO_WLAN_DEV_WAKE
PCIE_AP_TO_WLAN_TX_P
PCIE_AP_TO_WLAN_TX_N
PCIE_AP_TO_WLAN_REFCLK_P
PCIE_AP_TO_WLAN_REFCLK_N
PCIE_WLAN_TO_AP_TX_P
PCIE_WLAN_TO_AP_TX_N

OWL_TO_WLAN_CONTEXT_A
OWL_TO_WLAN_CONTEXT_B

AP DEBUG

PP1V8
FORCE_DFU
DFU_STATUS
PMU_AMUX_AY
PMU_AMUX_BY
PMU_TO_SYSTEM_COLD_RESET_L
I2C0_AP_SDA
I2C0_AP_SCL
I2C1_AP_SDA
I2C1_AP_SCL
BUTTON_HOLD_KEY_L
BUTTON_MENU_KEY_L
BUTTON_VOL_DOWN_L
BUTTON_VOL_UP_L
BUTTON_RINGER_A
PMU_GPIO20
PMU_GPIO21

AP_RESERVED0
AP_RESERVED1
AP_RESERVED2

STOCKHOLM

PP1V8_SDRAM
AP_TO_STOCKHOLM_SIM_SEL
STOCKHOLM_TO_PMU_HOST_WAKE
AP_TO_STOCKHOLM_FW_DWLD_REQ
PMU_TO_STOCKHOLM_EN
AP_TO_STOCKHOLM_DEV_WAKE
UART3_AP_TO_STOCKHOLM_TXD
UART3_STOCKHOLM_TO_AP_TXD
UART3_AP_TO_STOCKHOLM_RTS_L
UART3_STOCKHOLM_TO_AP_RTS_L

ANT

STOCKHOLM_ANT

POWER

PP1V8_SDRAM
VOLTAGE=1.8V
MAKE_BASE=TRUE
PP_1V8_S2R_VDDIO_WLAN_BT VOLTAGE=1.8V
PP_STOCKHOLM_1V8_S2R VOLTAGE=1.8V
RFFE_VIO_S2R VOLTAGE=1.8V

MLB PROBE POINTS

PCIE

PP3073_RF P2MM-NSM SM PP 1 PCIE0_AP_TO_BB_PERST_L 5 9 OMIT
PP3074_RF P2MM-NSM SM PP 1 PCIE0_BB_TO_PMU_HOST_WAKE_L 5 9 OMIT RADIO_DEBUG
PP3075_RF P2MM-NSM SM PP 1 PCIE0_AP_TO_BB_CLKREQ_L 5 9 OMIT
PP3076_RF P2MM-NSM SM PP 1 PCIE0_AP_TO_BB_DEV_WAKE 5 9 OMIT RADIO_DEBUG
PP3080_RF P2MM-NSM SM PP 1 PCIE0_AP_TO_BB_REFCLK_P 5 8 OMIT RADIO_DEBUG
PP3081_RF P2MM-NSM SM PP 1 PCIE0_AP_TO_BB_REFCLK_N 5 8 OMIT RADIO_DEBUG
PP3084_RF P2MM-NSM SM PP 1 PCIE0_AP_TO_BB_TX_P 5 8 OMIT RADIO_DEBUG
PP3085_RF P2MM-NSM SM PP 1 PCIE0_AP_TO_BB_TX_N 5 8 OMIT RADIO_DEBUG
PP3090_RF P2MM-NSM SM PP 1 BB_JTAG_SRST_L 8 OMIT RADIO_DEBUG
PP3091_RF P2MM-NSM SM PP 1 SWD_IO_BB_JTAG_TMS 5 8 OMIT RADIO_DEBUG

PMU

PP3032_RF P2MM-NSM SM PP 1 PMIC_RESOUT_L 8 10 OMIT
PP3033_RF P2MM-NSM SM PP 1 50_SLEEP_CLK_32K 8 10 OMIT
PP3034_RF P2MM-NSM SM PP 1 XO_OUT_D0_EN 8 10 OMIT
PP3036_RF P2MM-NSM SM PP 1 SPMI_CLK 8 10 OMIT RADIO_DEBUG
PP3037_RF P2MM-NSM SM PP 1 SPMI_DATA 8 10 OMIT RADIO_DEBUG

BASEBAND

PP3017_RF P2MM-NSM SM PP 1 BB_DEBUG_ERROR 9 OMIT
PP3018_RF P2MM-NSM SM PP 1 50_MDM_PCIE_CLK 8 10 OMIT
PP3019_RF P2MM-NSM SM PP 1 50_BBPMU_TO_STOCKHOLM_19P2M_CLK 10 26 OMIT
PP3006_RF P2MM-NSM SM PP 1 STOCKHOLM_TO_BBPMU_CLK_REQ 10 26 OMIT

PP3008_RF P2MM-NSM SM PP 1 I2S_AP_TO_BB_WS 5 9 OMIT RADIO_DEBUG
PP3009_RF P2MM-NSM SM PP 1 I2S_AP_TO_BB_CLK 5 9 OMIT RADIO_DEBUG
PP3010_RF P2MM-NSM SM PP 1 I2S_AP_TO_BB_TX 5 9 OMIT RADIO_DEBUG
PP3011_RF P2MM-NSM SM PP 1 I2S_BB_TO_AP_TX 5 9 OMIT RADIO_DEBUG
PP3012_RF P2MM-NSM SM PP 1 AP_TO_BB_MESA_ON_L 5 9 OMIT RADIO_DEBUG
PP3013_RF P2MM-NSM SM PP 1 BB_TO_AP_GSM_TXBURST_IND 5 9 OMIT RADIO_DEBUG
PP3014_RF P2MM-NSM SM PP 1 BB_TO_AP_GPS_TIME_MARK 5 9 OMIT RADIO_DEBUG

PP3016_RF P2MM-NSM SM PP 1 UART0_BB_TO_OWL_TX 5 9 OMIT RADIO_DEBUG
PP3020_RF P2MM-NSM SM PP 1 UART0_OWL_TO_BB_TX 5 9 OMIT RADIO_DEBUG

ANT TUNER

PP3001_RF P2MM-NSM SM PP 1 75_RFFE5_SDATA_BB 2 3 5 9 OMIT RADIO_DEBUG
PP3002_RF P2MM-NSM SM PP 1 75_RFFE5_SCLK_BB 2 3 5 9 OMIT RADIO_DEBUG

RFFE

PP3056_RF P2MM-NSM SM PP 1 75_RFFE1_SDATA_BB 9 16 OMIT RADIO_DEBUG
PP3077_RF P2MM-NSM SM PP 1 75_RFFE4_SDATA_BB 9 12 OMIT RADIO_DEBUG
PP3051_RF P2MM-NSM SM PP 1 75_RFFE5_SCLK_BB_BUFFER 9 OMIT RADIO_DEBUG
PP3052_RF P2MM-NSM SM PP 1 75_RFFE5_SDATA_BB_BUFFER 9 OMIT
PP3053_RF P2MM-NSM SM PP 1 75_RFFE2_SDATA_BB 9 17 18 19 20 21 22 OMIT RADIO_DEBUG
PP3054_RF P2MM-NSM SM PP 1 75_RFFE3_SDATA_BB 9 23 OMIT

STOCKHOLM

PP3062_RF P2MM-NSM SM PP 1 STOCKHOLM_DWPM_DBG 26 OMIT
PP3063_RF P2MM-NSM SM PP 1 STOCKHOLM_DWPS_DBG 26 OMIT
PP3064_RF P2MM-NSM SM PP 1 UART3_AP_TO_STOCKHOLM_TXD 5 26 OMIT
PP3065_RF P2MM-NSM SM PP 1 UART3_STOCKHOLM_TO_AP_TXD 5 26 OMIT
PP3066_RF P2MM-NSM SM PP 1 UART3_AP_TO_STOCKHOLM_RTS_L 5 26 OMIT
PP3067_RF P2MM-NSM SM PP 1 UART3_STOCKHOLM_TO_AP_RTS_L 5 26 OMIT

DEBUG CONNECTOR

ESD CAPS

PMU_TO_BBPMU_RESET_L
SIM2_RESET
C5101_RF 100PF 20% 16V X5R 01005
C3503_RF 100PF 20% 16V X5R 01005

NOSTUFF
J3000_RF
AXE550124
F-ST-SM

		SIM1_CLK	3 9
		SIM1_RST	3 9
25 9	UART_WLAN_TO_BB_COEX_TX	SIM1_IO	3 9
5	I2C0_AP_SDA	PP_UIM1_LDO11	3 7 11
5	I2C0_AP_SCL	SIM1_TRAY_DET	3 9
5	BUTTON_VOL_DOWN_L	4FF_SIM_SWP	3 24 26
5	BUTTON_VOL_UP_L	I2C1_AP_SDA	5
5	BUTTON_RINGER_A	I2C1_AP_SCL	5
24 9 5	SIM2_RESET	BUTTON_HOLD_KEY_L	5
24 9	SIM2_DATA	BUTTON_MENU_KEY_L	5
25 9	UART_BB_TO_WLAN_COEX_TX	PP1V8	5
9	SIM2_DETECT	FORCE_DFU	5
24	SIM2_DATA_R	SIM2_CLK	9 24
		PP_UIM2_LDO13	7 11 24

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PAGE TITLE: DEBUG CONN & TEST POINTS

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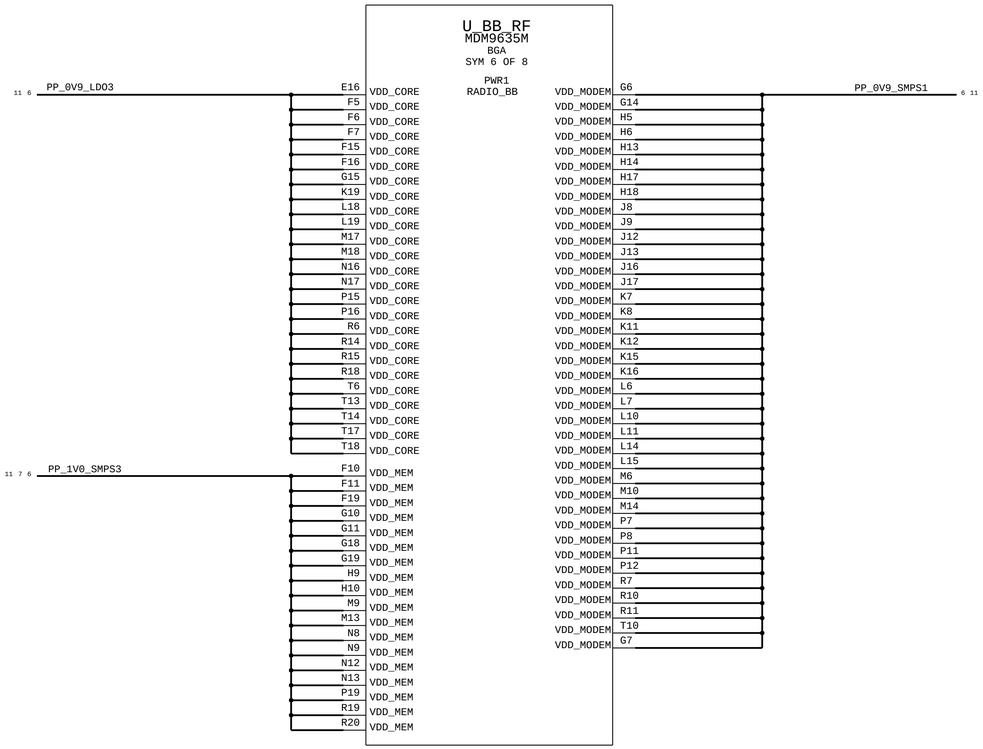
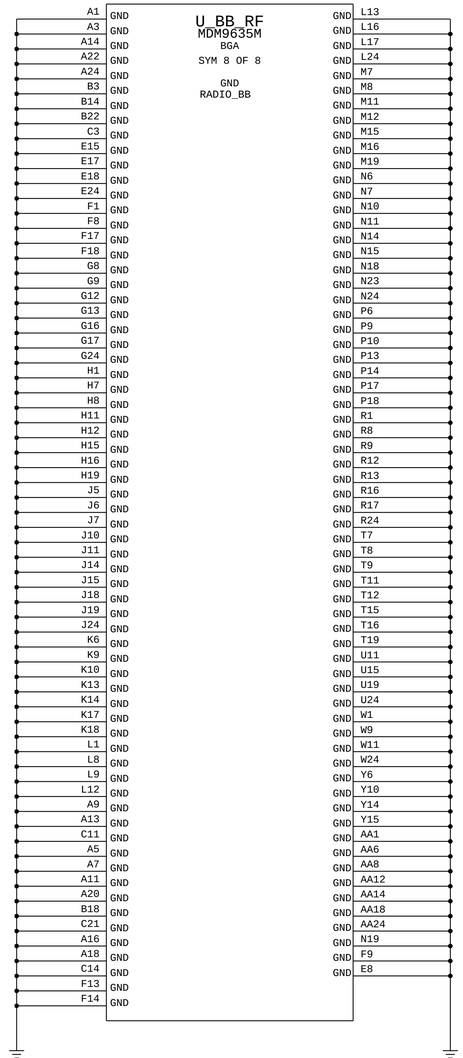
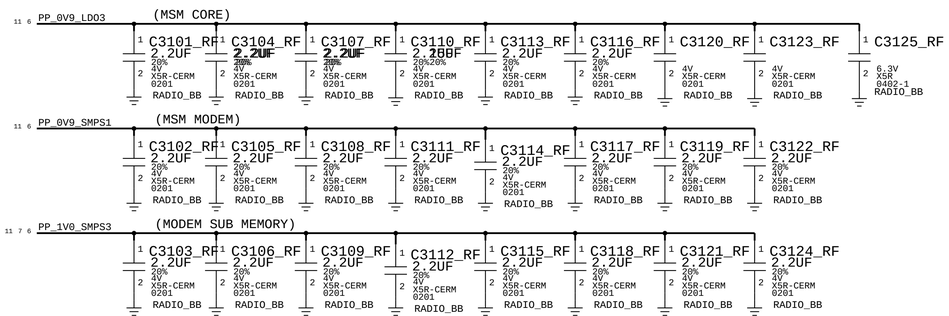
DRAWING NUMBER: 051-1902
SIZE: D
REVISION: A.0.0
BRANCH:
PAGE: 30 OF 51
SHEET: 38 OF 59

BASEBAND: POWER 1





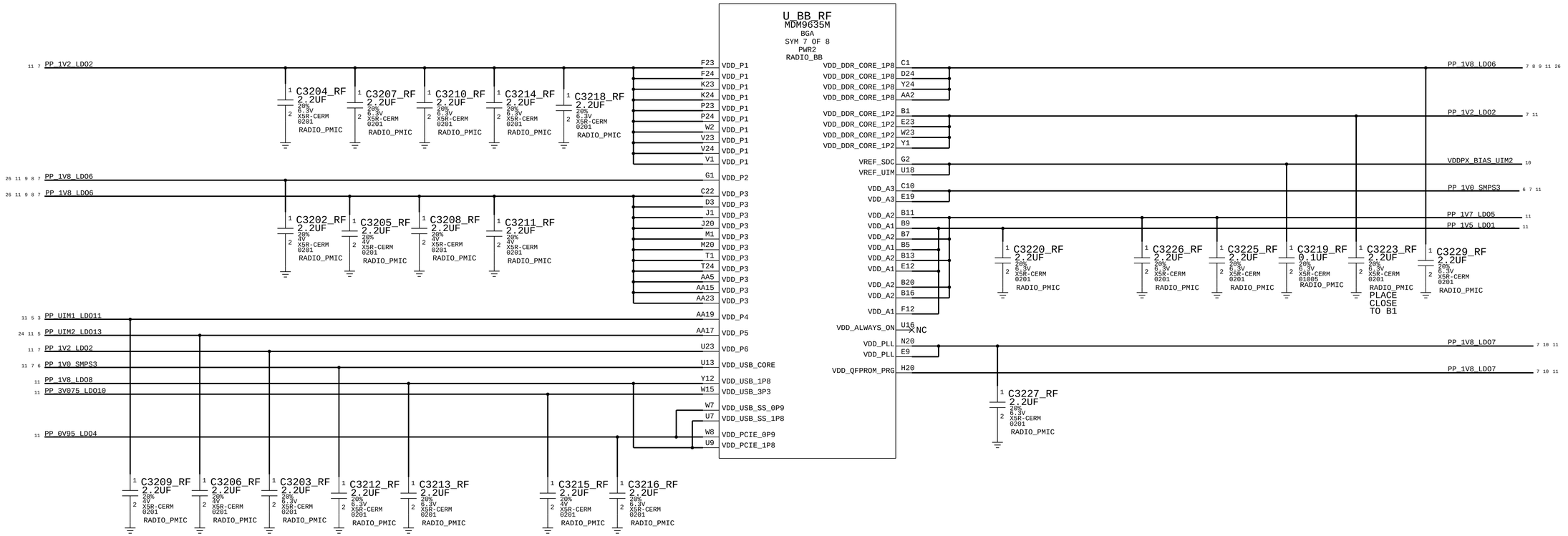


PAGE TITLE
CELLULAR BASEBAND: POWER1

Apple Inc.

DRAWING NUMBER 051-1902
SIZE D
REVISION A.0.0
BRANCH
PAGE 31 OF 51
SHEET 39 OF 59

BASEBAND: POWER 2

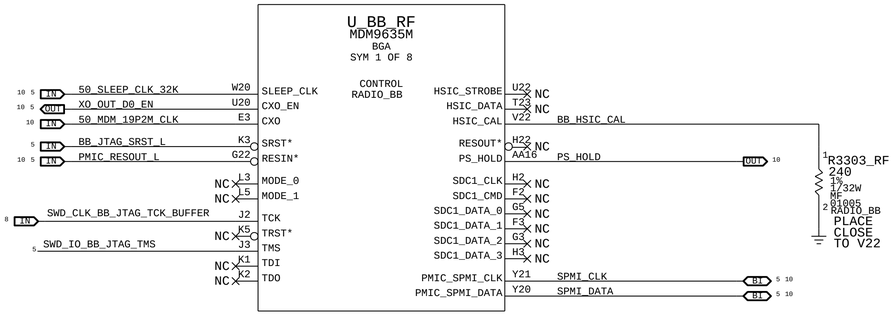


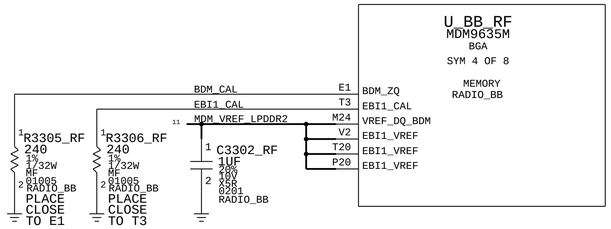
PAGE TITLE
CELLULAR BASEBAND: POWER2

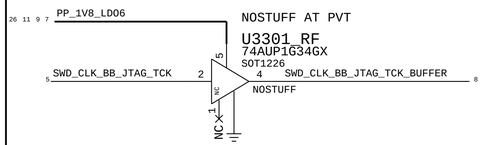
Apple Inc.

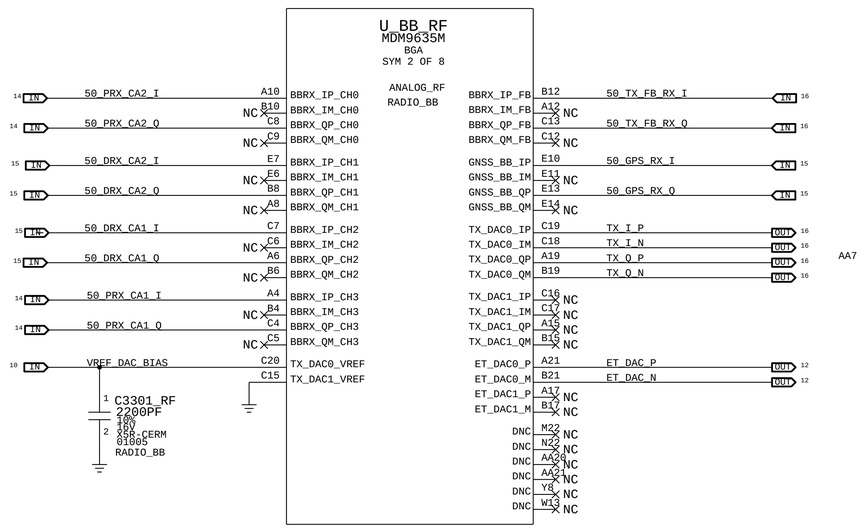
DRAWING NUMBER 051-1902
SIZE D
REVISION A.0.0
BRANCH
PAGE 32 OF 51
SHEET 40 OF 59

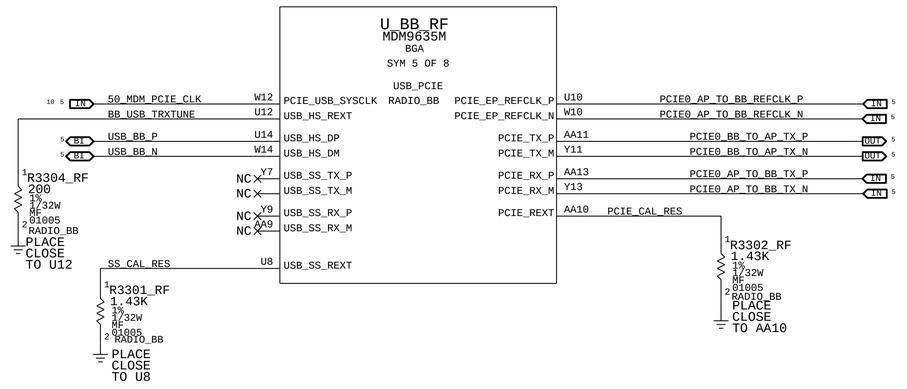
BASEBAND: CONTROL AND INTERFACES









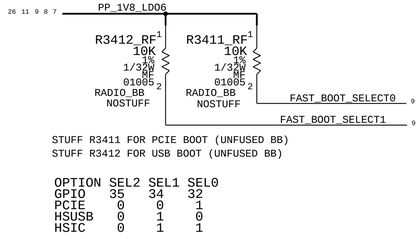


PAGE TITLE
CELLULAR BASEBAND: CONTROL AND INTERFACES

Apple Inc.

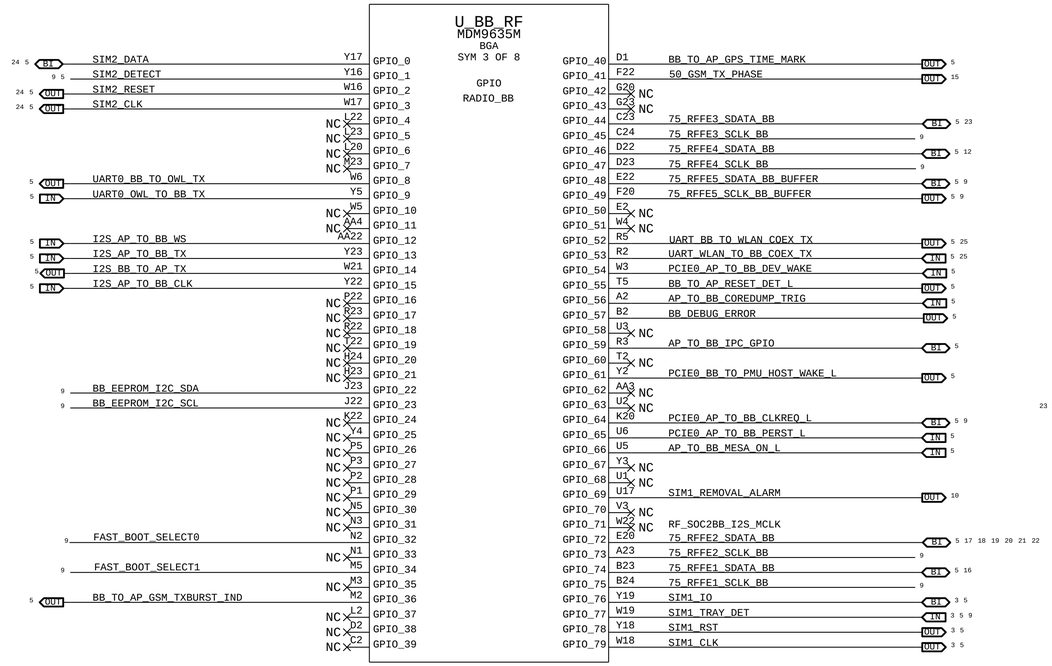
DRAWING NUMBER 051-1902
SIZE D
REVISION A.0.0
BRANCH
PAGE 33 OF 51
SHEET 41 OF 59

BASEBAND: GPIOS

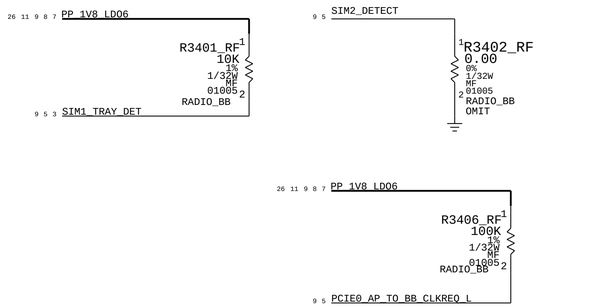


STUFF R3411 FOR PCIE BOOT (UNFUSED BB)
STUFF R3412 FOR USB BOOT (UNFUSED BB)

OPTION	SEL2	SEL1	SEL0
GPIO	35	34	32
PCIE	0	0	1
HSUSB	0	1	0
HSIC	0	1	1

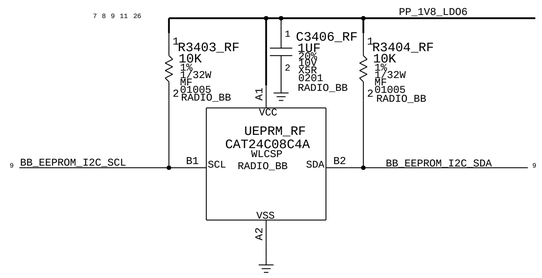


NOSTUFF R3402 WHEN VINYL PRESENT
STUFF R3402 WHEN VINYL NOT PRESENT

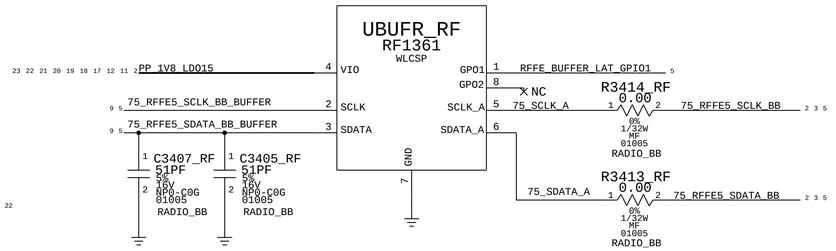


PCIE PULL-UPS TO BB RAIL

BB EEPROM

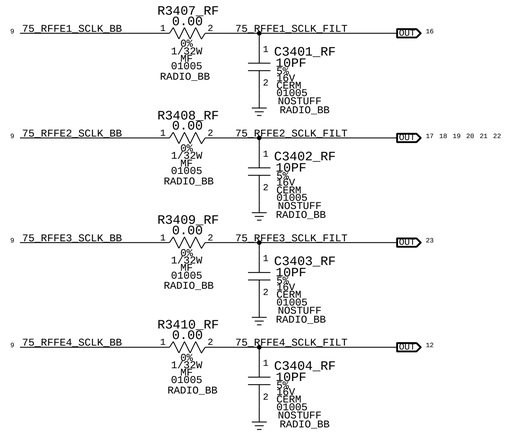


BUFFER ON RFFE5
SCLK/SDATA_A IS OUTPUT



PLACE C3405_RF CLOSE TO BUFFER
PLACE C3407_RF CLOSE TO MDM

RFFE CLOCK FILTERS



RFFE USAGE TABLE

RFFE1 WTR
RFFE2 LB/MB/HB PAD, 2G PA, LB/MB/HB ASM
RFFE3 DIV ASM
RFFE4 QPOET
RFFE5 DIV LNA, ANT TUNERS

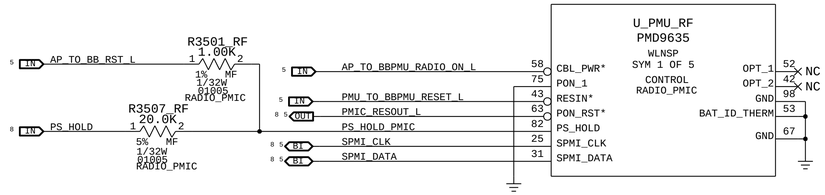
PAGE TITLE: CELLULAR BASEBAND: GPIOS
Apple Inc.
DRAWING NUMBER: 051-1902
SIZE: D
REVISION: A.0.0
BRANCH:
PAGE: 34 OF 51
SHEET: 42 OF 59

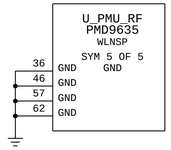
PMU: CONTROL AND CLOCKS

HW_REV2_ID	R3502	R3503	CONFIG
1.80V	698K	-	MLB
0.12V	698K	51.1K	SELF GEN

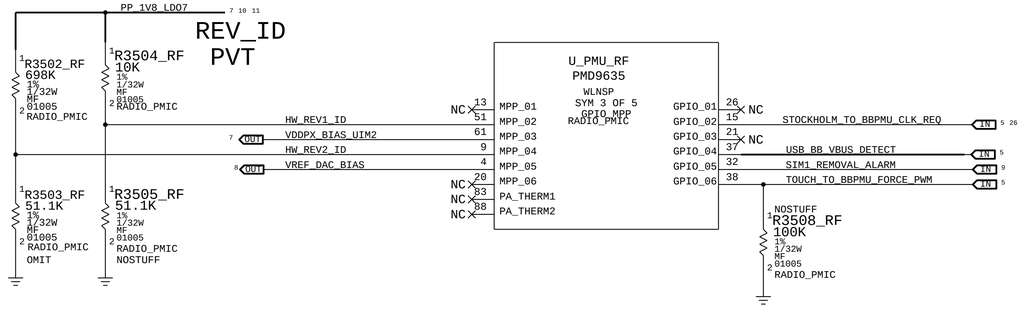
HW_REV_ID	R3504	R3505	REVISION
0.10V	887K	51.1K	DEV1
0.30V	255K	51.1K	DEV2
0.50V	124K	51.1K	DEV3
0.70V	82.5K	51.1K	DEV4/PROTOMLB1
0.90V	51.1K	51.1K	PROTOMLB2
1.10V	31.6K	51.1K	DEV5/PROTO1
1.20V	50K	100K	PROTO2
1.31V	39K	105K	EVT
1.43V	13.3K	51.1K	EVT_ALT
1.55V	8.25K	51.1K	CARRIER BUILD
1.67V	3.92K	51.1K	DVT
1.80V	10K	-	PVT

RESET AND CONTROL: PMU

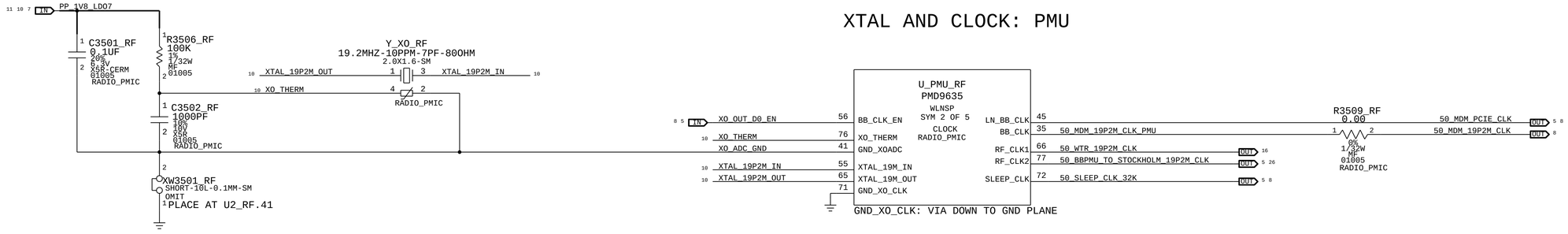




MPPS AND GPIOS: PMU



XTAL AND CLOCK: PMU



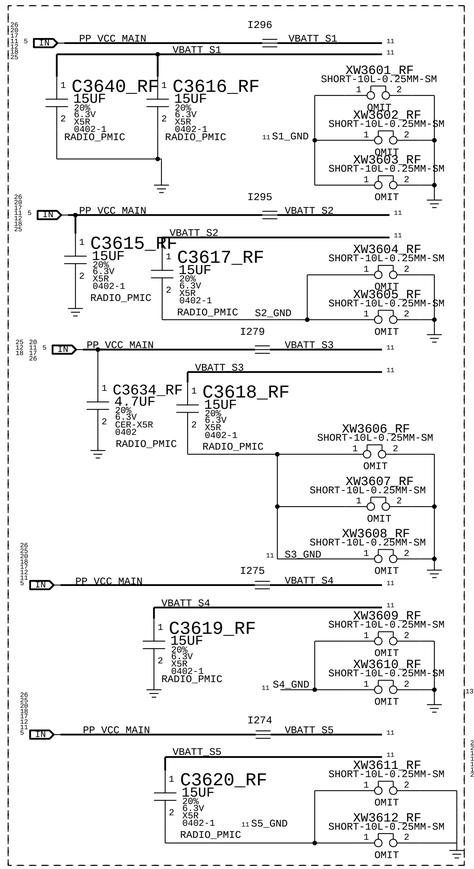
PAGE TITLE
CELLULAR PMU: CONTROL AND CLOCKS

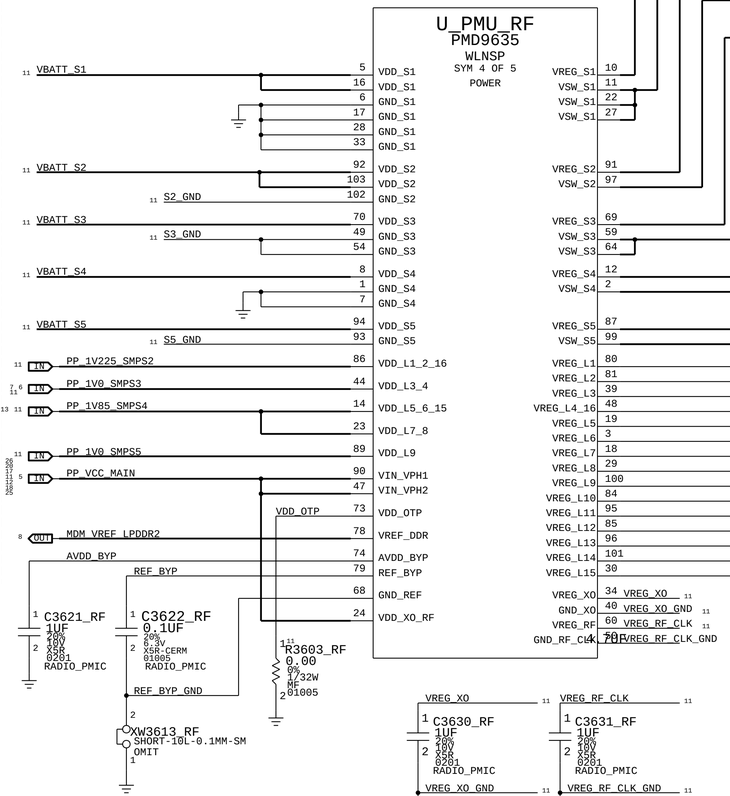
Apple Inc.

DRAWING NUMBER 051-1902 | SIZE D
REVISION A.0.0
BRANCH
PAGE 35 OF 51
SHEET 43 OF 59

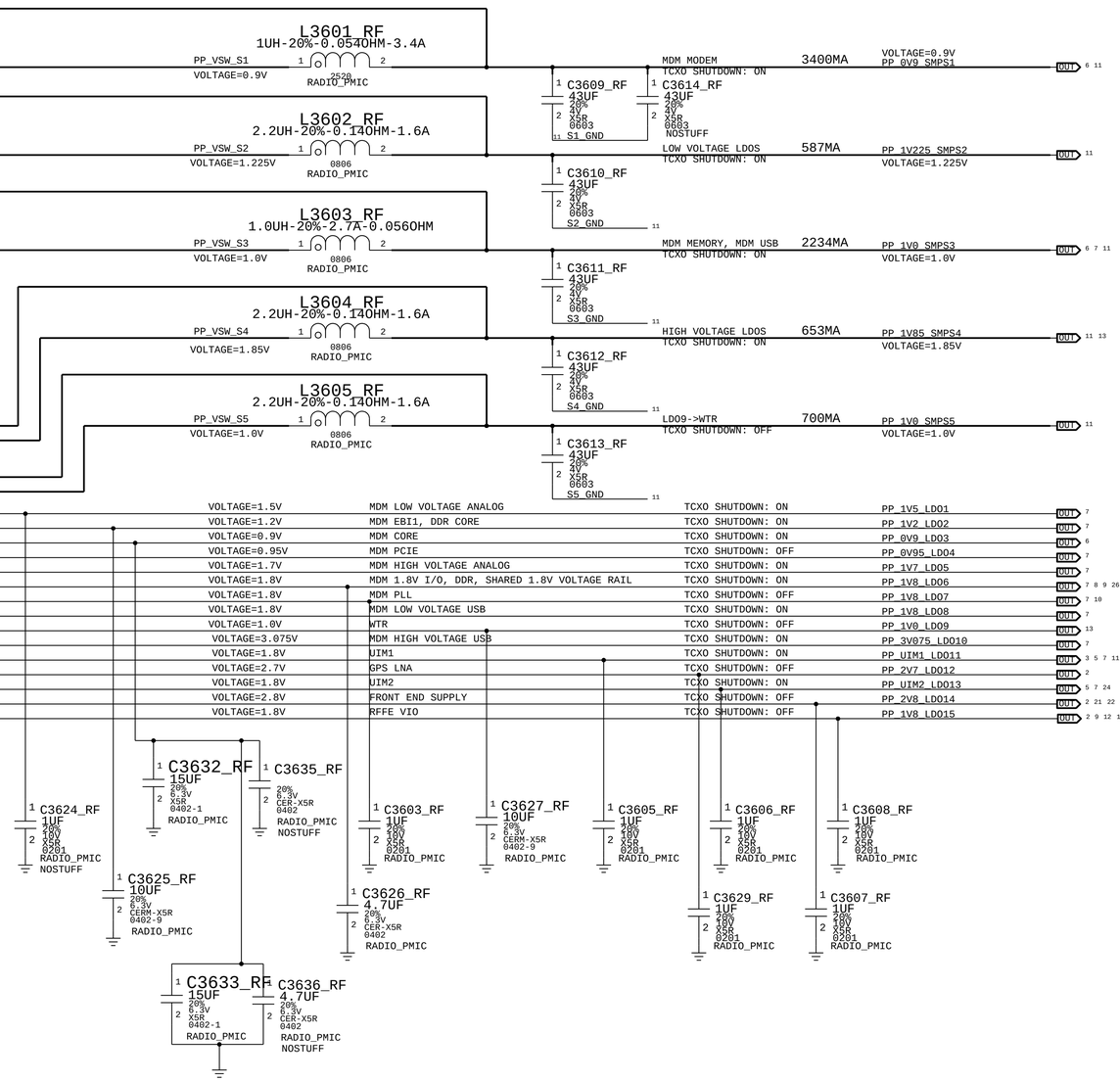
PMU: SWITCHERS AND LDOS

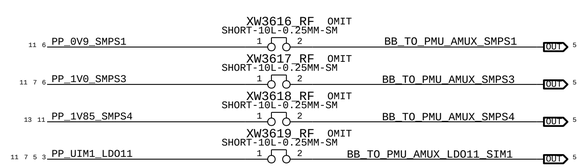
SWITCHERS BULK CAPS





PLACE XW CLOSE TO PMU
VIA XW DOWN TO THE GND PLANE



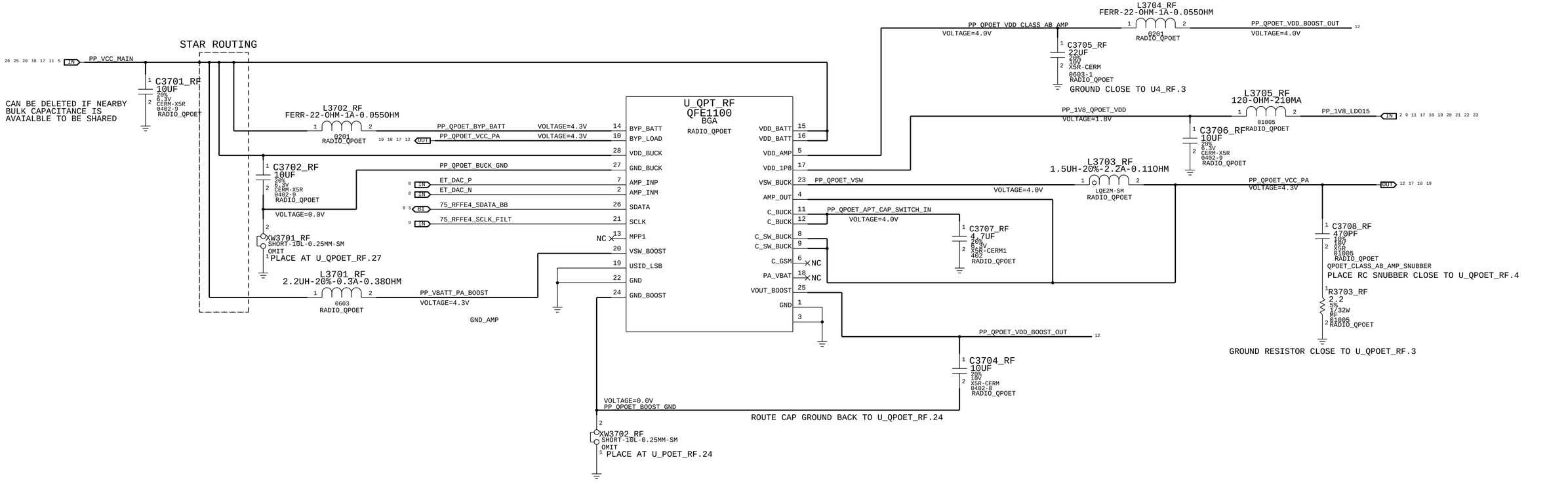


PAGE TITLE
CELLULAR PMU: SWITCHERS AND LDOS

Apple Inc.

DRAWING NUMBER 051-1902 SIZE D
REVISION A.0.0
BRANCH
PAGE 36 OF 51
SHEET 44 OF 59

PMU: ET MODULATOR



PAGE TITLE
CELLULAR PMU: ET MODULATOR

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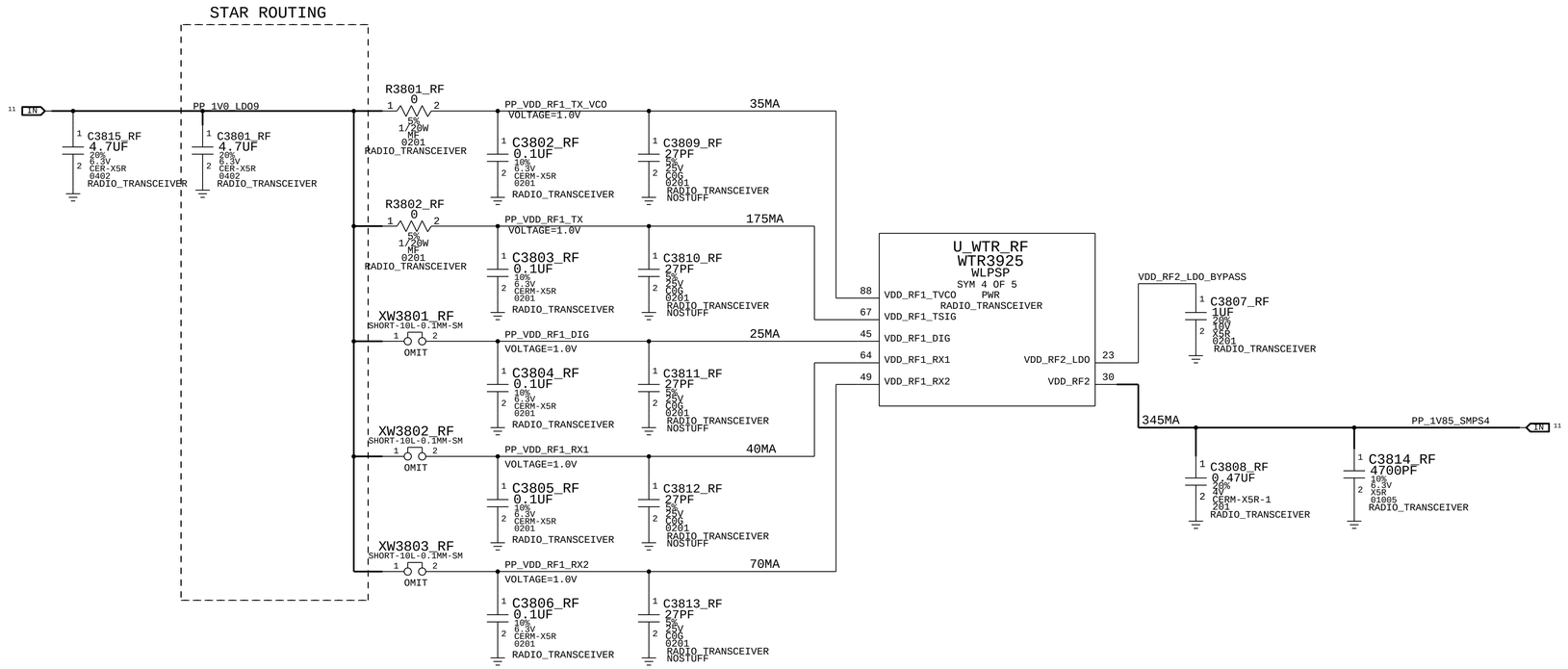
DRAWING NUMBER 051-1902 | SIZE D
REVISION A.0.0
BRANCH
PAGE 37 OF 51
SHEET 45 OF 59

TRANSCEIVER: POWER



PAGE TITLE
CELLULAR TRANSCEIVER: POWER

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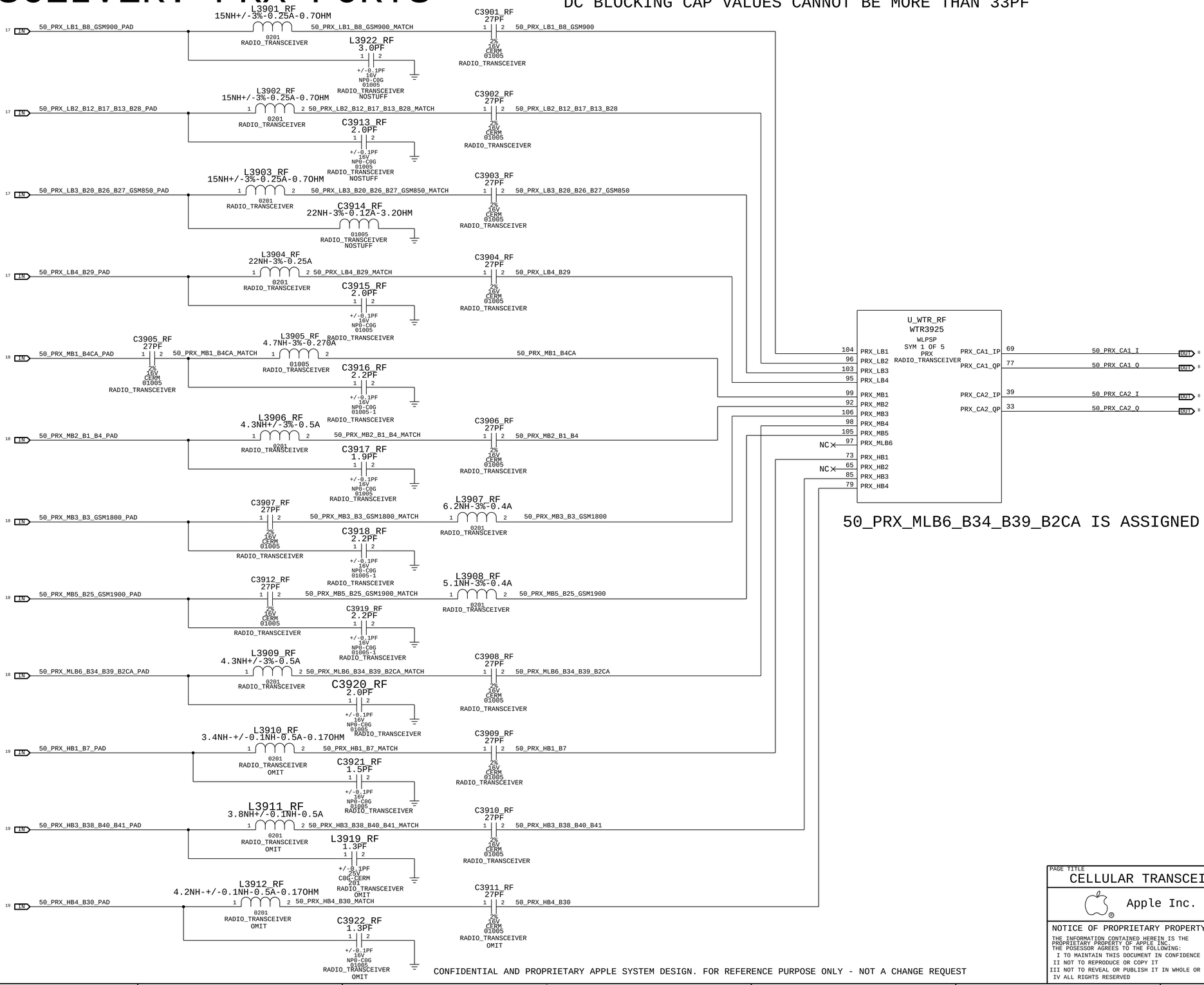
DRAWING NUMBER 051-1902
SIZE D
REVISION A.0.0
BRANCH
PAGE 38 OF 51
SHEET 46 OF 59

TRANSCEIVER: PRX PORTS

DC BLOCKING CAP VALUES CANNOT BE MORE THAN 33PF



50_PRX_MLB6_B34_B39_B2CA IS ASSIGNED TO MB4

PAGE TITLE
CELLULAR TRANSCEIVER: PRX PORTS

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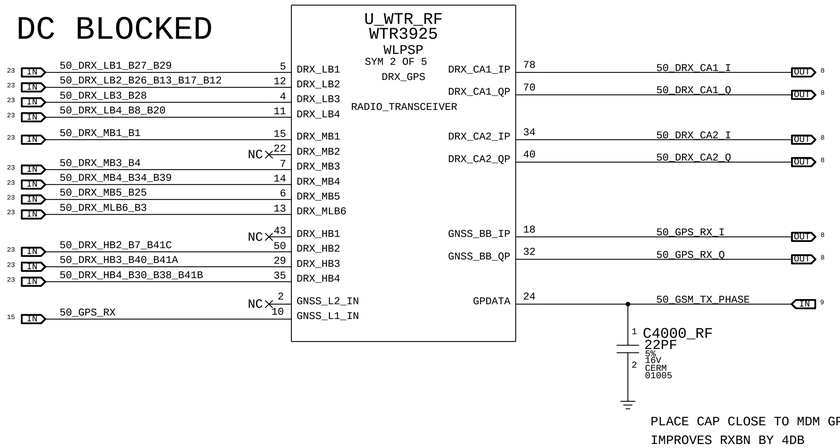
DRAWING NUMBER 051-1902 | SIZE D
REVISION A.0.0
BRANCH
PAGE 39 OF 51
SHEET 47 OF 59

TRANSCEIVER: DRX/GPS PORTS

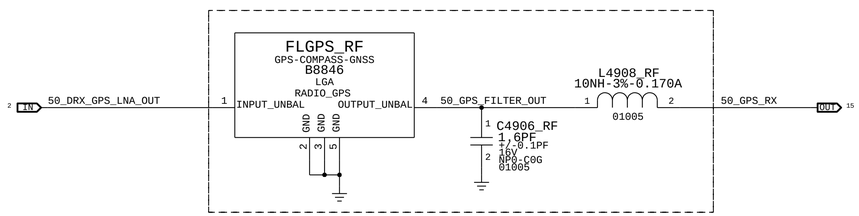
DRX MODULE PORTS ARE DC BLOCKED



PLACE CAP CLOSE TO MDM GPIO14
IMPROVES RXBN BY 4DB

GPS FILTER

PLACE NEAR U_WTR



PAGE TITLE: CELLULAR TRANSCEIVER: DRX/GPS PORTS

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DRAWING NUMBER: 051-1902 | SIZE: D

REVISION: A.0.0

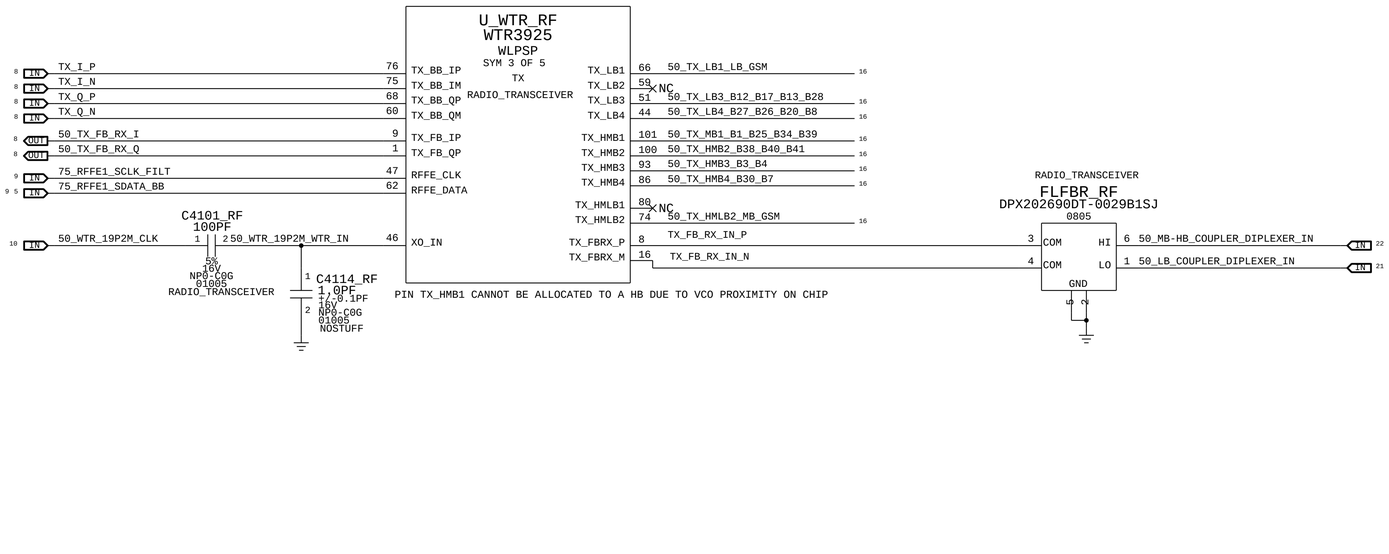
BRANCH:

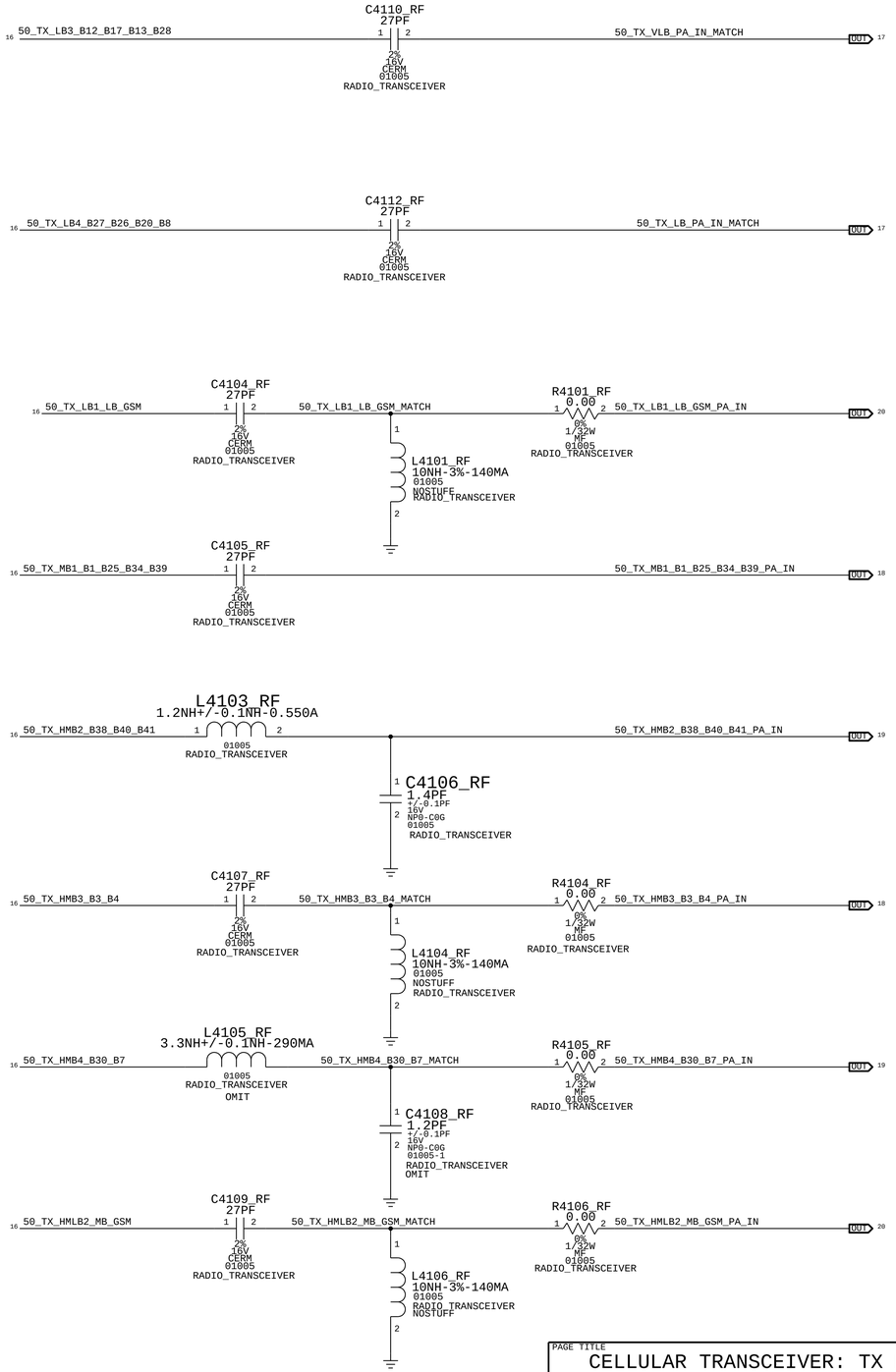
PAGE: 40 OF 51

SHEET: 48 OF 59

TRANSCEIVER: TX PORTS

B12/13 TX INTERSTAGE FILTER REMOVED



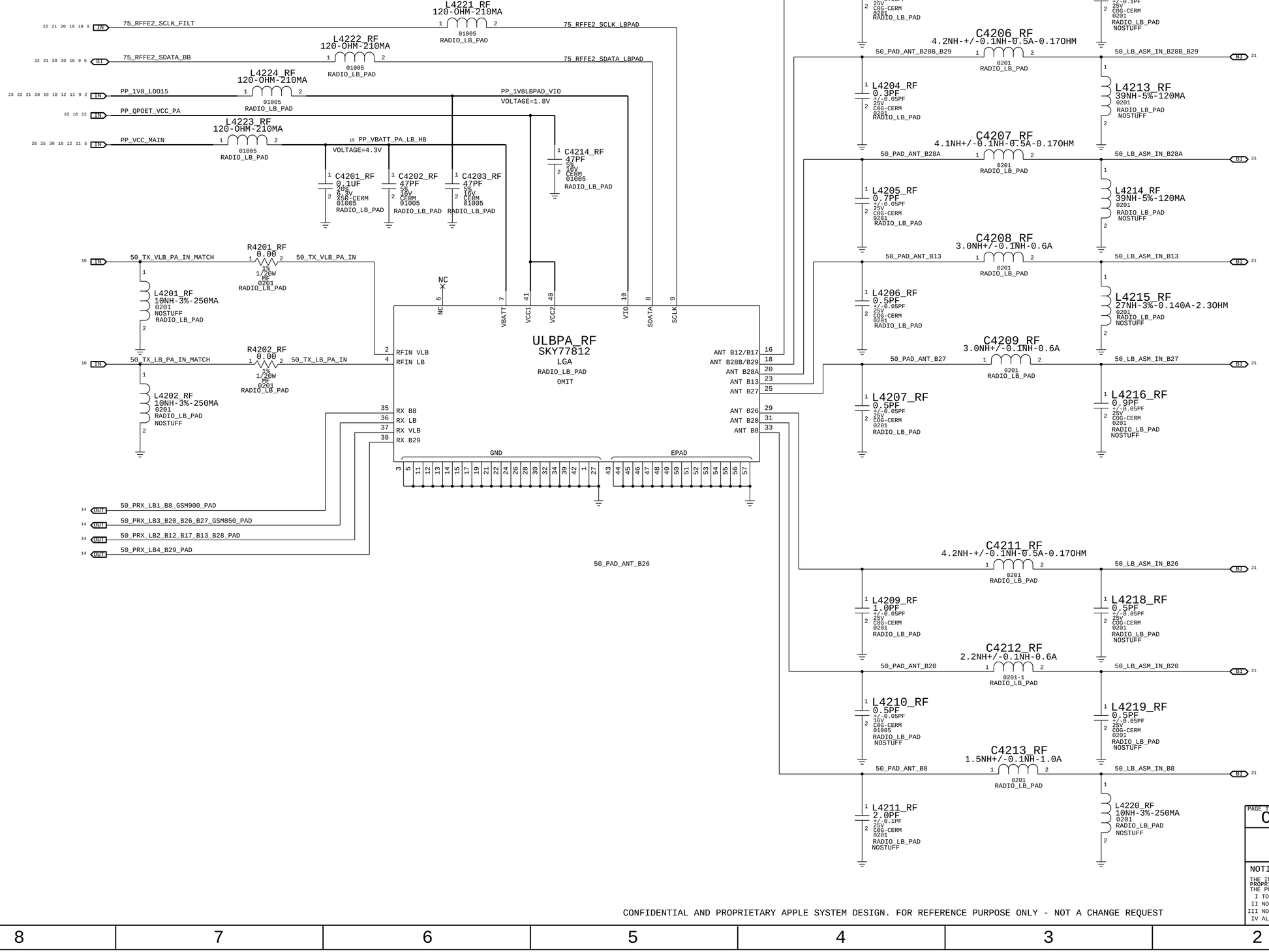


PAGE TITLE
CELLULAR TRANSCEIVER: TX PORTS

Apple Inc.

DRAWING NUMBER 051-1902
SIZE D
REVISION A.0.0
BRANCH
PAGE 41 OF 51
SHEET 49 OF 59

LOW BAND PA+DUPLEXERS



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PAGE TITLE
CELLULAR FRONT END: LB PAD

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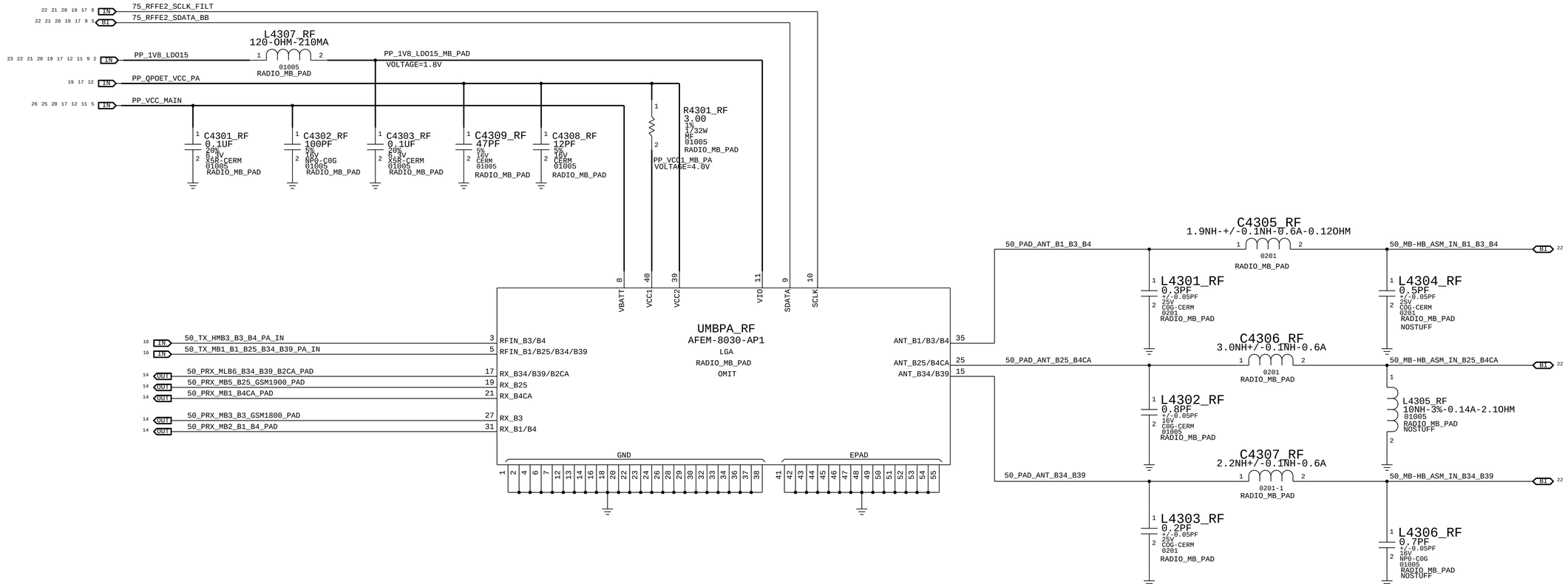
DRAWING NUMBER 051-1902 | SIZE D
REVISION A.0.0
BRANCH
PAGE 42 OF 51
SHEET 50 OF 59

MID BAND PA+DUPLEXERS

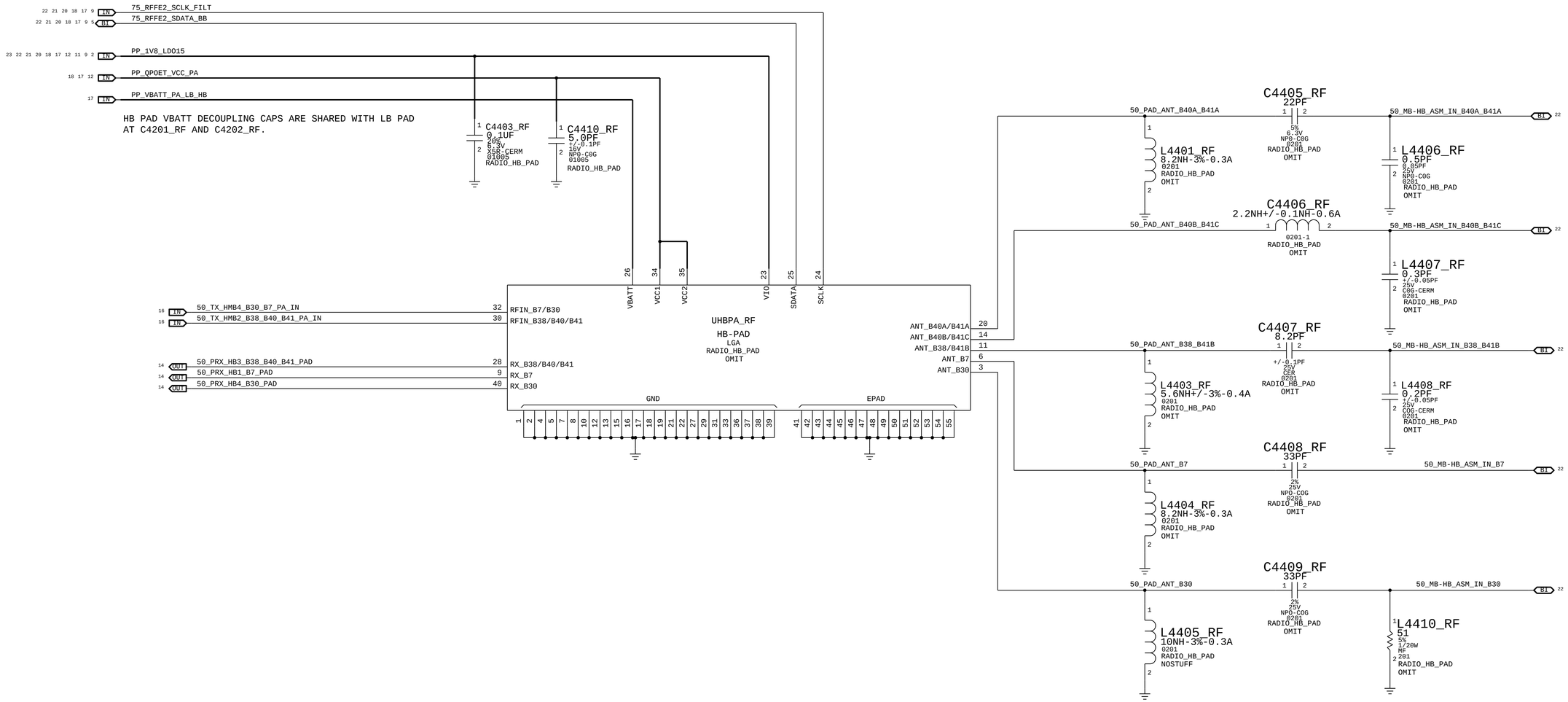


PAGE TITLE
CELLULAR FRONT END: MB PAD

Apple Inc.

DRAWING NUMBER 051-1902
SIZE D
REVISION A.0.0
BRANCH
PAGE 43 OF 51
SHEET 51 OF 59

HIGH BAND PA+DUPLEXERS



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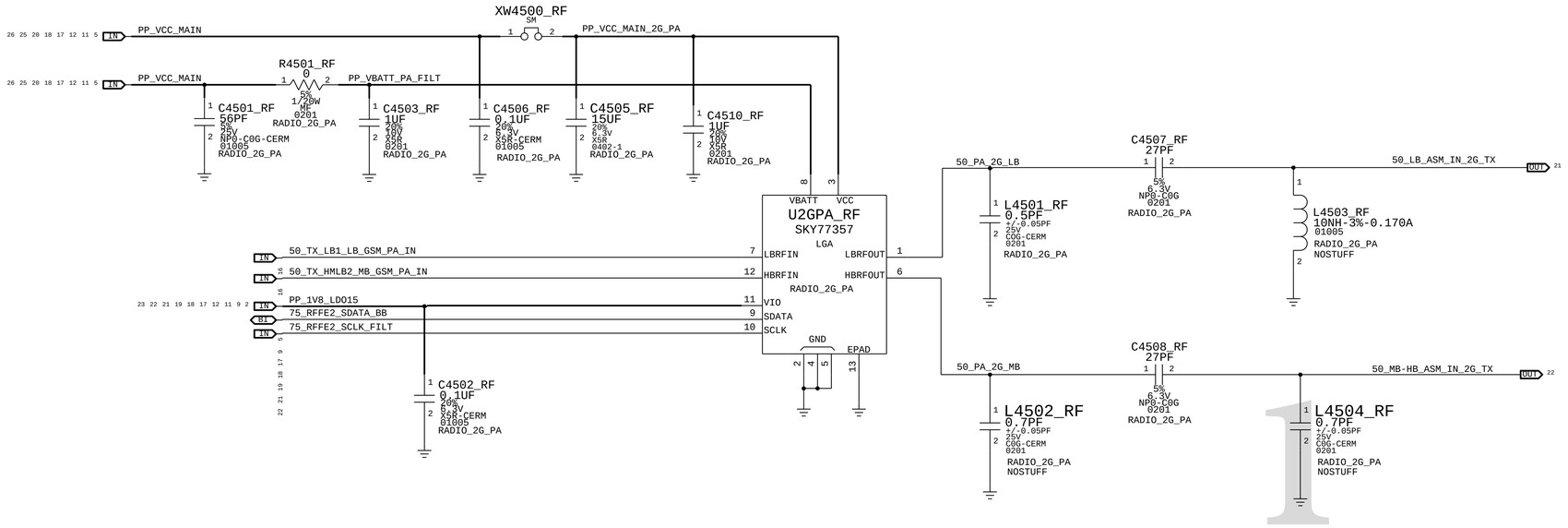
Apple Inc.

DRAWING NUMBER 051-1902
SIZE D
REVISION A.0.0
BRANCH
PAGE 44 OF 51
SHEET 52 OF 59

2G PA



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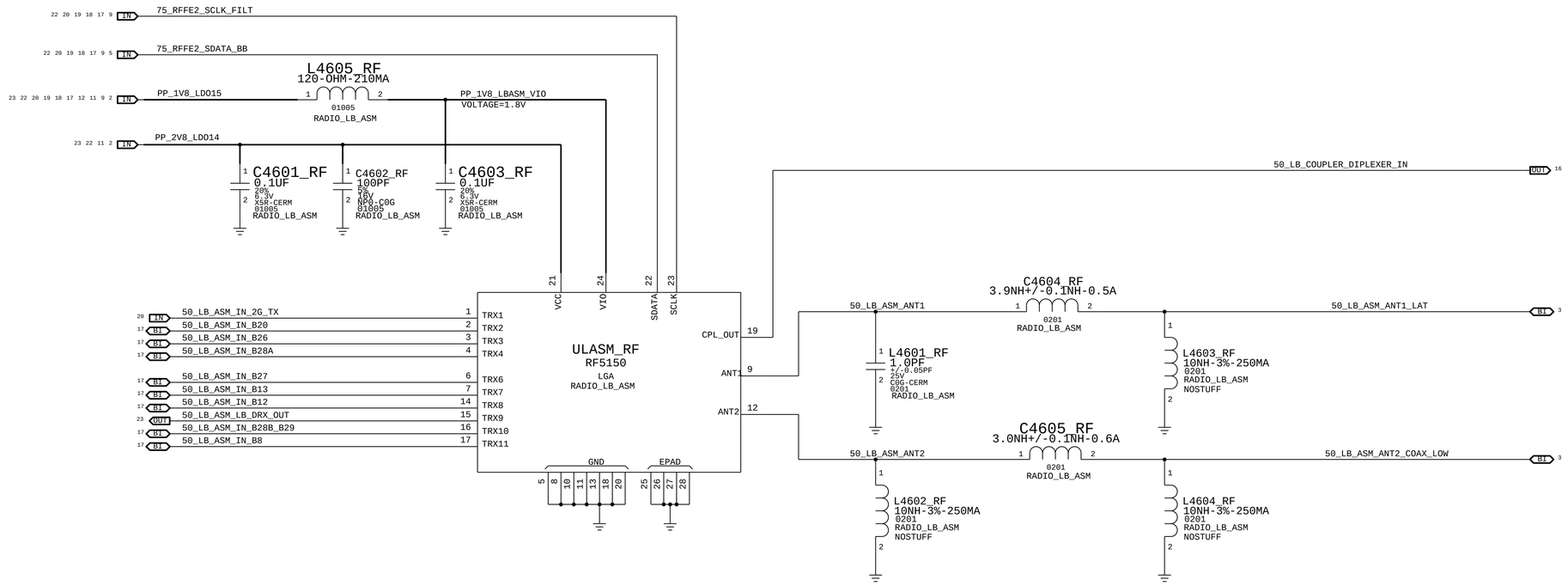
Apple Inc.

DRAWING NUMBER 051-1902 | SIZE D
REVISION A.0.0
BRANCH
PAGE 45 OF 51
SHEET 53 OF 59

LOW BAND ANTENNA SWITCH MODULE



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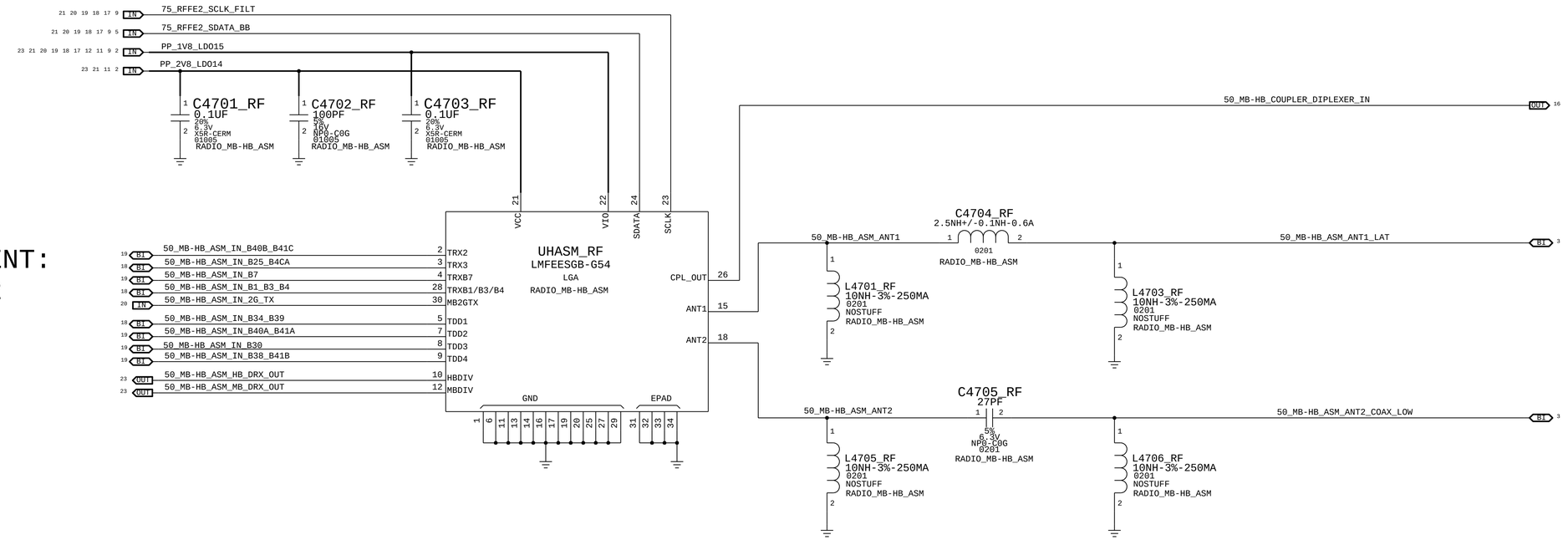
Apple Inc.

DRAWING NUMBER 051-1902
SIZE D
REVISION A.0.0
BRANCH
PAGE 46 OF 51
SHEET 54 OF 59

MID-HIGH BAND ANTENNA SWITCH MODULE

EVT ASM ASSIGNMENT:
B40B/B41C - TRX2
B30 - TDD3



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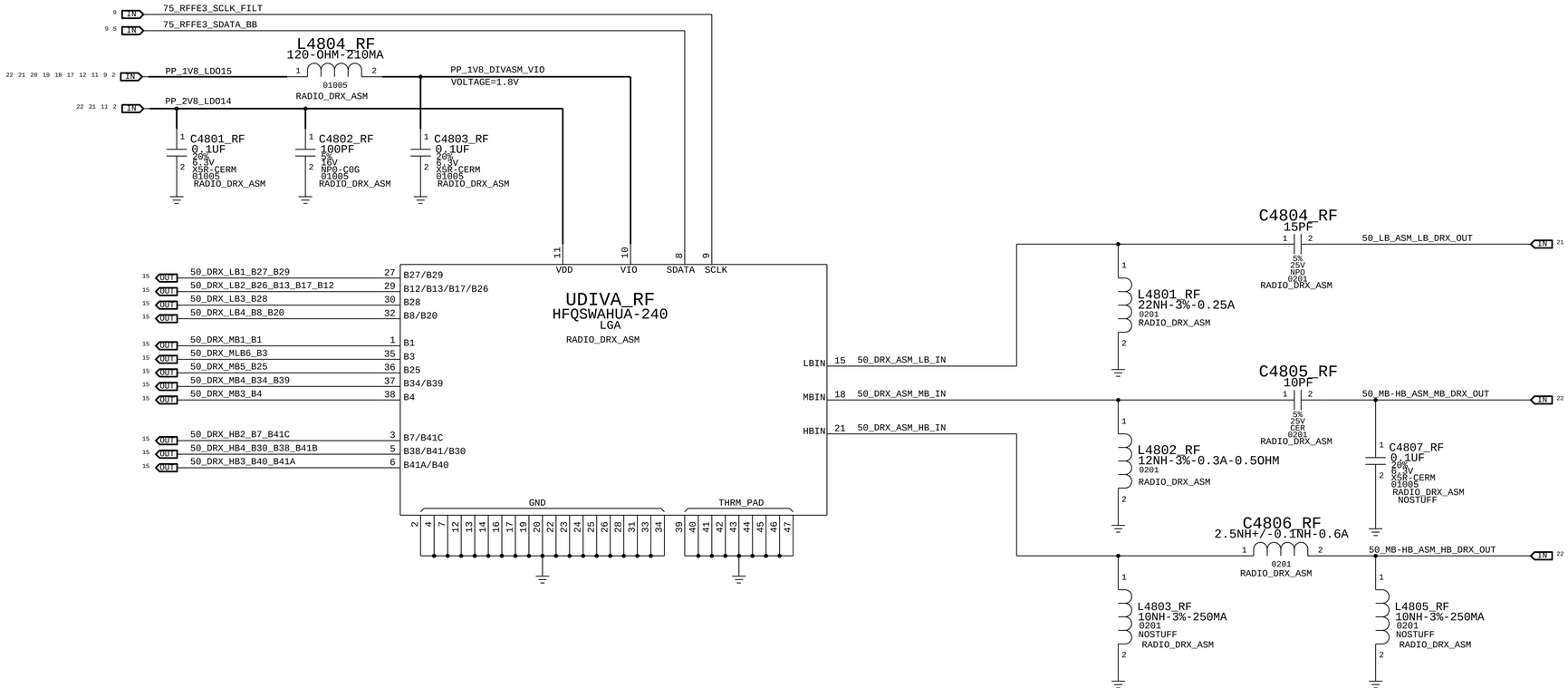
Apple Inc.

DRAWING NUMBER 051-1902 | SIZE D
REVISION A.0.0
BRANCH
PAGE 47 OF 51
SHEET 55 OF 59

DIVERSITY MODULE



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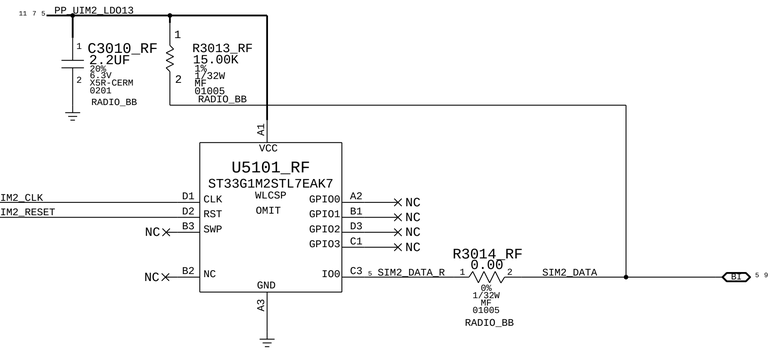
Apple Inc.

DRAWING NUMBER 051-1902
SIZE D
REVISION A.0.0
BRANCH
PAGE 48 OF 51
SHEET 56 OF 59

SIM



PAGE TITLE: SIM

Apple Inc.

DRAWING NUMBER: 051-1902 | SIZE: D

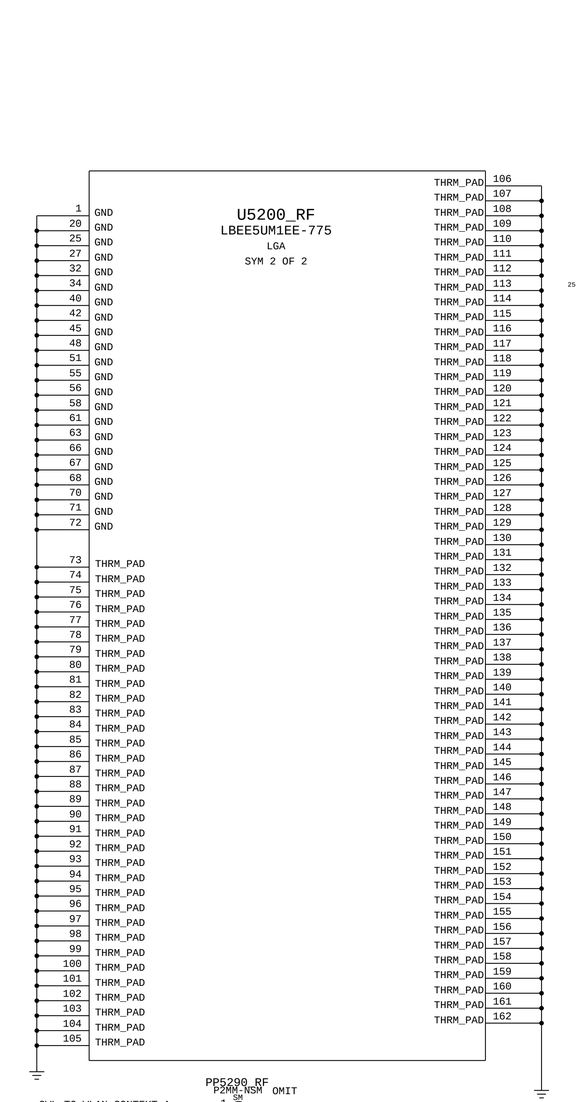
REVISION: A.0.0

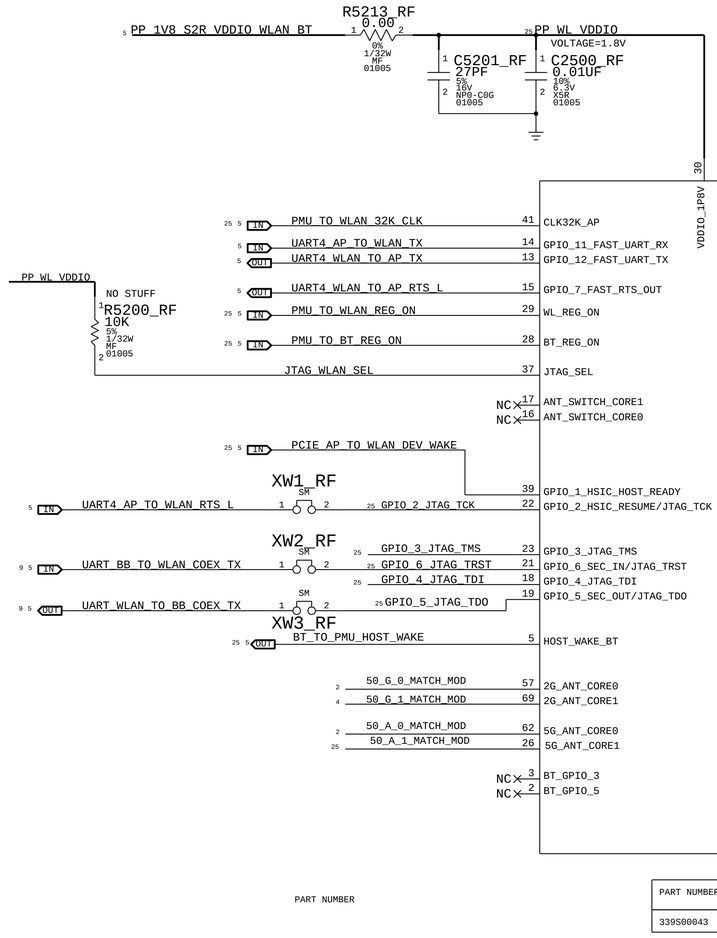
BRANCH:

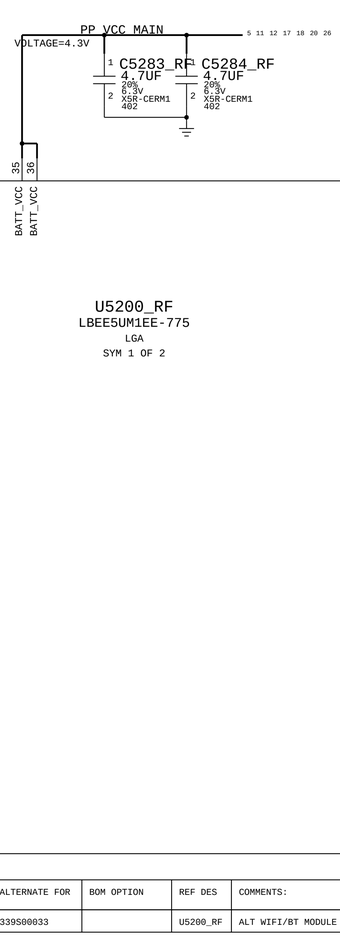
PAGE: 49 OF 51

SHEET: 57 OF 59

WIFI/BT







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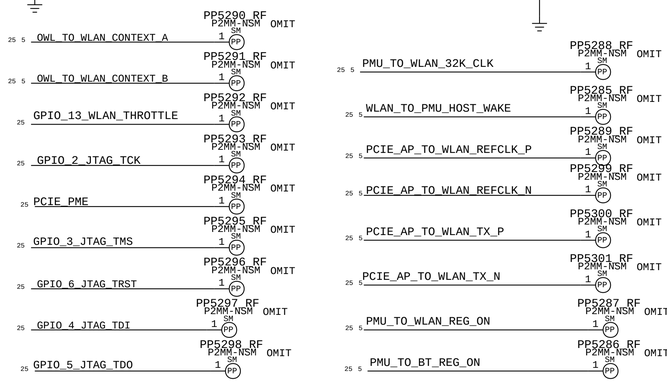
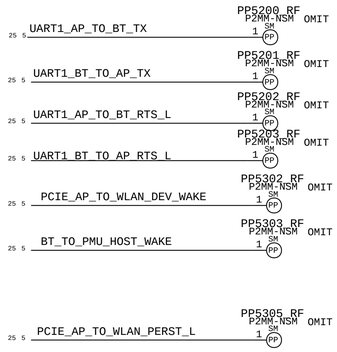
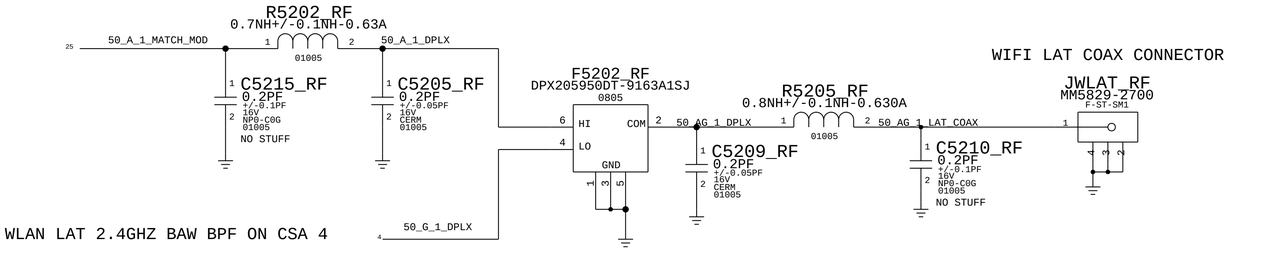
PART NUMBER







LAST UPDATED: 4/30/2014

SYNC_MASTER=WIFI SYNC_DATE=01/30/2014

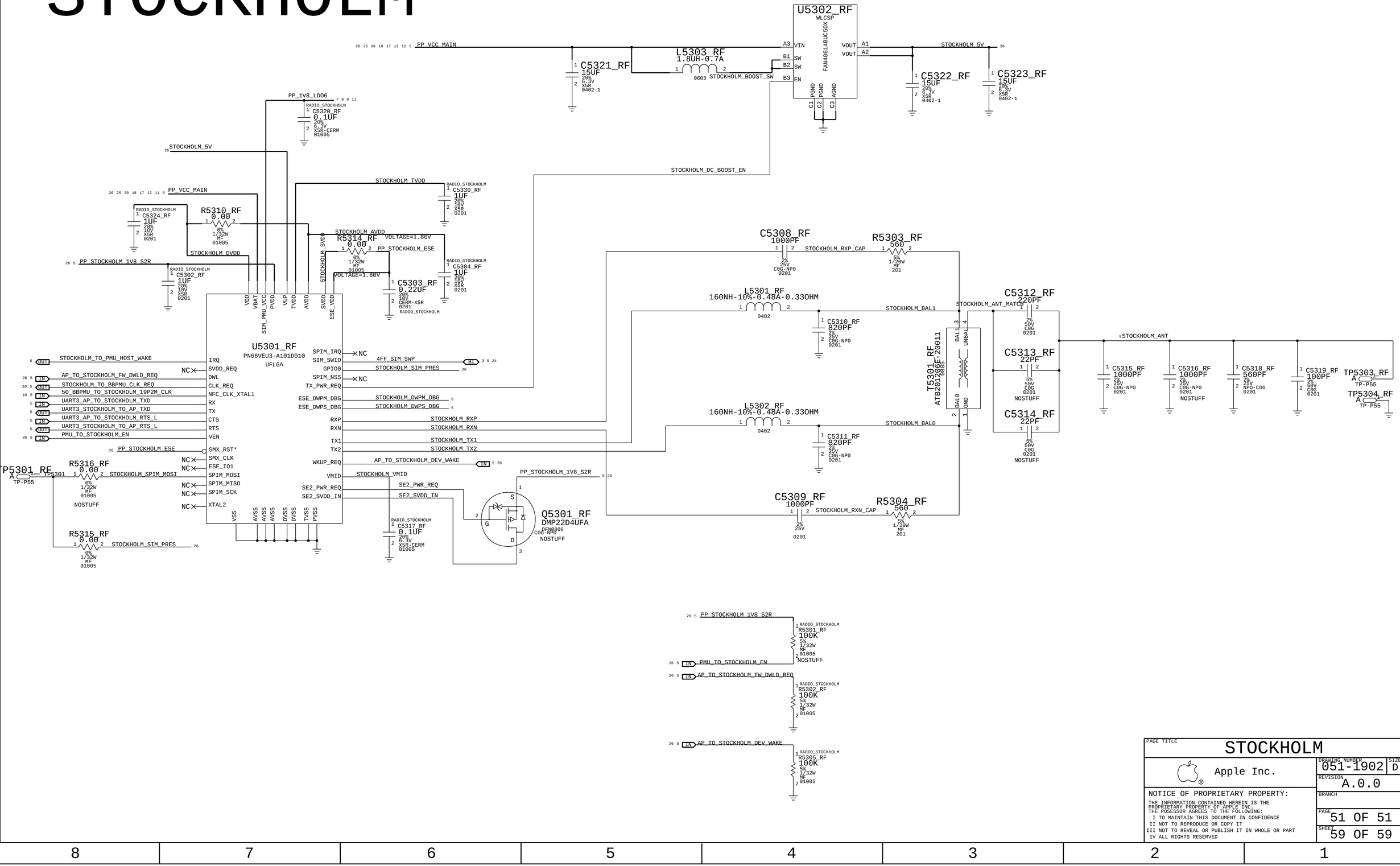
PAGE TITLE
WIFI/BT: WIFI/BT MODULE

Apple Inc.

DRAWING NUMBER 051-1902 SIZE D
REVISION A.0.0
BRANCH
PAGE 50 OF 51
SHEET 58 OF 59

STOCKHOLM

ALL NETNAMES NEED TO BE CHECKED



PAGE TITLE	STOCKHOLM
DRAWING NUMBER	051-1902
SIZE	D
REVISION	A.0.0
BRANCH	
PAGE	51 OF 51
SHEET	59 OF 59

Apple Inc.