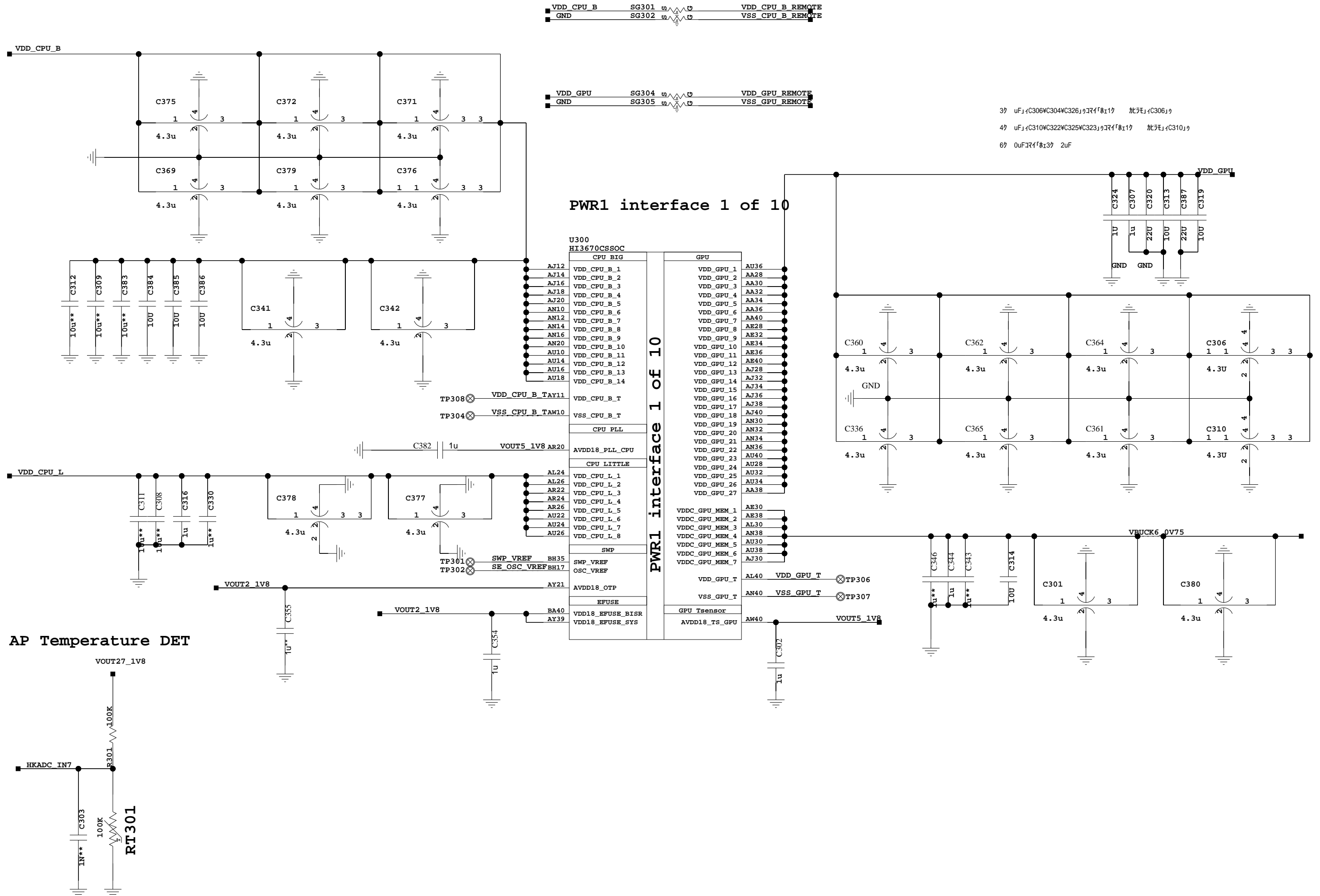


	1	2	3	4	5	6
A	Baseband Schematic			MODEM Schematic		
	1.	Contents		31.	RF Interface	
	2.	Block Diagramm		32.	APT Power	
	3.	SOC PWR1		33.	RF Transceiver_0	
	4.	SOC PWR2		34.	RF FRONT END HB	
	5.	SOC PWR3		35.	RF FRONT END B42	
	6.	SOC HS Interface		36.	RF FRONT END MB	
	7.	SOC GPIO Interface		37.	RF Front End LB	
	8.	SOC RF Interface		38.	RF Front End Switch /Main ANT	
	9.	SOC GND & NC		39.	RF Front End Diversity	
B	10.	PMU LDO		40.	RF Front End Diversity	
	11.	PMU BUCK		41.	Reserved for CDMA Modem	
	12.	PMU MISC & BUCKBOOST		42.	Reserved for CDMA Modem	
	13.	HI6422-2		43.	Reserved for CDMA Modem	
	14.	UFS and LPDDR4		44.	Reserved for CDMA Modem	
	15.	Battery & Fuel gauge		45.	Reserved for CDMA Modem	
	16.	Charge Management		46.	Reserved for CDMA Modem	
	17.	LCD Interface		47.	Reserved for CDMA Modem	
	18.	Direct Charge LoadSwitch		48.	Reserved for CDMA Modem	
	19.	Flash LED		49.	Reserved	
C	20.	Camera Interface		50.	Reserved	
	21.	ISP Reserved		51.	BCM43455 BB	
	22.	Codec HI6403		52.	BCM43455 POWER	
	23.	MIC/VIB		53.	Reserved	
	24.	Headphone		54.	WALN RF0	
	25.	Audio		55.	WLAN RF1	
	26.	X-Sensor1		56.	GPS	
	27.	X-Sensor2		57.	NFC	
	28.	SIM Card		58.	RF Transceiver2	
	29.	FPC Interface		59.	Reserved	
D	30.	Test Point/Shielding		60.	ANT Tuner	
	1	2	3		5	6

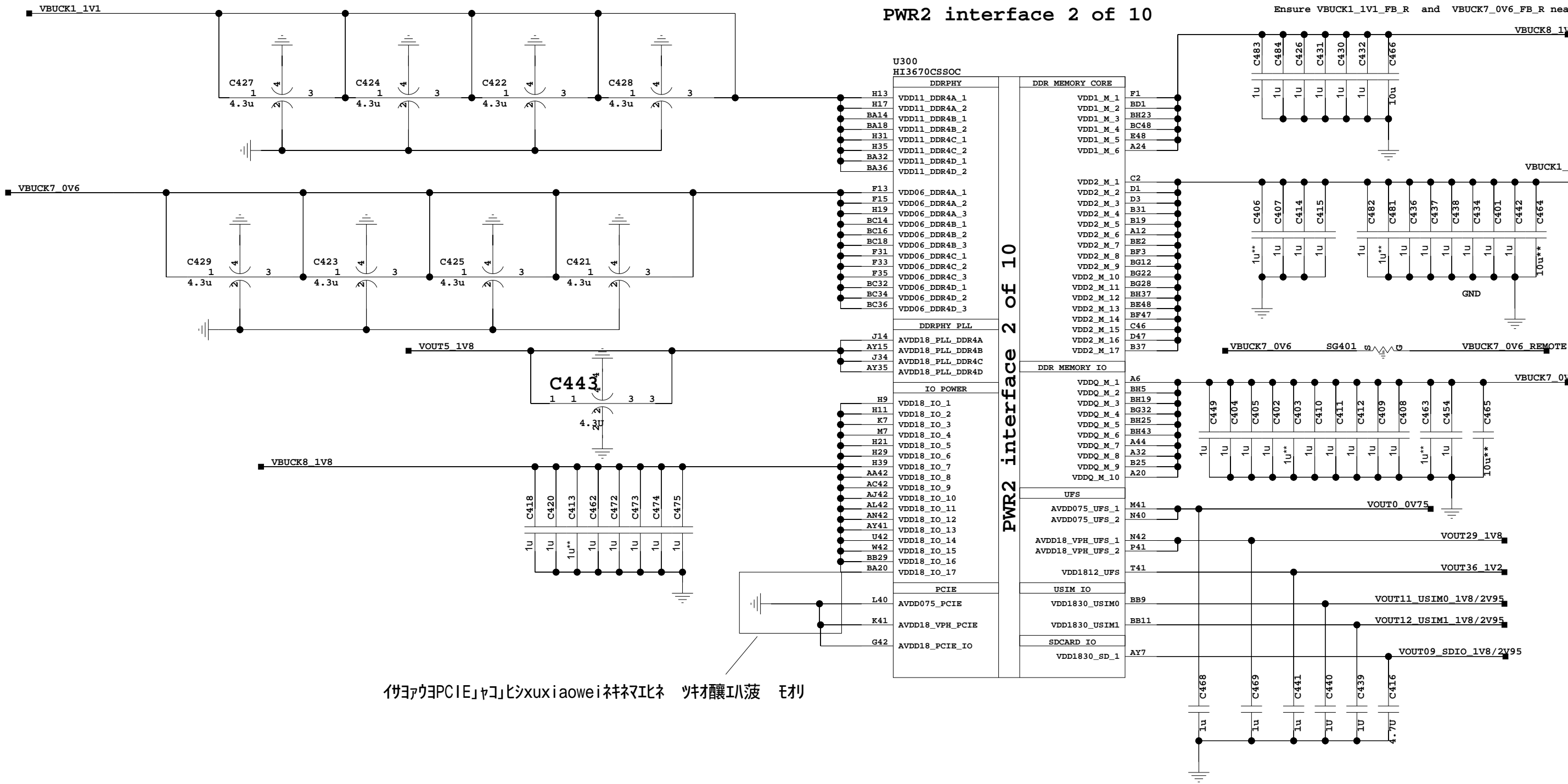
2.RES

1	2	3	4	5	6
A					A
B					B
C					C
D					
1	2	3		5	6

### 3.SOC PWR1



4.SOC PWR2



付ヨアウヨPCIE」ヤコ」ヒシxuxiaoweiネナマニネ ツナミ醸ハ波 モリ

PWR2 interface 2 of 10

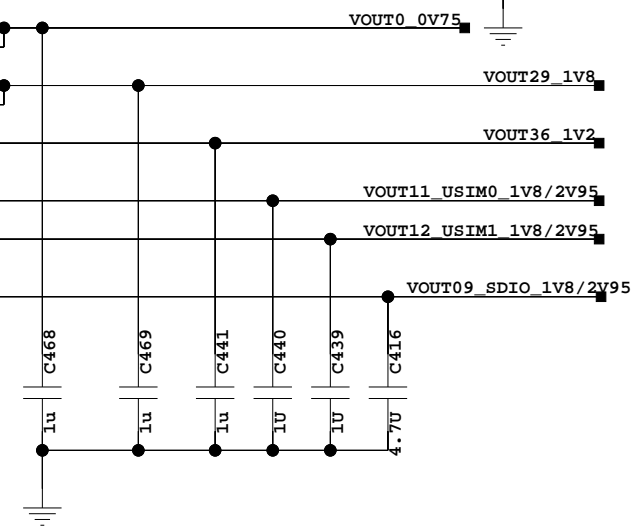
Ensure VBUCK1\_1V1\_FB\_R and VBUCK7\_0V6\_FB\_R near the CAP

PWR2 interface 2 of 10

U300  
HI3670CSSOC

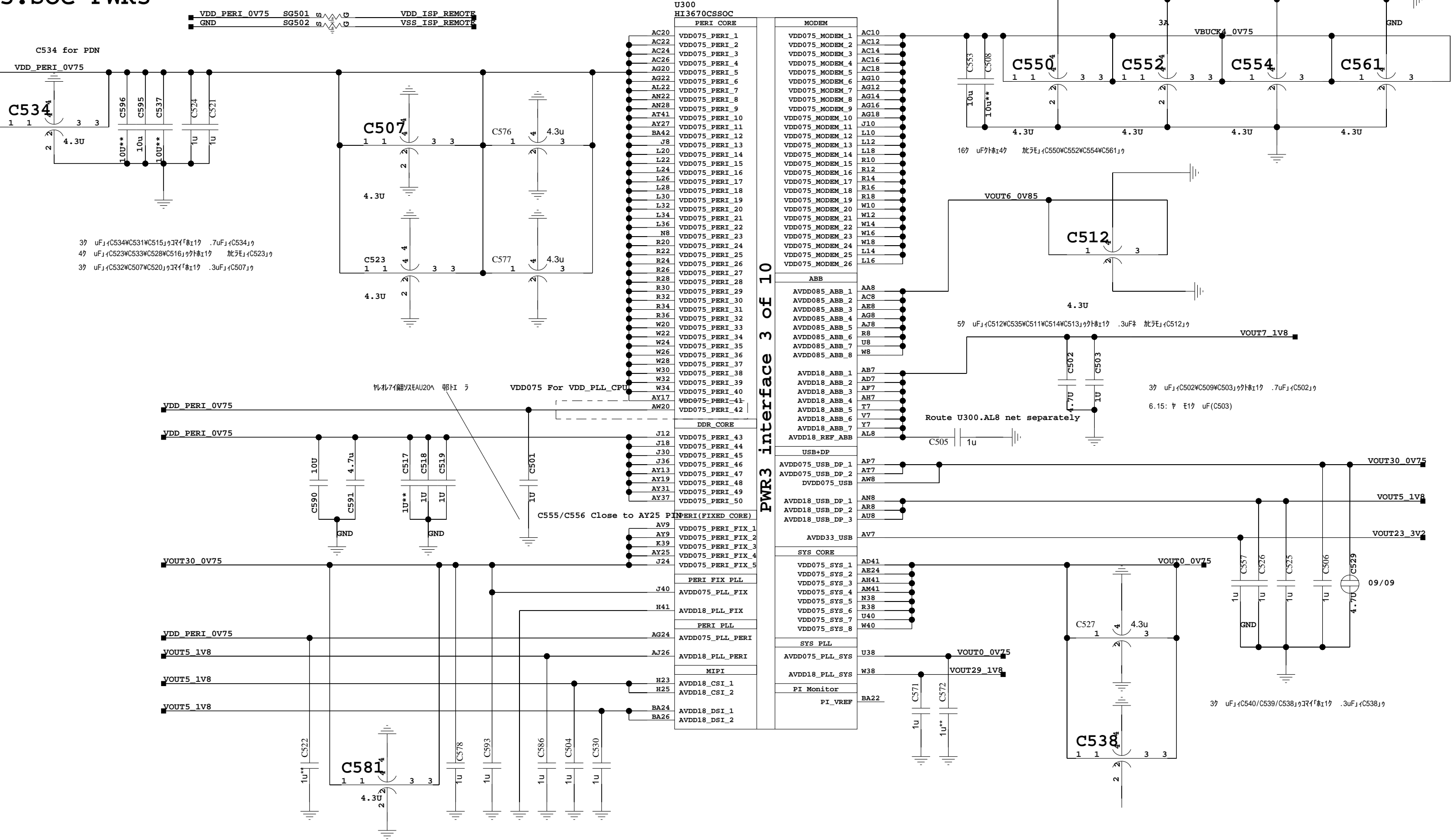
DDRPHY	
H13	VDD11_DDR4A_1
H17	VDD11_DDR4A_2
BA14	VDD11_DDR4B_1
BA18	VDD11_DDR4B_2
H31	VDD11_DDR4C_1
H35	VDD11_DDR4C_2
BA32	VDD11_DDR4D_1
BA36	VDD11_DDR4D_2
DDRPHY PLL	
J14	AVDD18_PLL_DDR4A
AY15	AVDD18_PLL_DDR4B
J34	AVDD18_PLL_DDR4C
AY35	AVDD18_PLL_DDR4D
IO POWER	
H9	VDD18_IO_1
H11	VDD18_IO_2
K7	VDD18_IO_3
M7	VDD18_IO_4
H21	VDD18_IO_5
H29	VDD18_IO_6
H39	VDD18_IO_7
AA42	VDD18_IO_8
AC42	VDD18_IO_9
AJ42	VDD18_IO_10
AL42	VDD18_IO_11
AN42	VDD18_IO_12
AY41	VDD18_IO_13
U42	VDD18_IO_14
W42	VDD18_IO_15
BB29	VDD18_IO_16
BA20	VDD18_IO_17
PCIE	
L40	AVDD075_PCIE
K41	AVDD18_VPH_PCIE
G42	AVDD18_PCIE_IO

DDR MEMORY CORE	
F1	VDD1_M_1
BD1	VDD1_M_2
BH23	VDD1_M_3
BC48	VDD1_M_4
E48	VDD1_M_5
A24	VDD1_M_6
DDR MEMORY IO	
A6	VDDQ_M_1
BH5	VDDQ_M_2
BH19	VDDQ_M_3
BG32	VDDQ_M_4
BH25	VDDQ_M_5
BH43	VDDQ_M_6
A44	VDDQ_M_7
A32	VDDQ_M_8
B25	VDDQ_M_9
A20	VDDQ_M_10
UFS	
M41	AVDD075_UFS_1
N40	AVDD075_UFS_2
N42	AVDD18_VPH_UFS_1
P41	AVDD18_VPH_UFS_2
USIM IO	
BB9	VDD1830_USIM0
BB11	VDD1830_USIM1
SDCARD IO	
AY7	VDD1830_SD_1

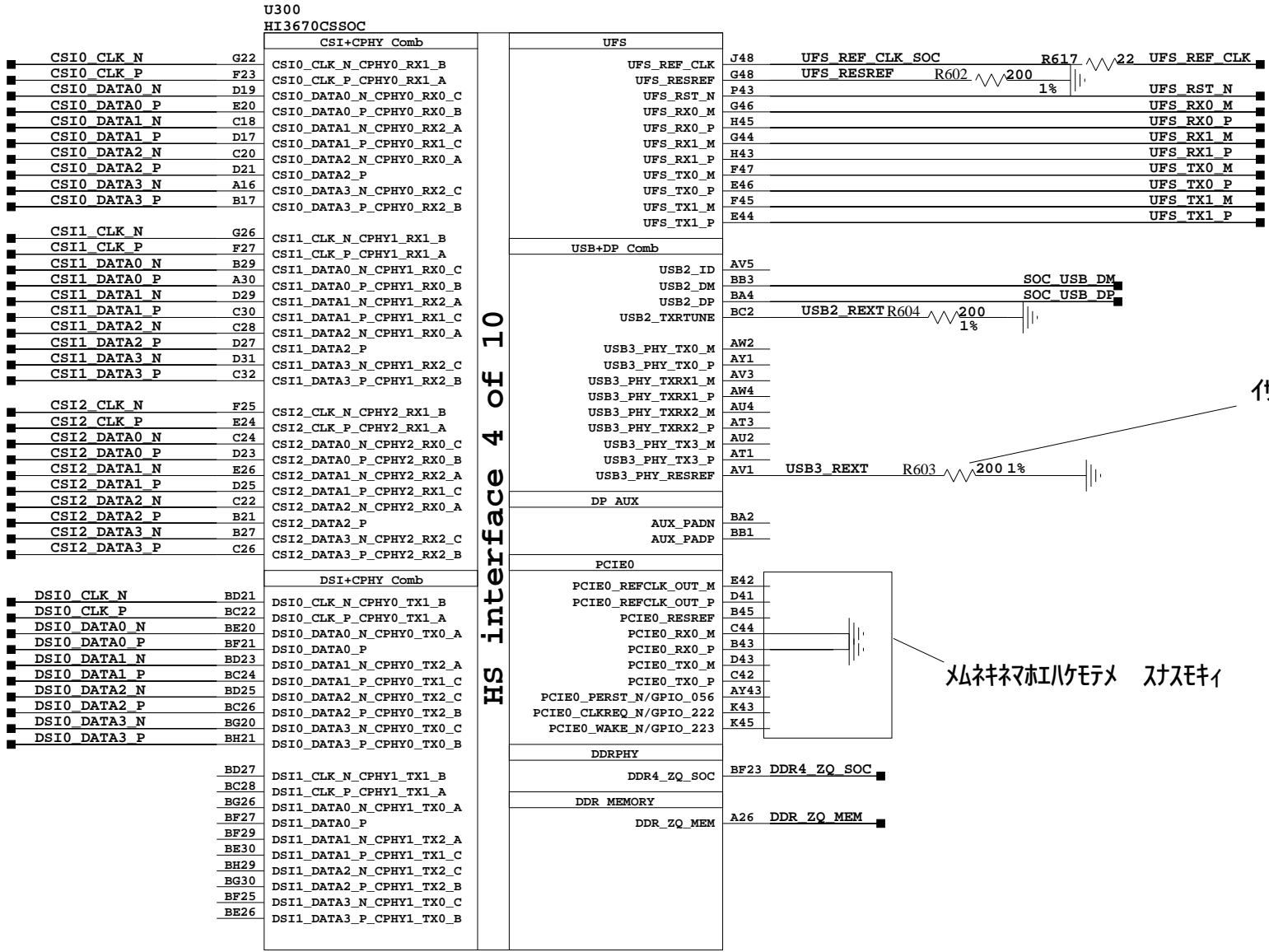


5.SOC PWR3

PWR3 interface 3 of 10



6.SOC HS INTERFACE



7.SOC GPIO INTERFACE1

U300  
HI3670CSSOC

ISP AO

GPIO\_202/ISP\_GPIO03\_PRTB  
GPIO\_203/ISP\_GPIO04\_FTPWM  
CODEC\_SSI  
GPIO\_204/ISP\_GPIO05\_BKPWM  
GPIO\_209/ISP\_GPIO08\_ENB  
GPIO\_208/ISP\_GPIO07\_ENA  
GPIO\_207/ISP\_GPIO09\_ENC  
GPIO\_218/ISP\_GPIO11  
SPI2\_CS2\_N/SPI4\_CS2\_N  
GPIO\_219/ISP\_GPIO12  
SPI2\_CS3\_N/SPI4\_CS3\_N

IO AO

GPIO\_177  
GPIO\_182/CLK\_OUT0/I3C\_SCL  
GPIO\_183/CLK\_OUT1/I3C\_SDA  
BLPWM\_CABC/GPIO\_184  
BLPWM\_BL/GPIO\_185  
PWM\_OUT0  
SLIMBUS\_CLK/GPIO\_192  
SLIMBUS\_DATA/GPIO\_193  
GPIO\_194/I2S0\_DI  
DSD\_DAT1\_6403  
GPIO\_195/I2S0\_DO  
DSD\_DAT0\_6403/UART7\_RXD  
GPIO\_196/I2S0\_XCLK  
DSD\_CLK\_6403/UART7\_TXD  
GPIO\_197/I2S0\_XFS  
GPIO\_201/I2S2\_XFS  
UART8\_TXD  
GPIO\_200/I2S2\_XCLK  
UART8\_RXD  
GPIO\_205/CLKIN\_AUX  
GPIO\_206  
GPIO\_210  
GPIO\_211  
GPIO\_212  
GPIO\_220  
GPIO\_221  
GPIO\_224

SPI AO

SPI0\_CLK/GPIO\_227/I3C\_SCL  
SPI0\_DI/GPIO\_228/I3C\_SDA  
SPI0\_DO/GPIO\_229  
SPI0\_CS0\_N/GPIO\_230  
SPI0\_CS1\_N/GPIO\_231  
SPI2\_CLK/GPIO\_213  
SPI4\_CLK  
SPI2\_DI/GPIO\_214  
SPI4\_DI  
SPI2\_DO/GPIO\_215  
SPI4\_DO  
SPI2\_CS0\_N/GPIO\_216  
SPI4\_CS0\_N  
SPI2\_CS1\_N/GPIO\_217  
SPI4\_CS1\_N  
SPI3\_CLK/GPIO\_144  
SPI3\_DI/GPIO\_145  
SPI3\_DO/GPIO\_146  
SPI3\_CS0\_N/GPIO\_147  
I2C7\_SCL  
SPI3\_CS1\_N/GPIO\_148  
I2C7\_SDA  
SPI3\_CS2\_N/GPIO\_149  
CDMA\_GPS\_SYNC/LTE\_GPS\_SYNC

ISP PERI

ISP\_GPIO00\_FTRSTN  
GPIO\_012  
ISP\_GPIO01\_BKRSTN  
GPIO\_013  
ISP\_GPIO02\_MNTRB  
GPIO\_014  
ISP\_GPIO06\_FSYNC  
GPIO\_015  
ISP\_GPIO10\_SBPWM  
GPIO\_016/LCD\_TE0  
ISP\_CLK0/GPIO\_017  
ISP\_CLK1/GPIO\_018  
ISP\_CLK2/GPIO\_019  
ISP\_SCL0/GPIO\_020  
ISP\_SDA0/GPIO\_021  
ISP\_SCL1/GPIO\_022  
ISP\_SDA1/GPIO\_023  
ISP\_SCL2/GPIO\_024  
ISP\_SDA2/GPIO\_025

SYS SIGNAL

CLK\_SLEEP  
CLK\_SYSTEM  
SYSCLK\_EN

PMU IF

SPMI\_CLK/GPIO\_226  
SPMI\_DATA/GPIO\_225  
PMU0\_SSI  
PMU\_AUXDAC0\_SSI/GPIO\_049  
PMU\_AUXDAC1\_SSI/GPIO\_050  
PMU\_PER\_EN  
SYS\_RSTIN\_N  
PMU\_RSTOUT\_N  
GPIO\_176\_PWR\_HOLD

BOOT CTRL

BOOT\_MODE  
DFT\_EN  
TEST\_MODE/GPIO\_001

LTE CTRL

LTE\_INACTIVE/GPIO\_051  
FRAME\_SYNC  
UART\_RXD\_BBP/UART\_CTS\_N\_MHS  
LTE\_RX\_ACTIVE/GPIO\_052  
UART\_RXD\_BBP/UART\_RXD\_MHS  
LTE\_TX\_ACTIVE/GPIO\_053  
UART\_TXD\_BBP/UART\_TXD\_MHS  
ISM\_PRIORITY/GPIO\_054  
UART\_RTS\_N\_MHS

PERI IO

GPS\_REF/GPIO\_005  
PWM\_OUT1/GPIO\_047  
GPIO\_000\_SWP  
GPIO\_055/ONEWIRE  
BOOT\_UFS/SPDIF

GPIO 012 LCM ENP  
GPIO 013 MCAM0 RST  
GPIO 014 IR CAM PWDN  
GPIO 015 TP RST N  
LCD TE0  
ISP\_CLK0 MCAM0  
ISP\_CLK1 SCAM1  
ISP\_CLK2 MCAM1  
ISP\_SCL0 MCAM0  
ISP\_SDA0 MCAM0  
ISP\_SCL1 SCAM1  
ISP\_SDA1 SCAM1  
ISP\_SCL2 MCAM1  
ISP\_SDA2 MCAM1  
PMU0\_CLK32 SYS  
SYS CLK  
SYS CLK EN  
SPMI\_CLK  
SPMI\_DATA  
PMU AUXDAC0 SSI  
PMU PERI EN  
PMU RST OUT N  
SOC RST PMU N  
PMU PWR HOLD  
BOOT MODE  
DFT EN  
GPIO 051 LTE INACTIVE  
GPIO 053 LTE TX ACTIVE  
AP GPS REF CLK

GPIO 008 MIPI SW SEL  
GPIO 009 LCD ID0  
GPIO 010 CC EN  
GPIO 011 LCD BL EN  
WL SDIO CLK  
WL SDIO CMD  
WL SDIO DATA0  
WL SDIO DATA1  
WL SDIO DATA2  
WL SDIO DATA3  
GPIO 134 SPK SMARTPA\_RST  
GPIO 136 MCAM1 RST  
GPIO 137 SPK ID

SD CARD

SD\_CLK/GPIO\_160  
SD\_CMD/GPIO\_161  
JTAG\_TMS\_SD  
SD\_DATA0/GPIO\_162  
SD\_DATA1/GPIO\_163  
JTAG\_TDI\_SD  
SD\_DATA2/GPIO\_164  
JTAG\_TDO\_SD  
SD\_DATA3/GPIO\_165  
JTAG\_TRST\_N\_SD  
VDD\_ODIO\_BIAS\_SD

AO JTAG

JTAG\_MODE  
JTAG\_SELO  
JTAG\_SEL1  
JTAG\_TCK\_SWCLK/GPIO\_178  
JTAG\_TDI/GPIO\_180  
JTAG\_TDO/GPIO\_181  
JTAG\_TMS\_SWCLK/GPIO\_179  
JTAG\_TRST\_N

USIM

USIM0\_CLK/GPIO\_166  
USIM0\_RST/GPIO\_167  
USIM0\_DATA/GPIO\_168  
VDD\_ODIO\_BIAS\_USIM0  
USIM1\_CLK/GPIO\_169  
USIM1\_RST/GPIO\_170  
USIM1\_DATA/GPIO\_171  
VDD\_ODIO\_BIAS\_USIM1

NFC IO

SWP\_IO

GPIO 003 USB MOS CTRL  
GPIO 031 CODEC RST N  
GPIO 032 SCAM0 RST N  
GPIO 033 PMU1 EN  
GPIO 034 LCM ENN  
GPIO 039 Hi1102 PWRON  
GPIO 040 NFC EN  
GPIO 036 FLASH EN  
DEBUG UART6 RXD  
DEBUG UART6 TXD  
GPIO 029 LCD0 RST N  
GPIO 030 NFC DWL REQ

I2C AO

I2C0\_SCL/GPIO\_186/I3C\_SCL  
I2C0\_SDA/GPIO\_187/I3C\_SDA  
I2C1\_SCL/GPIO\_188  
I2C1\_SDA/GPIO\_189  
I2C2\_SCL/GPIO\_190  
I2C7\_SCL  
I2C2\_SDA/GPIO\_191  
I2C7\_SDA  
PMUI2C1\_SCL/GPIO\_150  
SPMI\_CLK  
PMUI2C1\_SDA/GPIO\_151  
SPMI\_DATA/PMU0\_SSI  
I2C6\_SCL/GPIO\_199  
I2S2\_DO/UART8\_RTS\_N  
I2C6\_SDA/GPIO\_198  
I2S2\_DI/UART8\_CTS\_N

I2C PERI

I2C3\_SCL/GPIO\_006  
I2C3\_SDA/GPIO\_007  
I2C4\_SCL/GPIO\_026  
I2C4\_SDA/GPIO\_027  
PMUI2C0\_SCL/GPIO\_003  
PMUI2C0\_SDA/GPIO\_004

UART

UART2\_CTS\_N/GPIO\_031  
UART0\_RXD  
UART2\_RTS\_N/GPIO\_032/LCD\_TE0  
UART0\_TXD  
UART2\_TXD/GPIO\_033  
UART0\_RTS\_N  
UART2\_RXD/GPIO\_034  
UART0\_CTS\_N  
UART3\_CTS\_N/GPIO\_039  
UART5\_CTS\_N  
UART3\_RTS\_N/GPIO\_040  
UART5\_RTS\_N  
UART3\_RXD/GPIO\_041  
UART5\_RXD  
UART3\_TXD/GPIO\_042  
UART5\_TXD  
UART4\_CTS\_N/GPIO\_043  
UART4\_RTS\_N/GPIO\_044  
UART4\_RXD/GPIO\_045  
UART4\_TXD/GPIO\_046  
UART6\_CTS\_N/GPIO\_035  
UART0\_RXD  
UART6\_RTS\_N/GPIO\_036  
UART0\_TXD  
UART6\_RXD/GPIO\_037  
UART0\_RXD\_M/UART\_RXD\_MHS  
UART6\_TXD/GPIO\_038  
UART0\_TXD\_M/UART\_TXD\_MHS  
UART\_RXD\_UC/GPIO\_029  
UART\_TXD\_UC/GPIO\_030

DS1 interface 5 of 10

DS2 interface 6 of 10

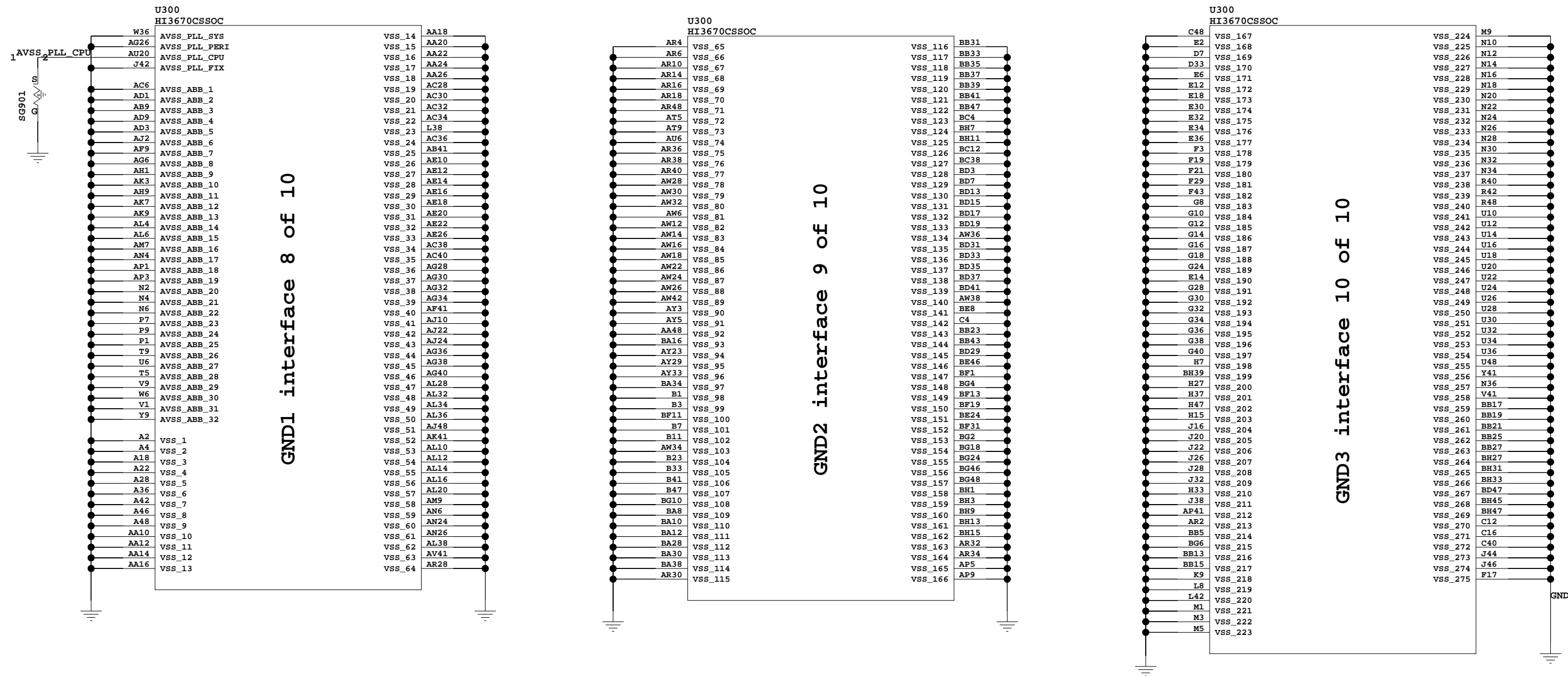
I2C For Charger Circuits pulled to BUCK8

VOUT18 1V8 R719 1.5K I2C0\_SCL  
R718 1.5K I2C0\_SDA  
VOUT18 1V8 R716 1.5K\*\* I2C3\_SCL  
R717 1.5K\*\* I2C3\_SDA  
VOUT18 1V8 R710 1.5K I2C4\_SCL  
R711 1.5K I2C4\_SDA  
VOUT18 1V8 R706 1.5K I2C1\_SCL  
R707 1.5K I2C1\_SDA  
VBUCK8 1V8 R708 1.5K I2C6\_SCL  
R709 1.5K I2C6\_SDA  
VOUT4 1V85 R720 1.5K TP I2C7\_SCL  
R713 1.5K TP I2C7\_SDA

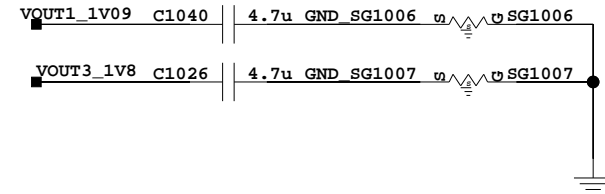




9.SOC GND

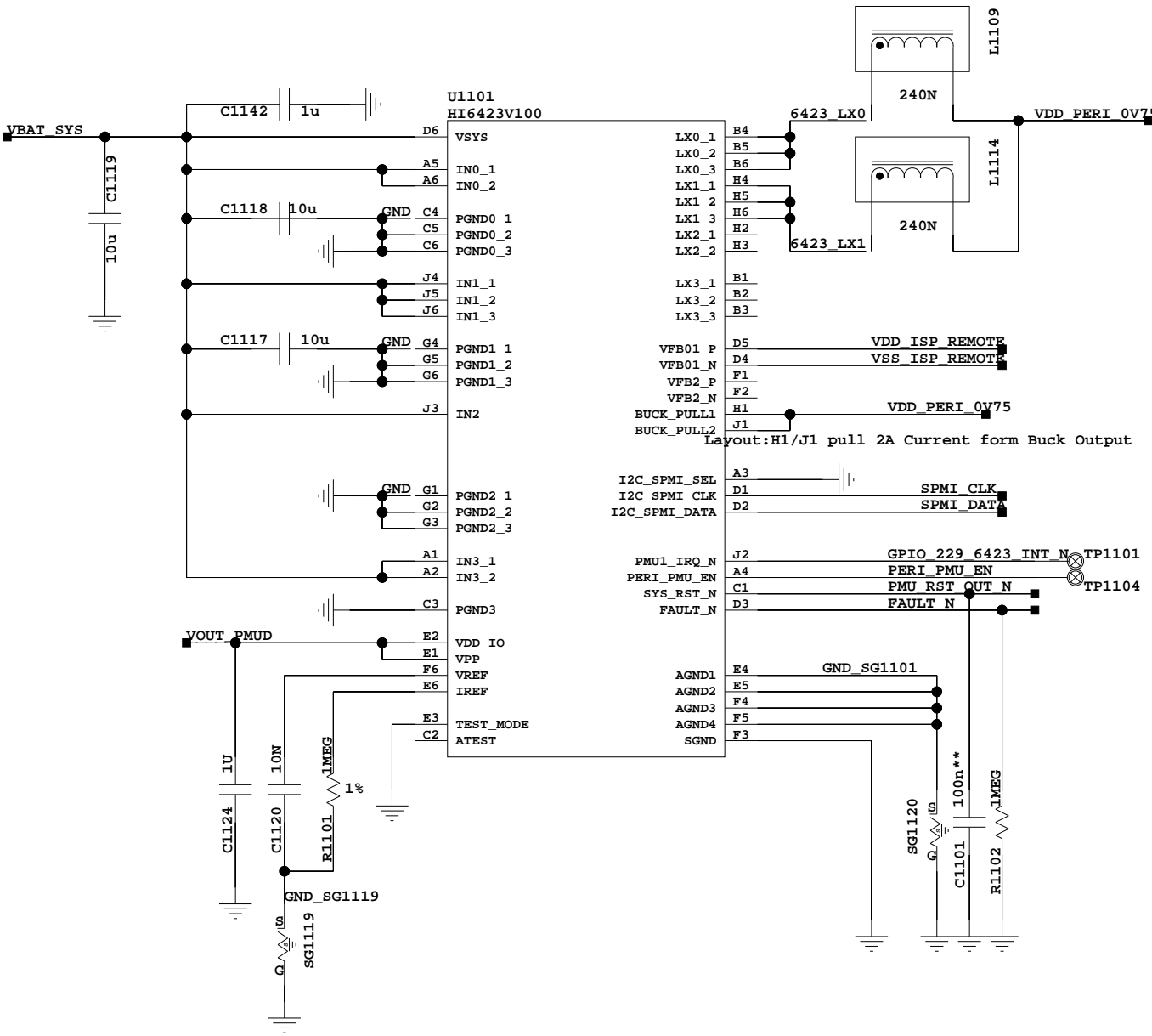
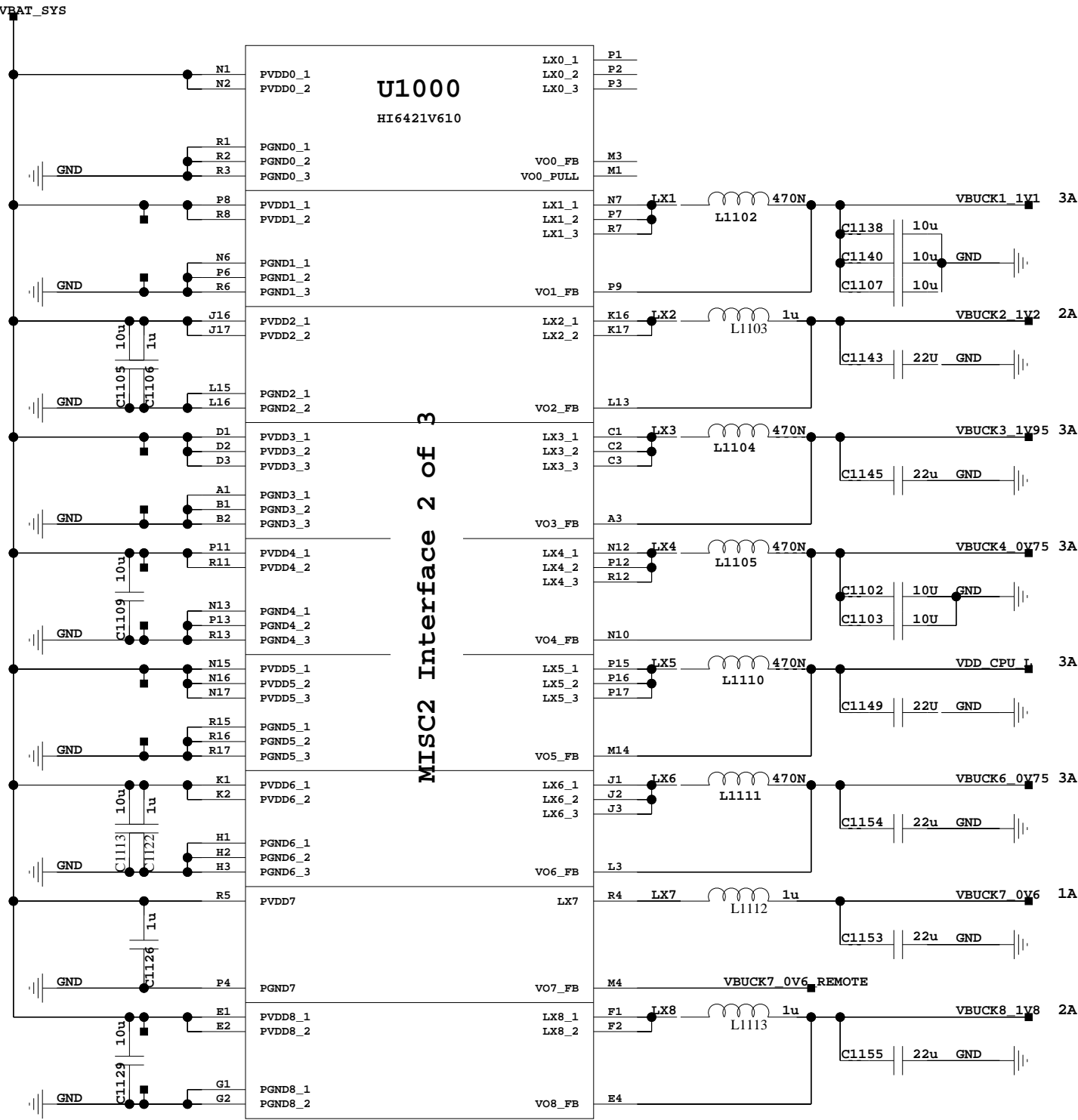


NUM	Vol	Current	Function
LDO0	0.75	300	SOC:UFS,SYS,PLL_SYS
LDO1	1.09	350	RFIC0 AVDD10
LDO2	1.8	120	SOC_EFUSE&HISEE
LDO3	1.8	360	RFIC AVDD18,LNA_VDD
LDO4	1.85	350	LCD&TP 1.8V IO
LDO5	1.8	350	SOC 1.8V AVDD
LDO6	0.85	550	SOC:AVDD085_ABB
LDO7	1.8	350	SOC:AVDD18_ABB
LDO8	1.8	250	IOVDD FOR Codec/RF
LDO9	1.8	50	SOC SDIO 1.8V
LDO11	1.8/2.95	50	SIM0
LDO12	1.8/2.95	50	SIM1
LDO13	2.8	150	CAM_AVDD
LDO14	2.85	50	RF switch VDD
LDO15	2.95	800	UFS_VCC
LDO16	2.95	800	SDCARD VDD
LDO17	3.3	200	MCAM_AFVDD1
LDO18	1.8	400	PERI IOVDD
LDO19	1.2	400	MCAM_DVDD0
LDO20	1.1	400	MCAM_DVDD1
LDO21	1.8	180	CAM IOVDD
LDO22	1.09	350	RESEVERD
LDO23	3.2	150	USB 2.0 PHY/PA
LDO24	2.8	200	Sensor VDD
LDO25	2.85	150	MCAM_AFVDD0
LDO26	1.7	30	38.4MHZ XO CORE
LDO27	1.8	30	HKADC,XOADC
LDO28	1.8	120	RF switch VIO
LDO29	1.8	120	VPH_UFS,PLL_SYS
LDO30	0.75	400	FIX 0.75 For SOC
LDO32	1.1	400	SlaveCAM_DVDD
LDO33	2.8	150	MCAM_AVDD0
LDO34	3.3	200	FP VDD
LDO35	2.9	50	CODEC_AVDD
LDO36	1.2	10	UFS refclk/rst IO



11.Hi6421 BUCK AND Hi6423

Hi6423



**A**



FAST_PWRON_SEL	
0	1
NORMAL	FAST

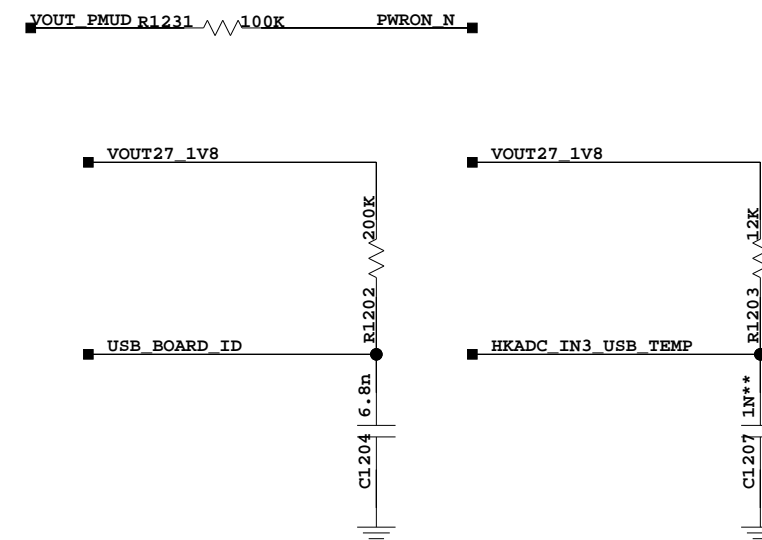
SPMI_SSI_SEL	
0	1
SPMI	SSI

## BOARD ID Table

## BUCK BOOST

The schematic diagram illustrates a buck-boost converter circuit. The central component is the U1201 (39111331) IC, which is configured as a buck-boost converter. The input side features a 10uF capacitor (C1211) connected to the VBAT SYS input. The output side includes a 121K resistor (R1215) and a 37.4K resistor (R1216) forming a feedback network. The output voltage is regulated by a feedback network consisting of resistors R1215 (121K) and R1216 (37.4K). The output capacitor is C1214 (22uF). The circuit also includes an input inductor L1201 (1uH) and an output capacitor C1206 (680pF). The IC is connected to ground through several pins, including SGND1, SGND2, PGND1, PGND2, and PGND3. The output voltage is labeled VOUT PMU 1V8.

Trace	Resistor	Value	Node	Resistor	Value	Node
1	R1229	150K	HKADC IN2	R1230	20K	VOUT27 1V8
2	R1228	150K**	HKADC IN1	R1207	150K	VOUT27 1V8
3	R1224	30K	HKADC IN0	R1208	100K	VOUT27 1V8



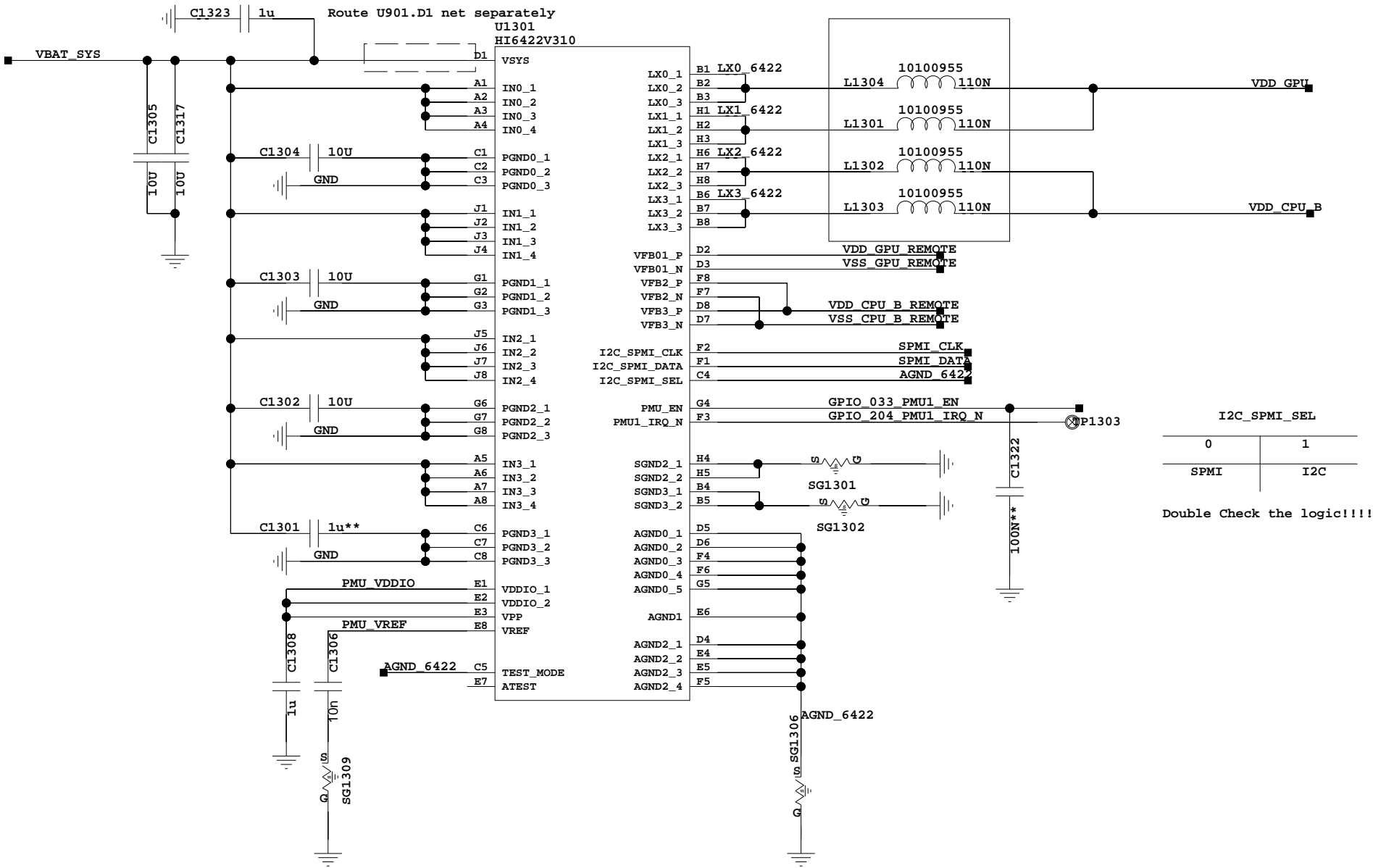
A

B

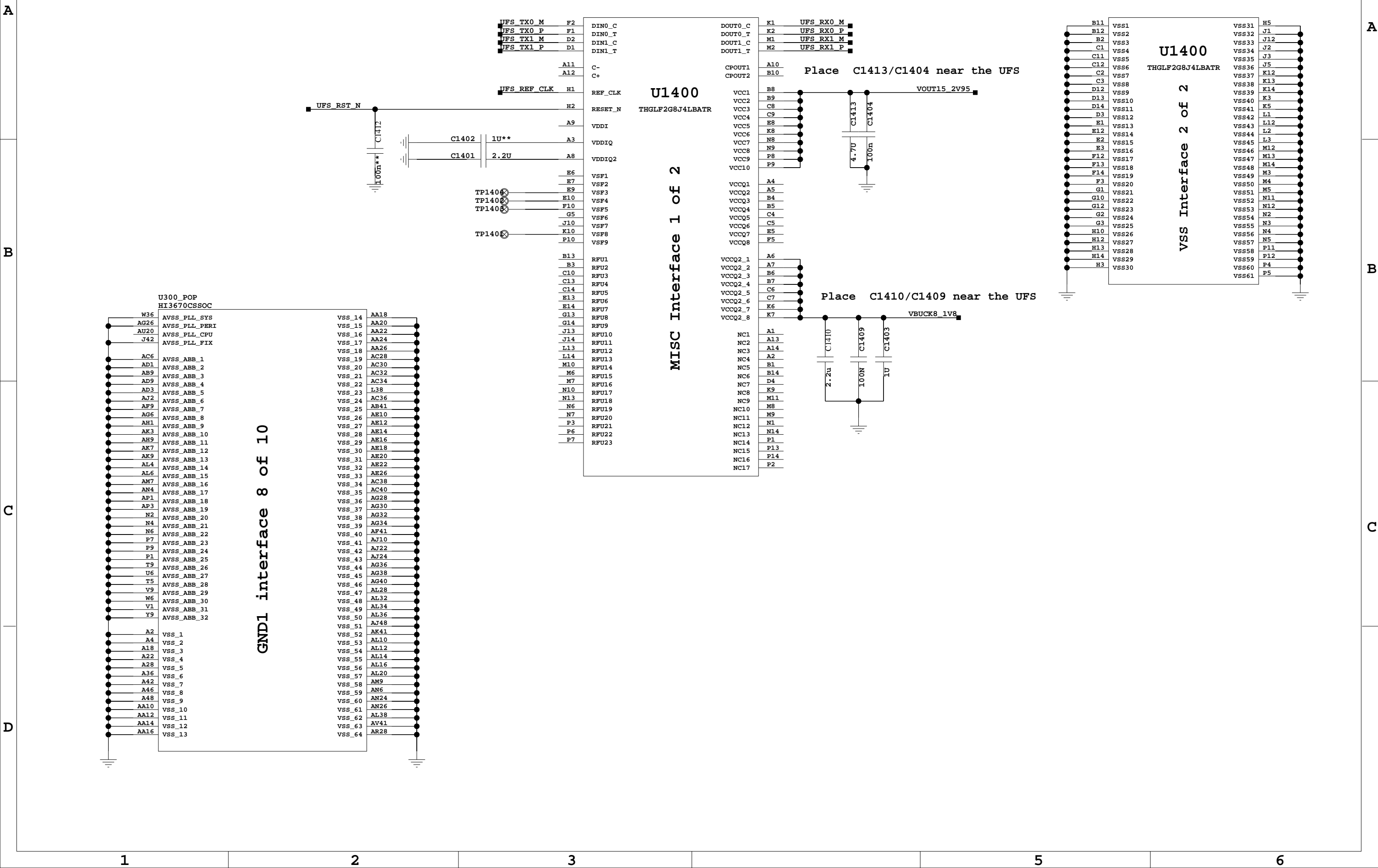
C

[illegible]

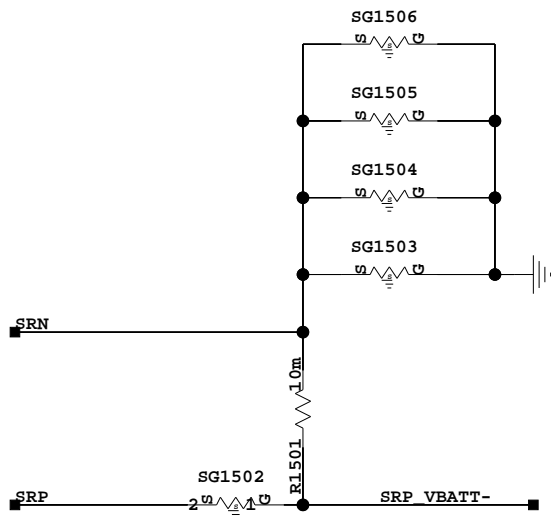
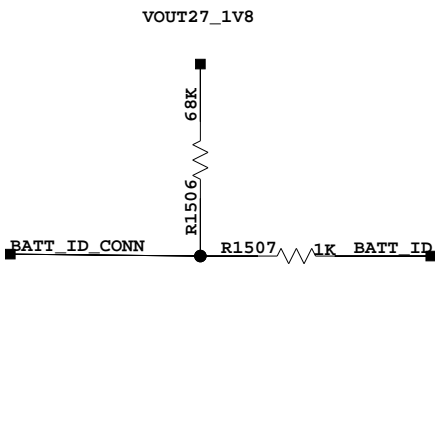
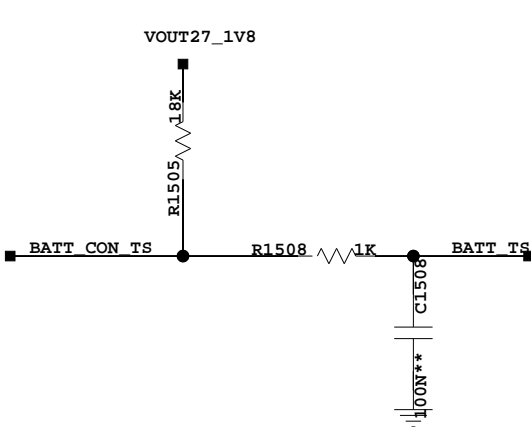
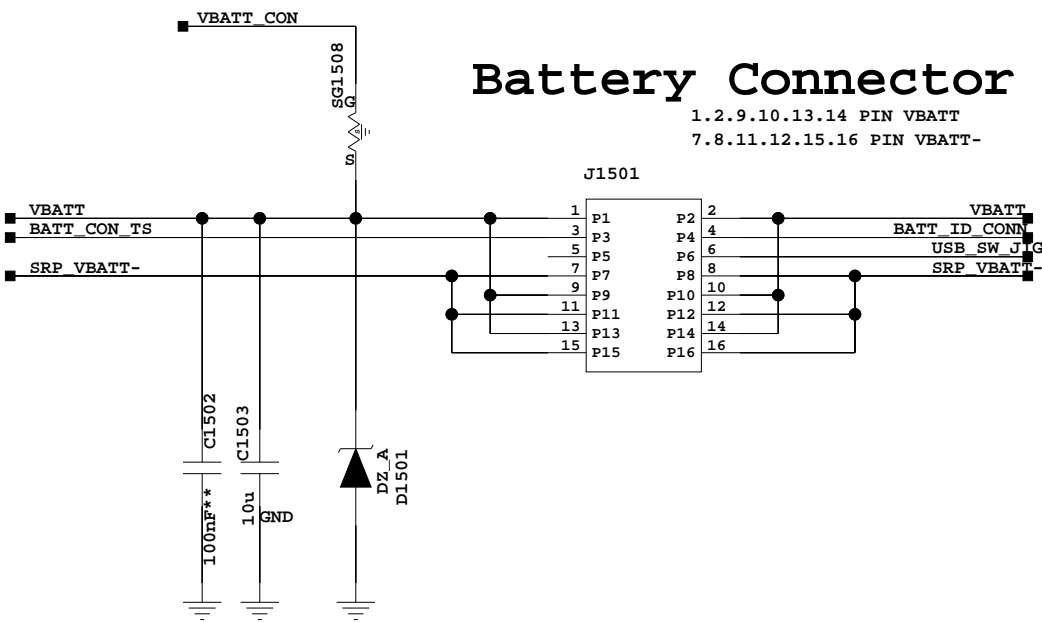
13.Hi6422V300



1	2	3	4	5	
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# 15. Battery & Fuel guage



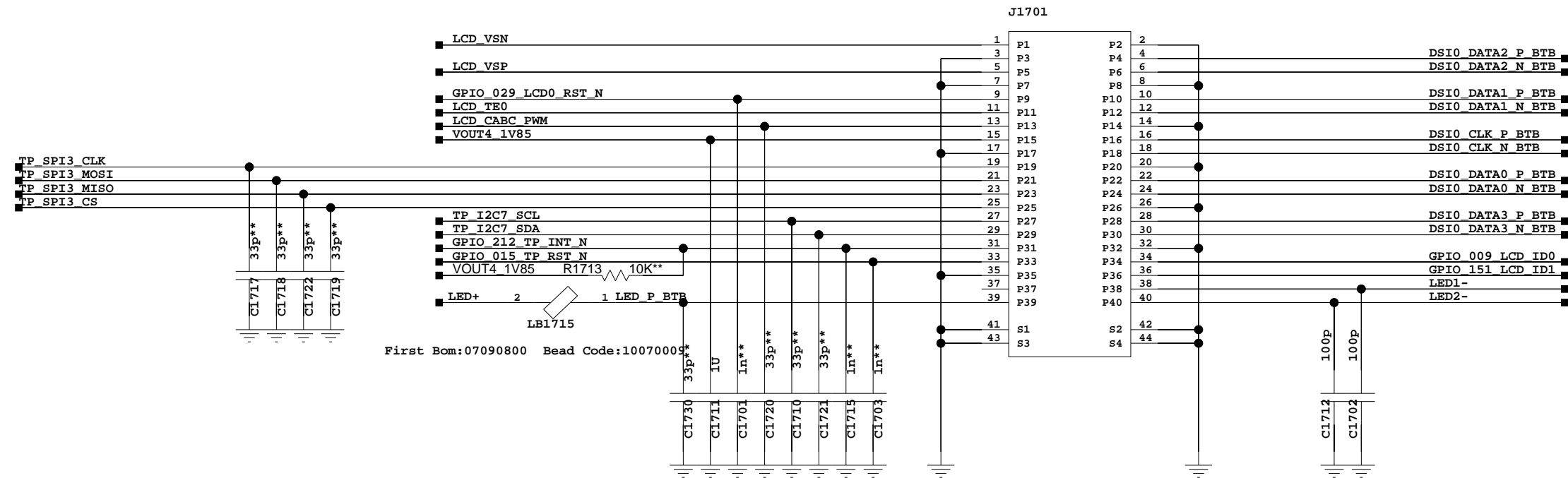
CAD note:  
1.Trace for 9A  
2.Differential trace

**A**

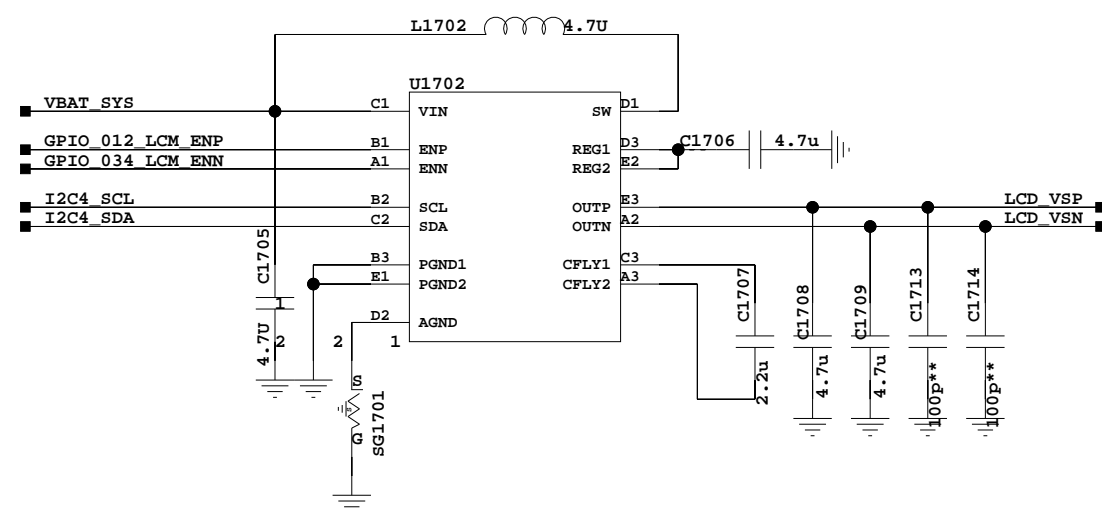




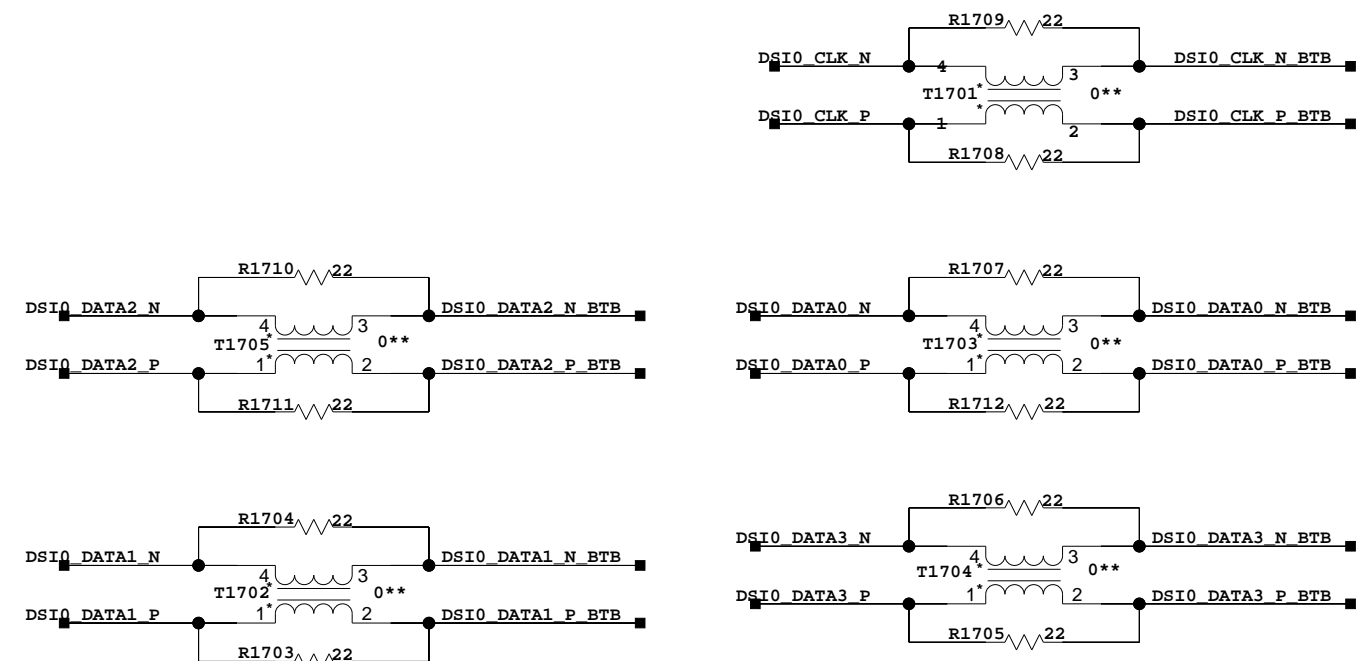
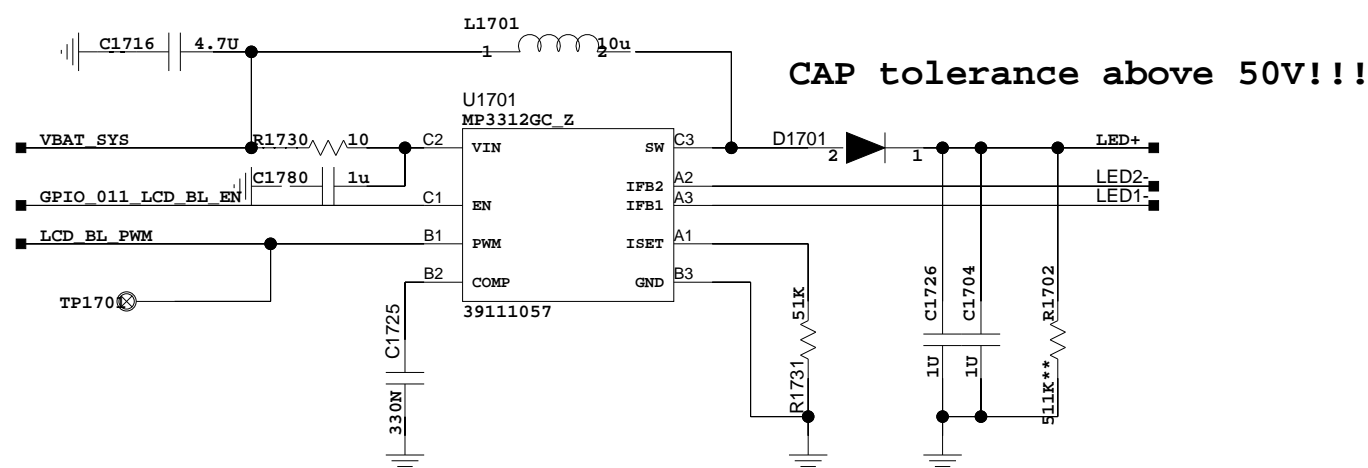
# 17. LCD and TP INTERFACE



## LCD POS/NEG Voltage Driver

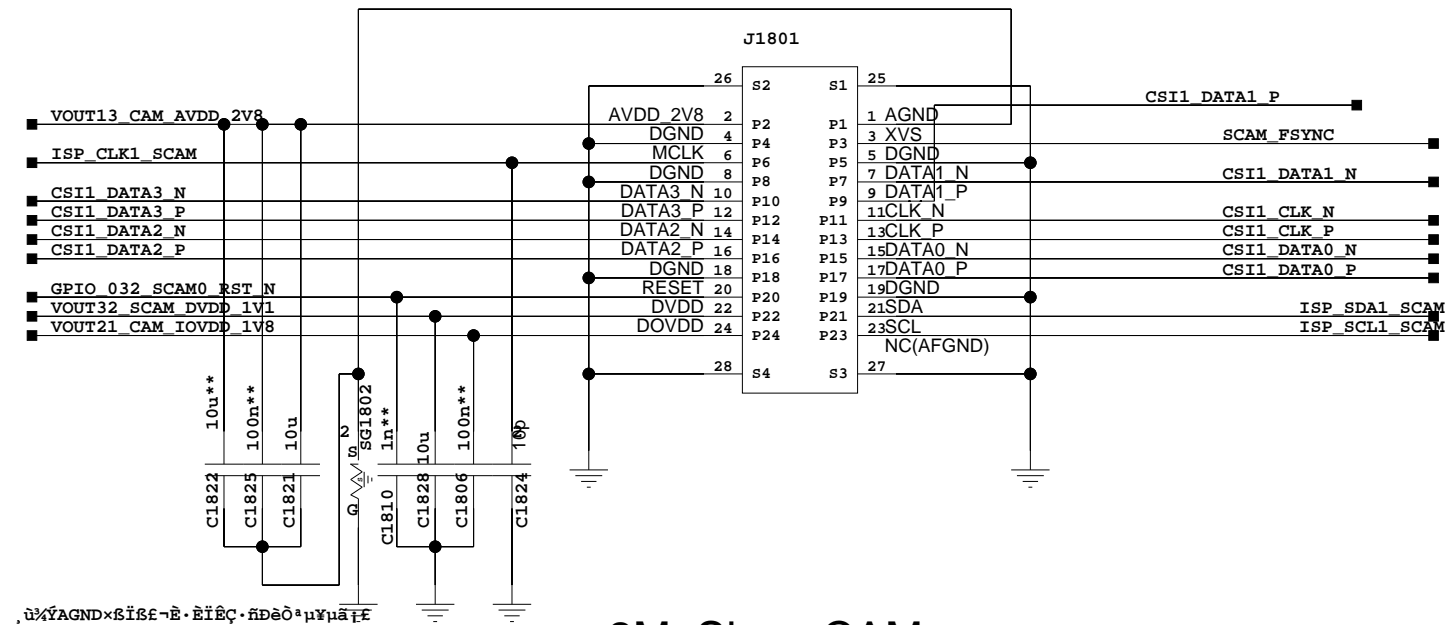


## LCD BL DRIVER

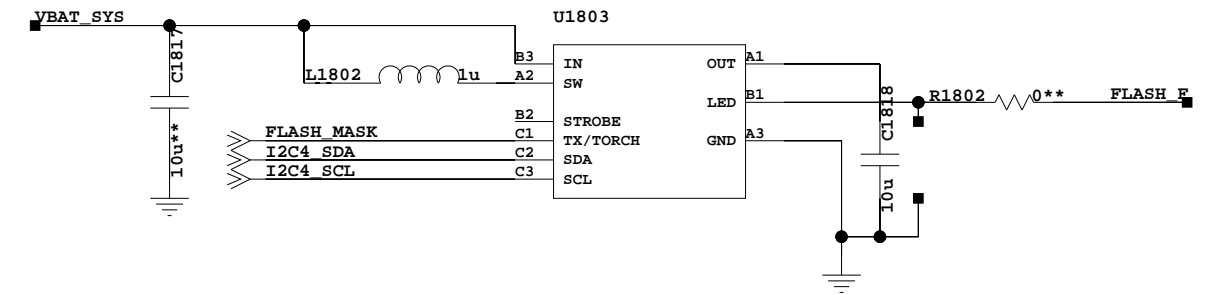


# 18. Front Camera/Flash

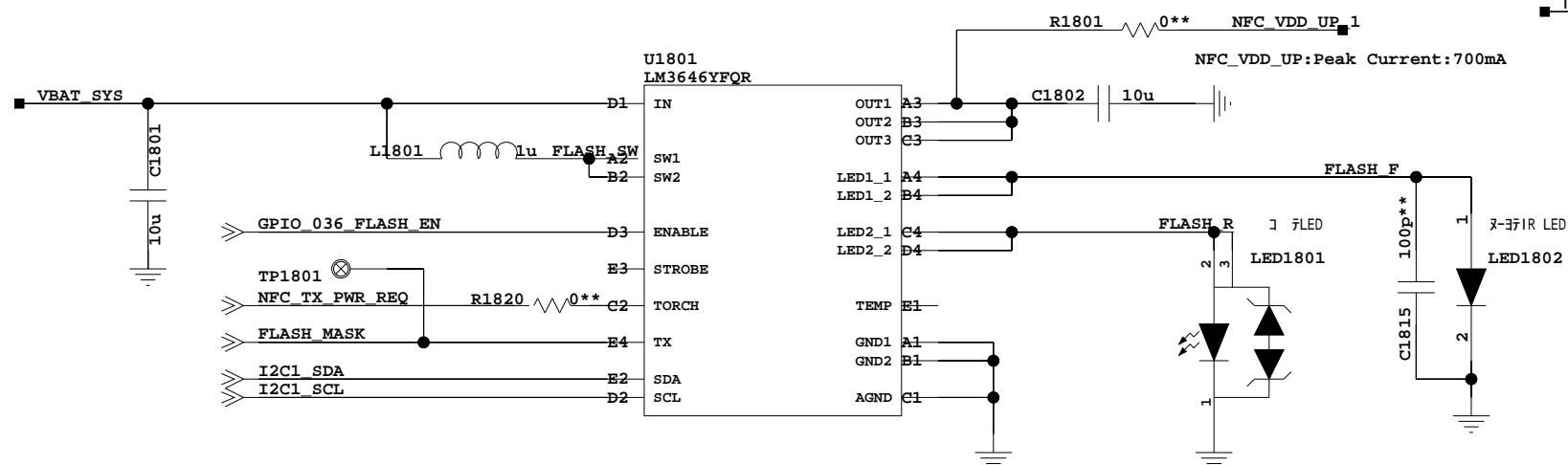
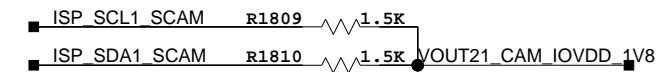
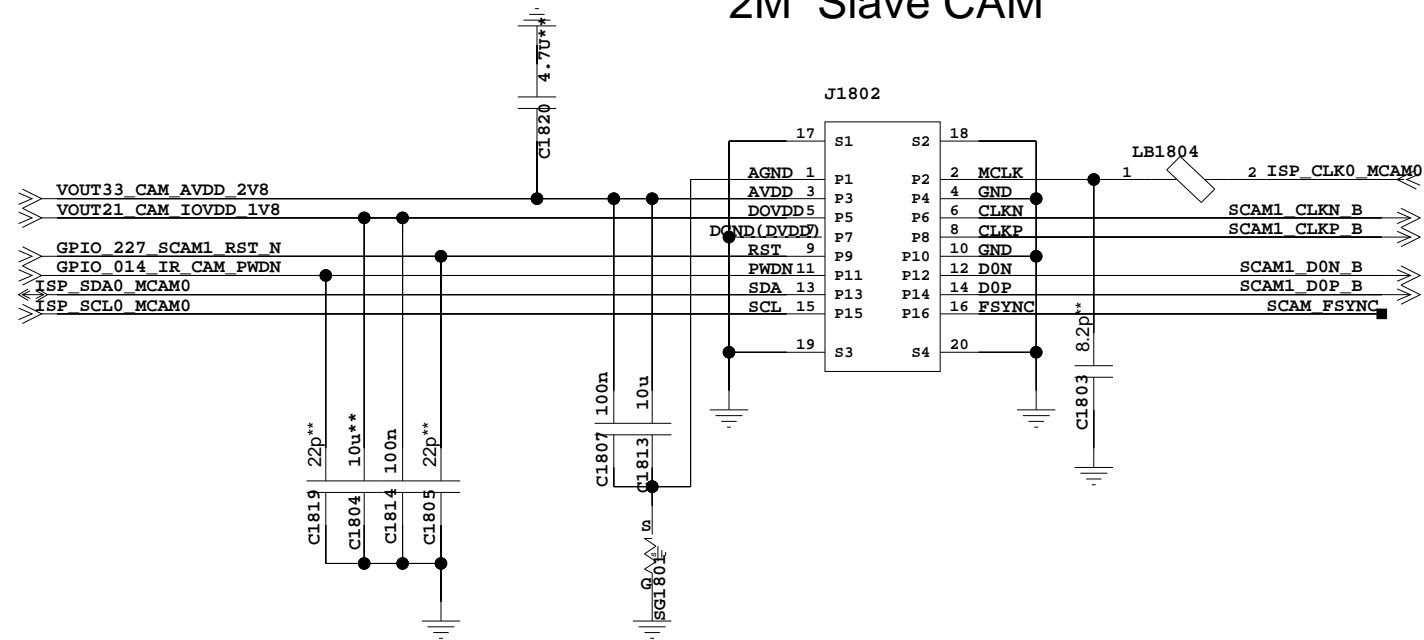
## 24M Slave CAM



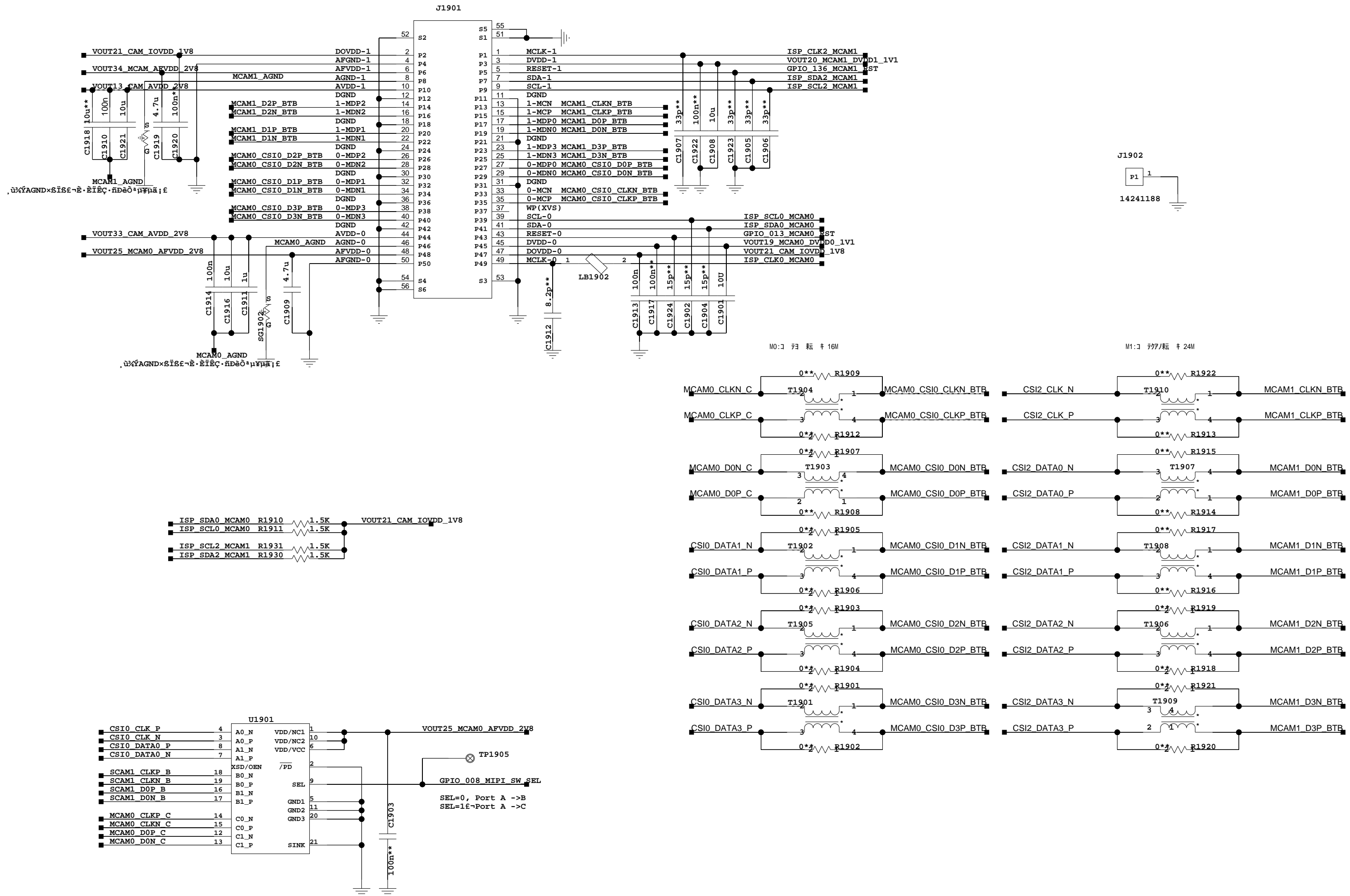
## IR LED闪烁ノカ



## 2M Slave CAM

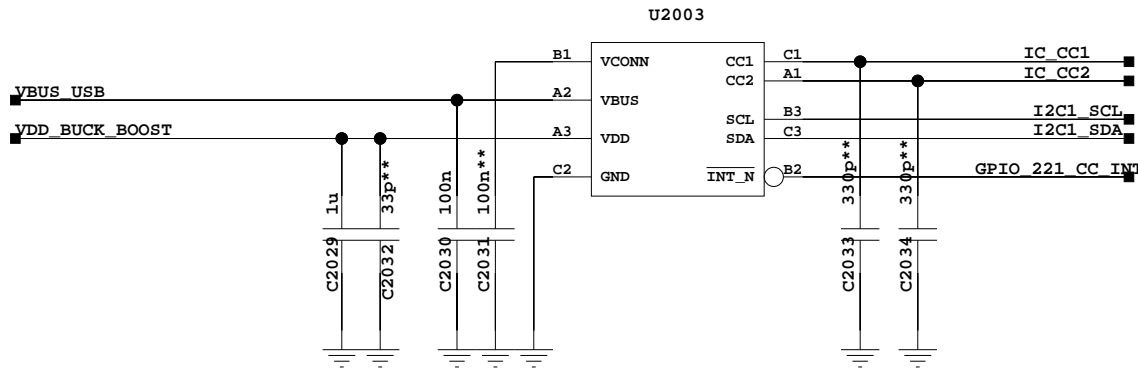


## 19. M0/M1

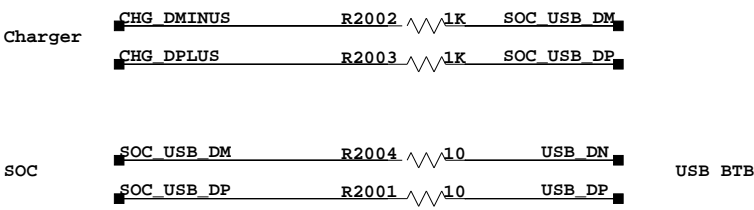
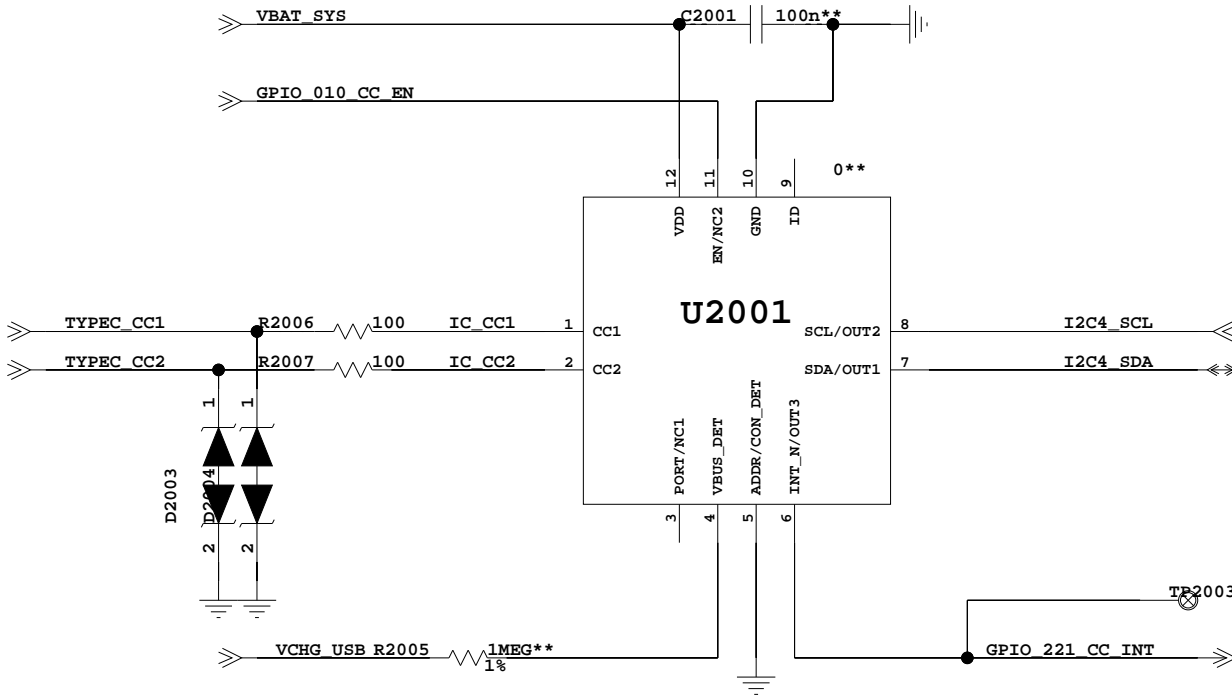


20. USB

PD

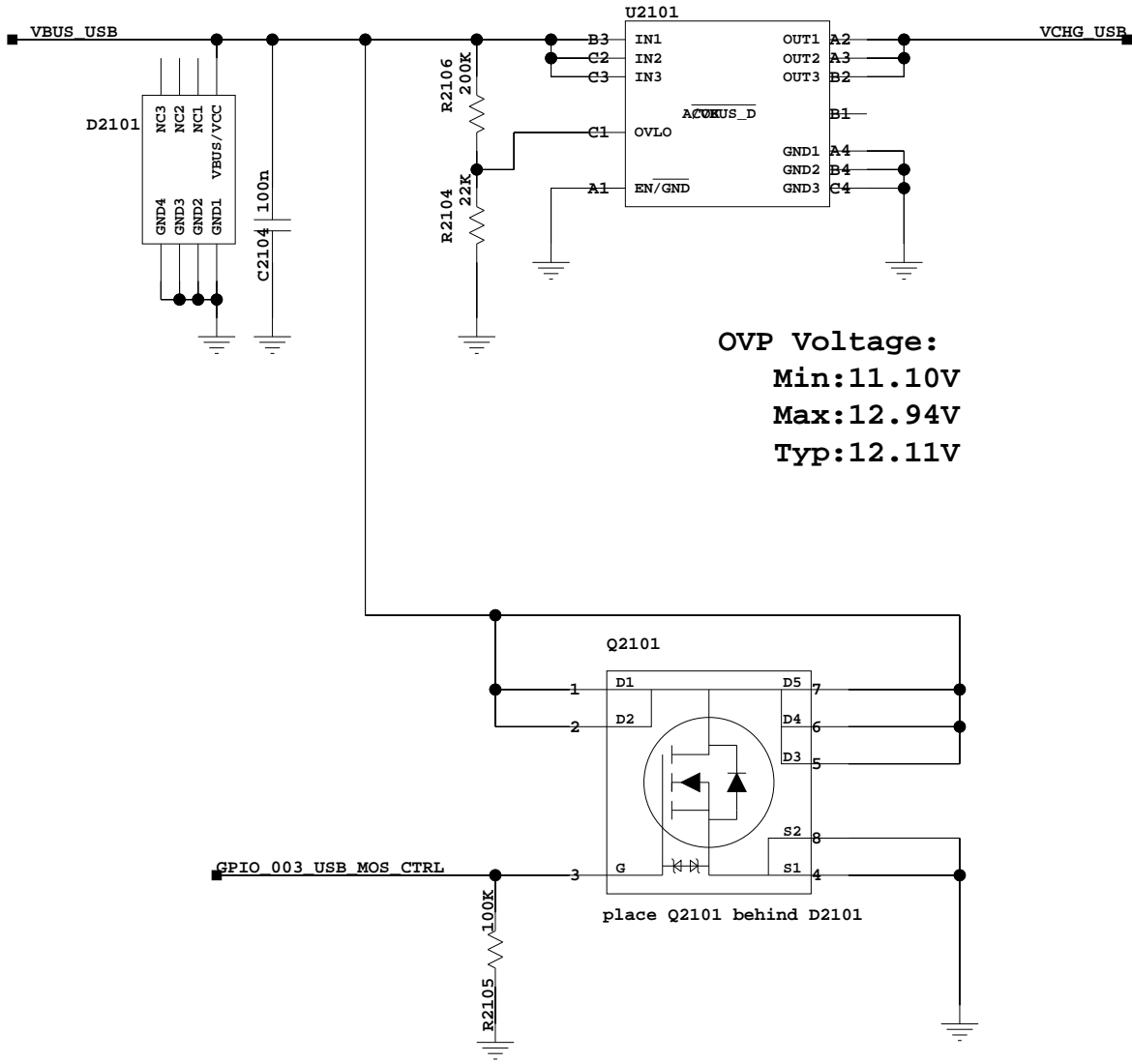
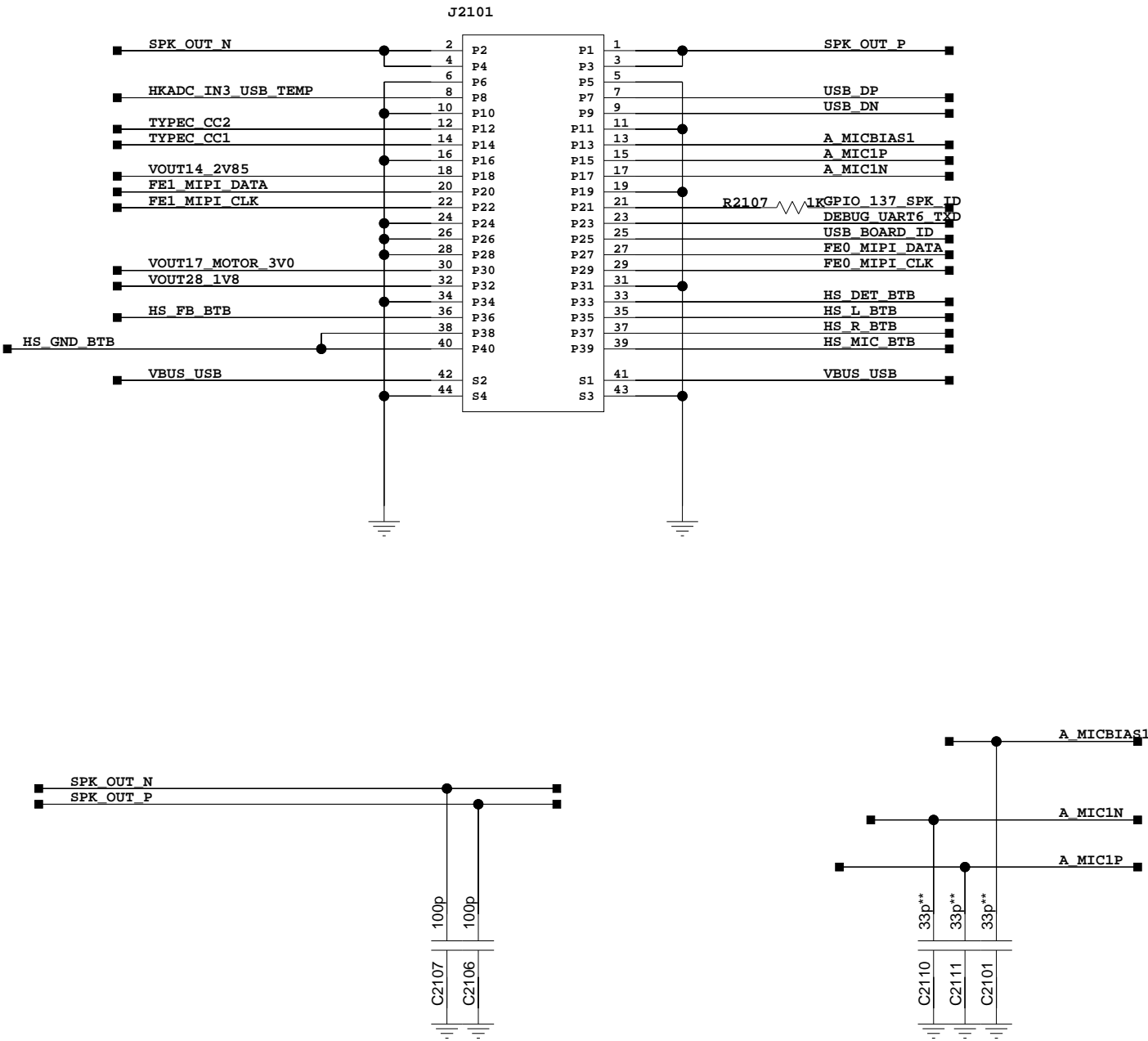


CC

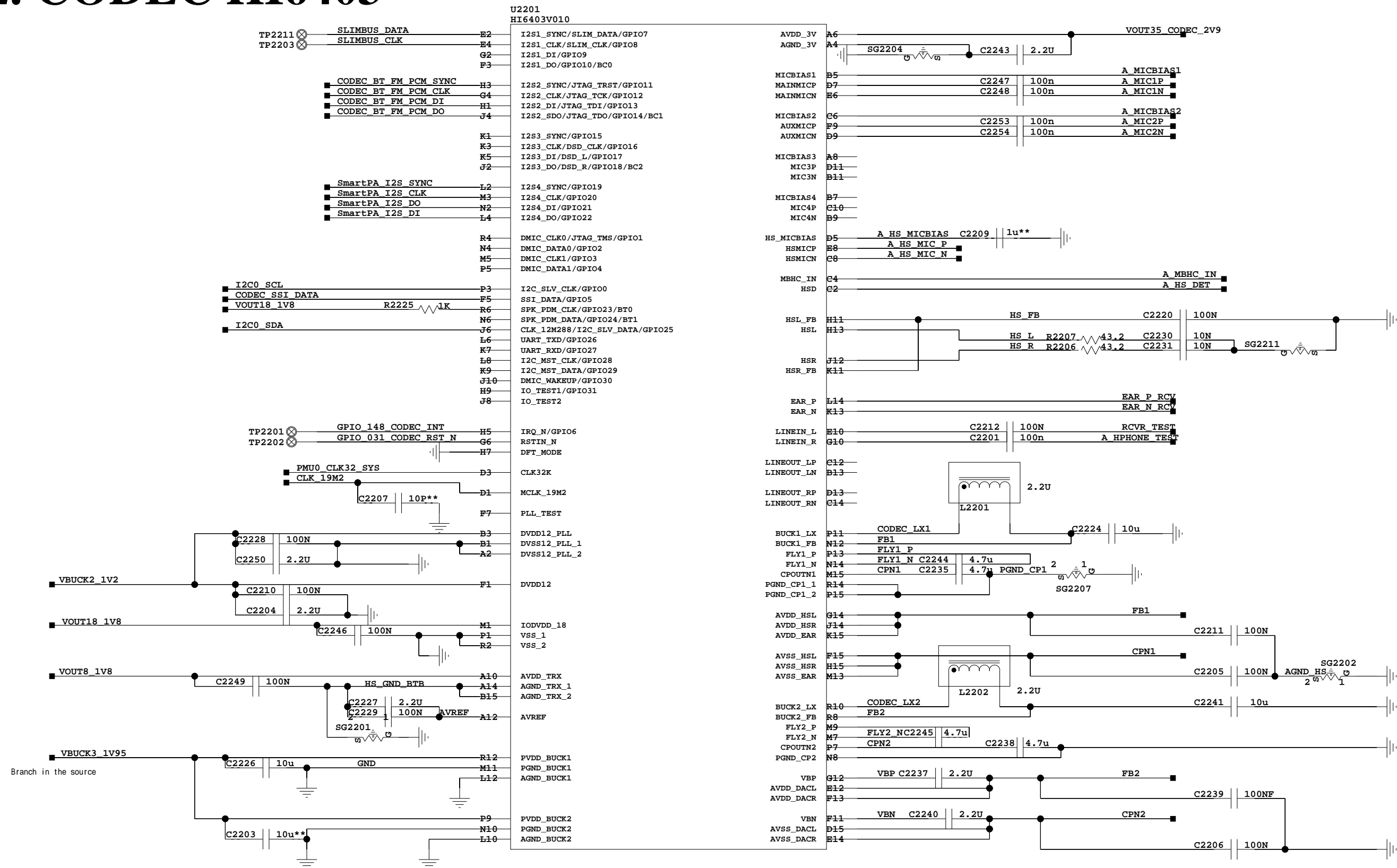


# 21. Main FPC

## Main BTB



## 22. CODEC HI6403



BootMode0	BootMode1	Function(BootROM Start)
1	1	SPI Start
1	0	SSI Start
0	1	I2C Start
0	0	SLIMBUS Start

1

2

3

4

5

6

# 23. SC Charge

A

A

B

B

C

C

D

1

2

3

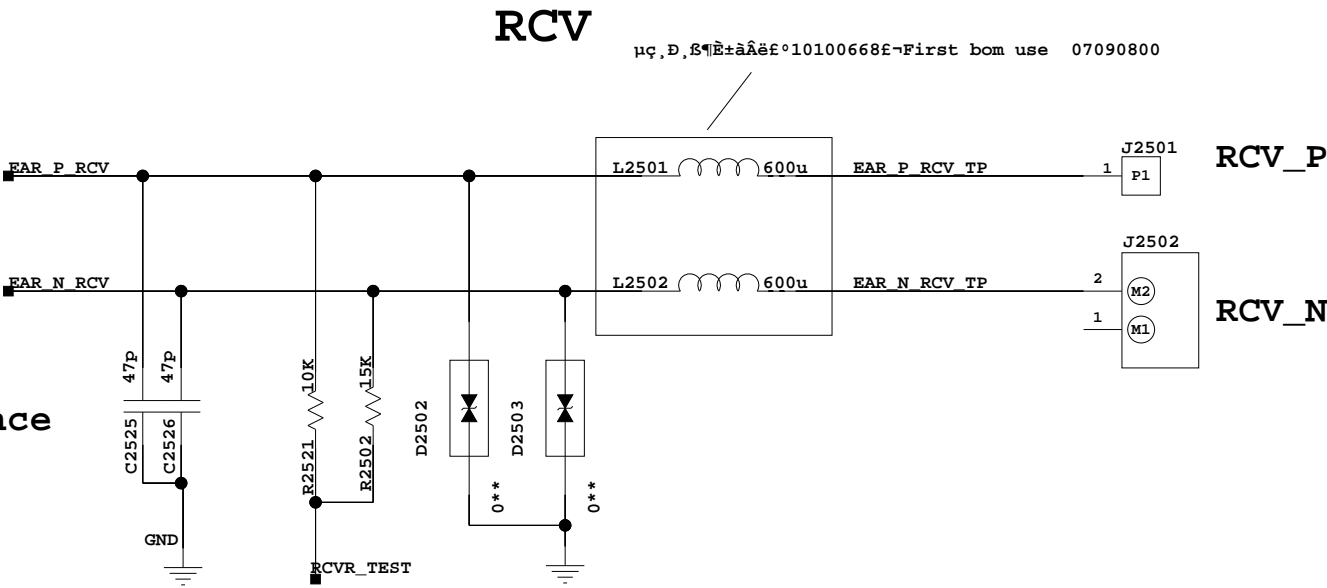
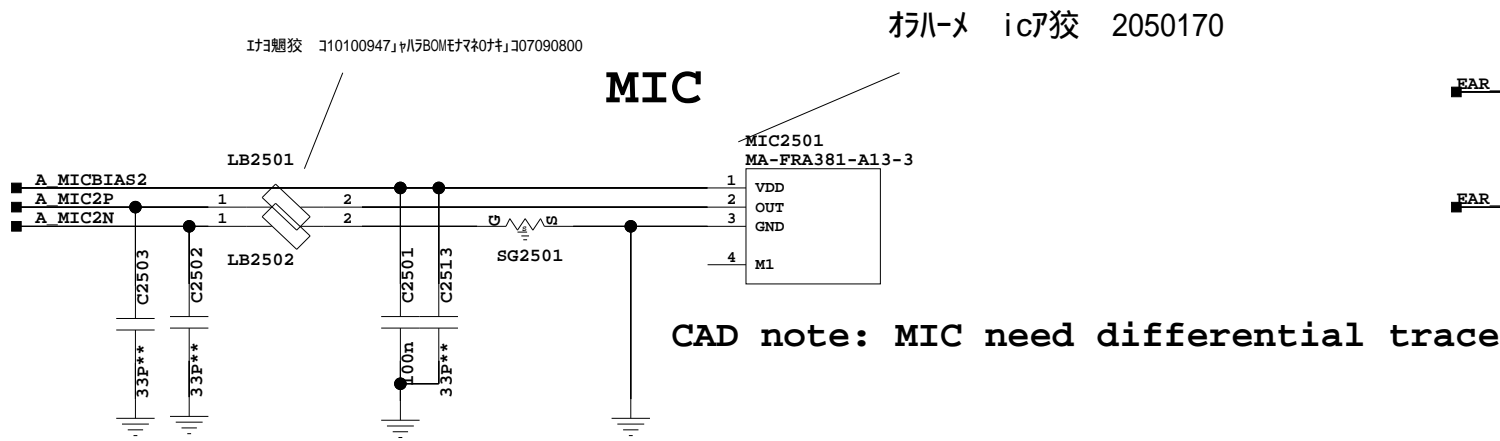
5

6

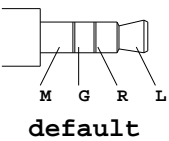
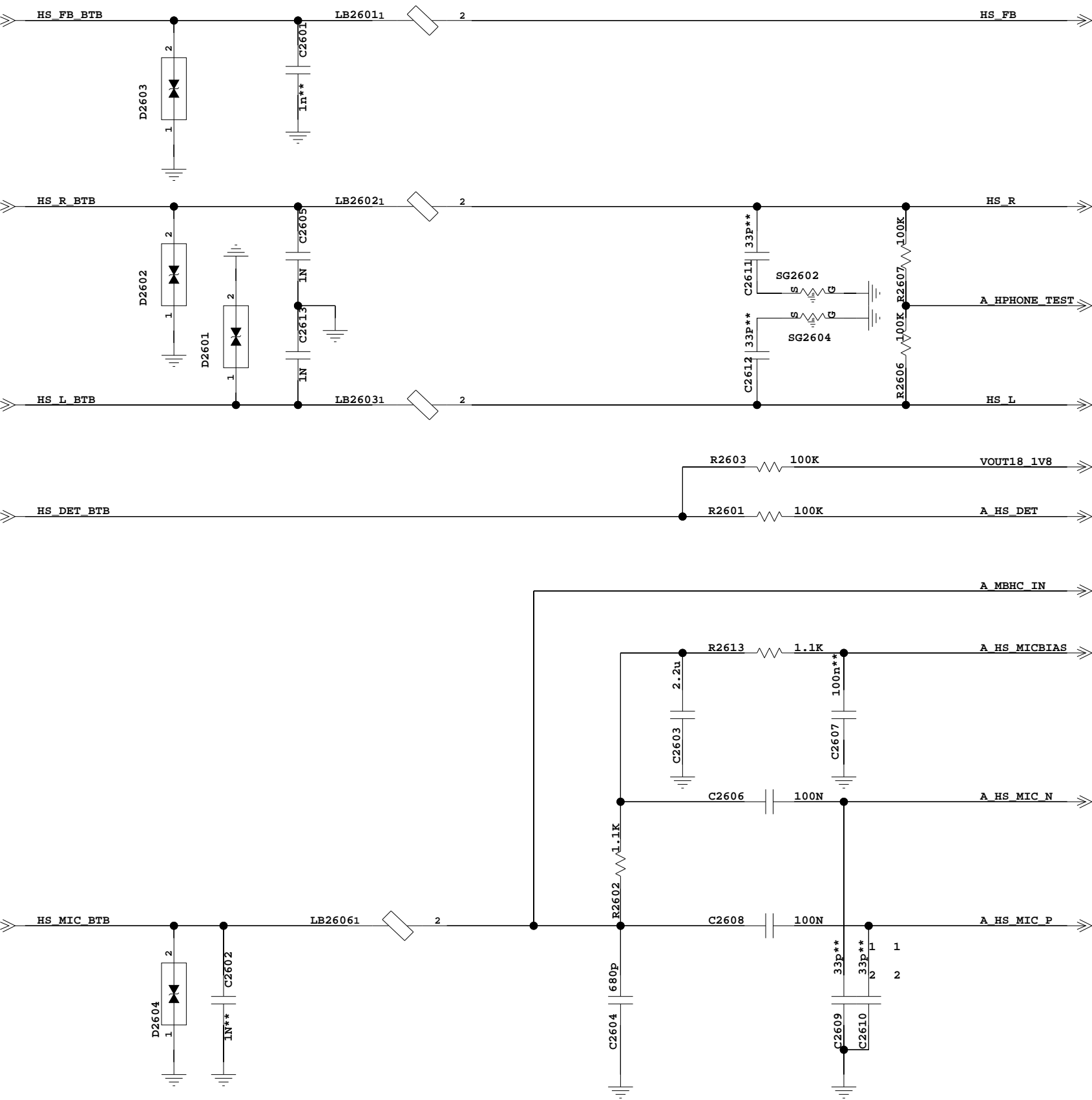
## 24. SPK SMART PA



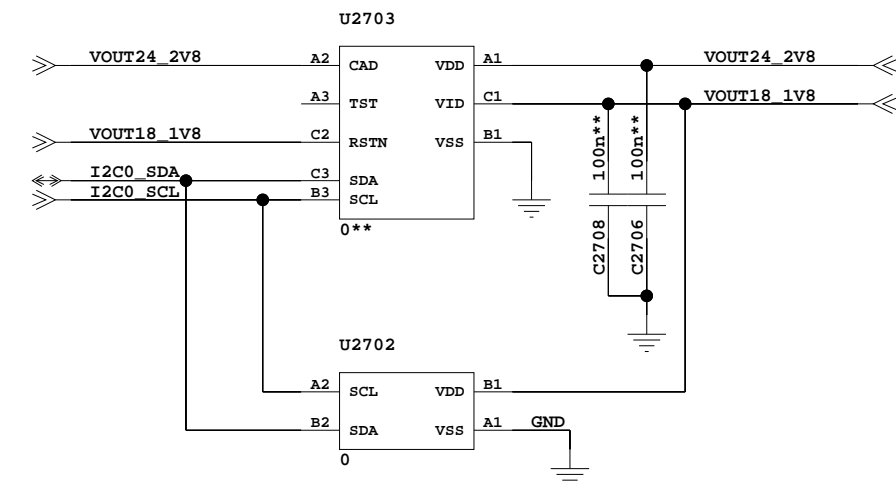
# 25. MIC/REC/HAC/HIFI



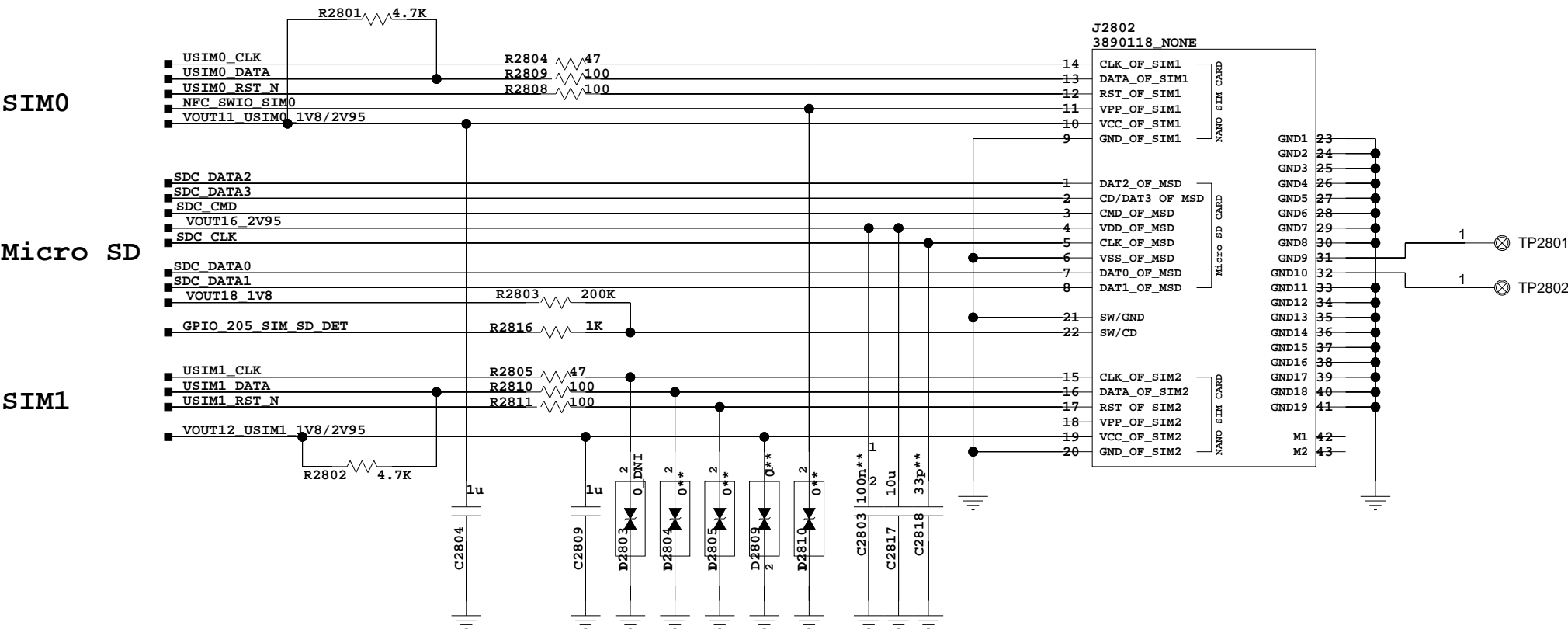
# 26. Headphone



## D



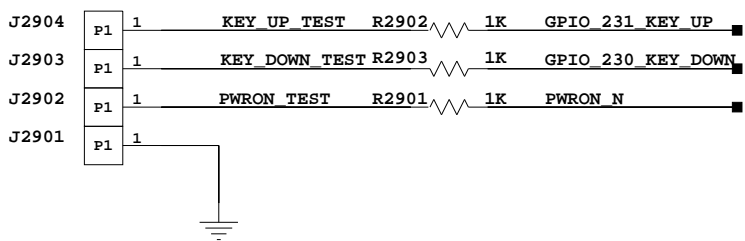
28.SIM/uSD Card



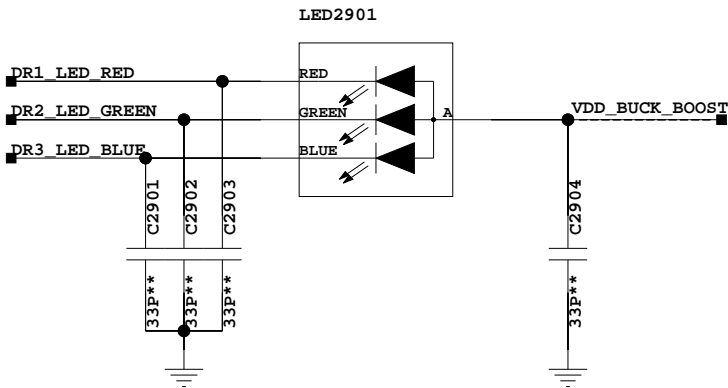
GPIO_202 \ SIM1_VCC	SIM1_VCC	
	SE_VCC	VOUT12_2V95
H		
L		

# 29. LED/FP/Key

KEY SPRING

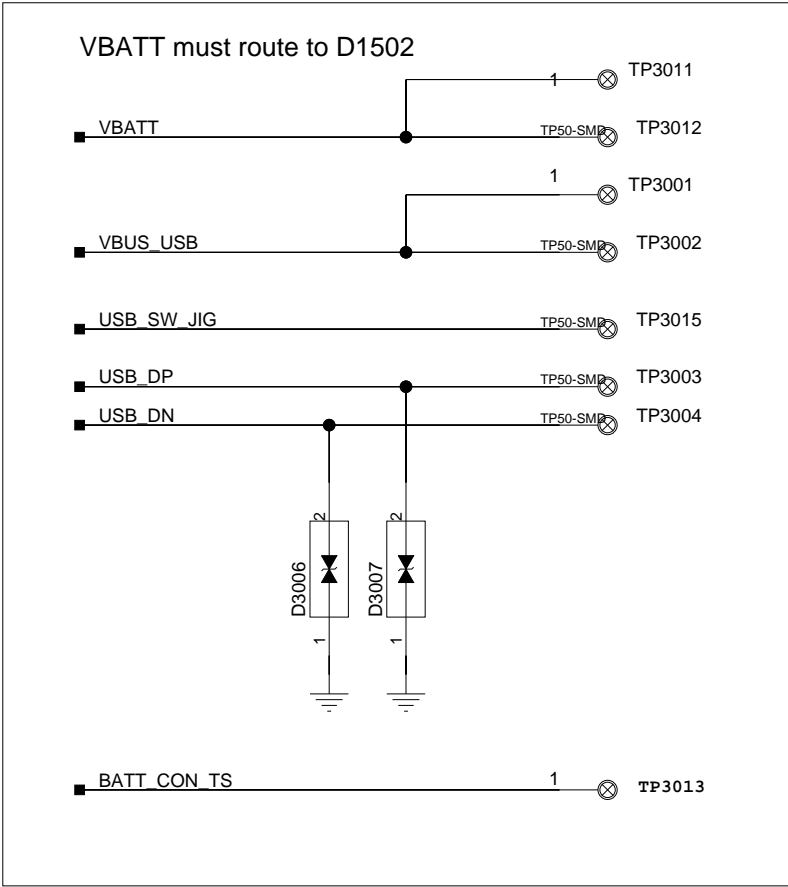


RGB LED

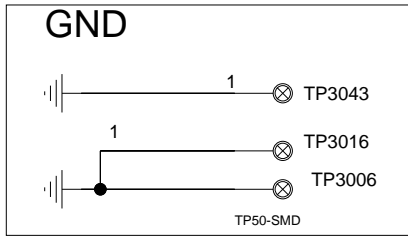
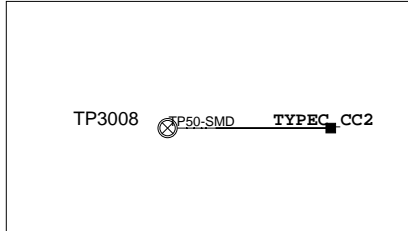
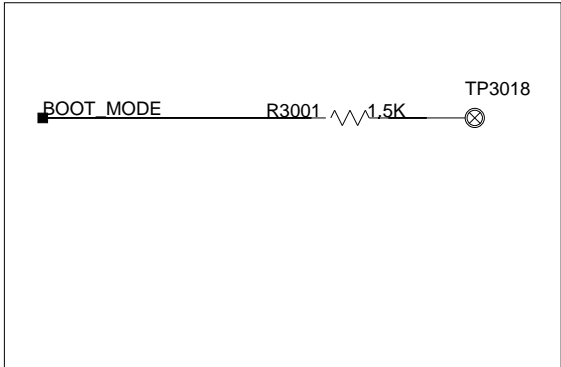


# 30. Test Points/Shields

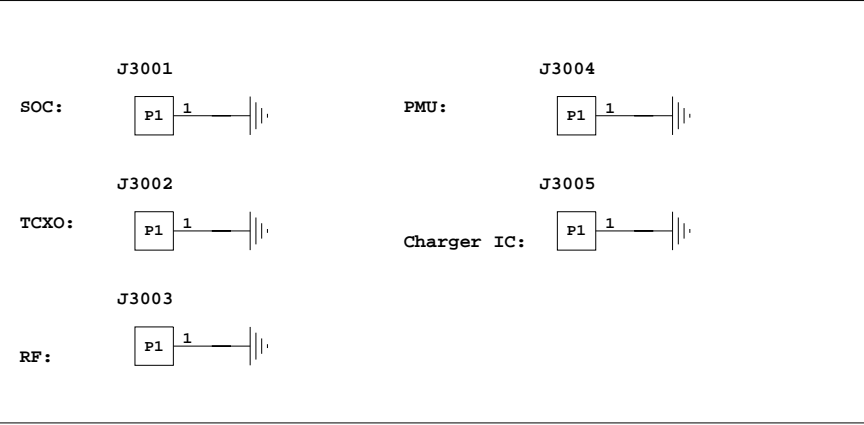
## CBT/PT



## BOOT MODE



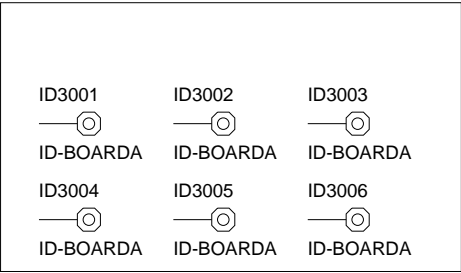
## Shielding



## HOLE

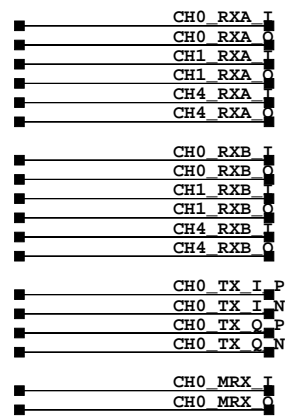


## MARK POINT

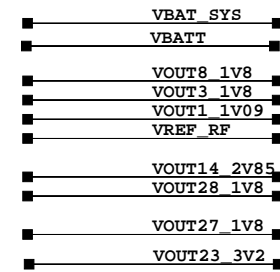


# 31.RF Interface

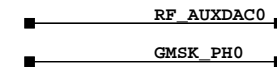
## RFIC IQ



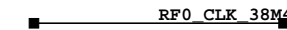
## POWER



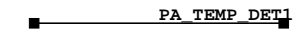
## GSM



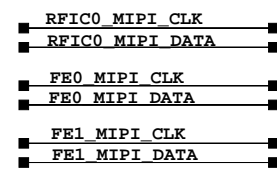
## CLK



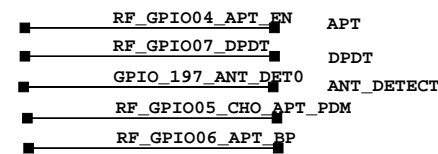
## HKADC



## MIPI Interface



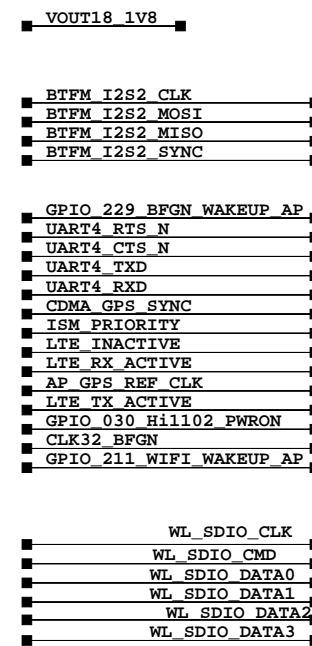
## GPIO Interface



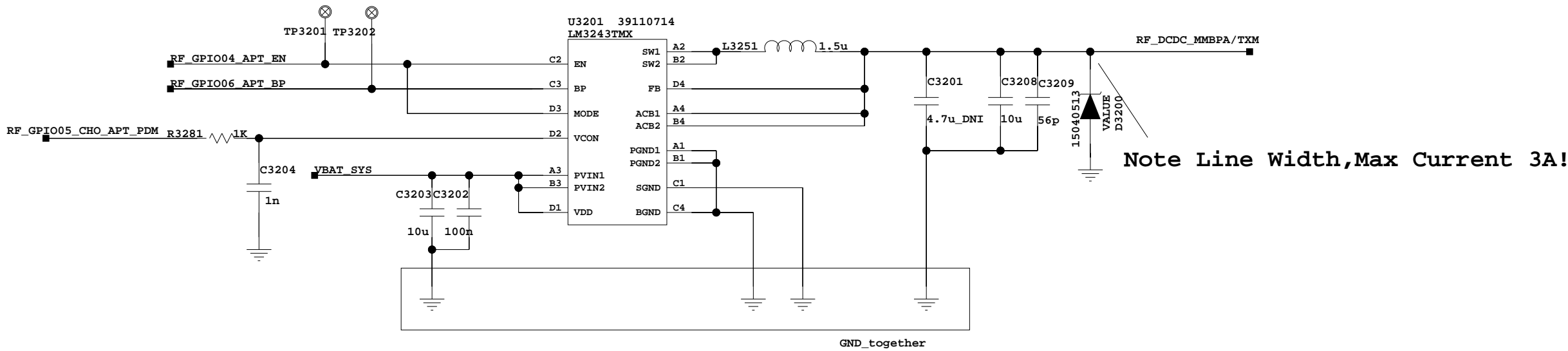
## ANT Interface

Bostonニフイ/セ

## NC Interface



32 APT\_LM3243





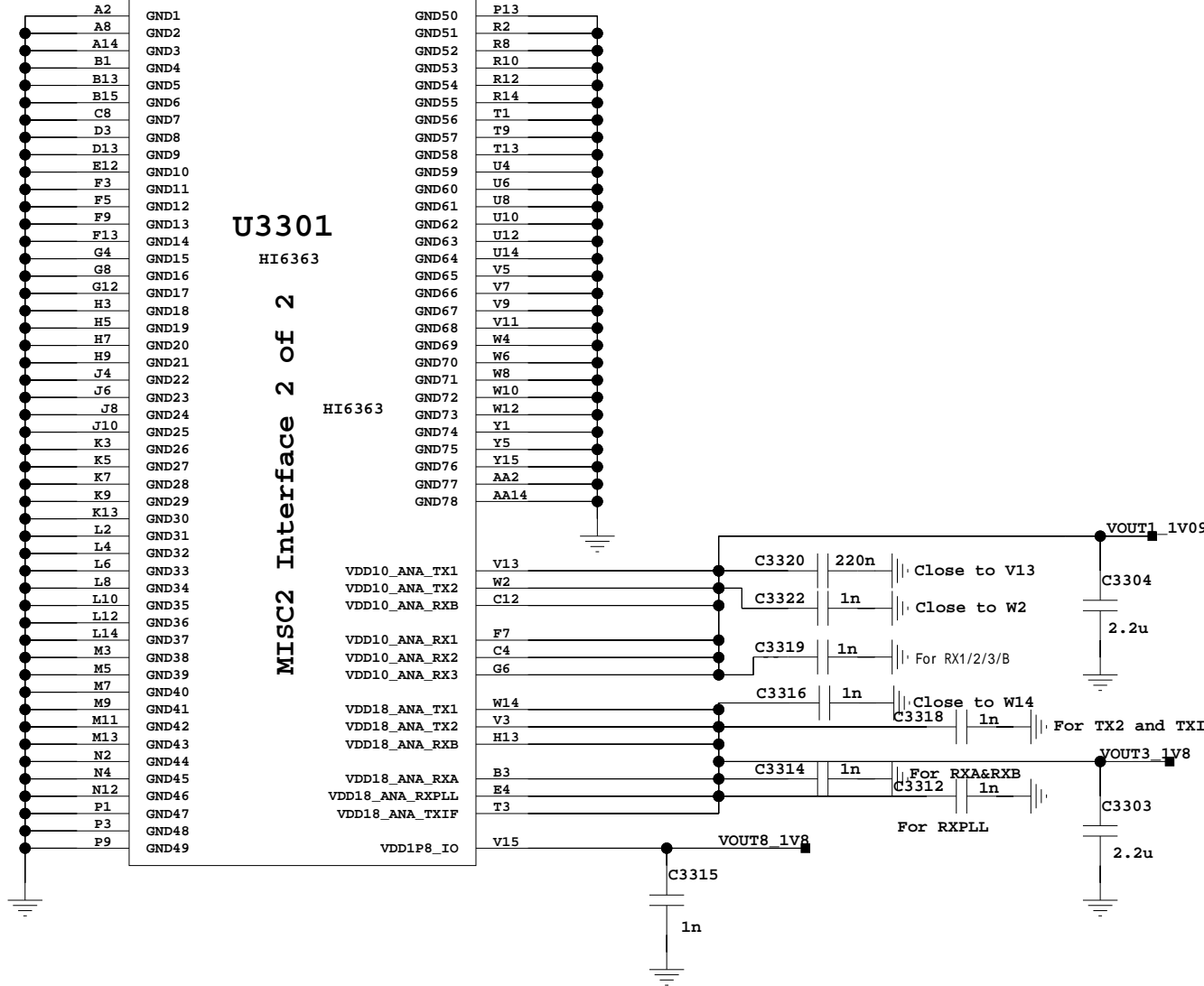
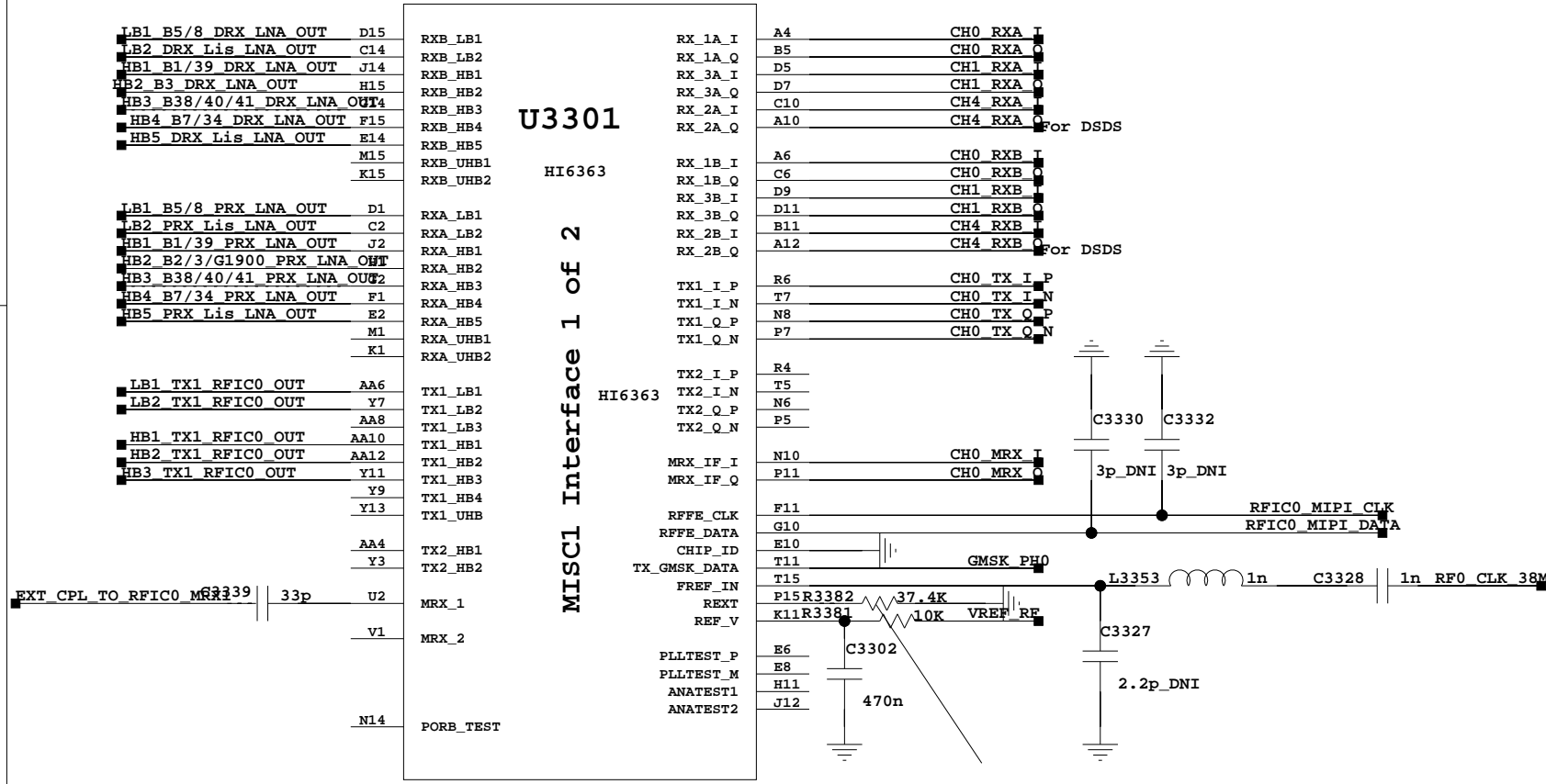
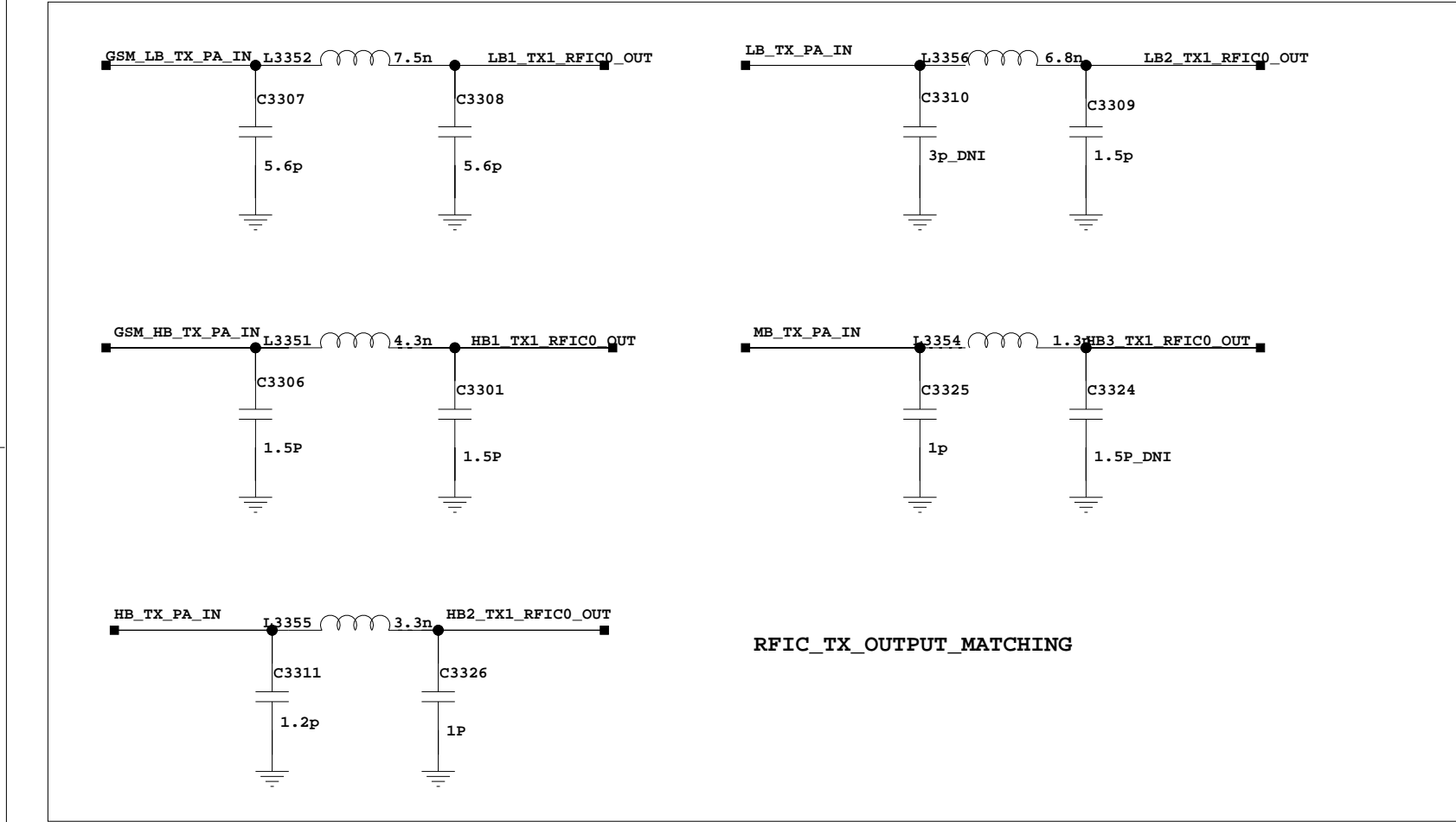
33.RFIC0\_Hi6363

A

B

C

D

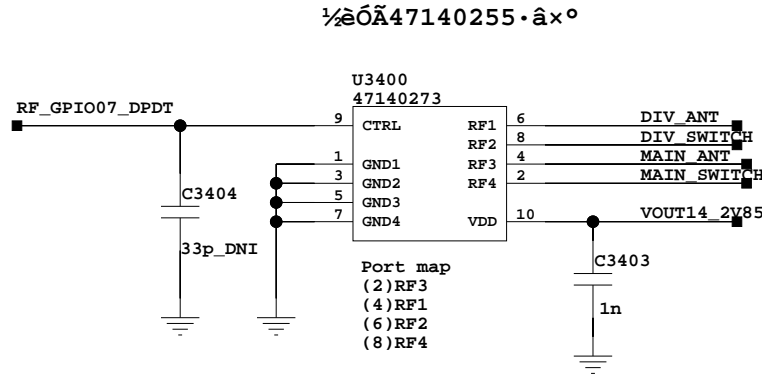


A

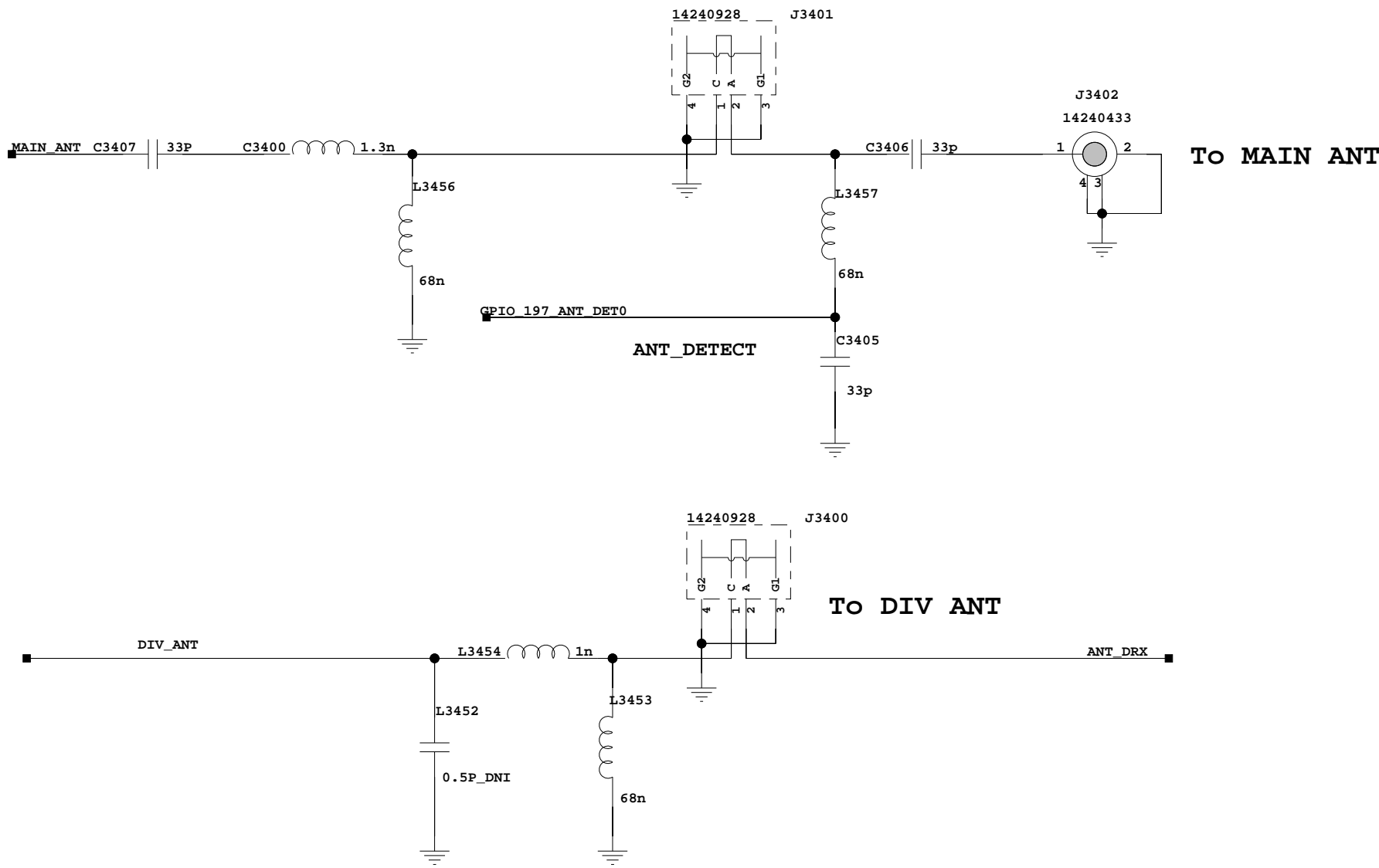
B

C

34 DPDT\_Connector



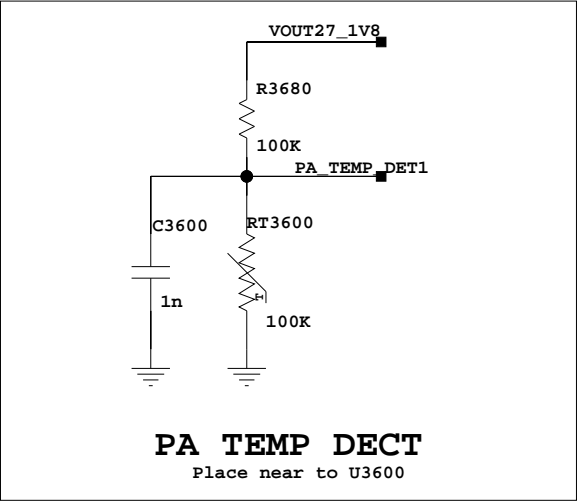
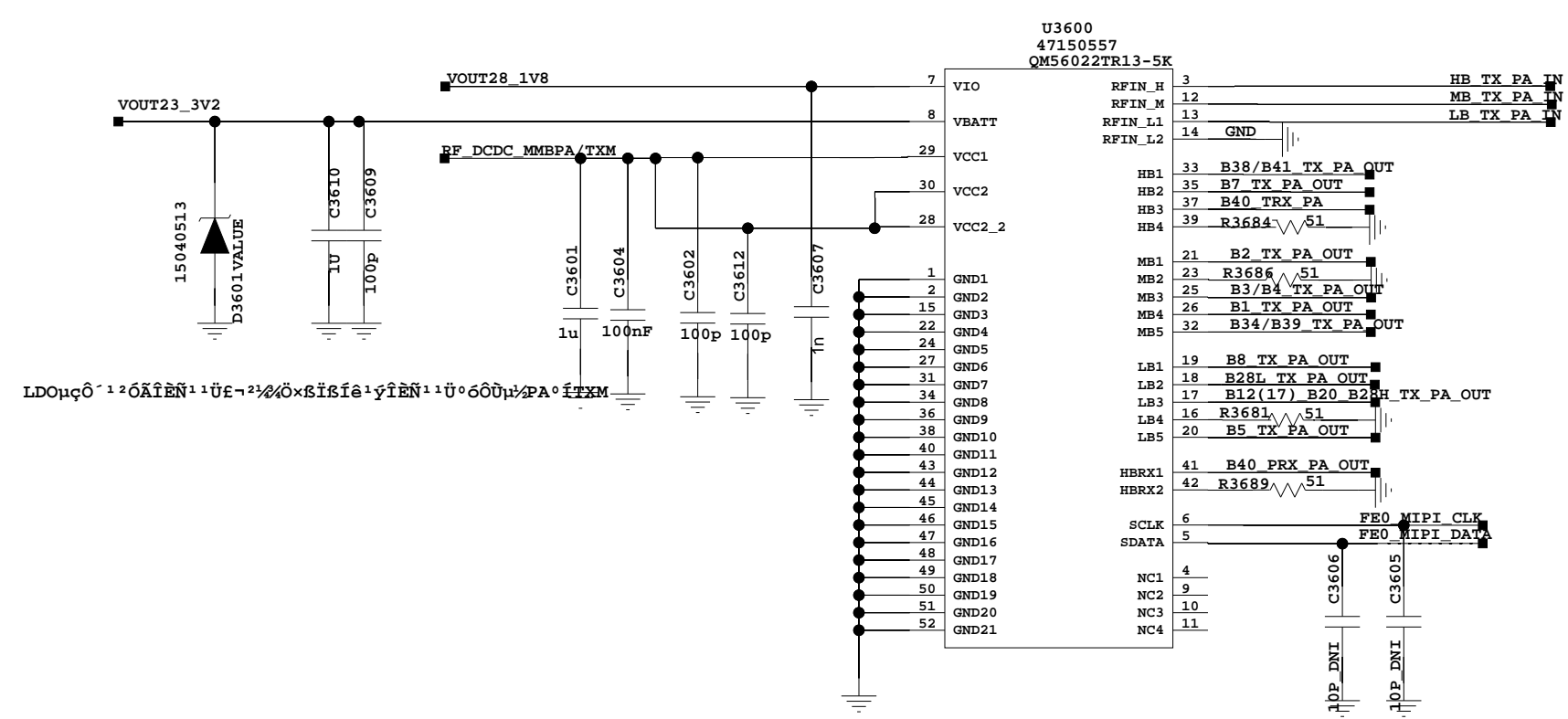
U3400 Truth Table	
CTRL1	State
0	RF1-RF3, RF2-RF4
1	RF1-RF4, RF2-RF3



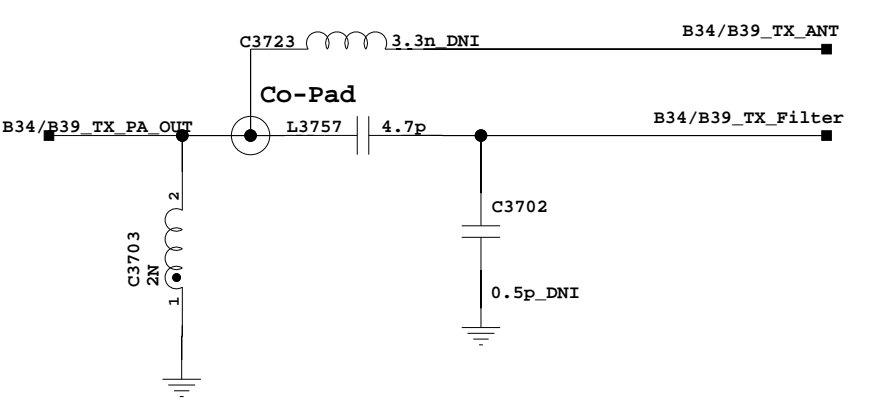
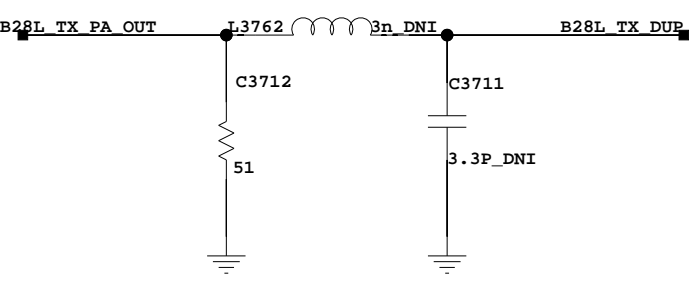
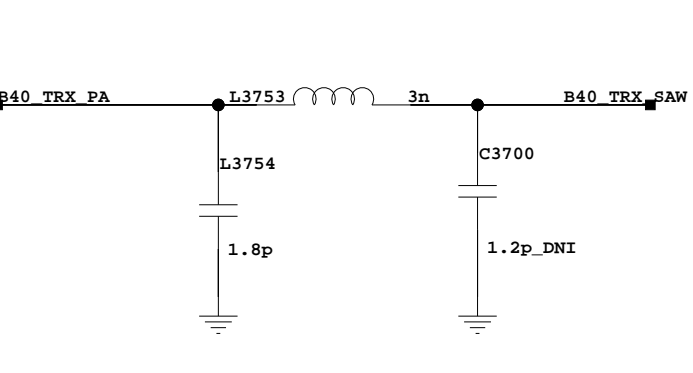
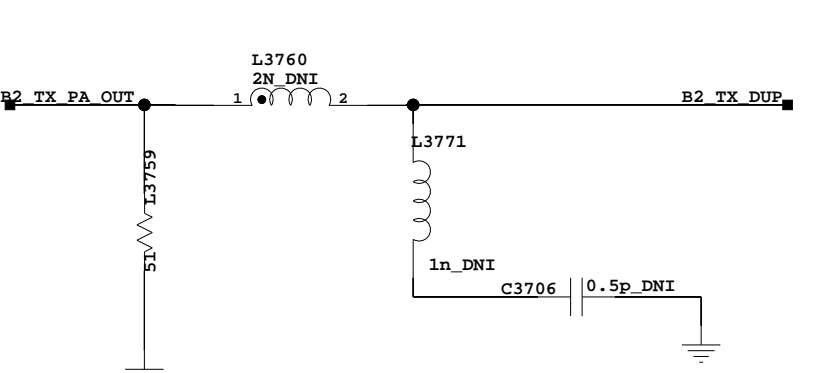
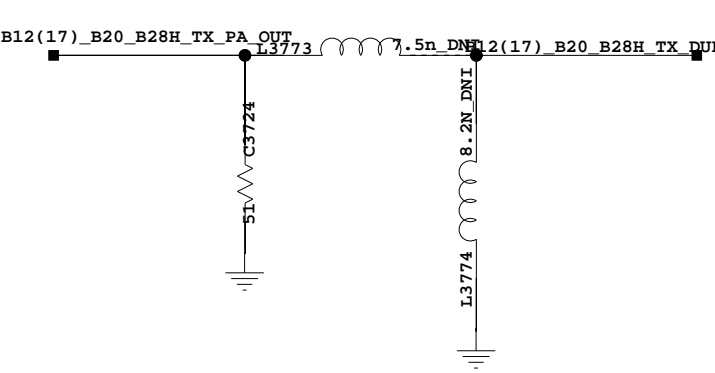
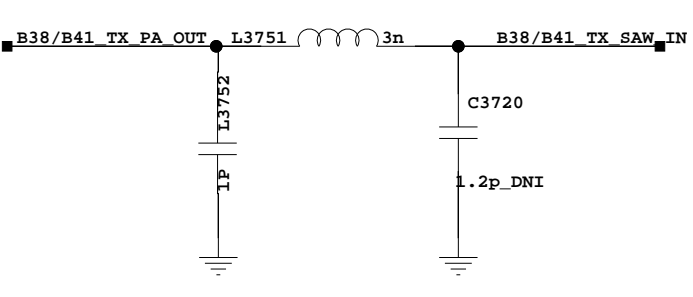
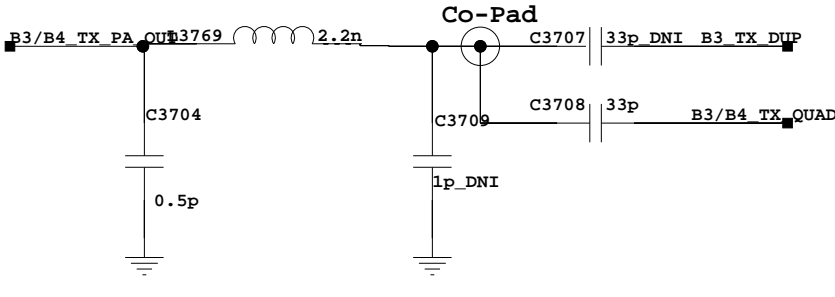
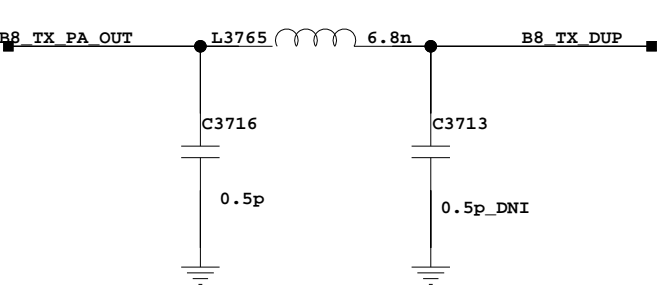
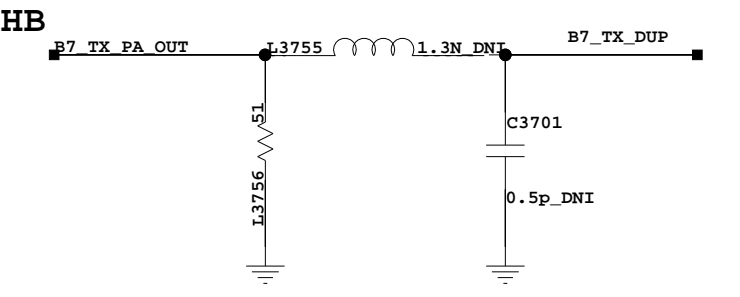
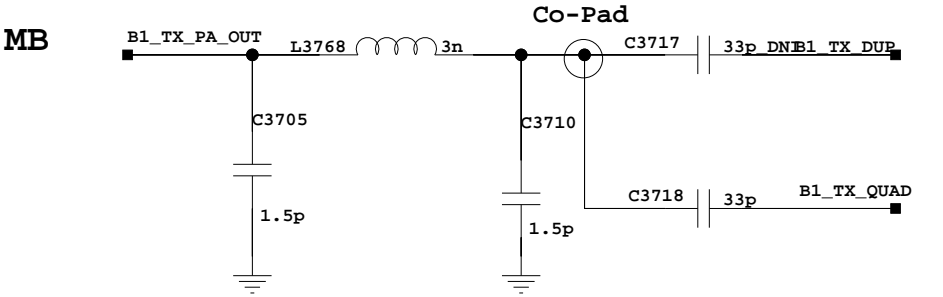
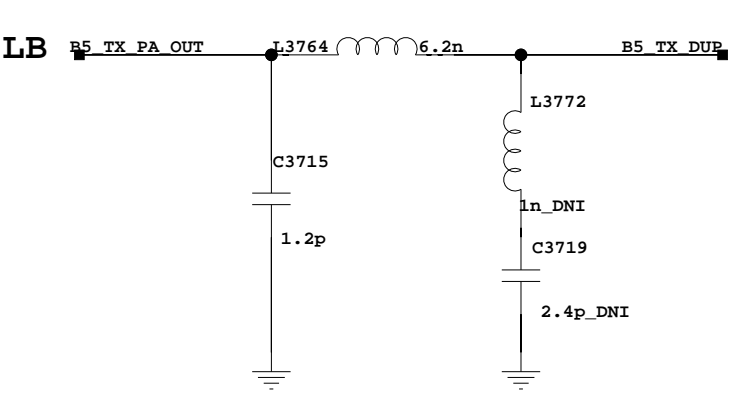
## D



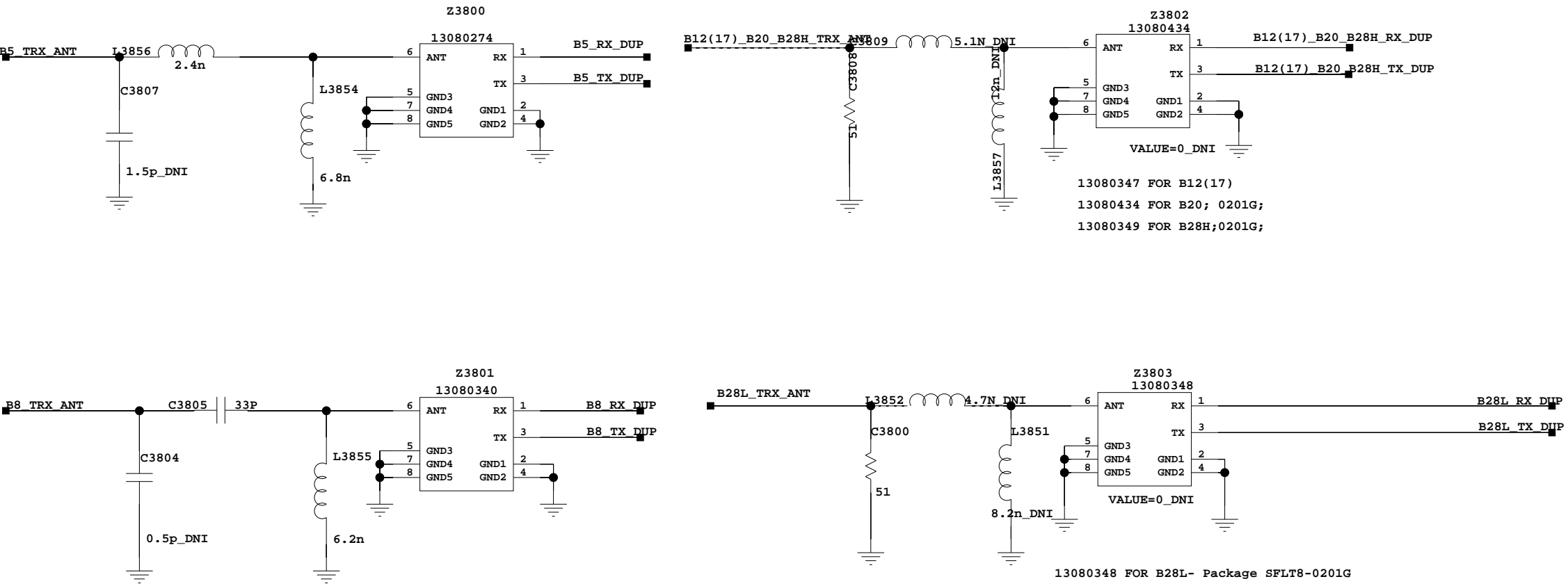
36 MMBPA



37.TX\_Loadpull

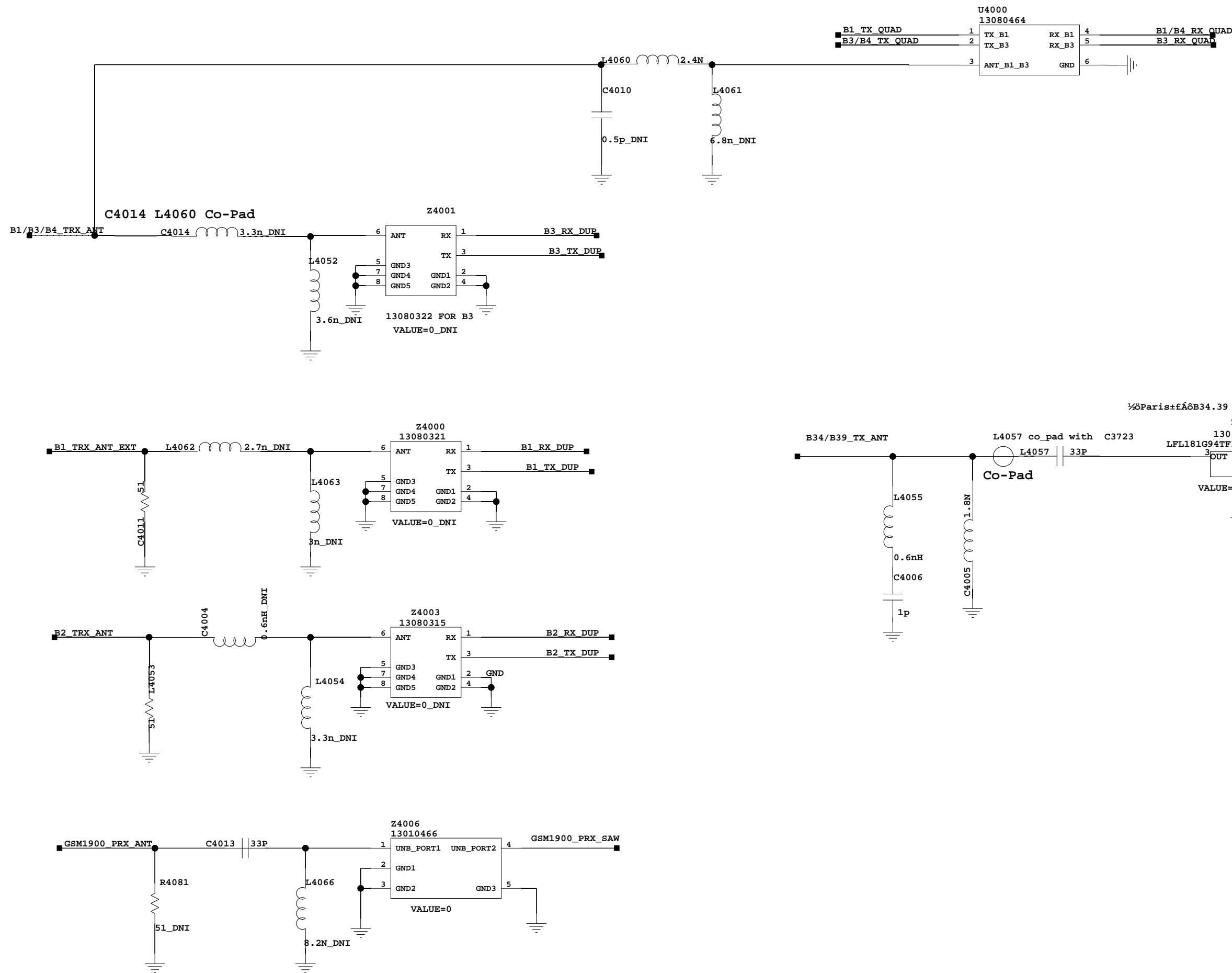


38 TRX\_LB\_1



1	2	3	4	5	6
39 TRX_LB_2					
A					A
B					B
C					C
D					
1	2	3		5	6

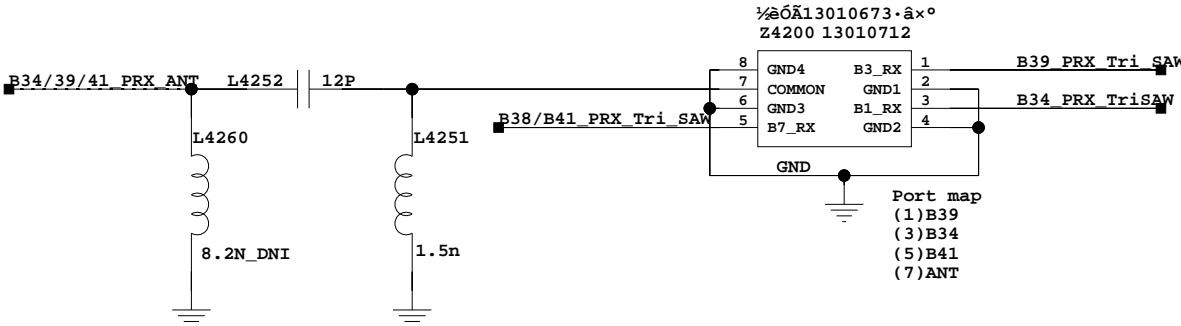
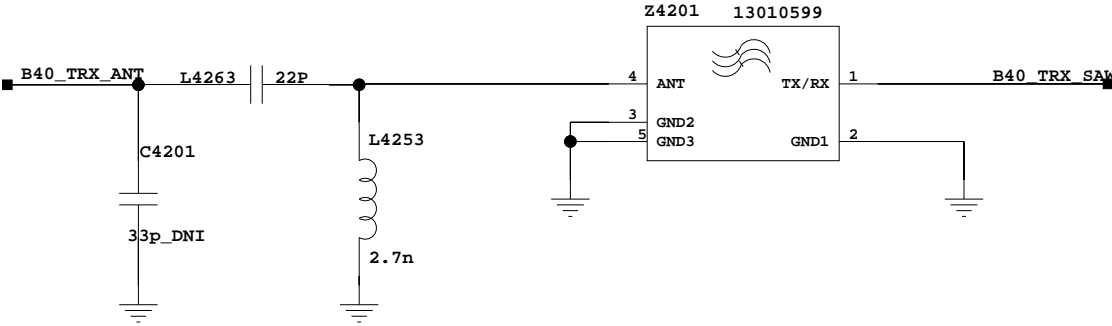
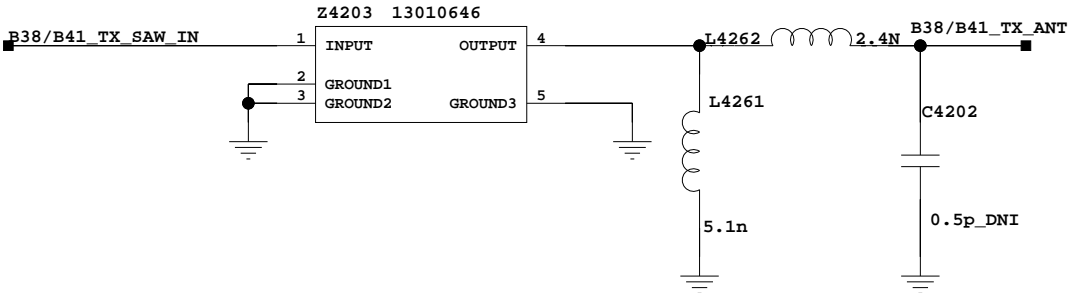
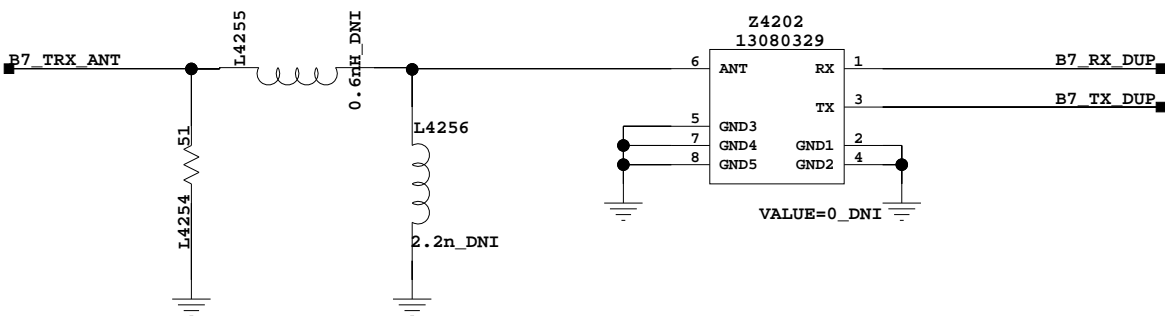
# 40 TRX\_MB\_1





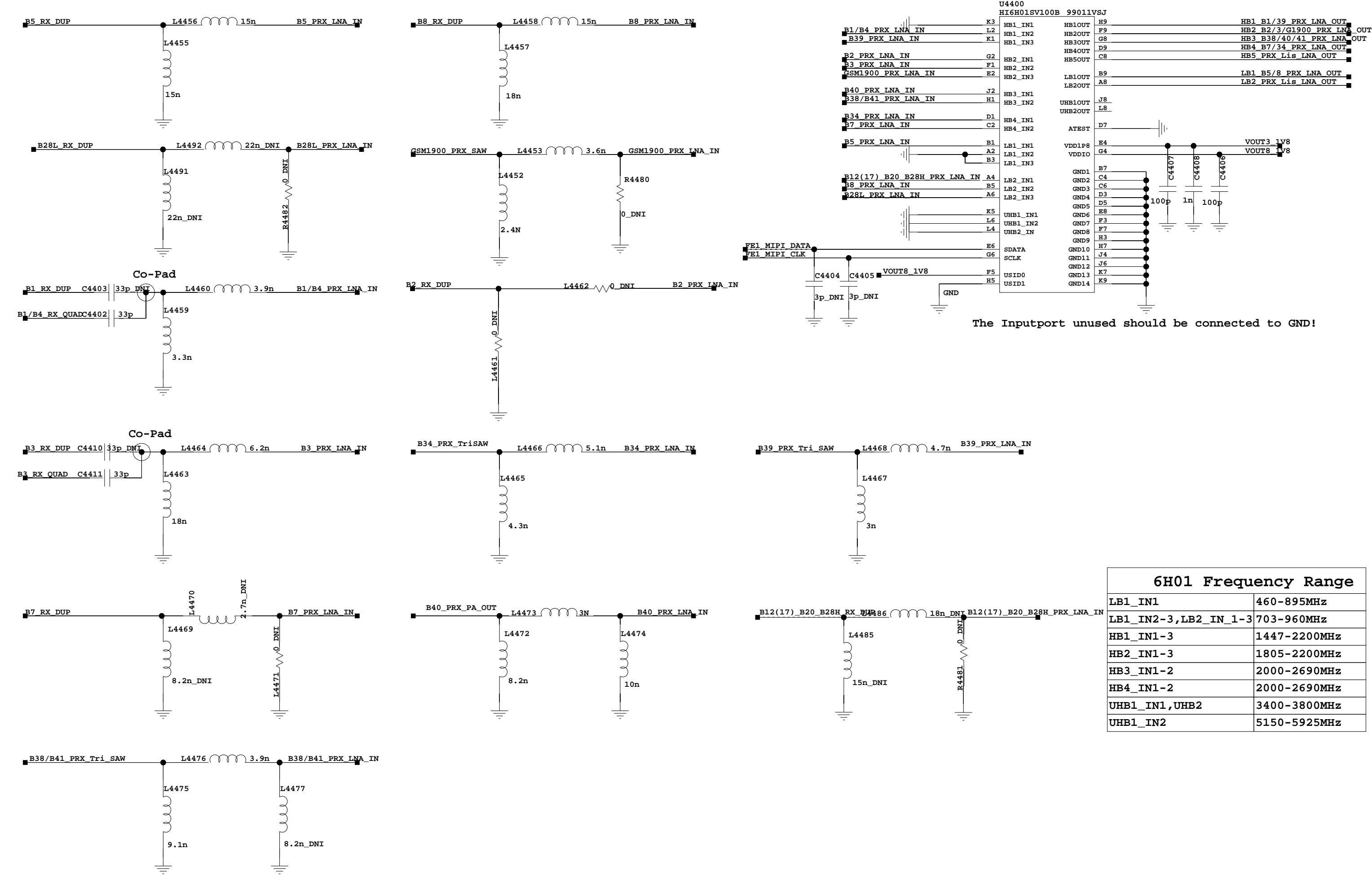
41 TRX_MB_2					
1	2	3	4	5	6
A					A
B					B
C					C
D					
1	2	3		5	6

42 TRX\_HB\_1

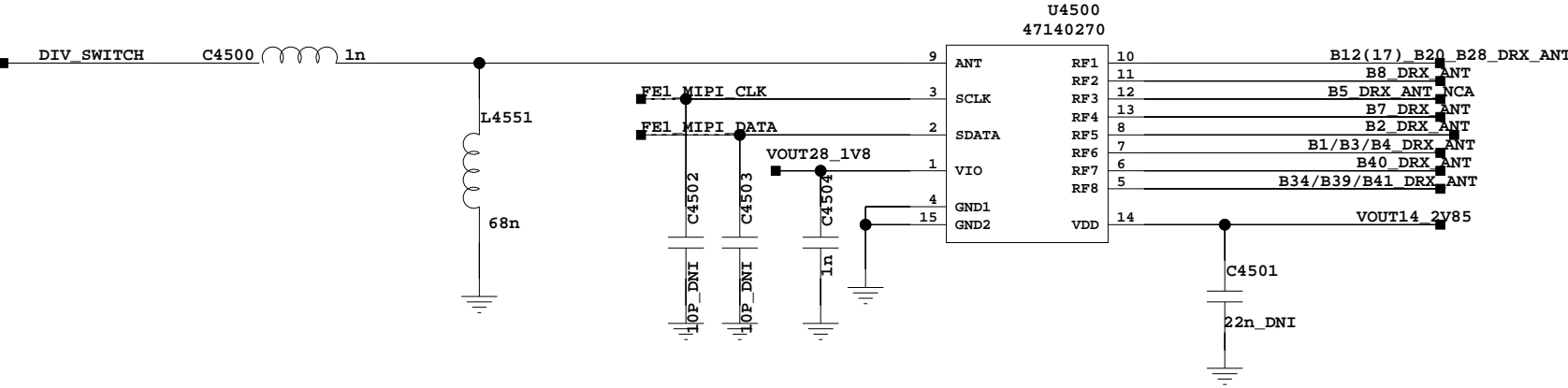


43. TRX_HB_2					
1	2	3	4	5	6
A					A
B					B
C					C
D					
1	2	3		5	6

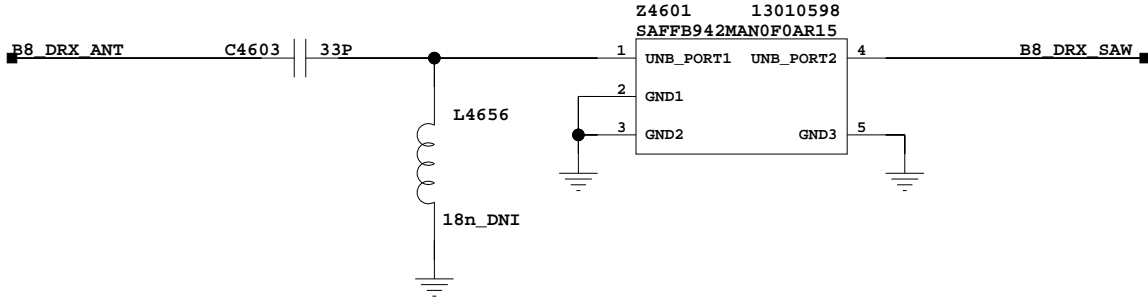
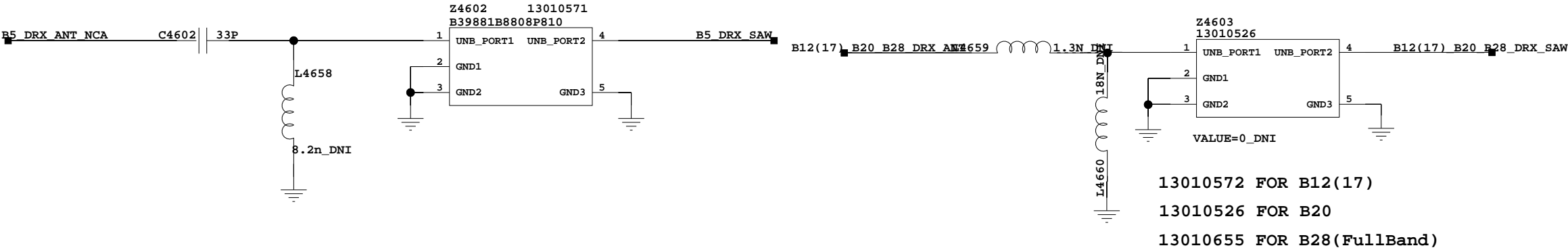
# 44. PRX\_LNA\_Module



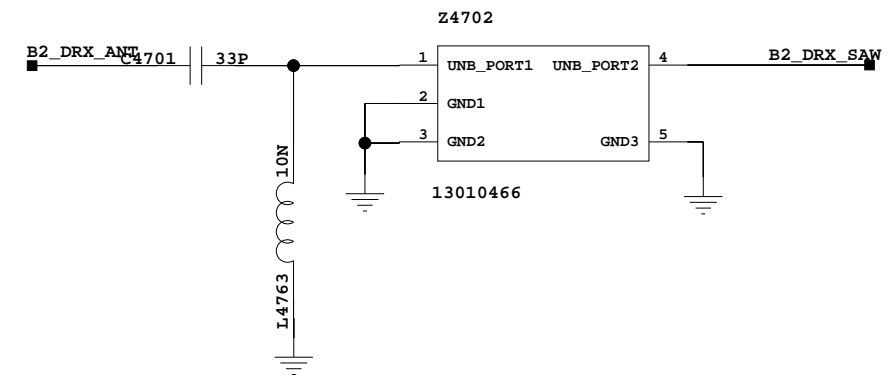
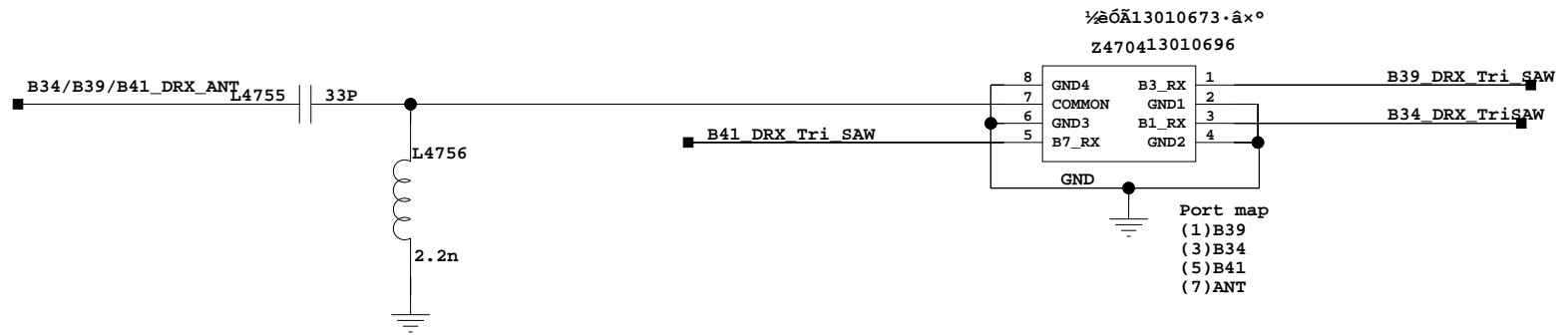
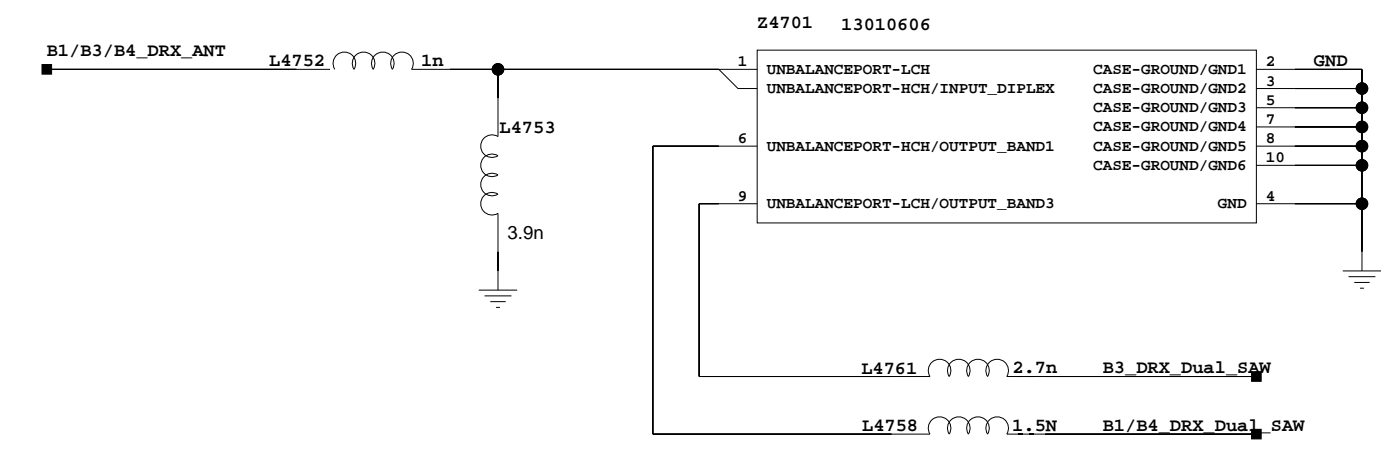
45.DRX\_SWITCH



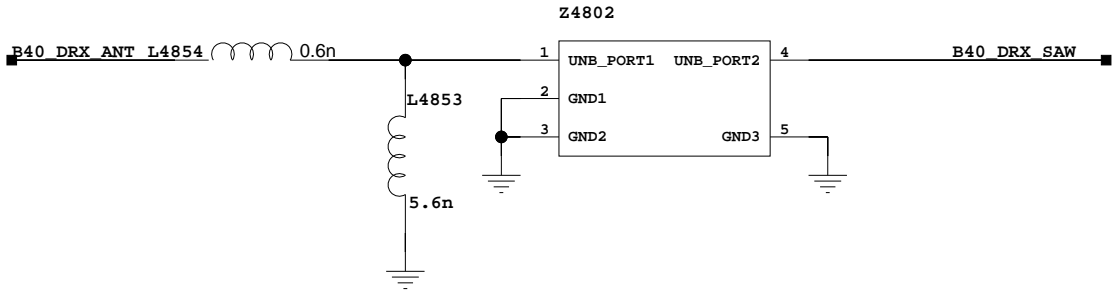
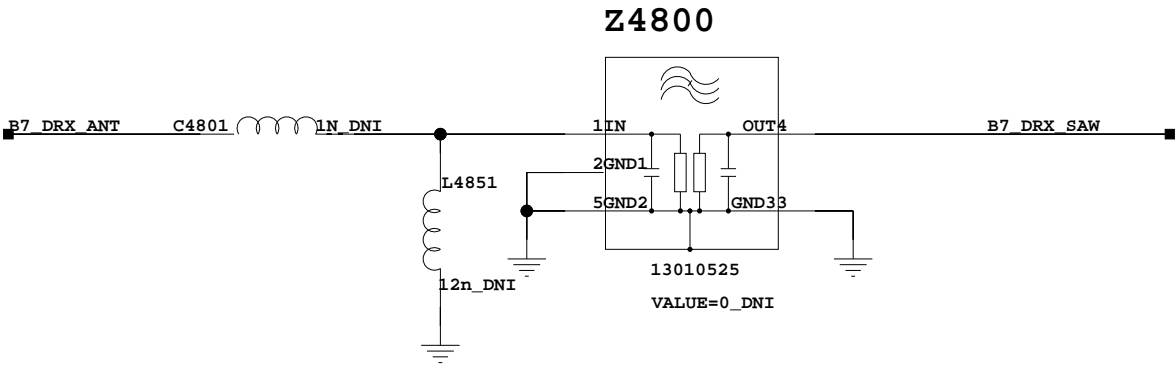
# 46. DRX\_LB



# 47. DRX\_MB

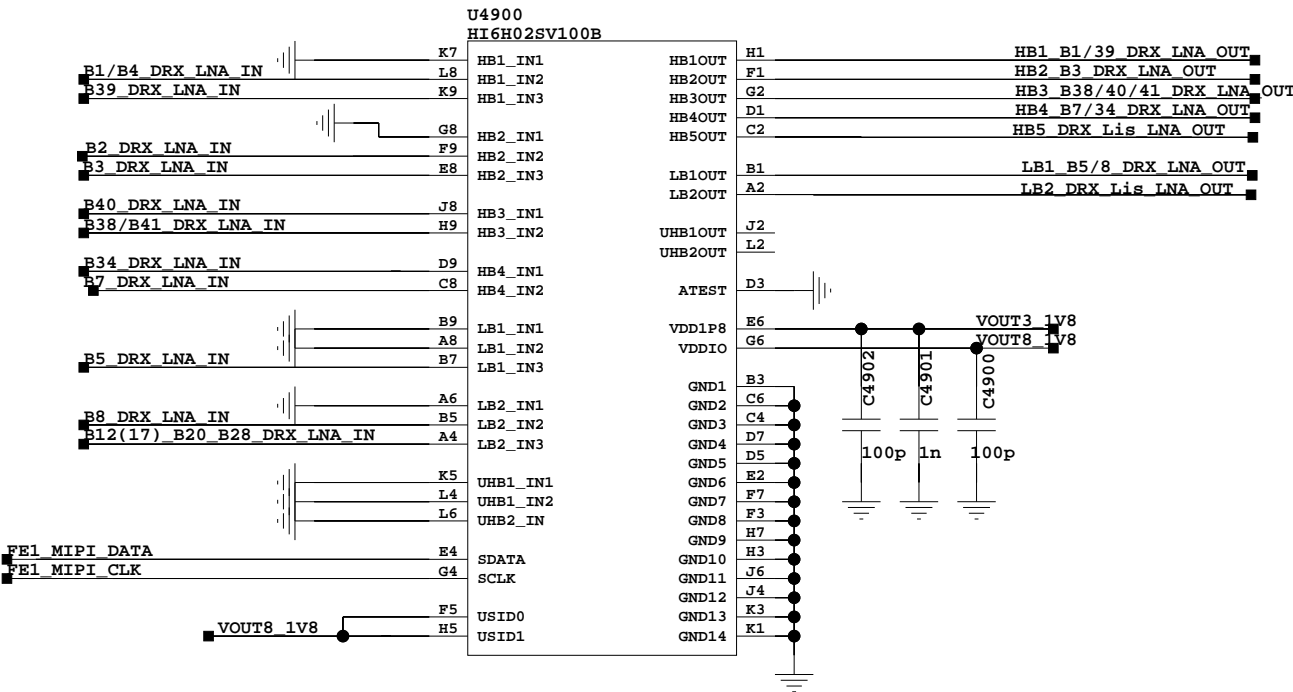
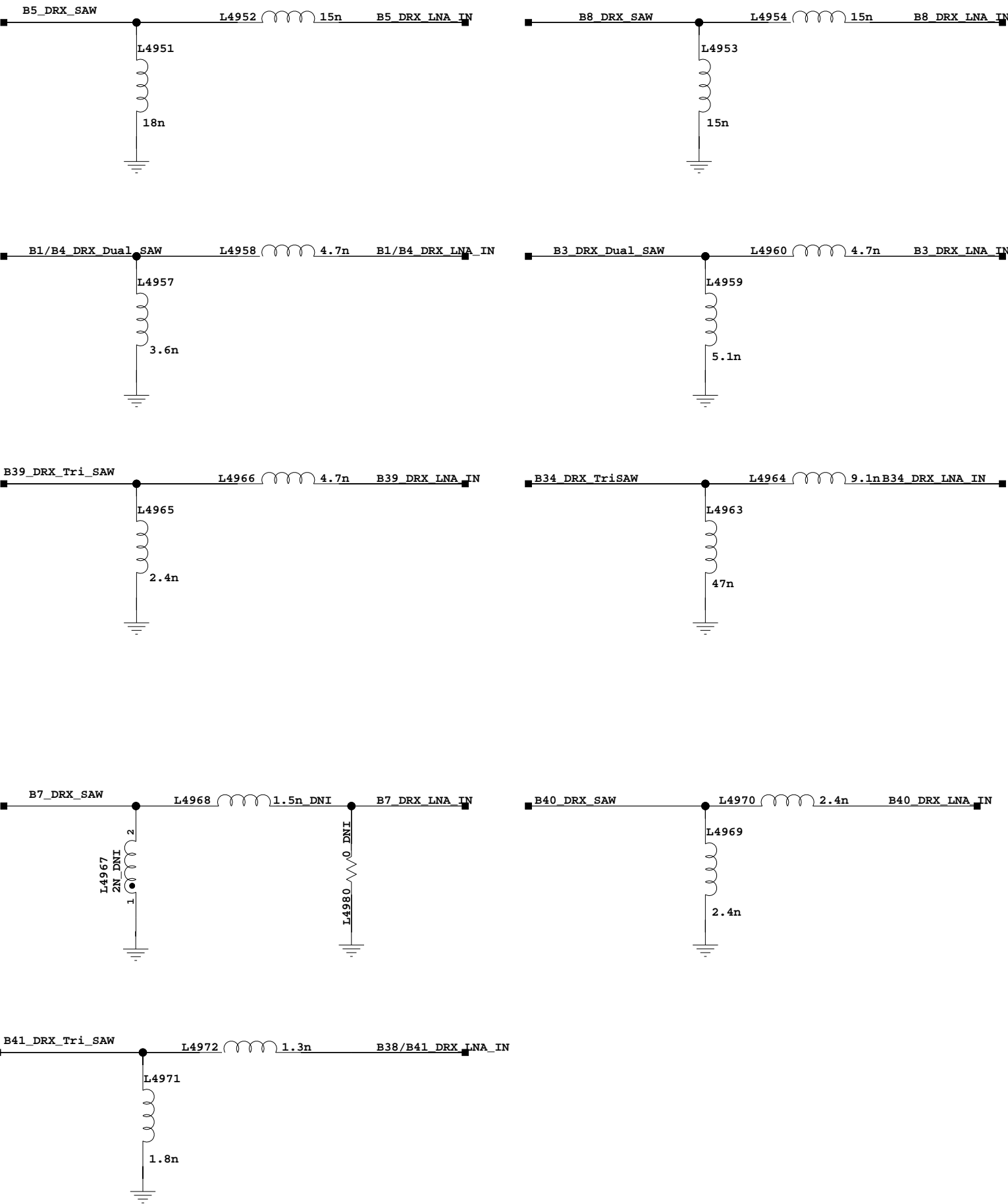


48. DRX\_HB

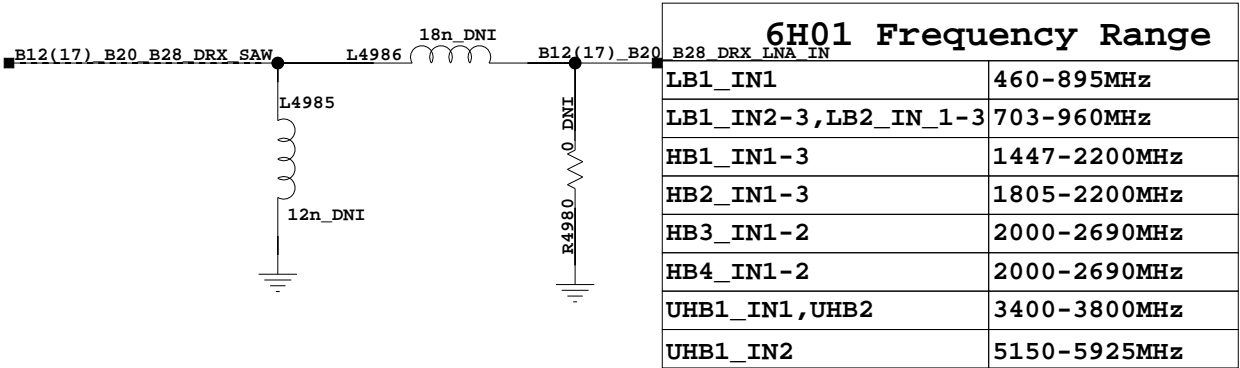
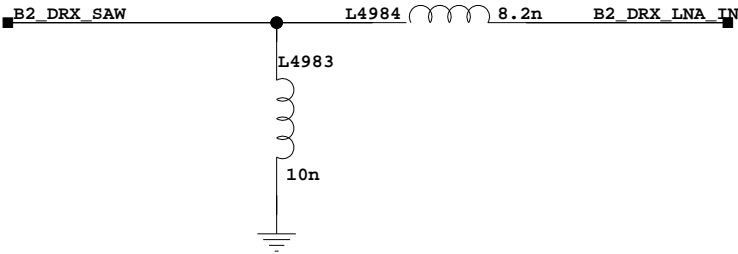




49. DRX\_LNA\_Module



The Inputport unused should be connected to GND!



6H01 Frequency Range	
LB1_IN1	460-895MHz
LB1_IN2-3, LB2_IN_1-3	703-960MHz
HB1_IN1-3	1447-2200MHz
HB2_IN1-3	1805-2200MHz
HB3_IN1-2	2000-2690MHz
HB4_IN1-2	2000-2690MHz
UHB1_IN1, UHB2	3400-3800MHz
UHB1_IN2	5150-5925MHz

	1	2	3	4	5	6
A	50. Res					
B						
C						
D						
	1	2	3		5	6

	1	2	3	4	5	6
A	51. Res					
B						
C						
D						
	1	2	3		5	6

	1	2	3	4	5	6
A	52. Res					
B						
C						
D						
	1	2	3		5	6

	1	2	3	4	5	6
A	53. Res					
B						
C						
D						
	1	2	3		5	6

	1	2	3	4	5	6
A	54. Res					
B						
C						
D						
	1	2	3		5	6

	1	2	3	4	5	6
A	55. Res					
B						
C						
D						
	1	2	3		5	6

	1	2	3	4	5	6
A	56. Res					
B						
C						
D						
	1	2	3		5	6



123456

57. Res

A

A

B

B

C

C

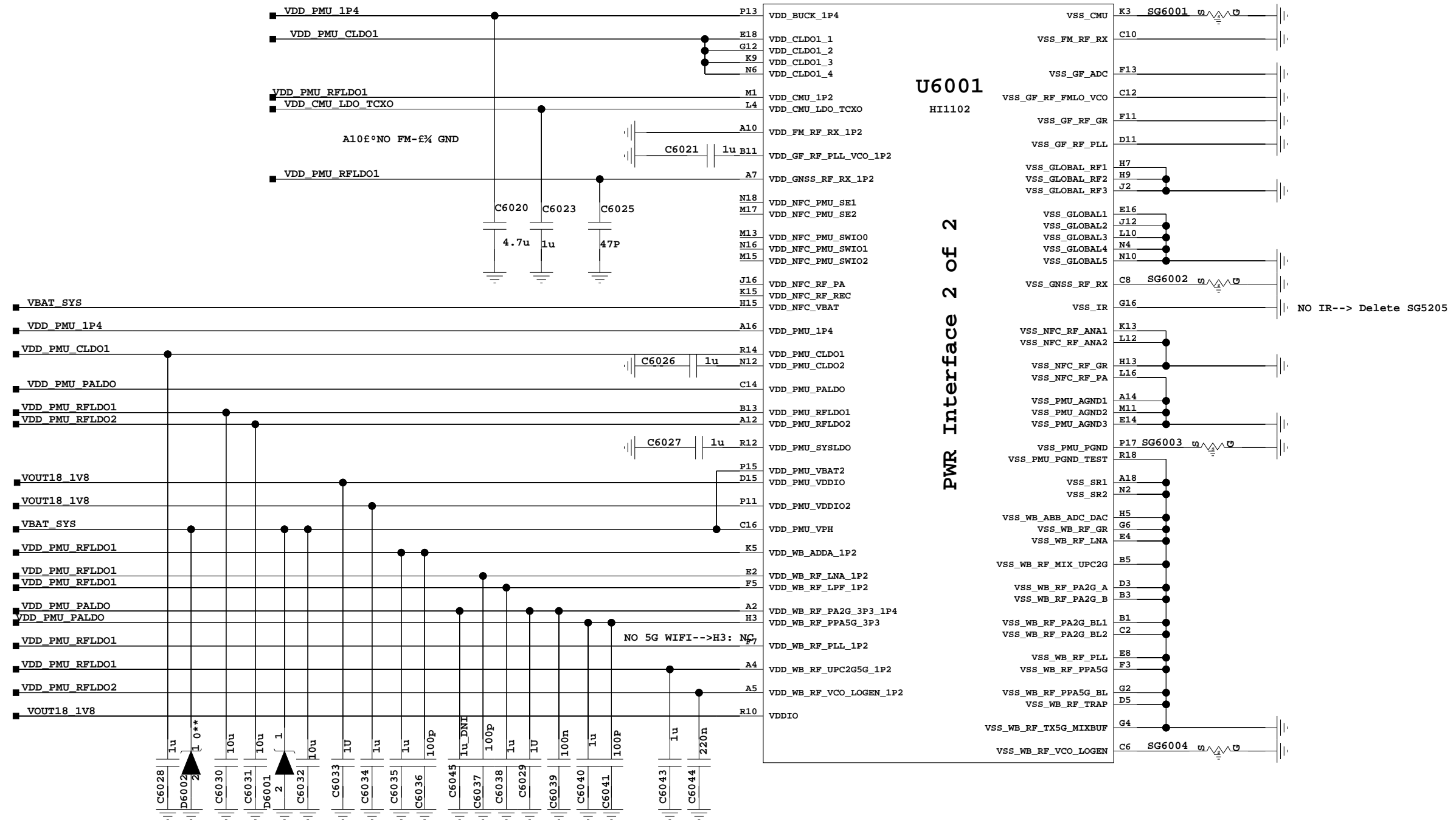
D

123456

	1	2	3	4	5	6
A	58. Res					
B						
C						
D						
	1	2	3		5	6

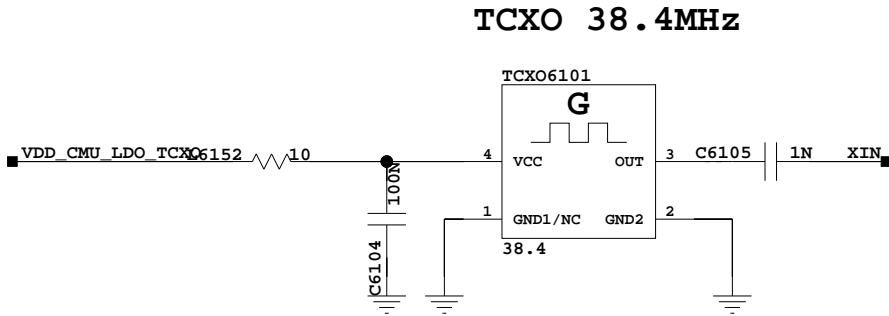
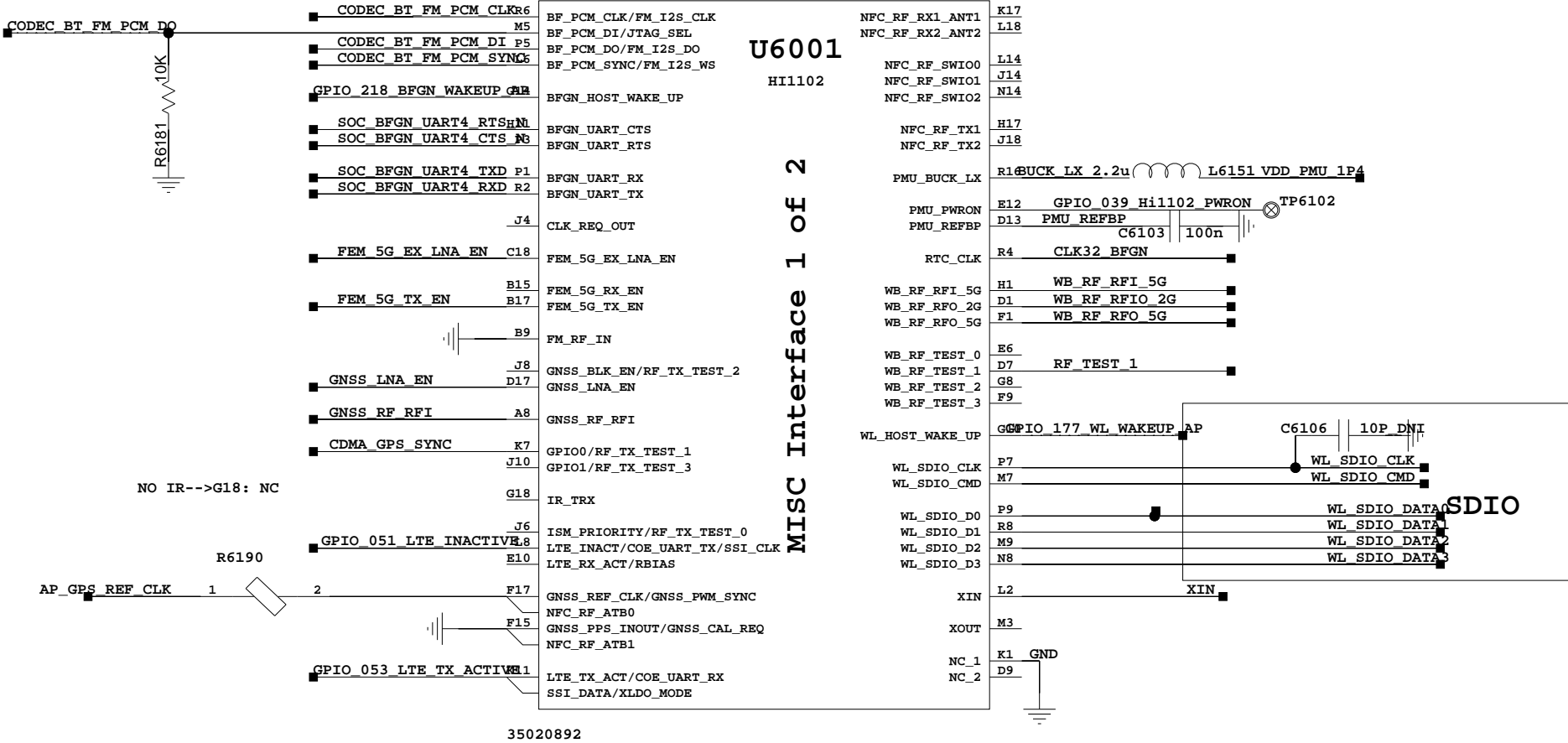
	1	2	3	4	5	6
A	59. Res					
B						
C						
D						
	1	2	3		5	6

# 60 NC\_POWER

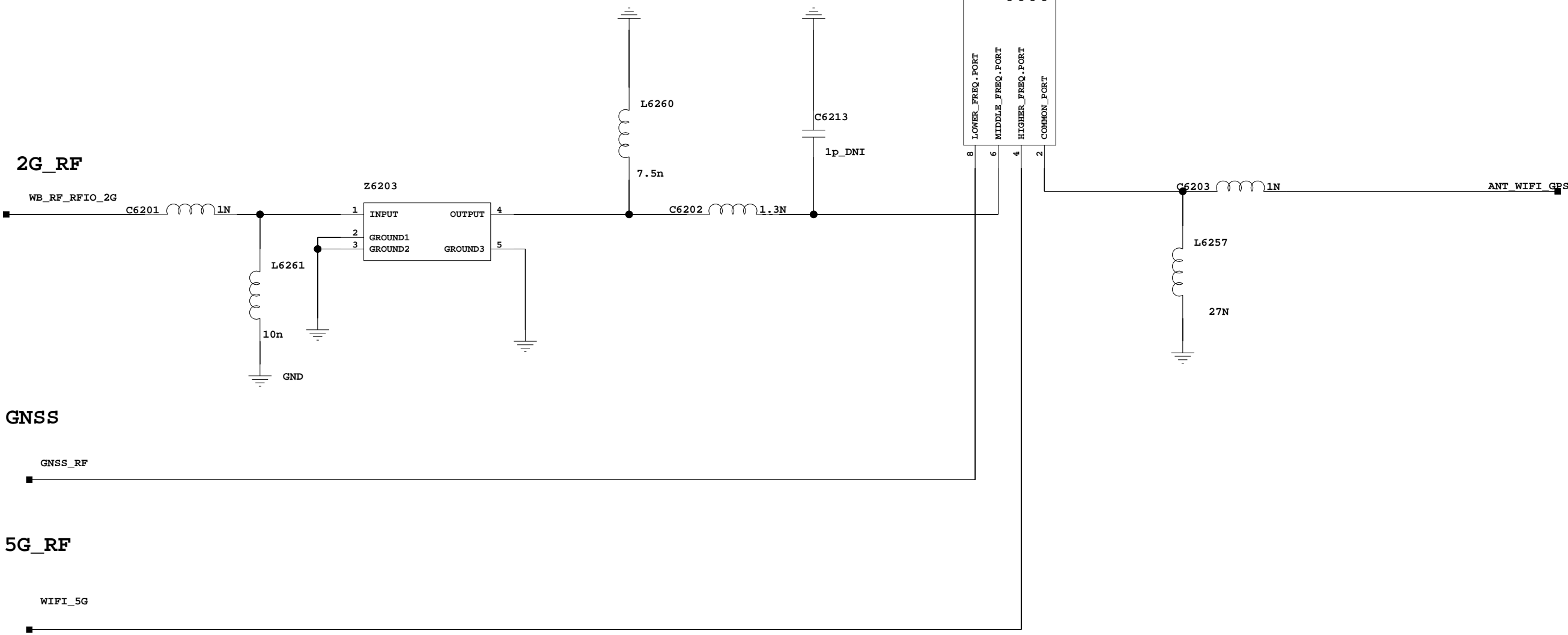


Add by Hisilicon for debug

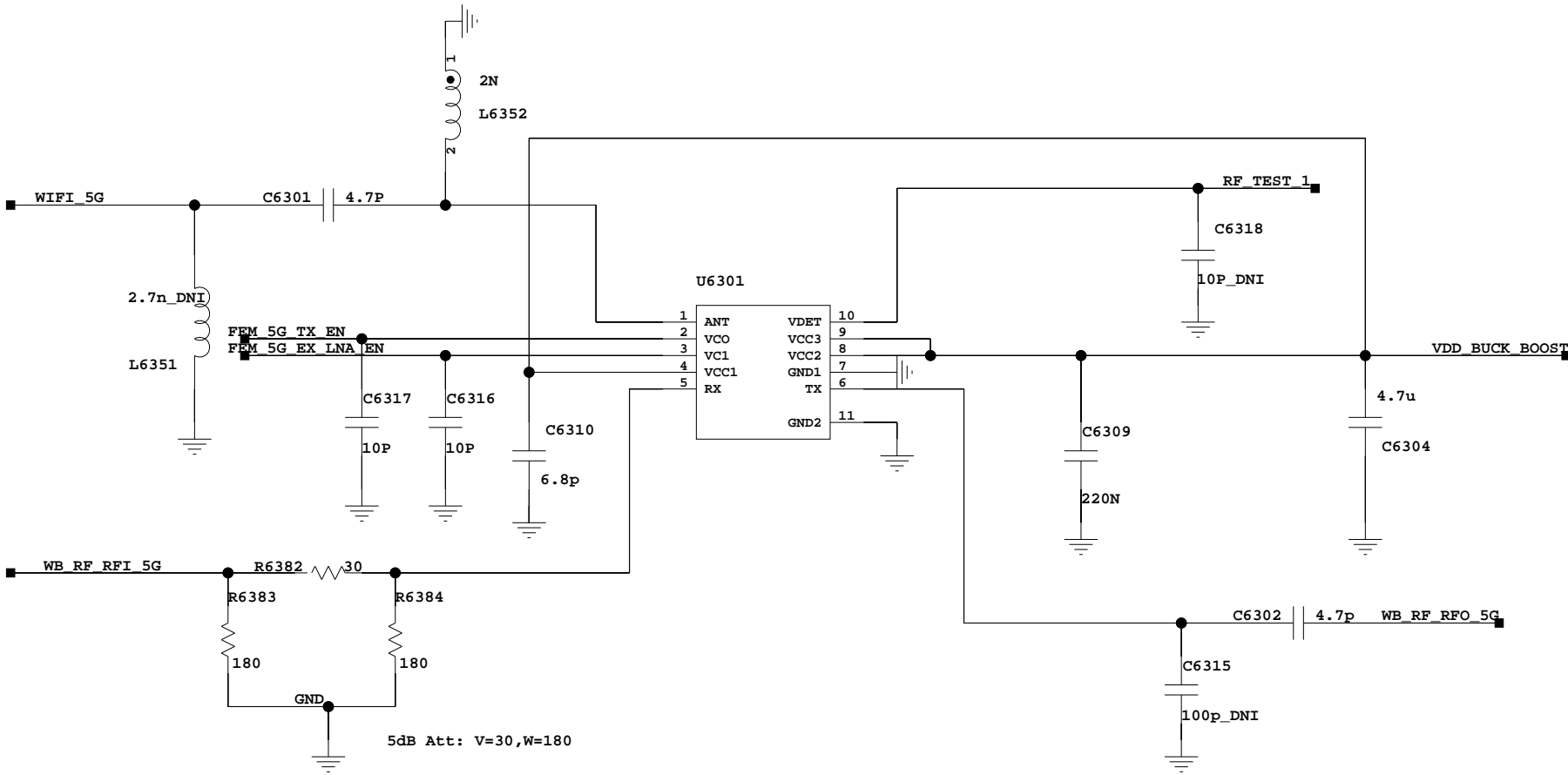
61 NC\_BB



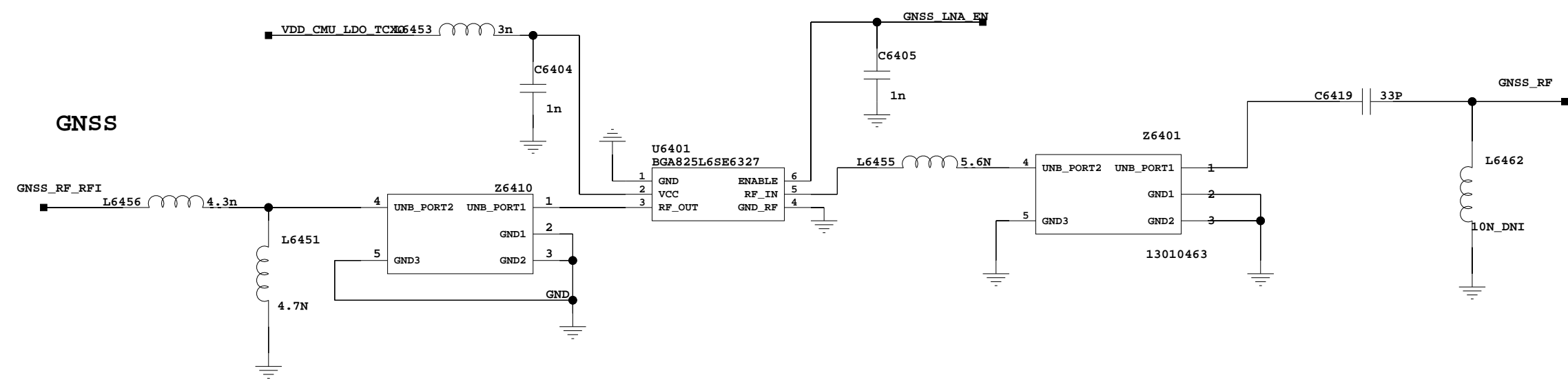
62 NC\_FE\_WIFI\_2G



63 NC\_FE\_WIFI\_5G



64 NC\_GPS





	1	2	3	4	5	6
A	65. Res					
B						
C						
D						
	1	2	3		5	6

	1	2	3	4	5	6
A	66. Res					
B						
C						
D						
	1	2	3		5	6

123456

67. Res

A

A

B

B

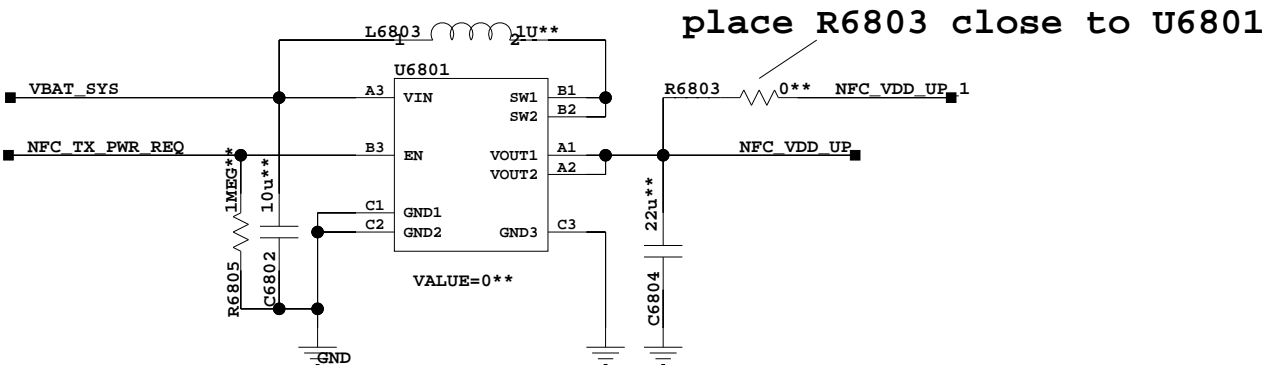
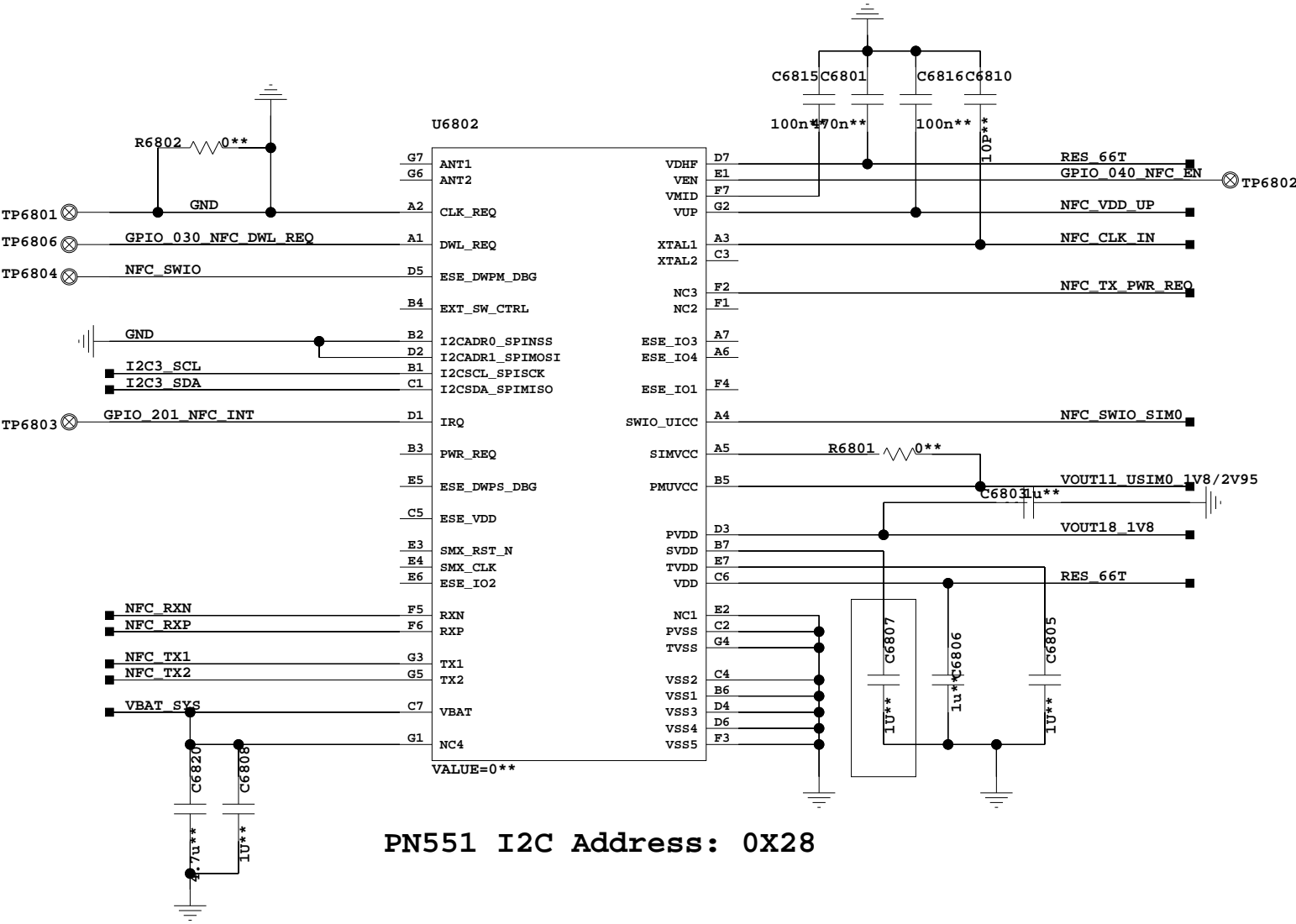
C

C

D

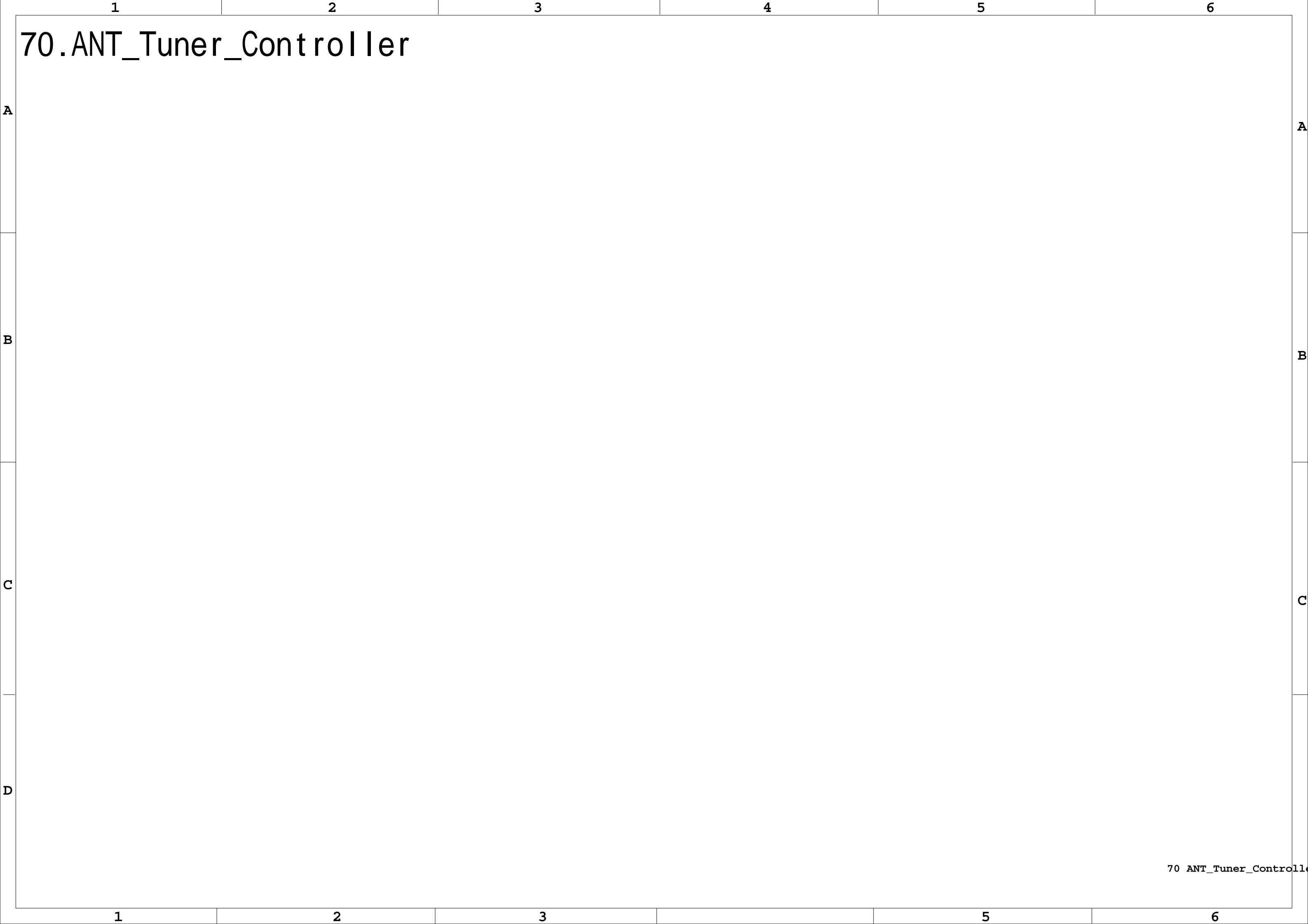
123456

68. NFC\_BB



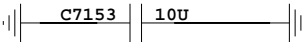
	1	2	3	4	5	6
A	69. Res					
B						
C						
D						
	1	2	3		5	6

70.ANT\_Tuner\_Controller

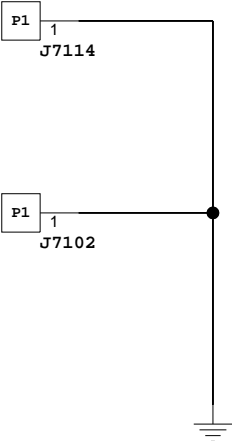
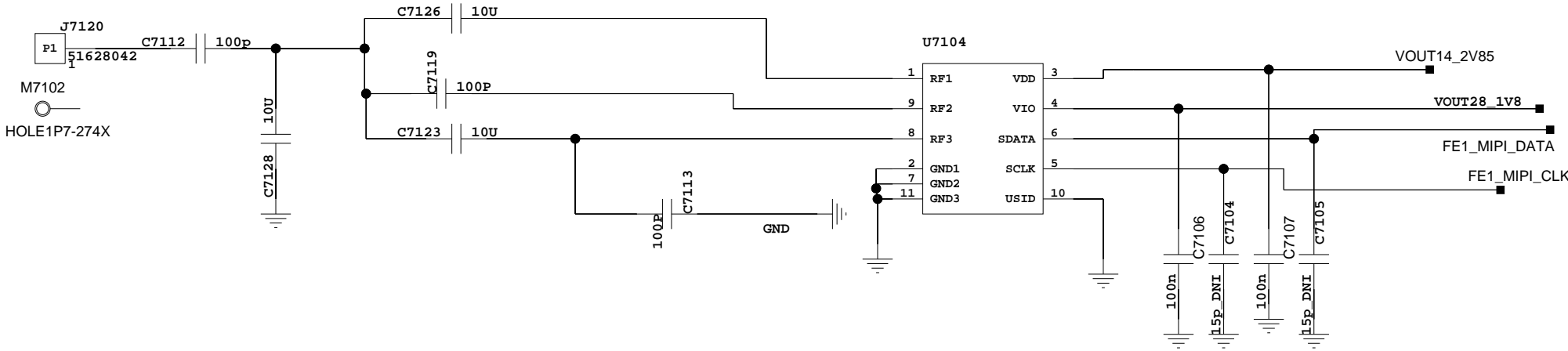


71.ANT\_DIV

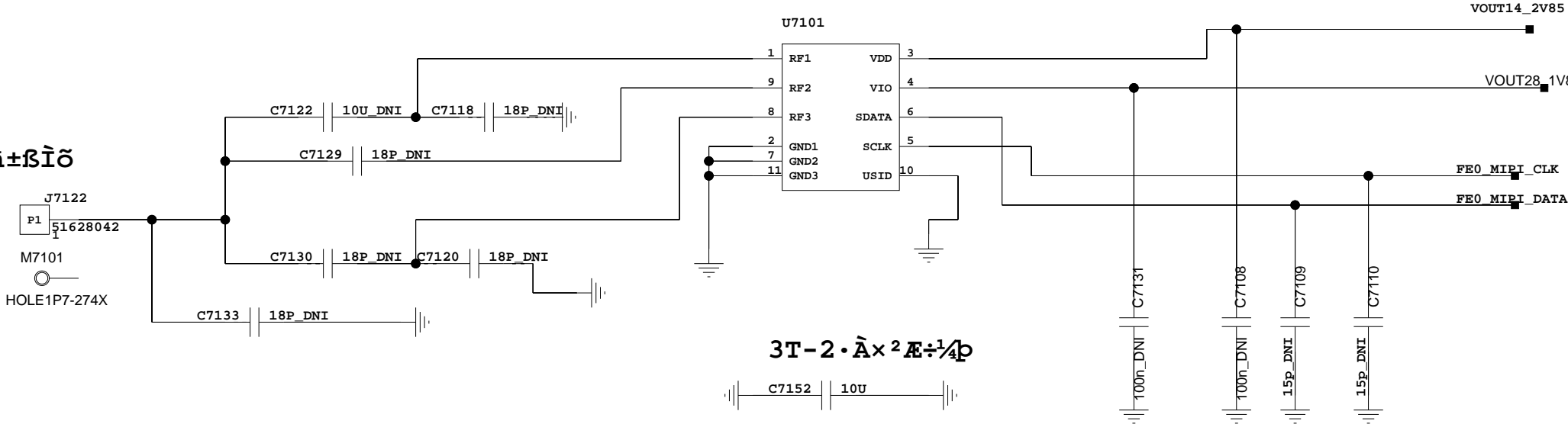
3T-1 · Å × ² Æ ÷ ¼ p



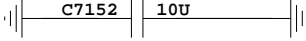
div near gnd



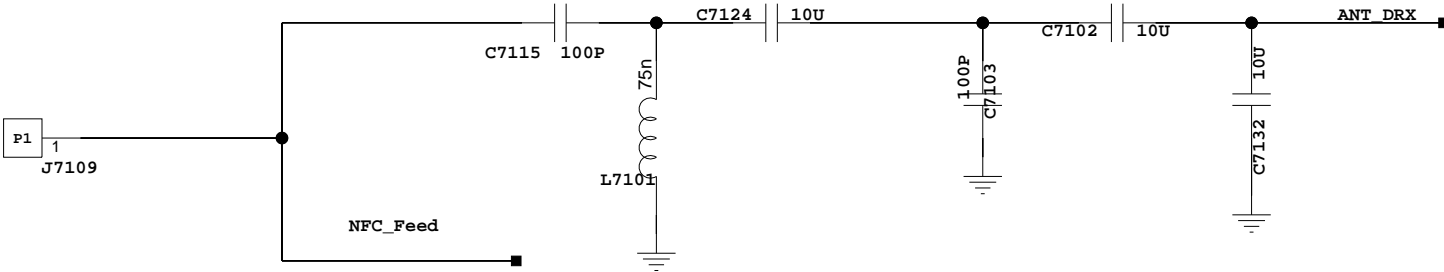
div ² à ± ß Ì Õ



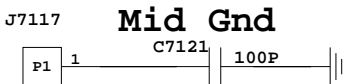
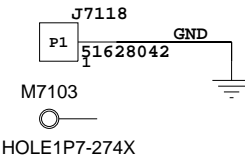
3T-2 · Å × ² Æ ÷ ¼ p



DIV Ant Feed

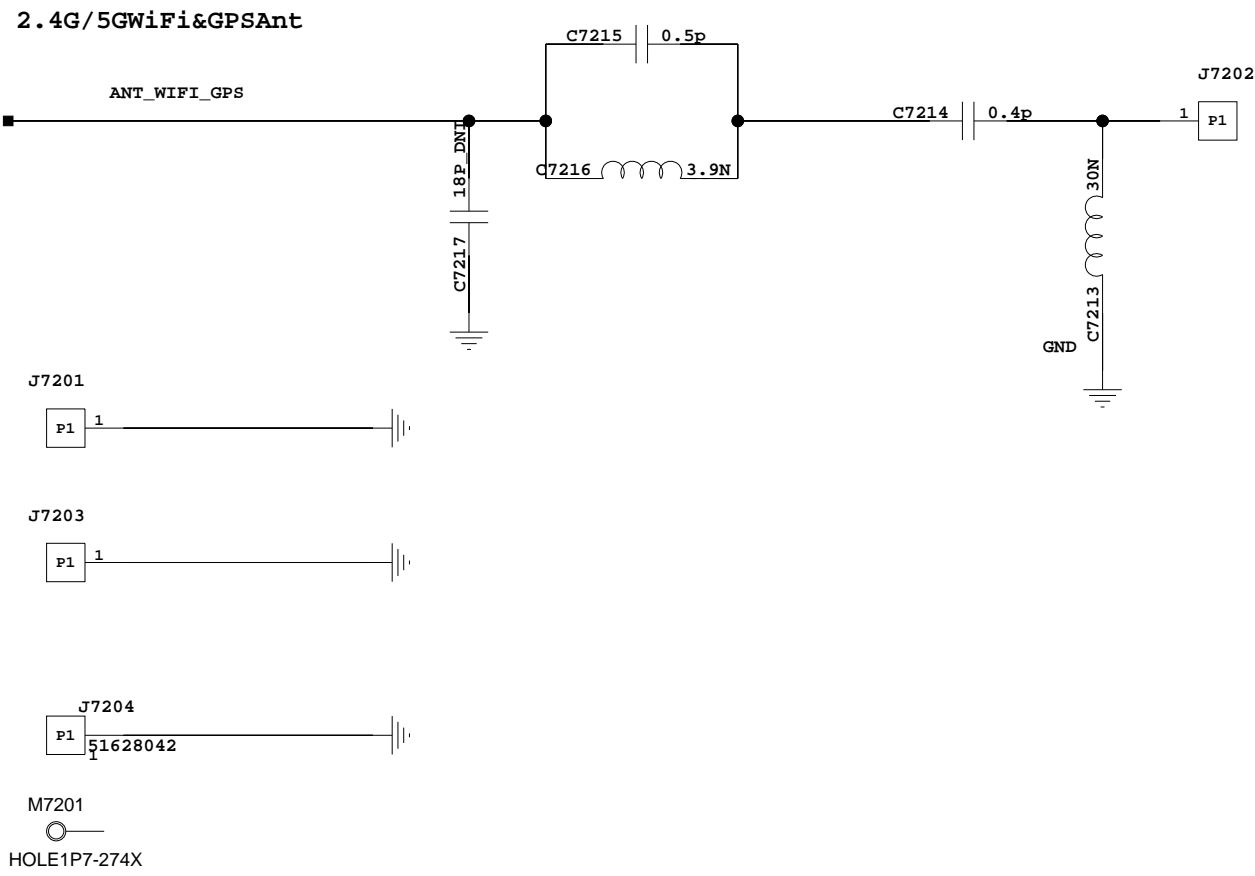


div ½ ü µ Ø Ì Â µ Ø Â Ý ¶



Mid Gnd

72 ANT\_GPS\_WIFI







1	2	3	4	5	6
74. ANT_CELL_MIMO					
A					A
B					B
C					C
D					
1	2	3		5	6