

# I2C\_ID\_OVERVIEW

REVISION RECORD			
LTR	ECO NO:	APPROVED:	DATE:

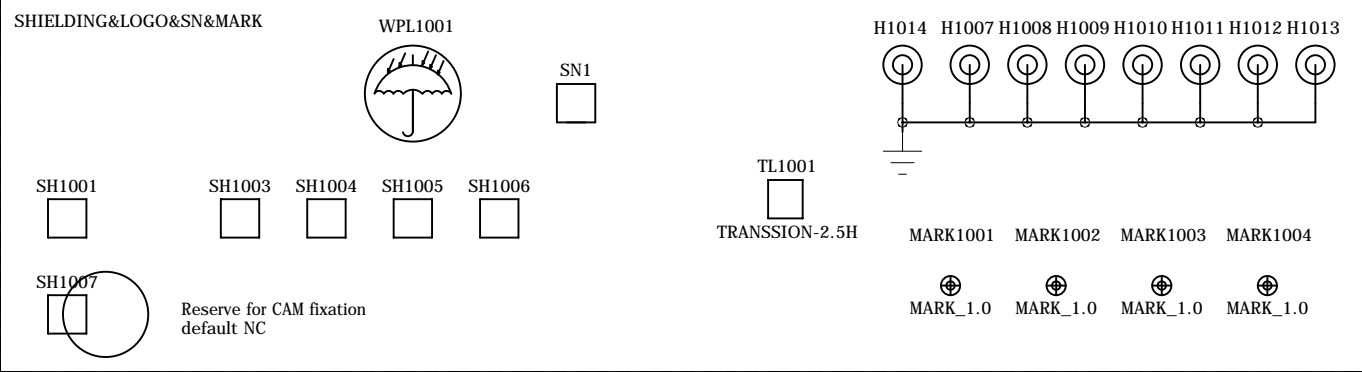
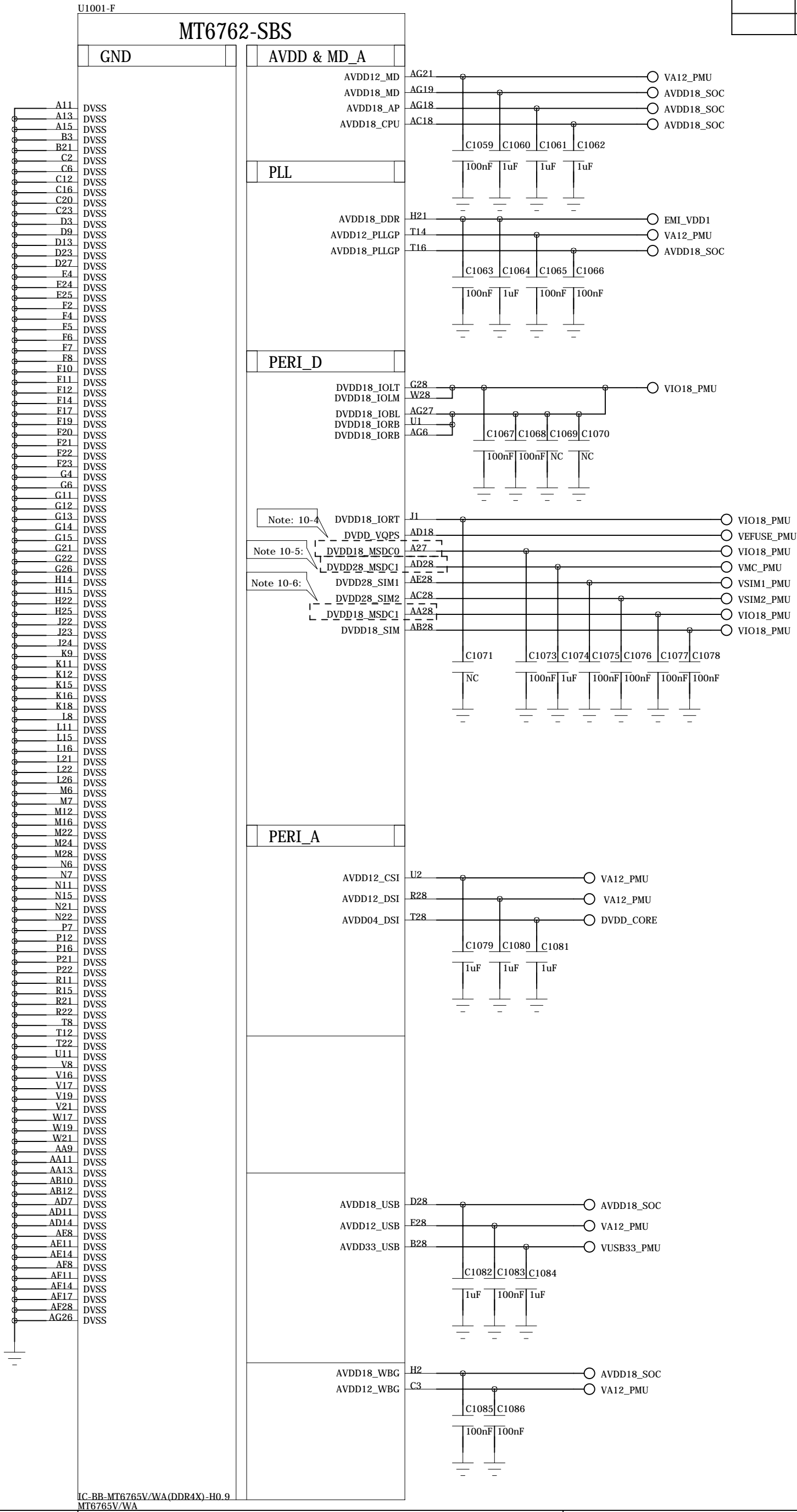
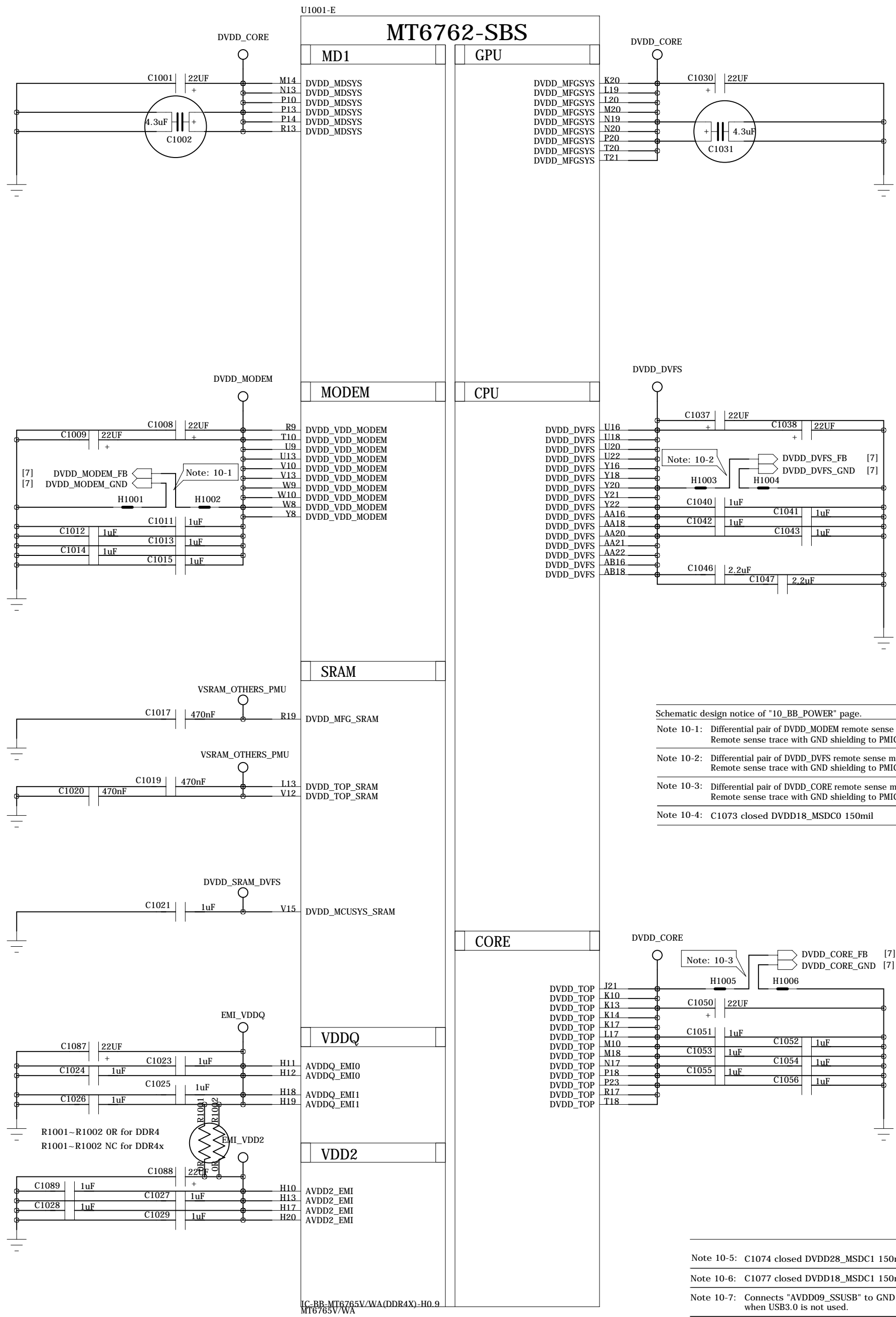
I2C	Function	I2C Spec.	Budget Timing	I2C Slave Address (7-bit mode)
I2C-0	CTP	400 Kbps	Yes.	CTP (NT35672) I2C address: 0X01 (Write:0x02, Read:0x03)
I2C-1	M Sensor	400 Kbps	Yes.	AF6133:I2C ADDRESS:0x18(Write)/0x19(Read)
	ALS / PS Sensor	400 Kbps	Yes.	STK3332-SV address: Write:0xEE, Read:0xEF
	Gsensor	400 Kbps	Yes.	MC3416-P:ADDRESS:0x98(Write)/0x99(Read)
I2C-2	REAR CAMERA Wide (13M+AF)	400 Kbps	Yes.	Back camera(S5K3L6XX03-FGX9) I2C address: (Write:0x20, Read:0x21) EEPROM IC(BL24SA64) I2C address: (Write:0xA2, Read:0xA3 ) MOTOR IC(DW9718S) I2C address: (Write:0x18, Read:0x19 )
	REAR 4 CAMERA	400 Kbps	Yes.	Back camera(GC6133) I2C address: (Write:0x80, Read:0x81)
I2C-3	HL7593WL02	400 Kbps	Yes.	I2C address: 0X57 (Write:0xAE, Read:0xAF)
I2C-4	REAR CAMERA MONO (2M+FF)	400 Kbps	Yes.	Back camera(SP250ACSP) I2C address: (Write:0x78, Read:0x79)
	FRONT CAMERA (32M+FF)	400 Kbps	Yes.	Front camera(S5KGD1SP03-FGX9)I2C address: (Write:0x5A, Read:0x5B) EEPROM Ǝ" P24C64E-C4H-MIR) I2C address: (Write:0xA2, Read:0xA3)
I2C-5				
	LCM Gate Driver	400 Kbps	Yes.	OCP2131:I2C ADDRESS:0x7C(Write)/0x7D(Read)
	Flash Driver	400 Kbps	Yes.	AW3644YFFR:I2C ADDRESS:0xC6(Write)/0xC7(Read)
I2C-6	REAR CAMERA Tele	400 Kbps	Yes.	Back camera(GC8034W) I2C address: (Write:0x6E, Read:0x6F) EEPROM IC(P24C64E-C4H-MIR) I2C address: (Write:0xA0, Read:0xA1)

Note : I2C Spec. : Standard mode (100 kbps) and Fast mode (400 kbps), Fast mode Plus (1 Mbps) and High-speed mode (3.4 Mbps)

COMPANY: TRANSSION HOLDINGS				MODEL: H6126		Modified Date: 2021/9/2	
DRAWN	DJF/TS	DATED	20200928	TITLE: 01_I2C_ID_OVERVIEW		VERSION: V1.0	SHEET: 2 OF 24
CHECKED	<CHECKED>	DATED	< >	Confidentiality	CONFIDENTIAL		

# BB\_POWER

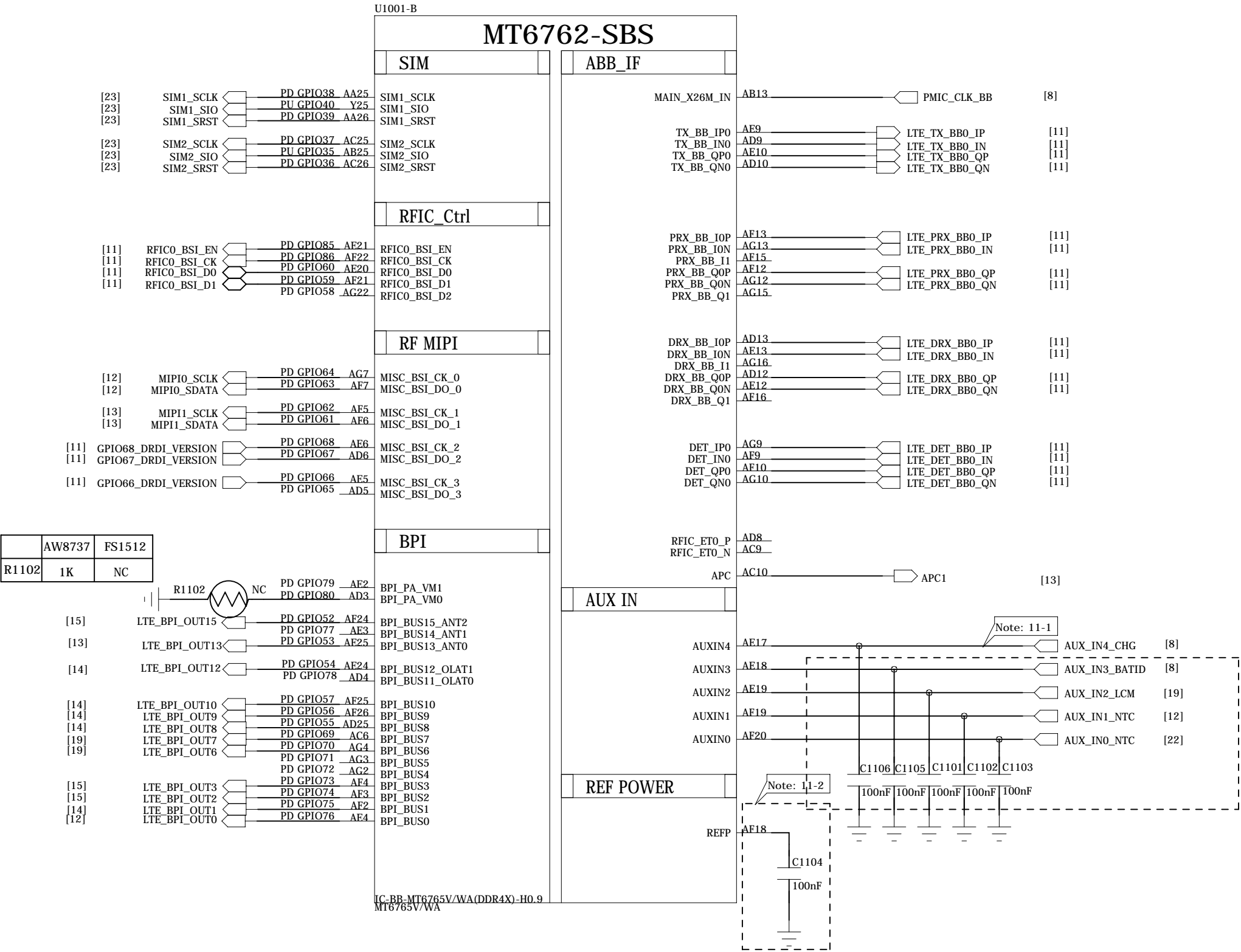
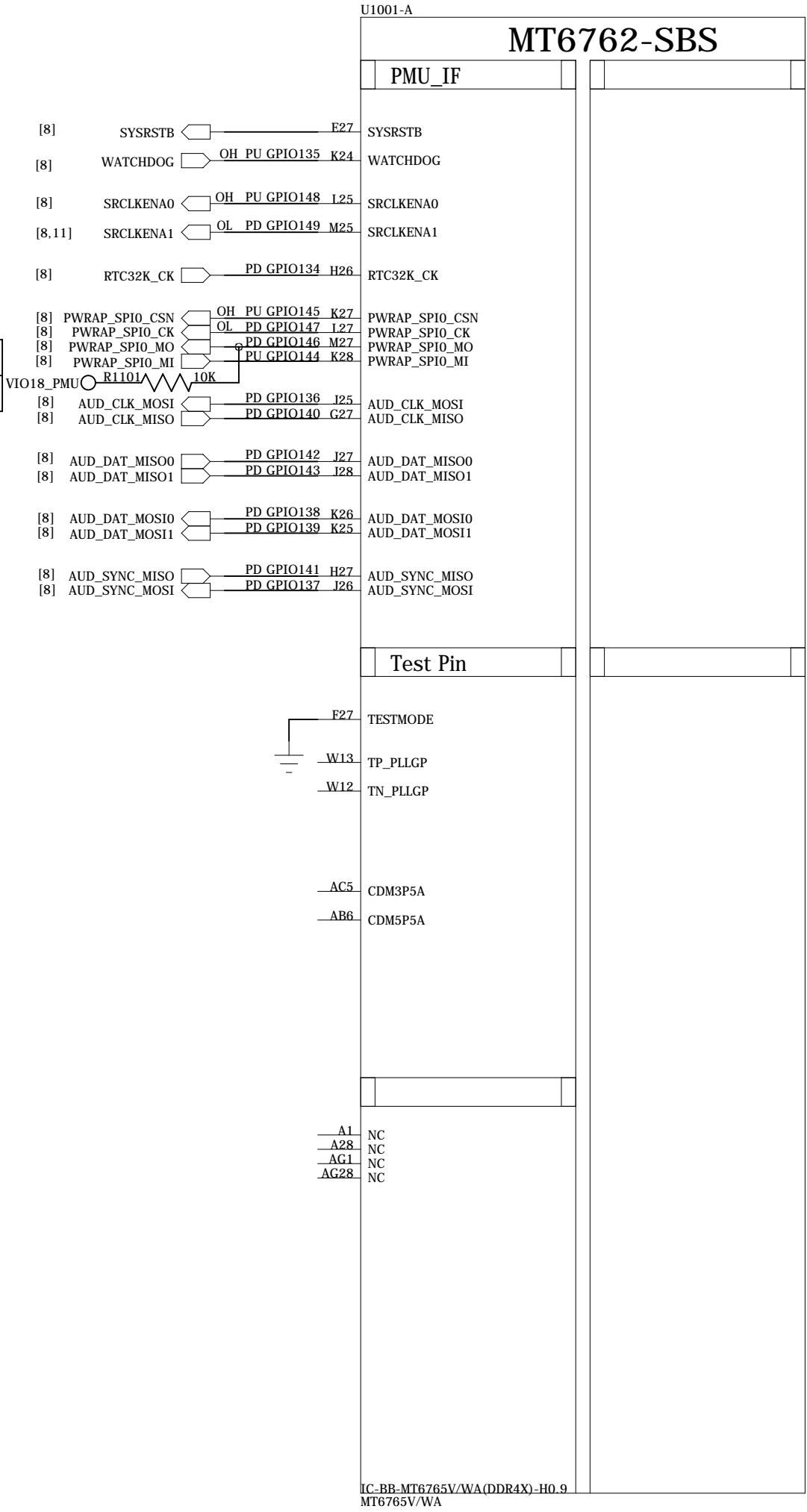
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DRAWN	DJF/TS	DATED	20200928	TITLE: 10_BB_POWER		VERSION: V1.0	SHEET: 3 OF 24
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	LPDDR4(discrete)	LPDDR4X “EMCP”
R1101	10K	NC

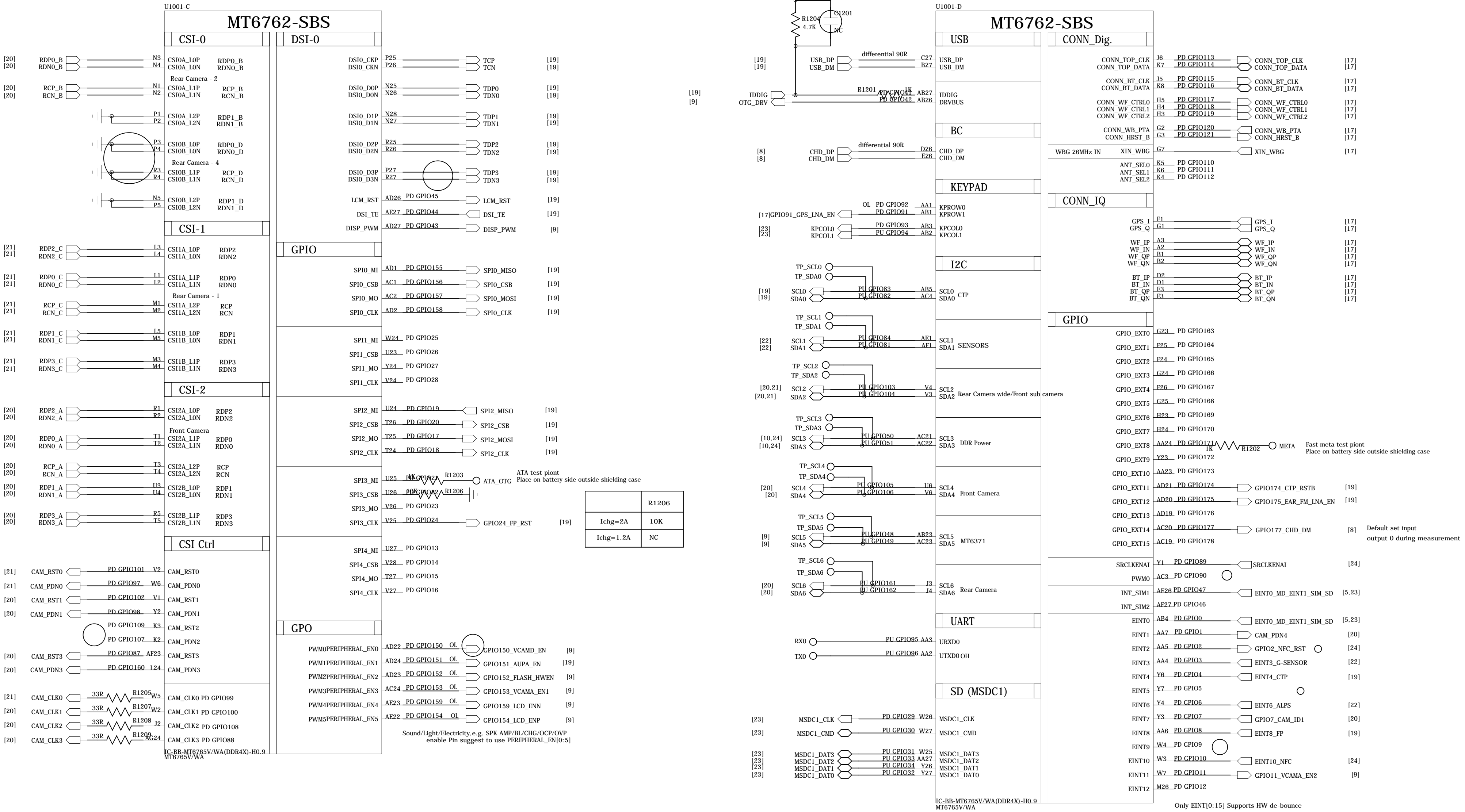


"PWRAP_SPI0_CSN" and "AUD_DAT_MOSIO" are bootstrap pin to select which interface will be the JTAG pin out.				
	PWRAP_SPI0_CSN	AUD_DAT_MOSIO	AP_JTAG	IO_JTAG
Default	(PU) HI	(PD) LO	N/A	N/A
	HI	HI (by ext. PU)	SPI_CSB/SPI_CLK/SPI_MO/SPI_MI/EINT8	N/A
	LO (by ext. PD)	LO	SPI_CSB/SPI_CLK/SPI_MO/SPI_MI/EINT8	SPI1+SPI3
	LO (by ext. PD)	HI (by ext. PU)	MSDC1_CLK/CMD/DAT0/DAT1/DAT2	N/A

Note 22-4: PWRAP_SPI0_MI are DDR type feature in bootstrap			
	PWRAP_SPI0_MI	Bootting interface	
	Default=PU	DDR	MSDC0 pin mux
	LO (by ext. PD)	LPDDR3	follow LP3 Ref SCH.
Default	HI	LPDDR4X	follow LP4X Ref SCH.

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DRAWN	DJF/TS	DATED	20200928	TITLE: 11_BB_I		VERSION: V1.0	SHEET: 4 OF 24
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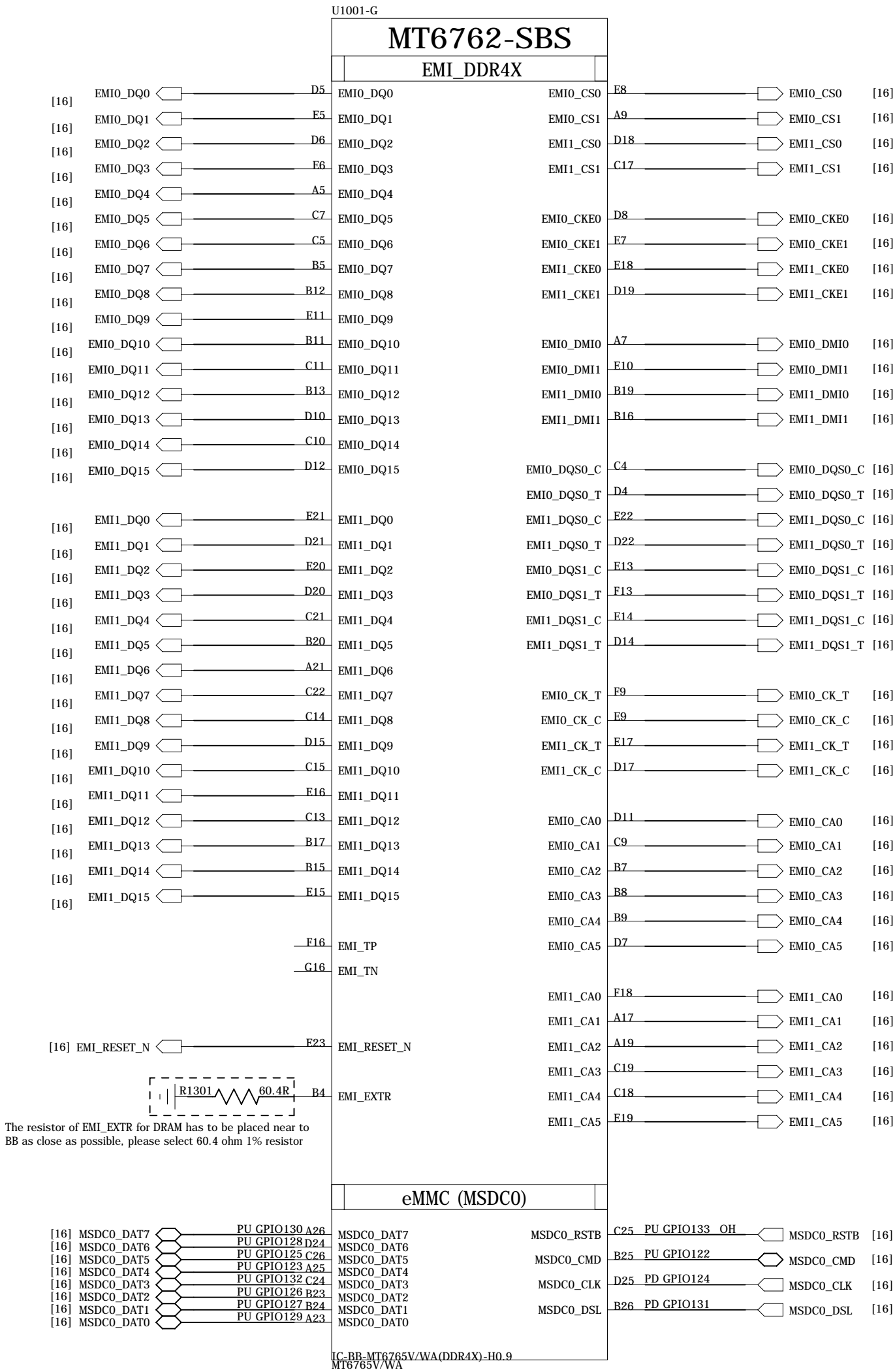
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COMPANY: TRANSSION HOLDINGS				MODEL: H6126		Modified Date: 2021/9/2	
DRAWN	DJF/TS	DATED	20200928	TITLE: 12_BB_II		VERSION: V1.0	SHEET: 5 OF 24
CHECKED	<CHECKED>	DATED	< >	Confidentiality	CONFIDENTIAL		

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LTR	ECO NO:	APPROVED:	DATE:

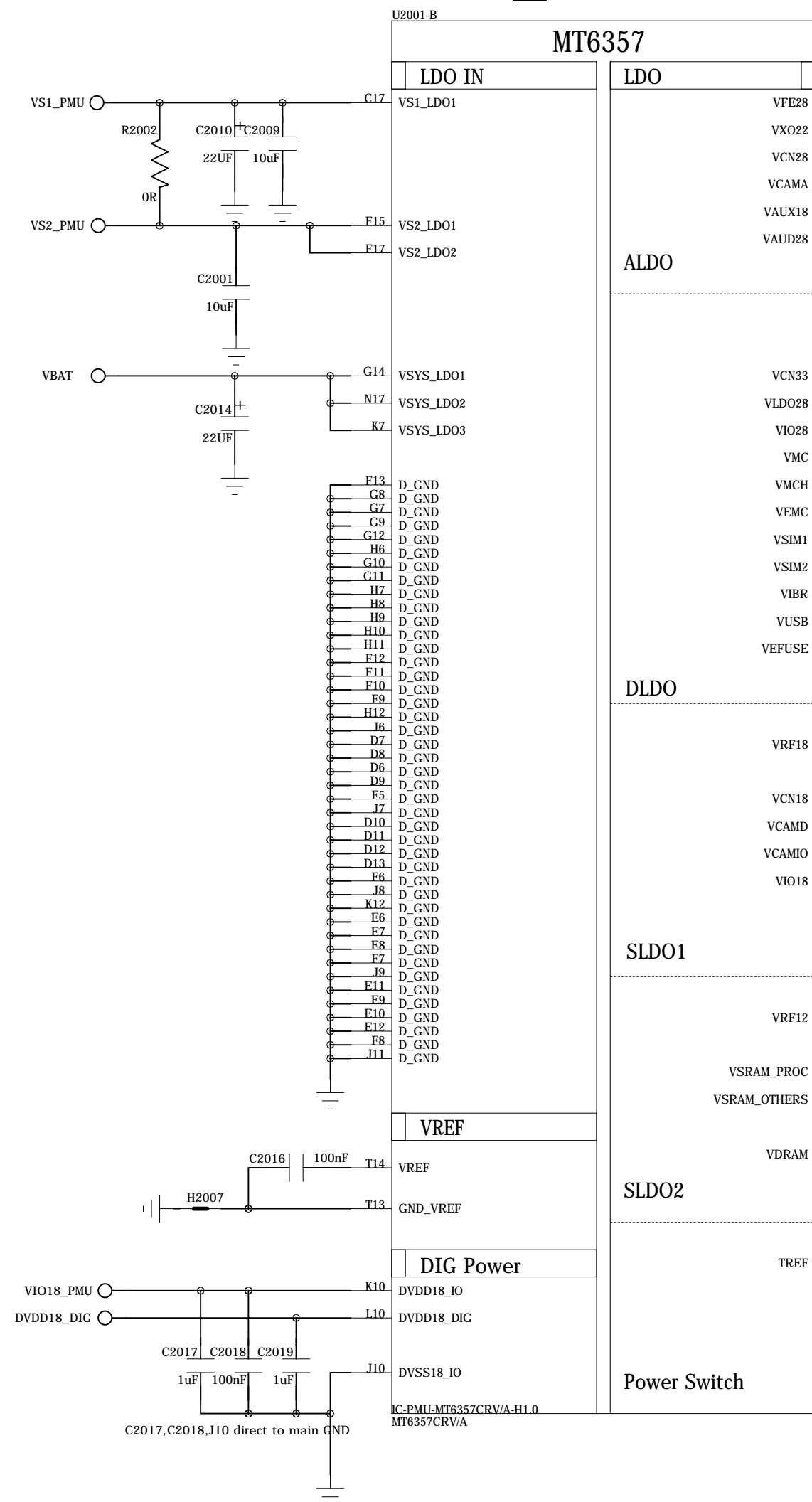
LPDDR4X\_EMI\_IF



COMPANY: TRANSSION HOLDINGS				MODEL: H6126		Modified Date: 2021/9/2	
DRAWN	DJF/TS	DATED	20200928	TITLE: 13_BB_III		VERSION: V1.0	SHEET: 6 OF 24
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LTR	ECO NO:	APPROVED:	DATE:

## PMU\_LDO



With/Trace length

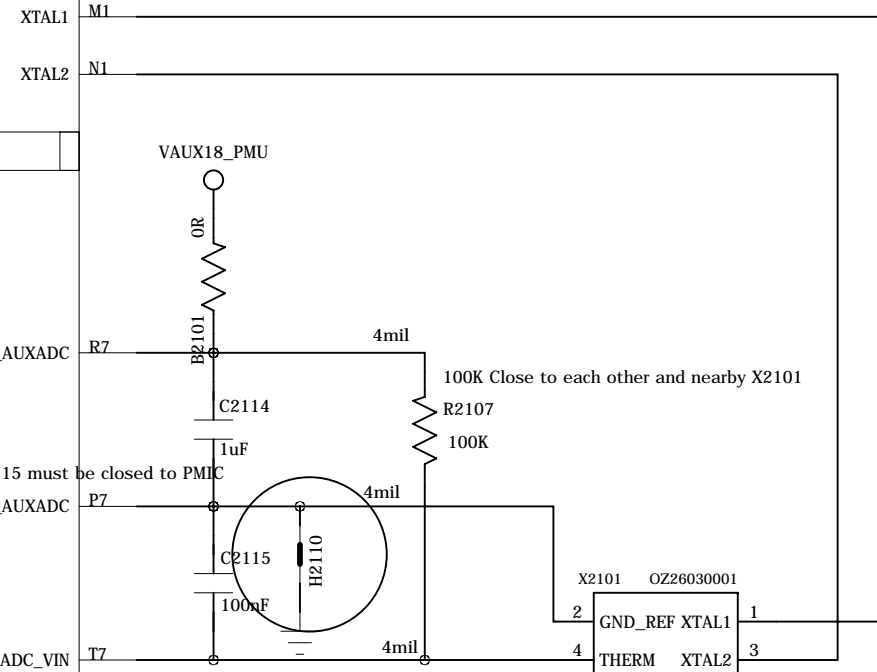
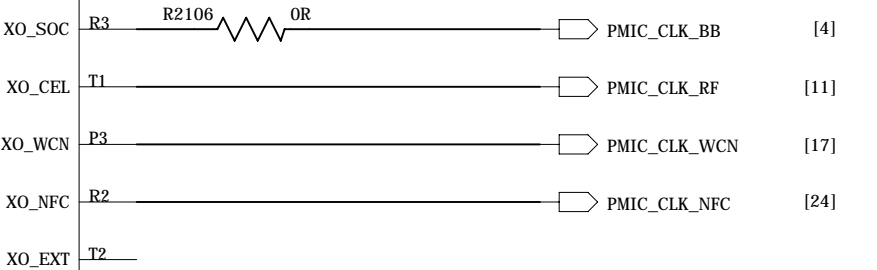
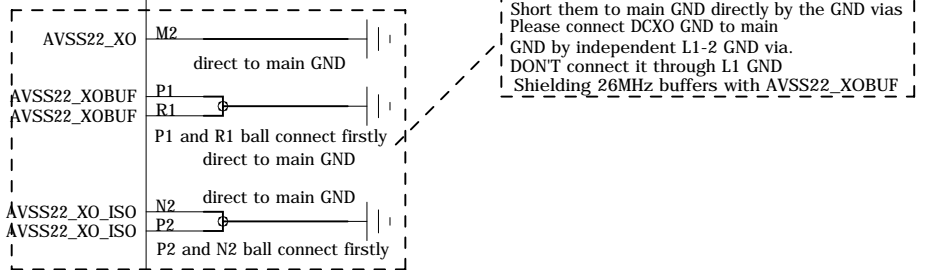
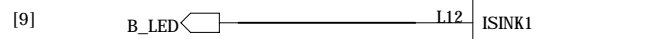
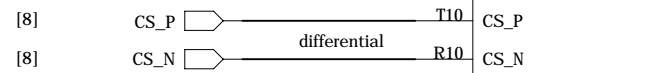
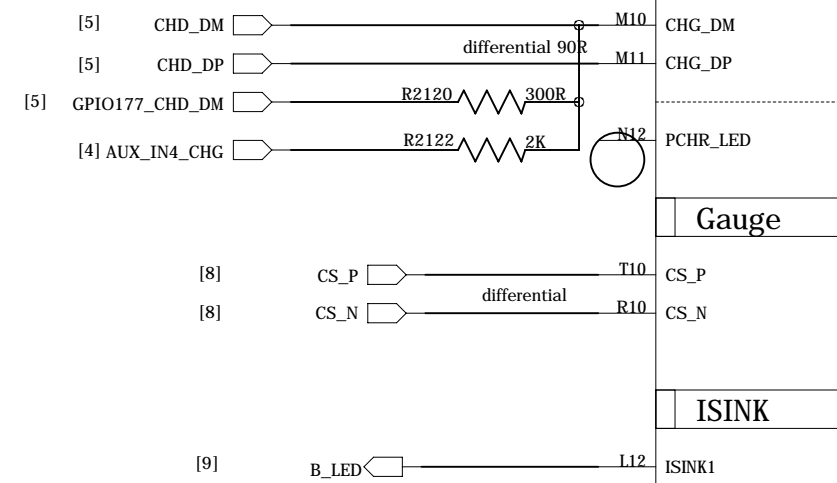
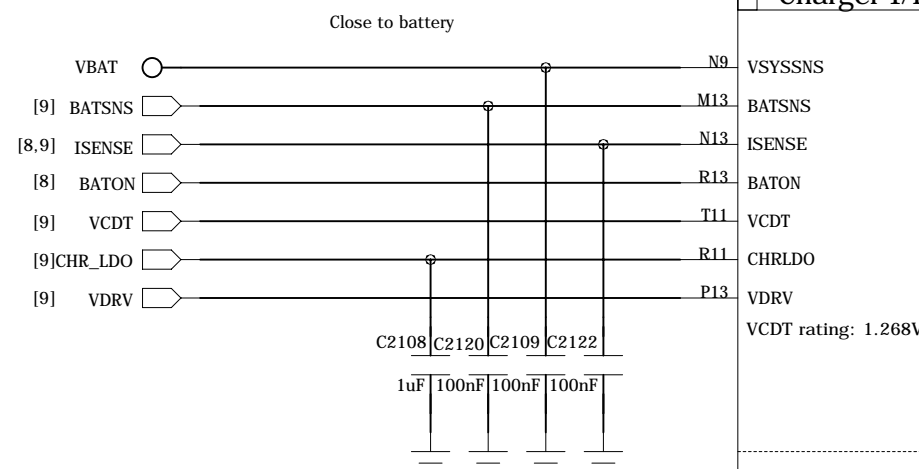
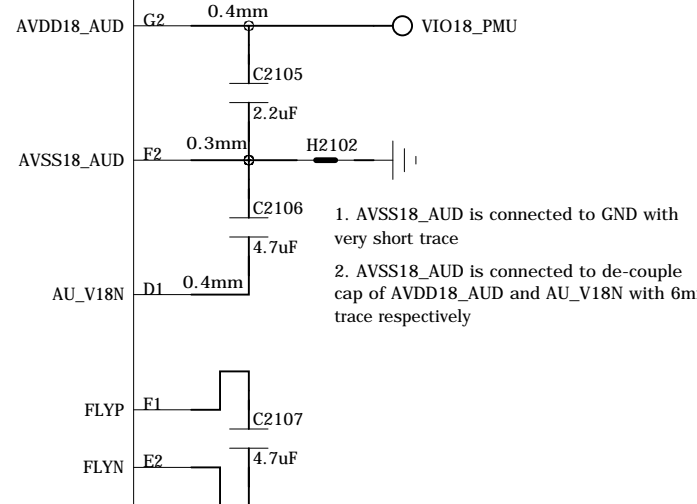
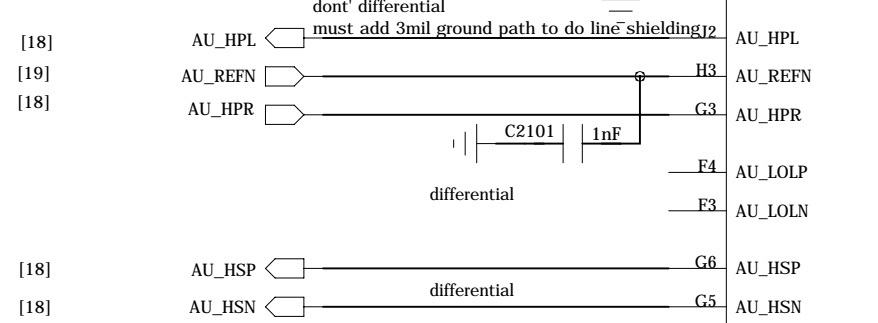
Signal	Trace Length	Component	Value
VFE28	L14 0.15mm/62.5mm	VFE28_PMU	2.8V/40mA
VX022	T4 0.15mm/62.5mm	VX022_PMU	2.24V/25mA
VCN28	K13 0.15mm/62.5mm	VCN28_PMU	2.8V/40mA
VCAMA	H16 0.2mm/75mm	VCAMA_PMU	1.8V/2.5V/2.7V/2.8V/2.9V/2.95V/3V/145mA
VAUX18	T5 0.15mm/62.5mm	VAUX18_PMU	1.8V/20mA
VAUD28	L7 0.15mm/62.5mm	VAUD28_PMU	2.8V/50mA
		Note:	20-1
VCN33	P17 0.5mm	VCN33_PMU	3.3V/3.4V/3.5V/3.6V/400mA
VLD028	L16 0.3mm/75mm	CTP_AFVDD_PMU2	8V/3.0V/360mA
VIO28	K15 0.2mm/75mm	VIO28_PMU	2.8V/200mA
VMC	L15 0.2mm/75mm	VMC_PMU	1.86V/2.9V/3.0V/3.3V/200mA
VMCH	N16 0.5mm/25mm	VMCH_PMU	2.9V/3.0V/3.3V/800mA
VEMC	L17 0.3mm/25mm	VEMC_PMU	2.9V/3.0V/3.3V/400mA
VSIM1	J17 0.15mm/62.5mm	VSIM1_PMU	1.7V/1.8V/1.86V/2.76V/3.0V/3.1V/50mA
VSIM2	K16 0.15mm/62.5mm	VSIM2_PMU	1.7V/1.8V/1.86V/2.76V/3.0V/3.1V/50mA
VIBR	M16 0.15mm/62.5mm	VIBR_PMU	1.2V/1.3V/1.5V/1.8V/2.0V/2.8V/3.0V/3.3V/100mA
VUSB	J14 0.15mm/62.5mm	VUSB33_PMU	3.07V/50mA
VEFUSE	H15 0.2mm/75mm	VEFUSE_PMU	1.2V/1.3V/1.5V/1.8V/2.0V/2.8V/3.0V/3.3V/200mA
VRF18	D16 0.35mm/75mm	VRF18_PMU	1.81V/450mA
VCN18	F15 0.2mm/75mm	VCN18_PMU	1.8V/200mA
VCAMD	F17 0.35mm/75mm	VCAMD_PMU	1V/1.0V/1.1V/1.2V/1.3V/1.5V/350mA/1.8V/200mA
VCAMIO	A17 0.2mm/75mm	VCAMIO_PMU	1.8V/140mA
VIO18	B17 0.4mm/25mm	VIO18_PMU	1.8V/600mA
		H2010	AVDD18_SOC
VRF12	F16 0.2mm/75mm	VRF12_PMU	1.2V/200mA
RAM_PROC	G15 0.2mm/25mm	DVDD_SRAM_DVFS	0.6V~1.31V/460mA
M_OTHERS	G16 0.2mm/25mm	VSRAM_OTHERS_PMU	0.6V~1.31V/460mA
VDRAM	H17 0.45mm/25mm	VDRAM_PMU	1.12V/1.24V/1200mA
TREF	R9 0.15mm/50/75mm	TREF_PMU	

Note 20-1: If these power trace can meet LDO layout constraint, these CAP can be NC or removed.  
Please refer to MT6357 design notice.

COMPANY: TRANSSION HOLDINGS				MODEL: H6126		Modified Date: 2021/9/2	
DRAWN	DJF/TS	DATED	20200928	TITLE: 20_POWER_MT6357_I		VERSION: V1.0	SHEET: 7 OF 24
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REVISION RECORD			
LTR	ECO NO:	APPROVED:	DATE:

U2001-D		MT6357	
AUDIO IF		UL POWER	
16.	AUD_CLK_MISO	AVDD28_AUD	
17.	AUD_DAT_MISO0		
17.	AUD_DAT_MISO1		
16.	AUD_SYNC_MISO		
16.	AUD_CLK_MOSI	AVSS28_AUD	
15.	AUD_DAT_MOSI0		
14.	AUD_DAT_MOSI1		
14.	AUD_SYNC_MOSI		
AUDIO INPUT		AU_MICBIAS0	
		AU_MICBIAS1	
		CHARGE PUMP	
13.	AU_VIN0_P	AVDD18_AUD	
14.	AU_VIN0_N		
15.	AU_VIN1_P		
15.	AU_VIN1_N		
14.	AU_VIN2_P	AVSS18_AUD	
15.	AU_VIN2_N		
ACCDDET		AU_V18N	
14.	ACCDDET	FLYP	
11.	HP_EINT	FLYN	
AUDIO OUTPUT			
12.	AU_HPL		
13.	AU_REFN		
13.	AU_HPR		
14.	AU_LOLP		
13.	AU_LOLN		
16.	AU_HSP		
15.	AU_HSN		
IC:PMU-MT6357CRV/A-H1.0			
MT6357CRV/A			



Route AVDD18\_AUXADC/AUXADC\_VIN as differential trace (4 mil each) with well GND shielding and route AVSS18\_AUXADC with 4mil trace width with well GND shielding

Connect PMIC pin AVDD18\_AUXADC to AUXADC GND first  
 and then connect it to main GND by a inner\_layer short\_pad  
 Connect Vaux18\_PMU to C2114 first, and then connect to 100Kohm and AVDD18\_AUXADC  
 Keep the crystal 4~4.4mm away from PMIC, and XTLA11 and XTLA12 length <10mm for signal quality consideration  
 Keep-out all crystal components >0.25mm away from surrounding metal  
 Place the crystal inside the shielding case, and keep >1mm away from the PCB edge ,and >20mm away from USB ,headphones, vibrator

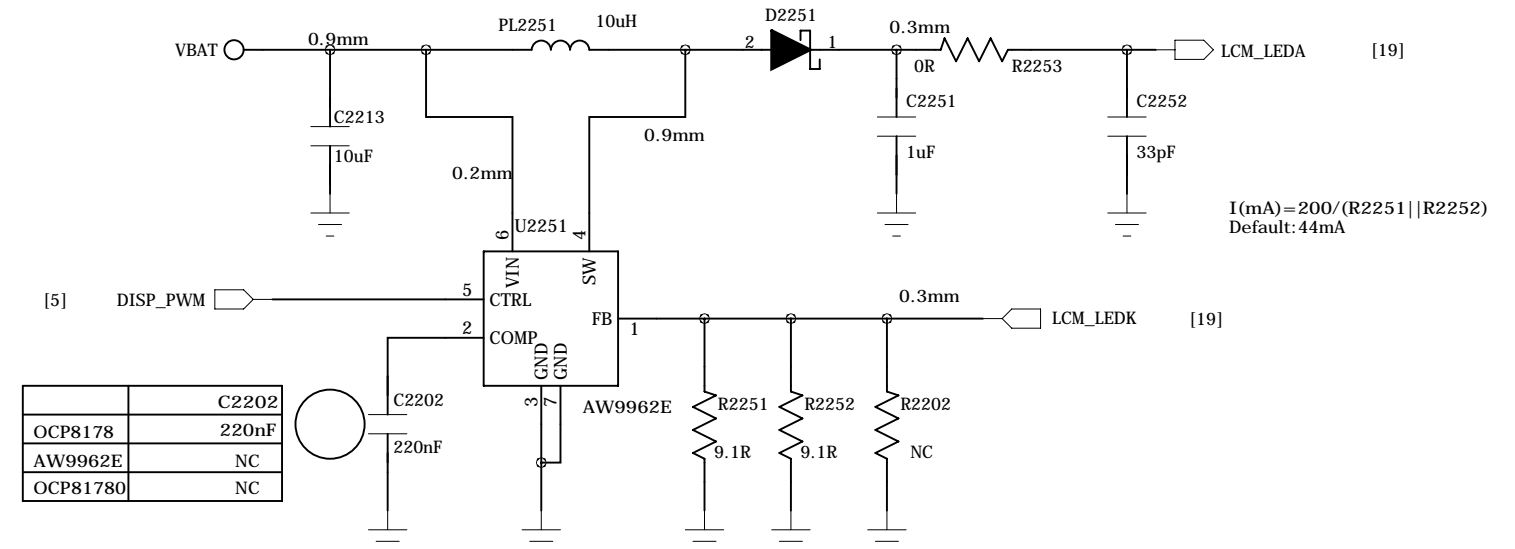
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COMPANY: TRANSSION HOLDINGS				MODEL: H6126		Modified Date: 2021/9/2	
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## VCAMA\_M1 (1.05V)

# SW CHARGER

## Backlight and face flash

[illegible]

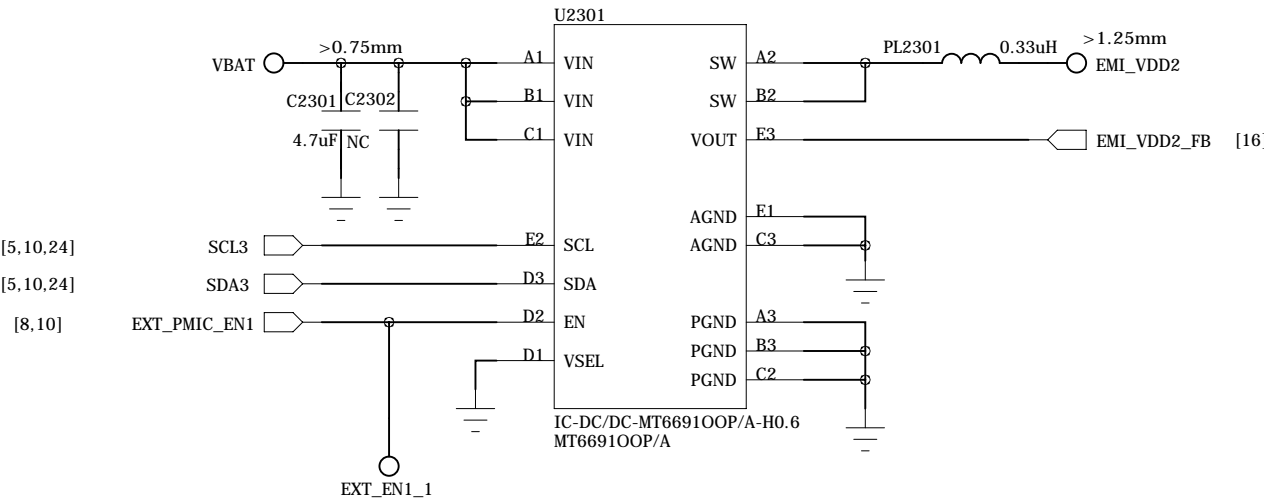
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DRAWN	DJF/TS	DATED	20200928	TITLE: 22_POWER_THIRD-PARTY_I		VERSION: V1.0	SHEET: 9 OF 24
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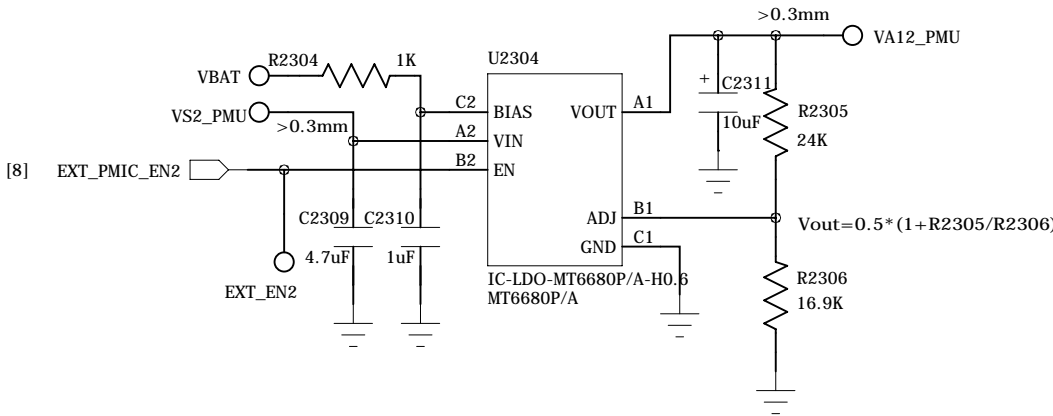
POWER\_THIRD-PARTY\_II

Ext. buck LP4 VDRAM

HL7593WL02 / Ext. buck LP4X VDRAM (VDD2)Default  
MT6691OOP/A / Ext. buck LP4X VDRAM (VDD2) Reserve  
I2C address: 0X57 (Write:0xAE, Read:0xAF)

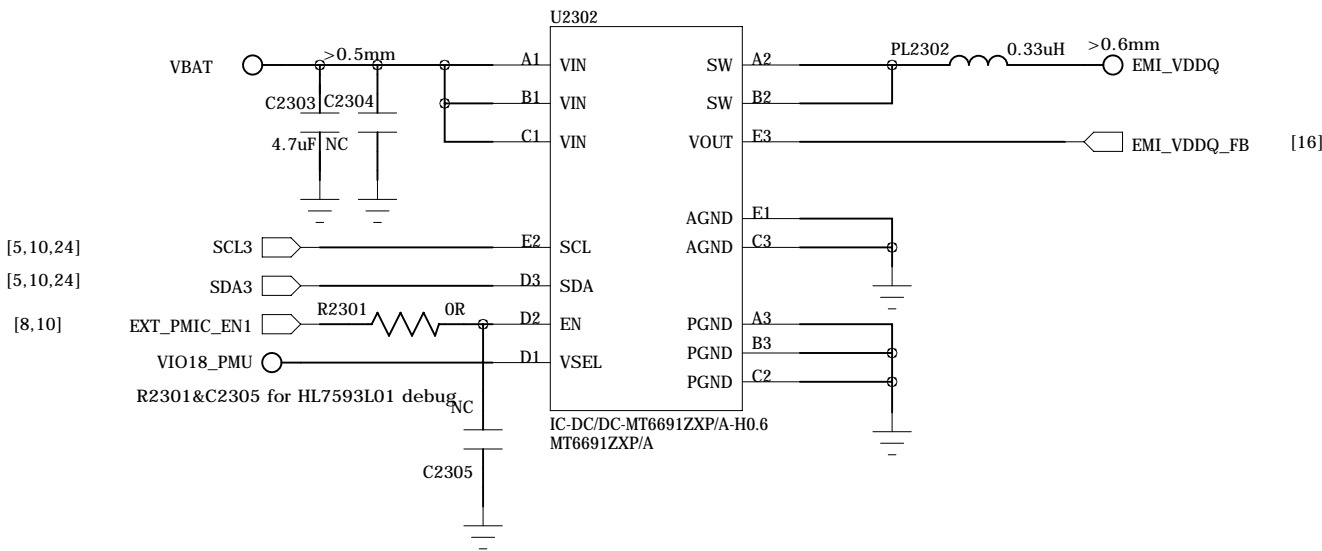


LDO 1.2V for VA12

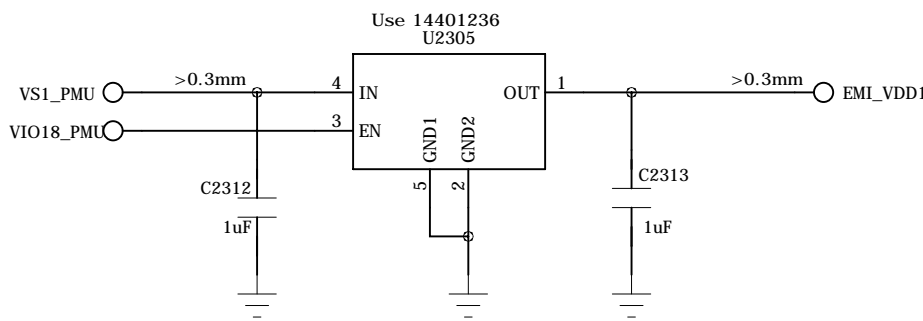


Ext. buck LP4X VDDQ

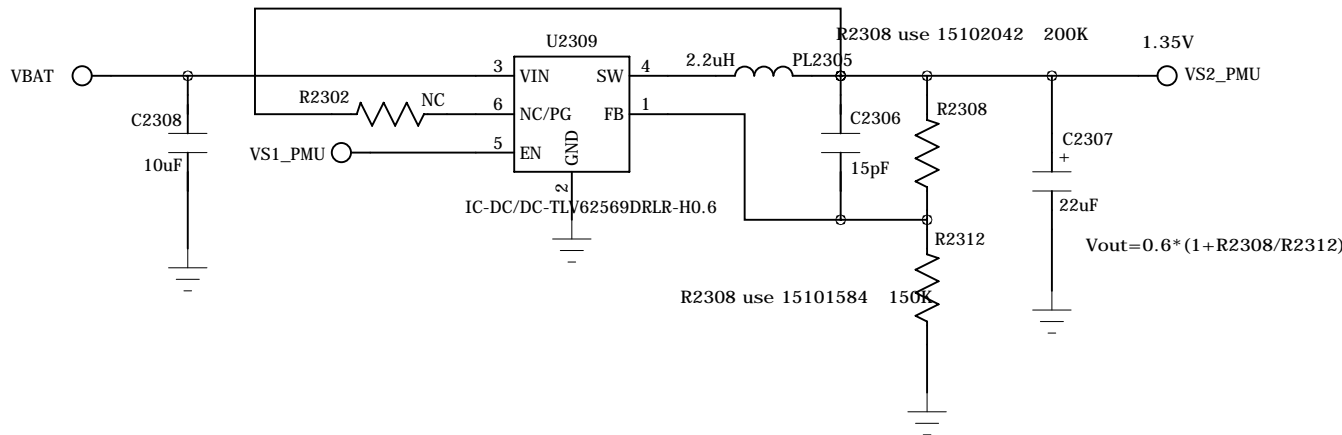
HL7593WL01 / Ext. buck LP4X VDRAM (VDDQ)Default  
MT6691ZXP/A / Ext. buck LP4X VDRAM(VDDQ)Reserve  
I2C address: 0x50 (Write:0xA0, Read:0xA1)



LPDDR4 VDD1 1.8V LDO

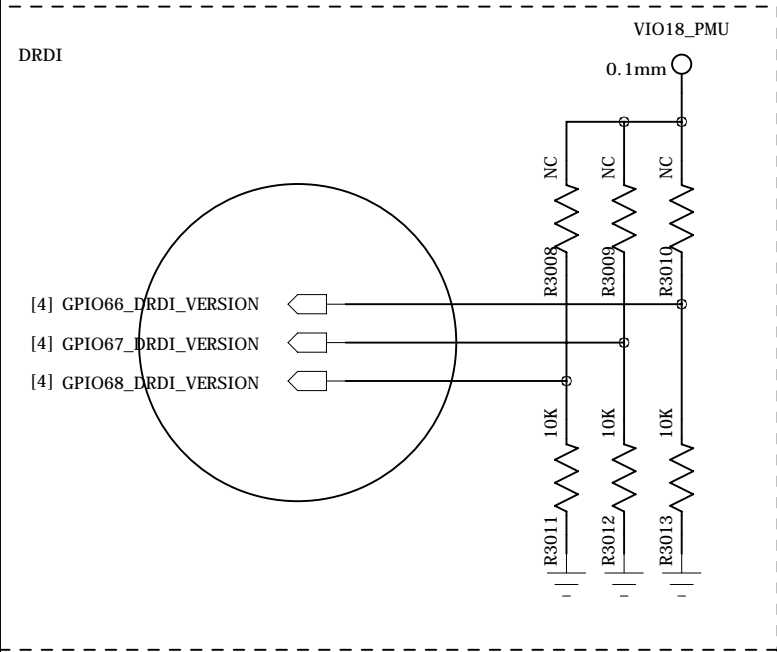


buck for VS2\_PMU



COMPANY: TRANSSION HOLDINGS				MODEL: H6126		Modified Date: 2021/9/2	
DRAWN	DJF/TS	DATED	20200928	TITLE: 23_POWER_THIRD-PARTY_II		VERSION: V1.0	SHEET: 10 OF 24
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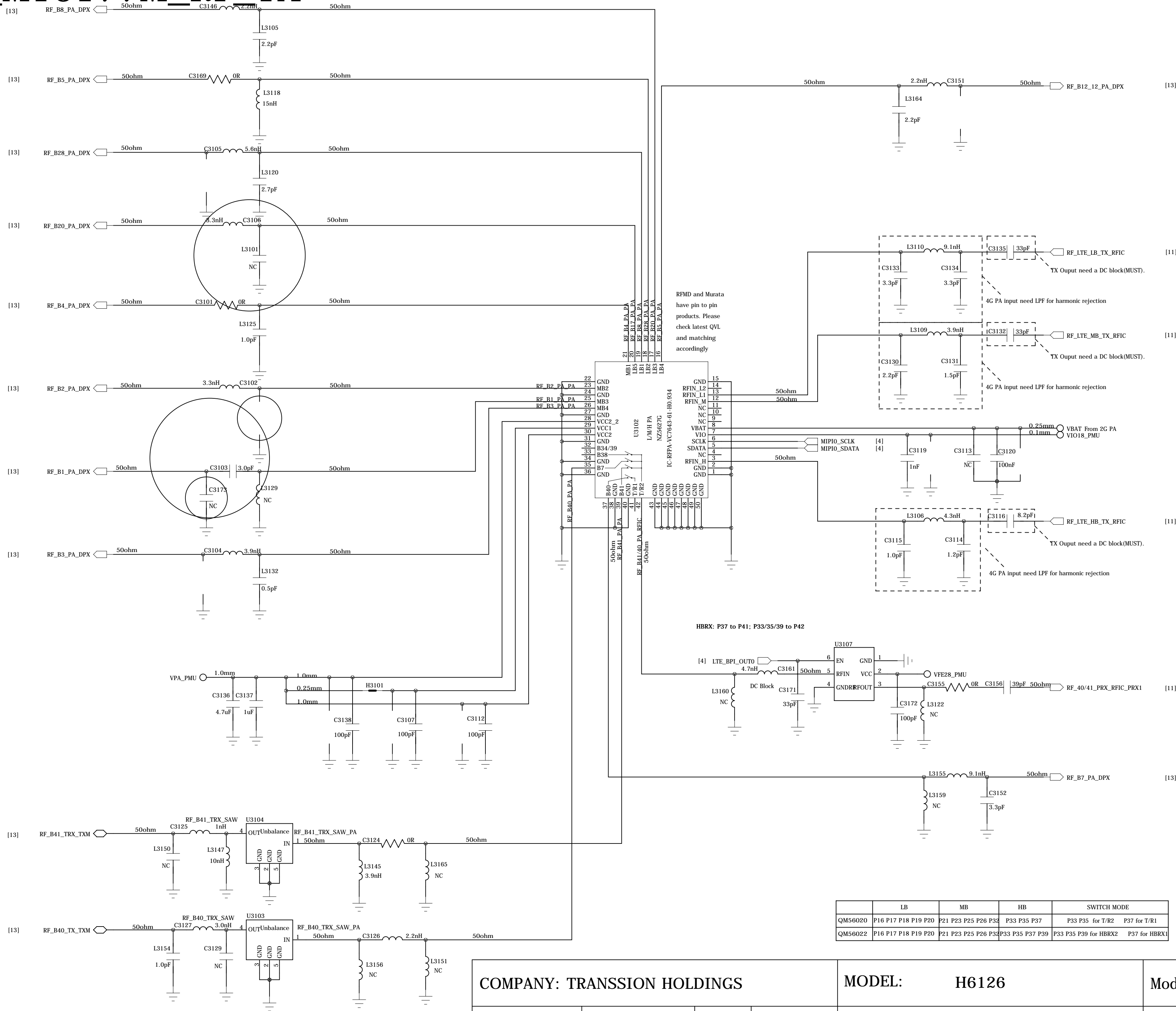
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COMPANY: TRANSSION HOLDINGS				MODEL: H6126		Modified Date: 2021/9/2	
DRAWN	DJF/TS	DATED	20200928	TITLE: 30_RF_MT6177M_PIN_OUT		VERSION: V1.0	SHEET: 11 OF 24
CHECKED	<CHECKED>	DATED	< >	Confidentiality	CONFIDENTIAL		

# RF\_MT6177M\_RF\_TX

REVISION RECORD			
LTR	ECO NO:	APPROVED:	DATE:

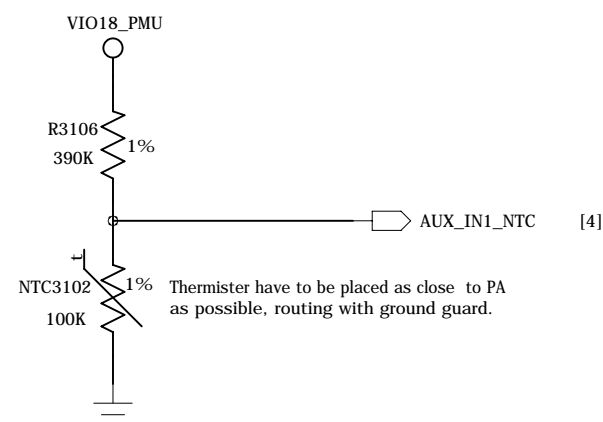


3/4G\_PAIN\_LB

3/4G\_PAIN\_MB

3/4G\_PAIN\_HB

Temp Sensor

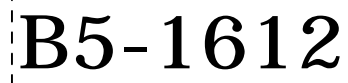
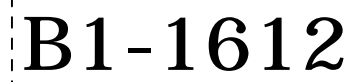
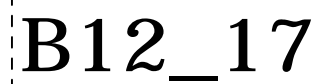


COMPANY: TRANSSION HOLDINGS				MODEL: H6126		Modified Date: 2021/9/2	
DRAWN	DJF/TS	DATED	20200928	TITLE: 31_RF_MT6177M_RF_TRX		VERSION: V1.0	SHEET: 12 OF 24
CHECKED	<CHECKED>	DATED	< >	Confidentiality	CONFIDENTIAL		

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LTR	ECO NO:	APPROVED:	DATE:

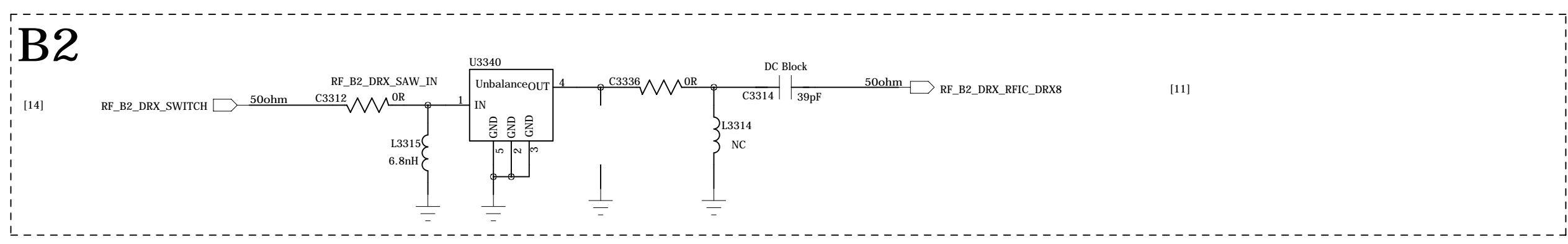
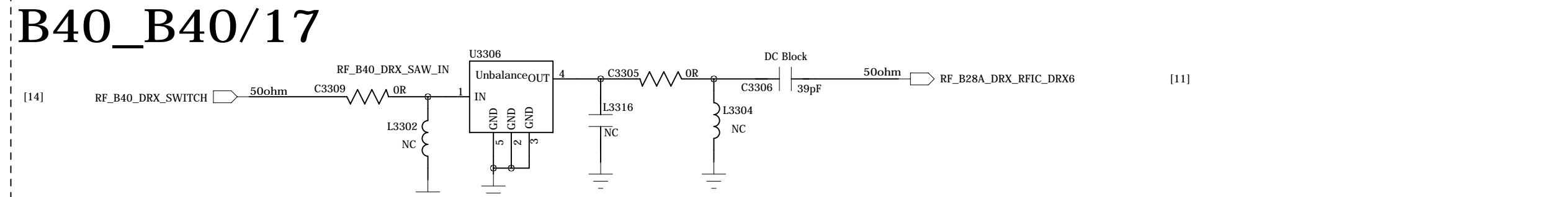
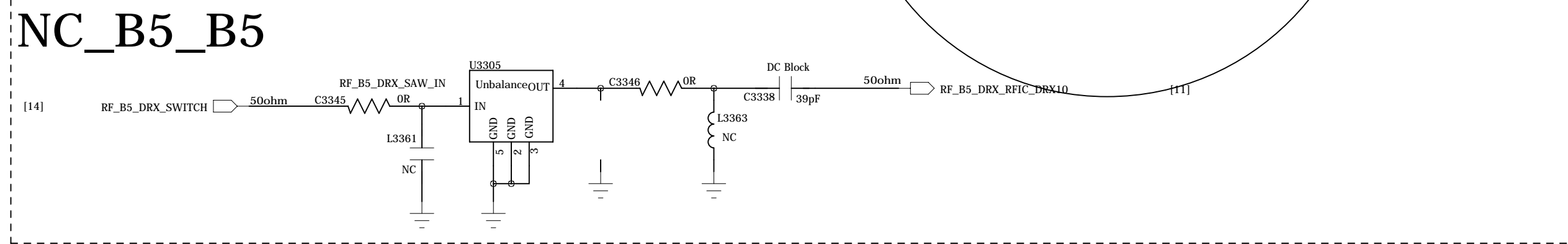
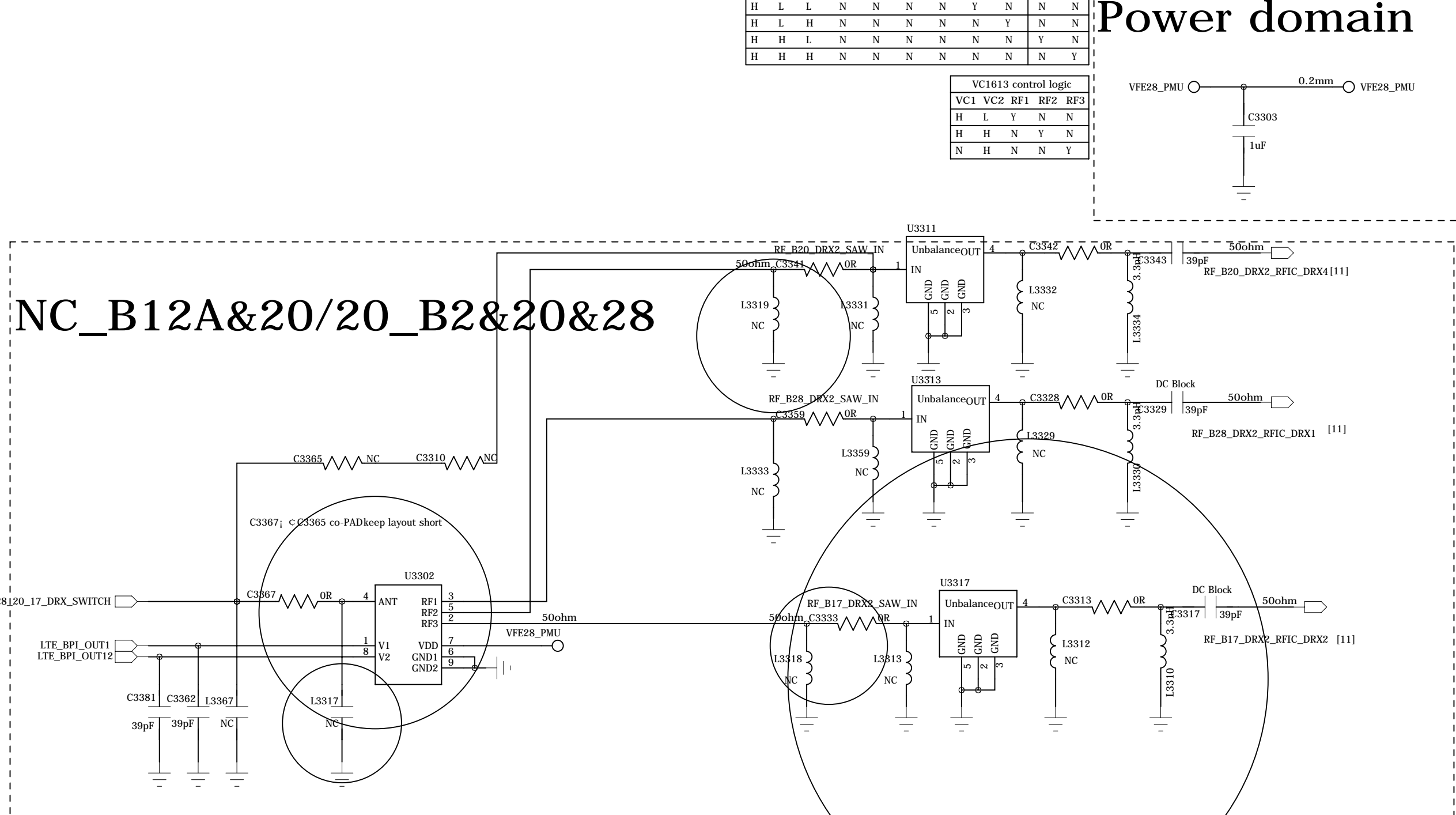
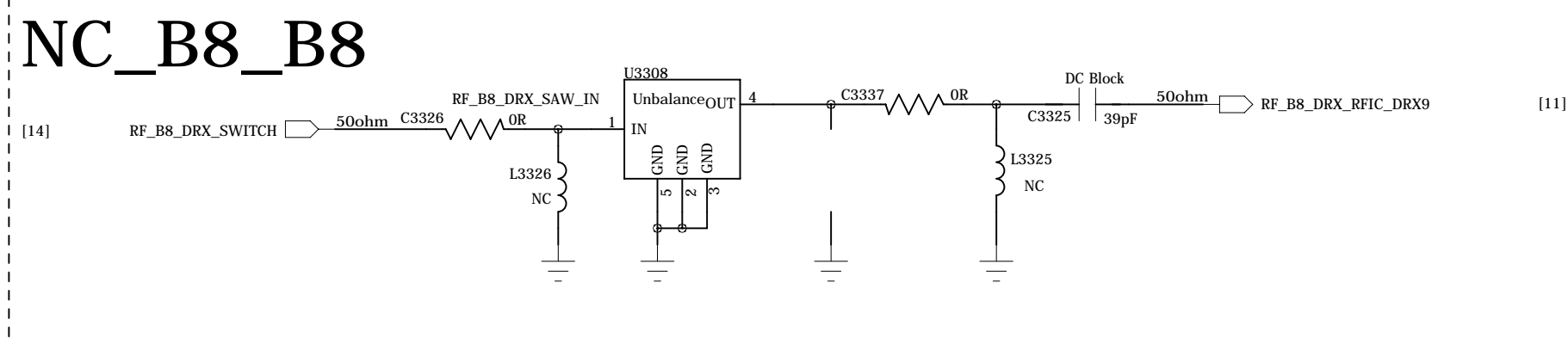
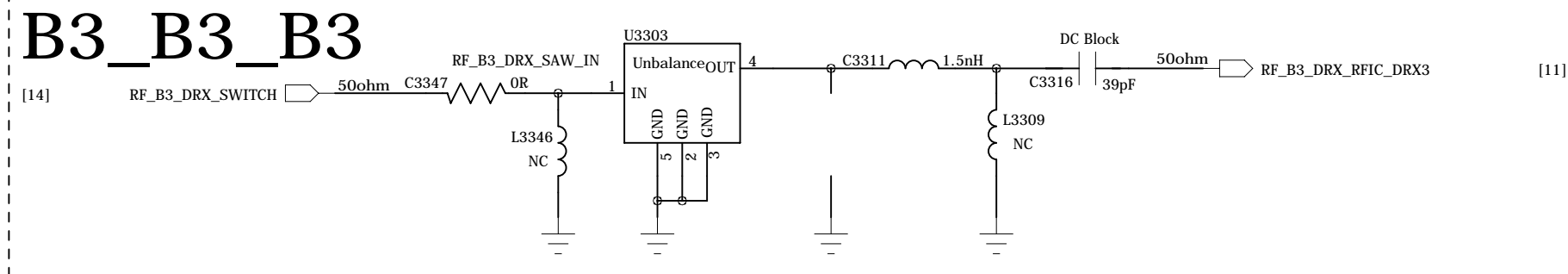
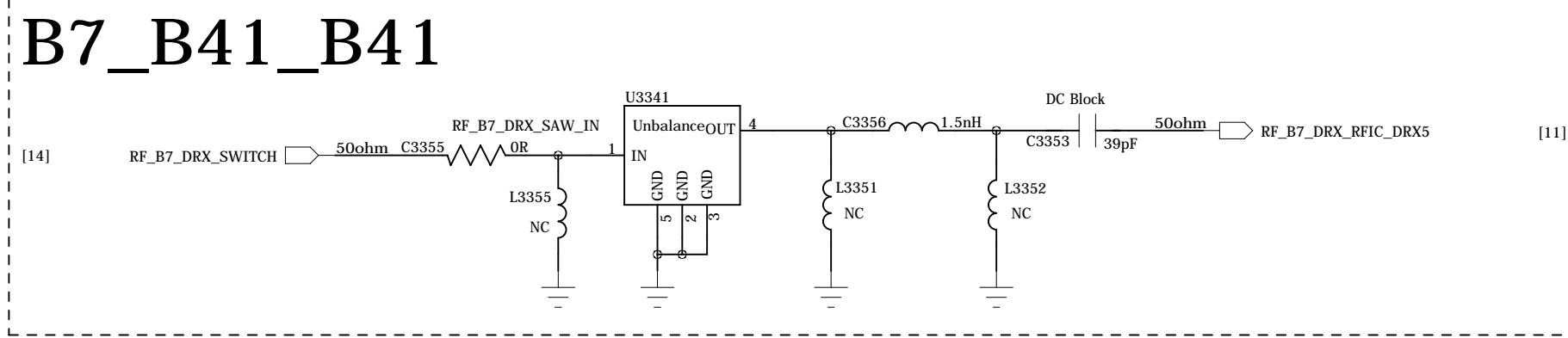
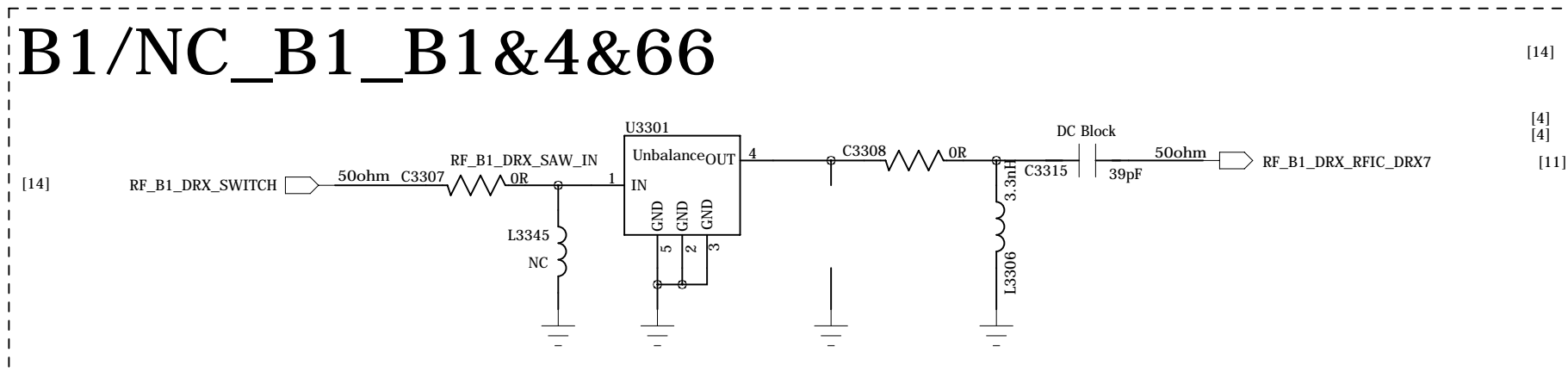
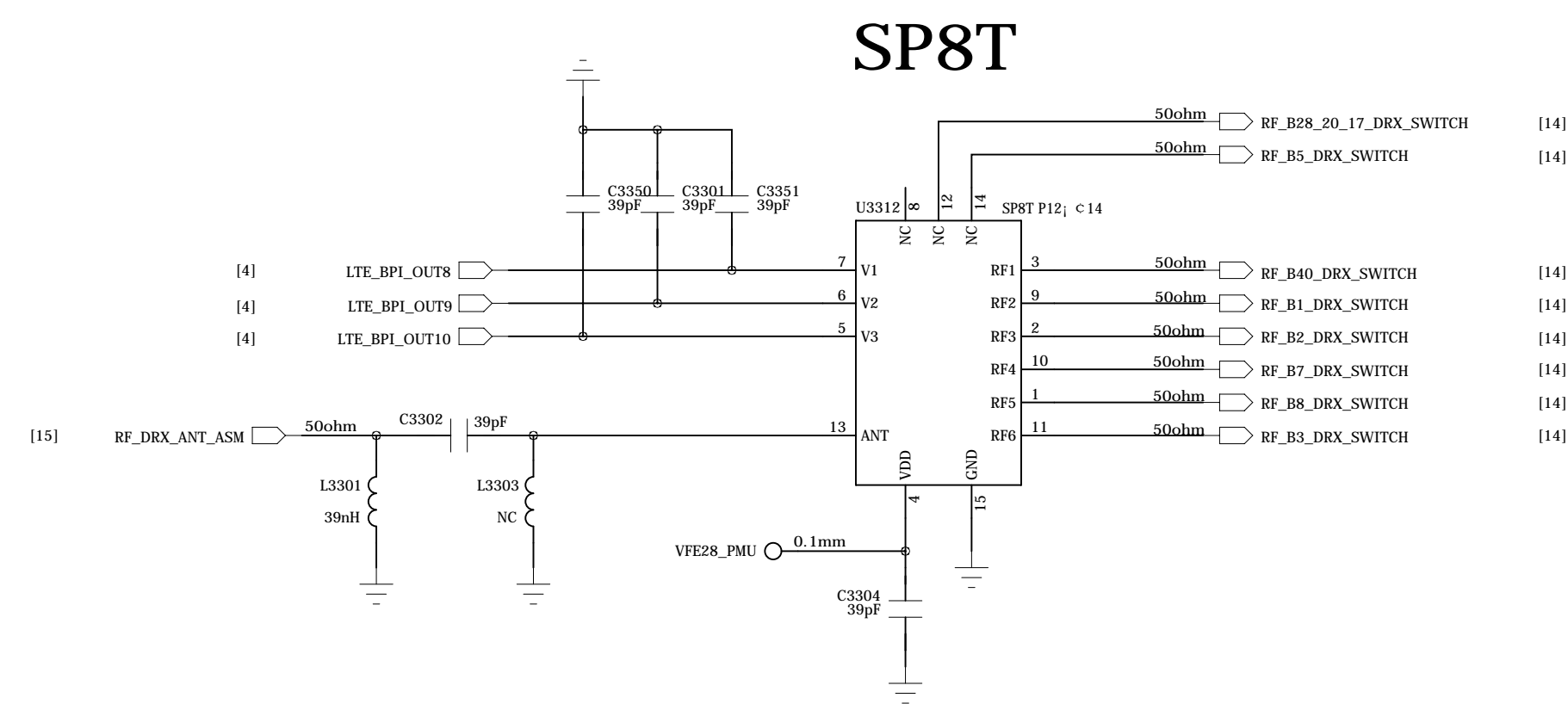


B28 or B28A



COMPANY: TRANSSION HOLDINGS				MODEL: H6126		Modified Date: 2021/9/2	
DRAWN	DJF/TS	DATED	20200928	TITLE: 32_RF_MT6177M_RF_PRX		VERSION: V1.0	SHEET: 13 OF 24
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## RF\_MT6177M\_RF\_DRX



SP8T control logic										
SP6T control logic										
V1	V2	V3	RF1	RF2	RF3	RF4	RF5	RF6	RF7	RF8
L	L	L	Y	N	N	N	N	N	N	N
L	L	H	N	Y	N	N	N	N	N	N
L	H	L	N	N	Y	N	N	N	N	N
L	H	H	N	N	Y	N	N	N	N	N
H	L	L	N	N	N	Y	N	N	N	N
H	L	H	N	N	N	N	Y	N	N	N
H	H	L	N	N	N	N	N	N	Y	N
H	H	H	N	N	N	N	N	N	N	Y

VC1613 control logic				
VC1	VC2	RF1	RF2	RF3
H <td>L<td>Y<td>N<td>N</td></td></td></td>	L <td>Y<td>N<td>N</td></td></td>	Y <td>N<td>N</td></td>	N <td>N</td>	N
H <td>H<td>N<td>Y<td>N</td></td></td></td>	H <td>N<td>Y<td>N</td></td></td>	N <td>Y<td>N</td></td>	Y <td>N</td>	N
N <td>H<td>N<td>N</td><td>Y</td></td></td>	H <td>N<td>N</td><td>Y</td></td>	N <td>N</td> <td>Y</td>	N	Y

REVISION RECORD			
LTR	ECO NO:	APPROVED:	DATE:

# Power domain

VFE28\_PMU

0.2mm

VFE28\_PMU

C3303

1uF

50ohm

3343 39pF  
RF\_B20\_DRX2\_RFIC\_DRX4[11]

L3334

DC Block

Figure 1 shows a schematic diagram of a 1-bit full adder. The circuit includes a 3329 CMOS inverter, a 39pF capacitor, and a 50ohm load resistor. The input is labeled 'OR' and the output is labeled '11'.

RF\_B17\_DRX2\_RFIC\_DRX2 [11]

L3310

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2021/0/2

2021/9/2

0 SHEET 14 OF 24

	SHEET: 11 OF 31
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COMPANY: TRANSSION HOLDINGS				MODEL: H6126		Modified Date: 2021/9/2	
DRAWN	DJF/TS	DATED	20200928	TITLE: 33_RF_MT6177M_RF_DRX		VERSION: V1.0	SHEET: 14 OF 24
CHECKED	<CHECKED>	DATED	< >	Confidentiality	CONFIDENTIAL		

RF\_MT6177M\_RF\_ANT

REVISION RECORD			
LTR	ECO NO:	APPROVED:	DATE:

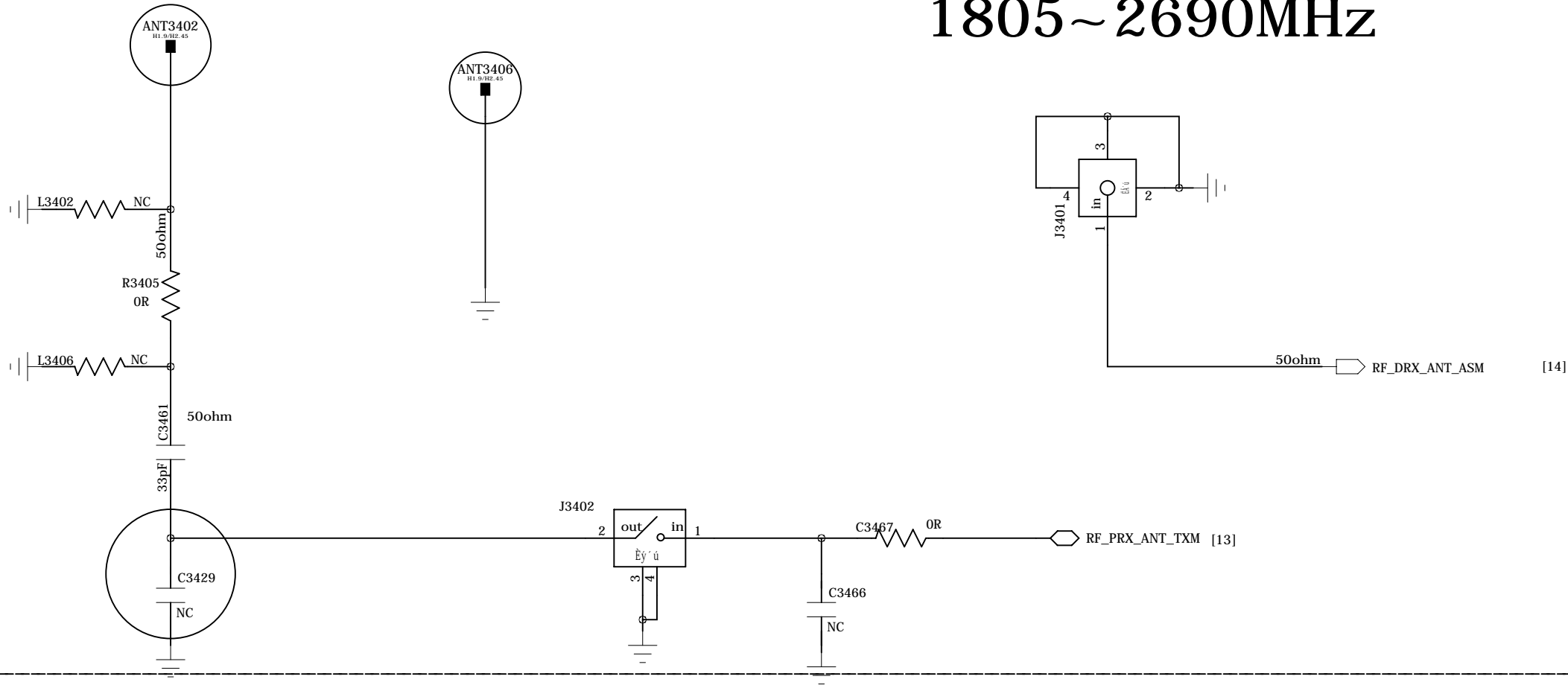
ASM\_Main

791~960MHz + 1710~2690MHz

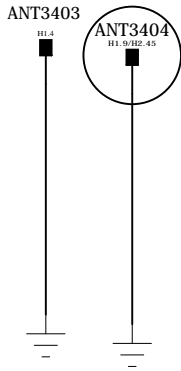
DRX ANT

791~821MHz

1805~2690MHz



ANT switch

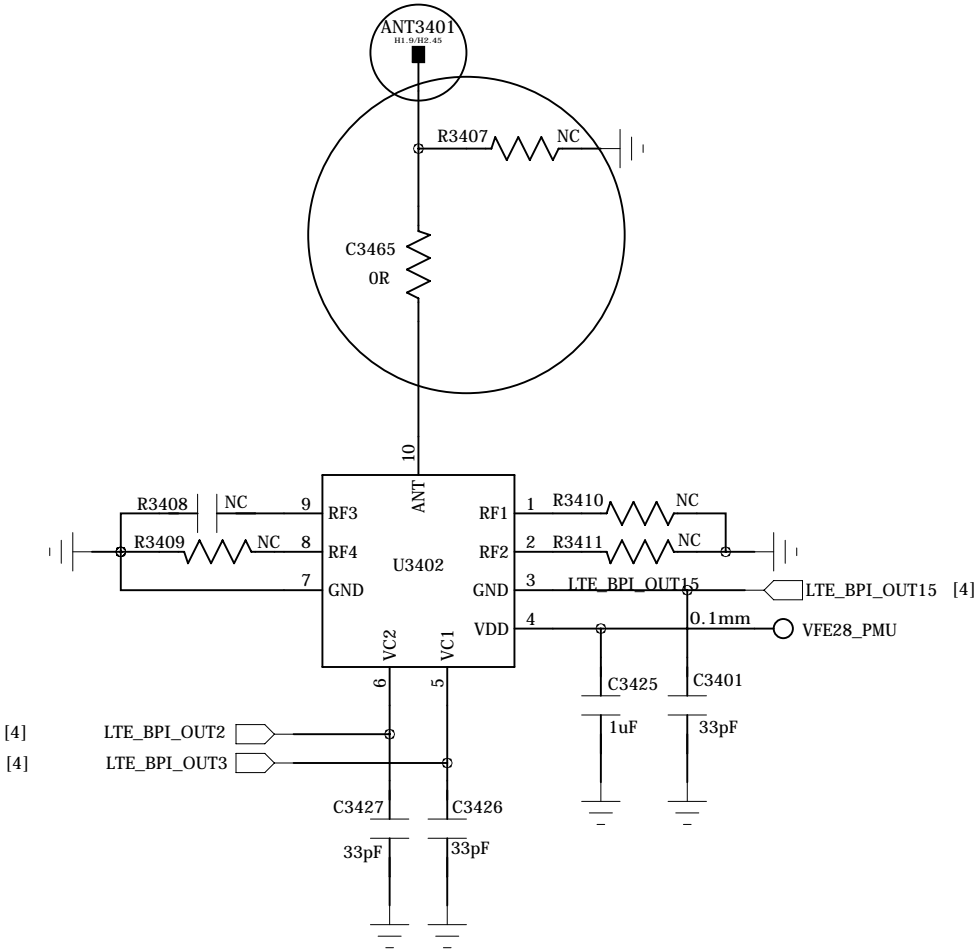


ANT switch

RF1119A & RF1694 control logic					
VC1	VC2	RF1	RF2	RF3	RF4
L	L	Y	N	N	N
L	H	N	Y	N	N
H	L	N	N	Y	N
H	H	N	N	N	Y

DPDT

C3405,C3407,C3403,C3406,R3406,R3416,R3417,U3401,U3404		R3412,R3415
Without DPDT	Without Material	With Material
DPDT	With Material	Without Material



COMPANY: TRANSSION HOLDINGS

MODEL: H6126

Modified Date: 2021/9/2

DRAWN DJF/TS DATED20200928

TITLE: 34\_RF\_ANT\_CONTROLLER

VERSION: V1.0 SHEET: 15 OF 24

CHECKED <CHECKED> DATED < >

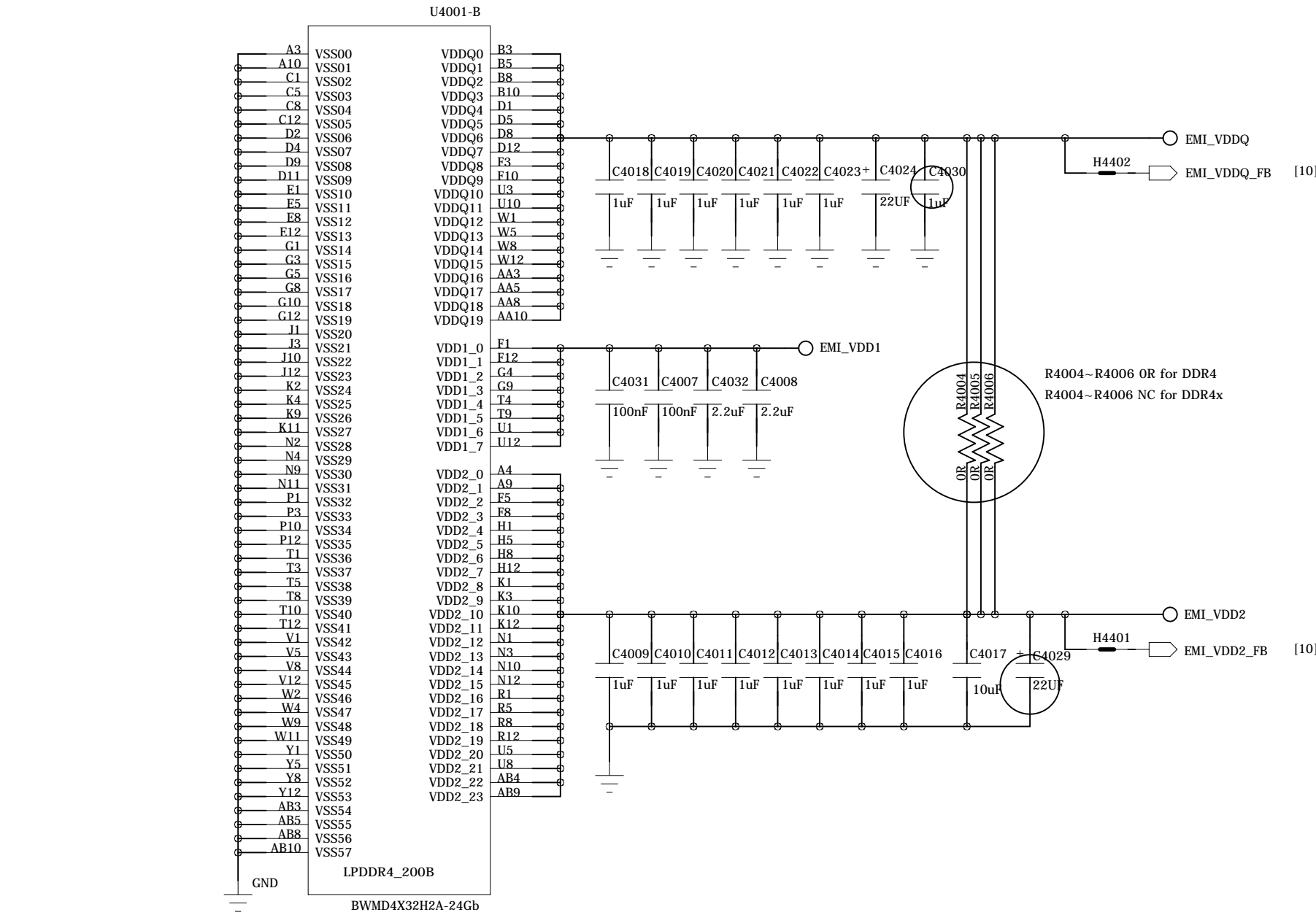
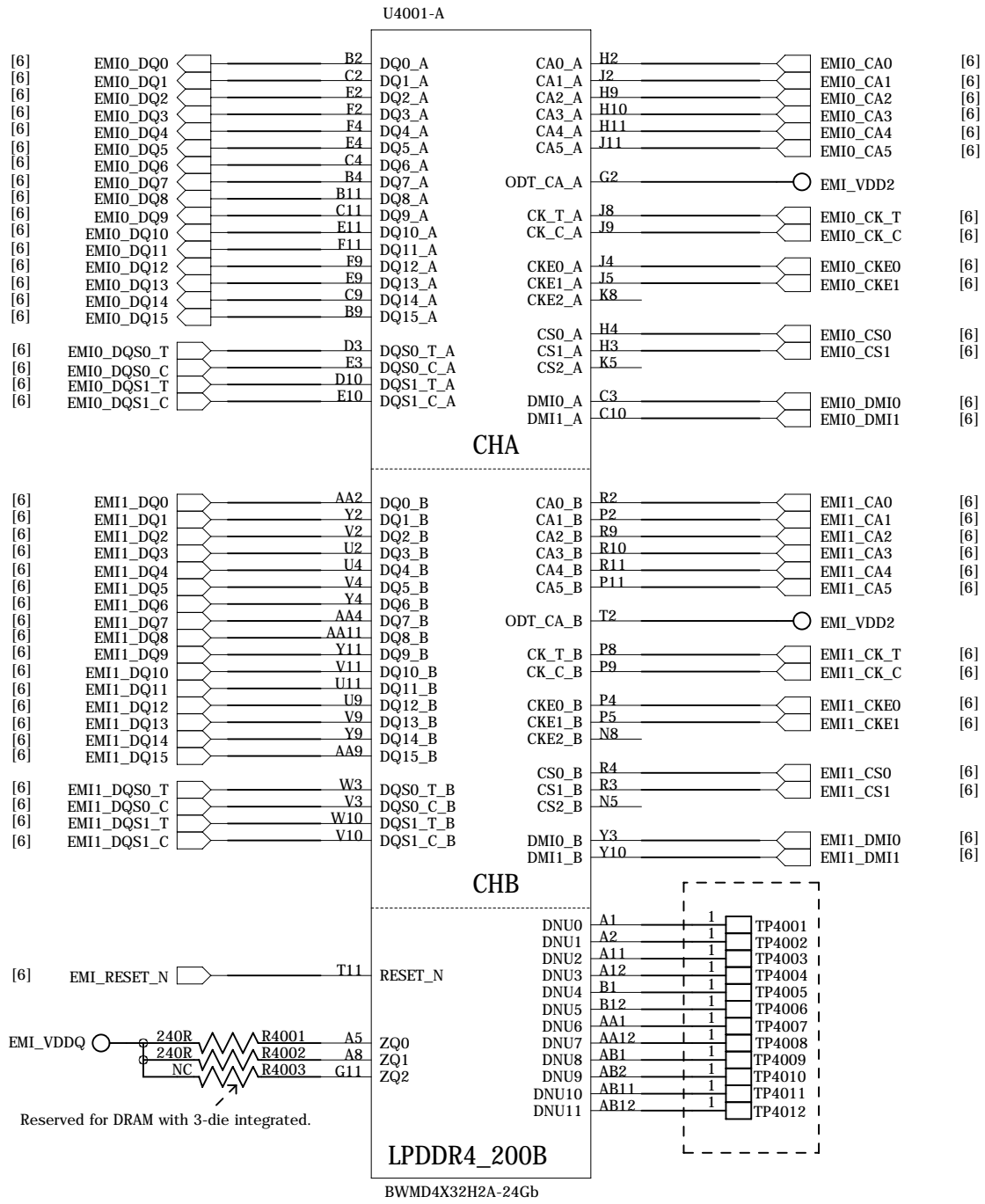
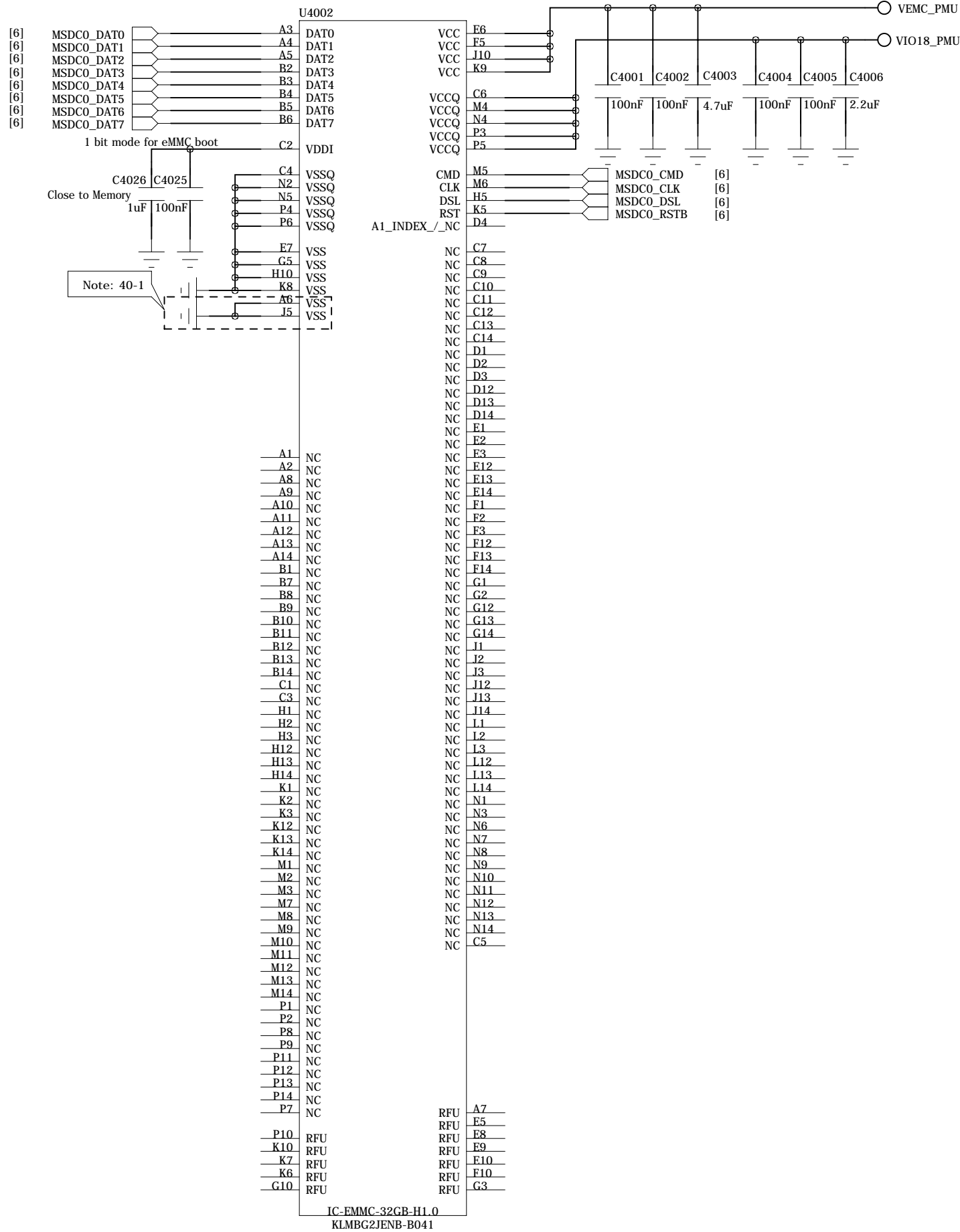
Confidentiality CONFIDENTIAL

MEMORY\_eMMC\_LPDDR4/4X

MEMORY\_LPDDR4

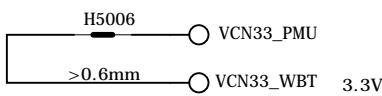
REVISION RECORD			
LTR	ECO NO:	APPROVED:	DATE:

153 ball eMMC



COMPANY: TRANSSION HOLDINGS				MODEL: H6126		Modified Date: 2021/9/2	
DRAWN	DJF/TS	DATED	20200928	TITLE: 40_MEMORY_EMMC_LPDDR4X		VERSION: V1.0	SHEET: 16 OF 24
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REVISION RECORD			
LTR	ECO NO:	APPROVED:	DATE:

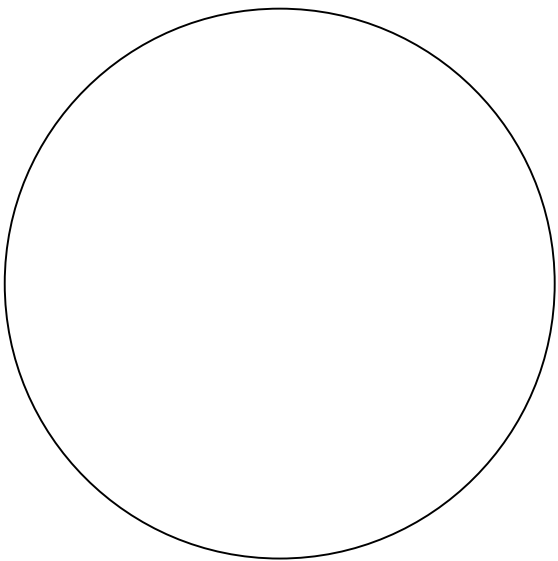


COMPANY: TRANSSION HOLDINGS				MODEL: H6126		Modified Date: 2021/9/2	
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CHECKED	<CHECKED>	DATED	< >	Confidentiality	CONFIDENTIAL		



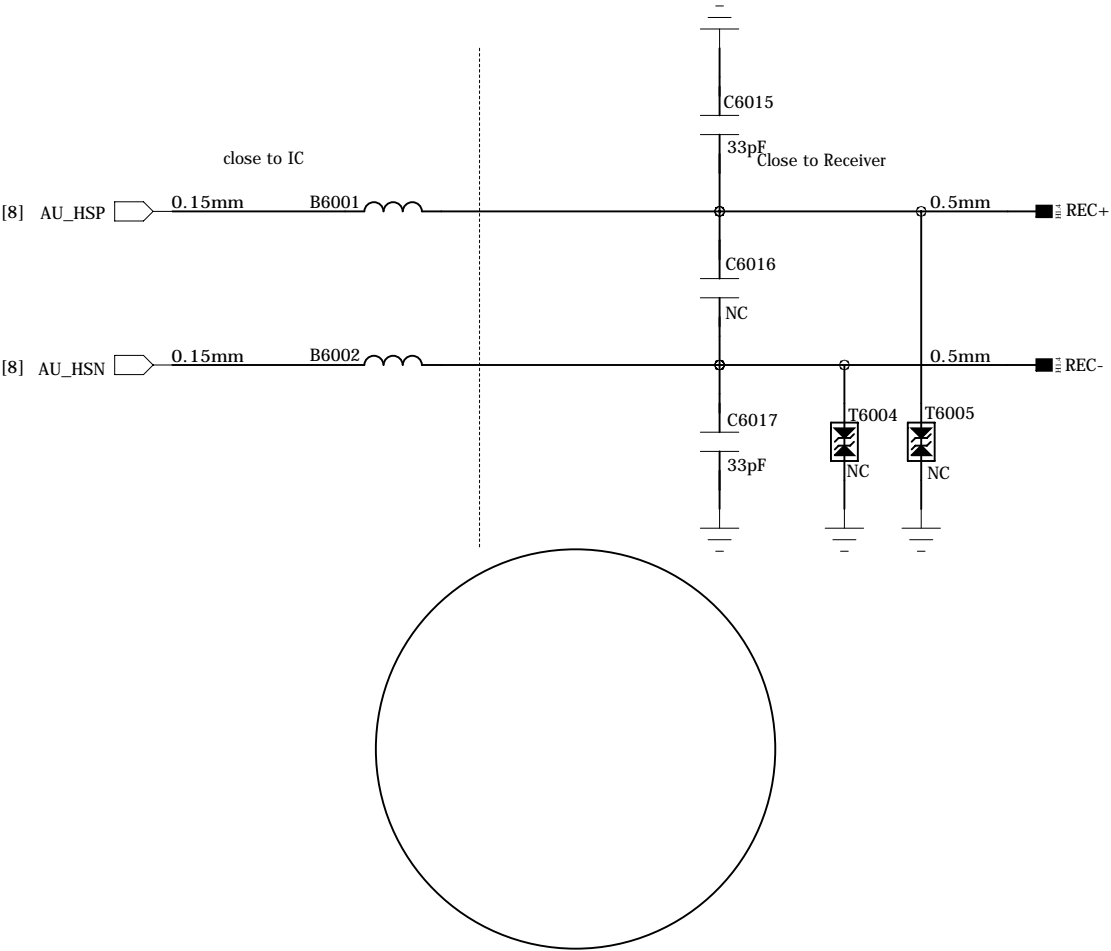
PERI\_AUDIO\_IO

Audio PA

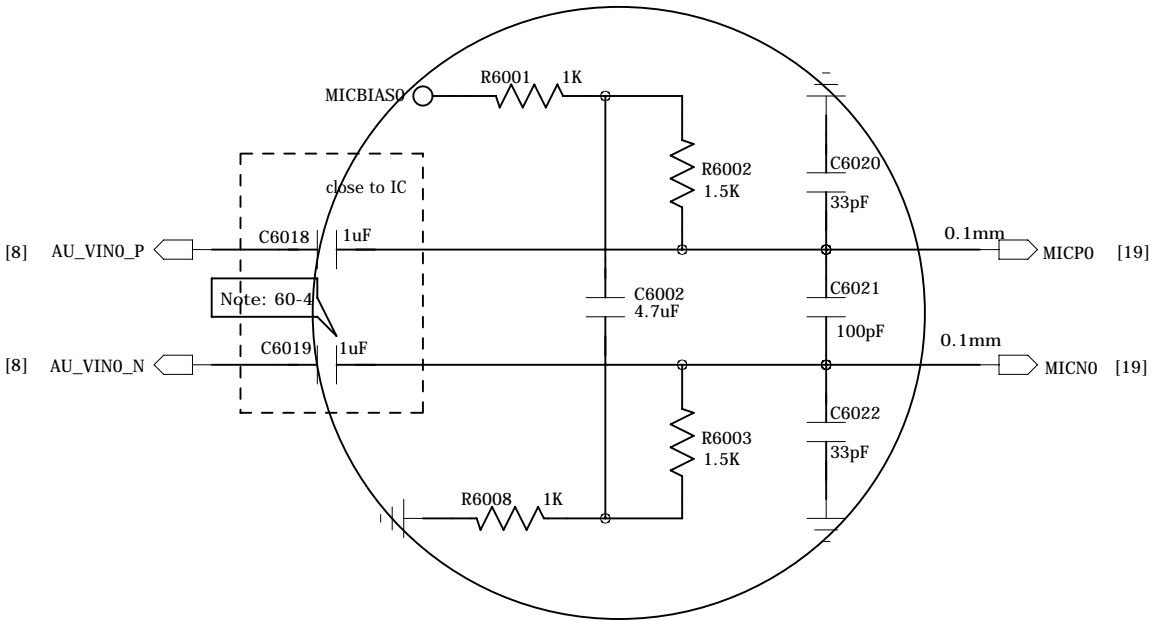


SUB MICPHONE

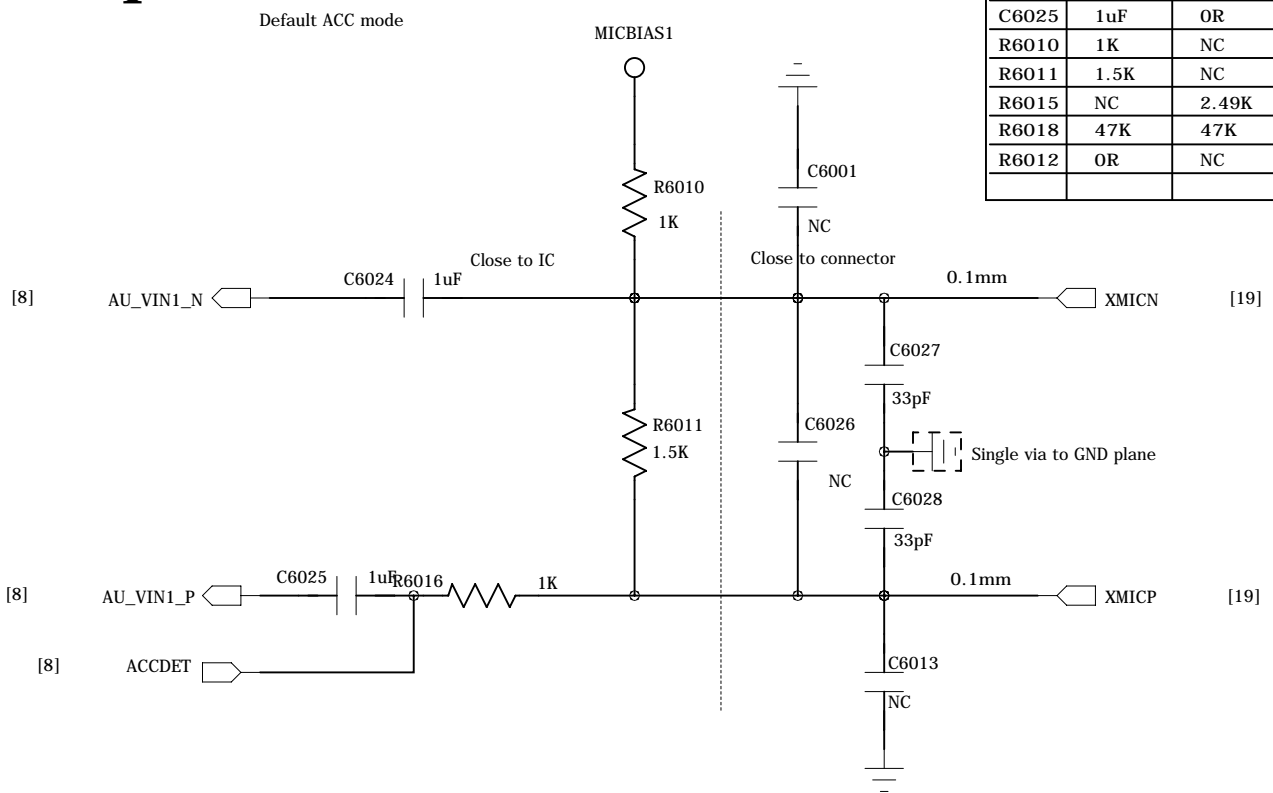
Receiver



Main MICPHONE

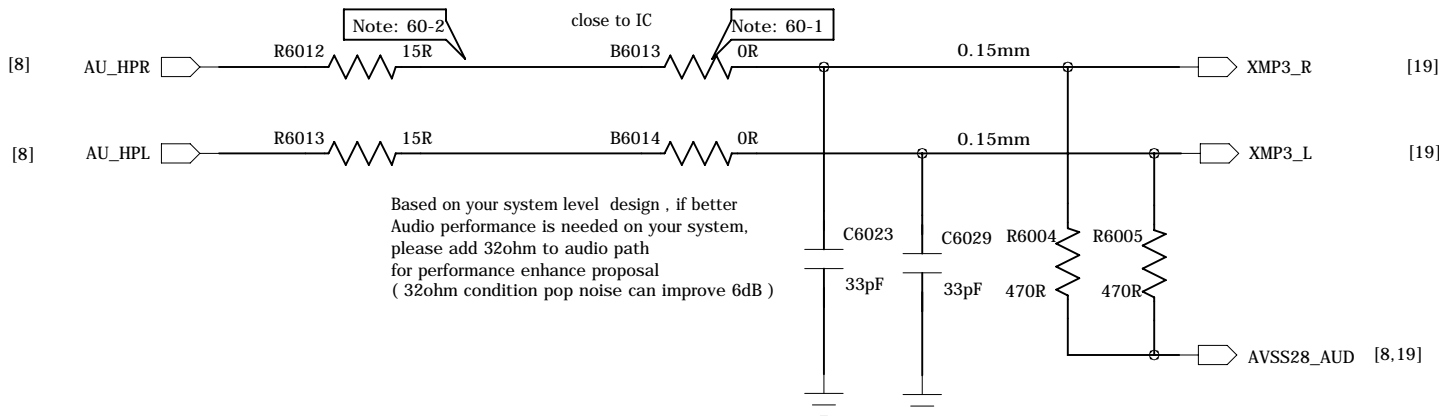


Earphone MICPHONE



Earphone MIC mode		
	ACC mode	DCC mode
C6024	1uF	OR
C6025	1uF	OR
R6010	1K	NC
R6011	1.5K	NC
R6015	NC	2.49K
R6018	47K	47K
R6012	OR	NC

Earphone Receiver



Schematic design notice of "60\_PERI\_AUDIO\_IO" page.

Note 60-1:B6009 B6010 B6013 B6014 needs change to "BLM18BD102SN1" for high THD performance(-90dB), but this BOM change will result in FM RSSI 10dB degraded.

Note 60-2:To reserve a resistor in HPL and HPR in series connection both in order to optimize headphone pop noise. The recommended value of this resistor is 33R.

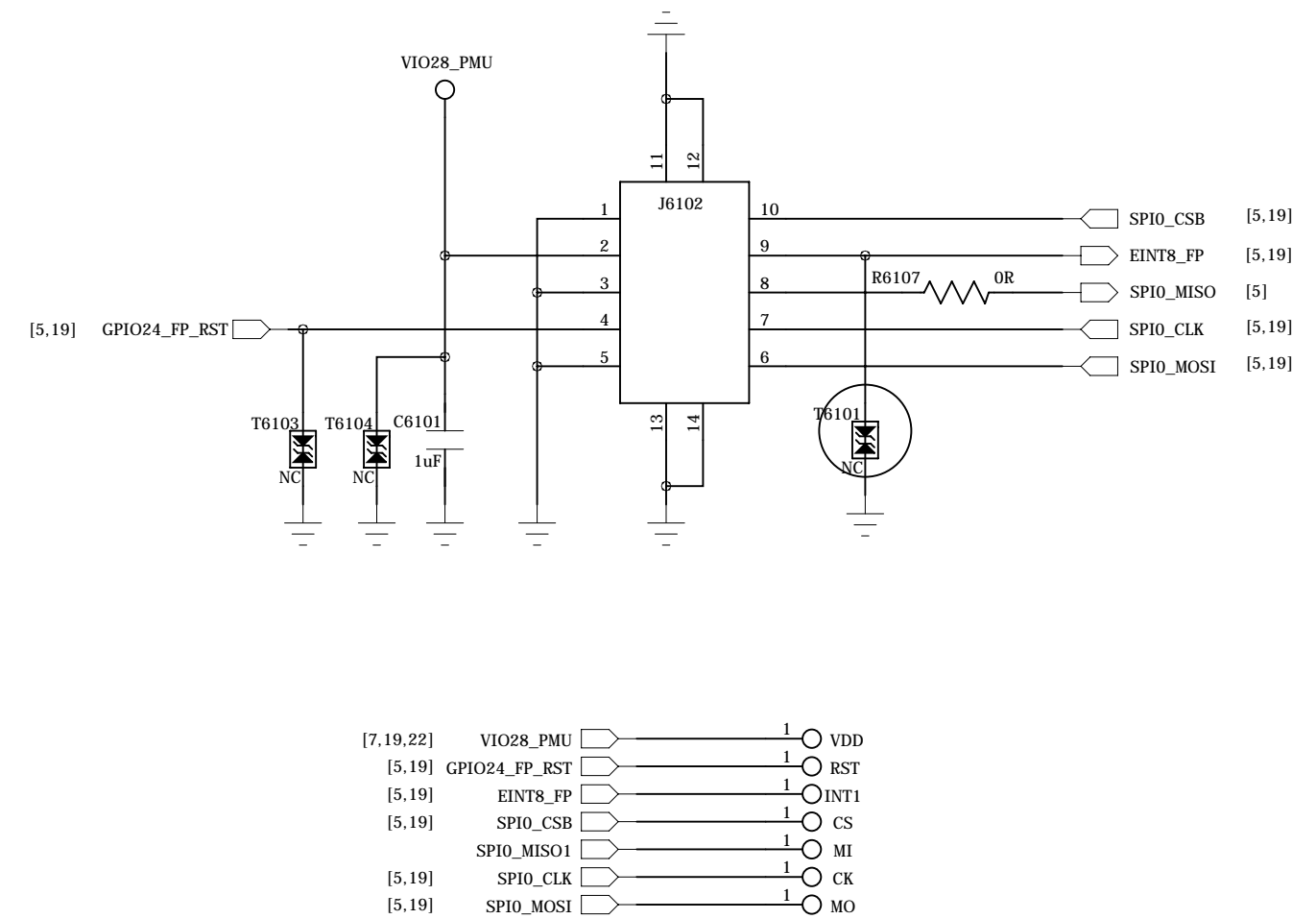
Note 60-3:Layout trace from MT6353 ball J3 AUDREFN to Audio jack GND must surround shield with GND.

Note 60-4:0.1/1uF for ACC mode(1uF for WB\_AMR Speech/0.1uF for NB\_AMR Speech),OR for DCC mode.

COMPANY: TRANSSION HOLDINGS				MODEL: H6126		Modified Date: 2021/9/2	
DRAWN	DJF/TS	DATED	20200928	TITLE: 60_PERI_AUDIO		VERSION: V1.0	SHEET: 18 OF 24
CHECKED	<CHECKED>	DATED	< >	Confidentiality	CONFIDENTIAL		

REVISION RECORD			
LTR	ECO NO:	APPROVED:	DATE:

# FINGER PRINT

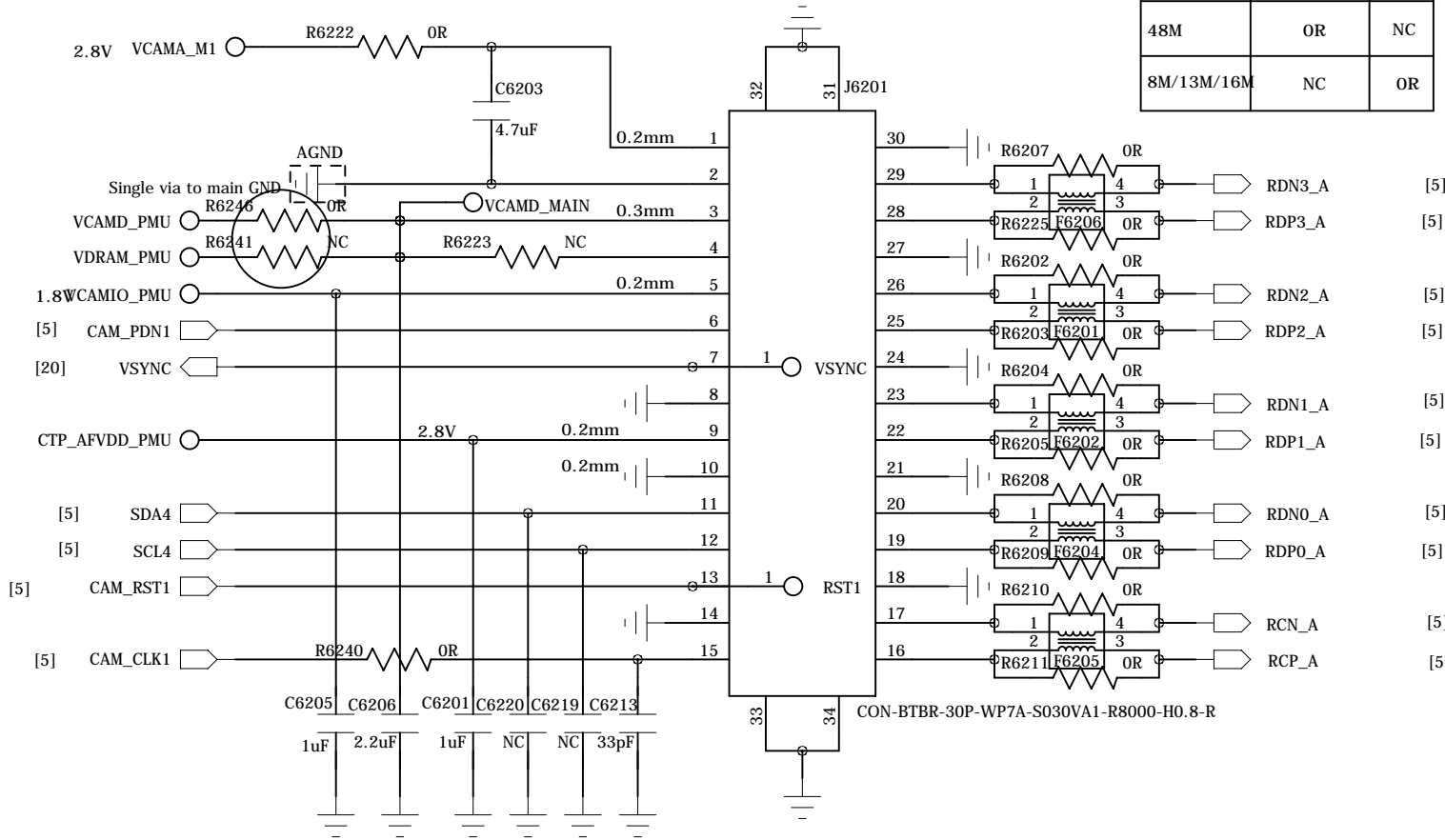


COMPANY: TRANSSION HOLDINGS				MODEL: H6126		Modified Date: 2021/9/2	
DRAWN	DJF/TS	DATED	20200928	TITLE: 61_PERI_LCM_CTP_FP		VERSION: V1.0	SHEET: 19 OF 24
CHECKED	<CHECKED>	DATED	< >	Confidentiality	CONFIDENTIAL		

PERI\_REAR\_CAMERA

REVISION RECORD			
LTR	ECO NO:	APPROVED:	DATE:

REAR CAMERA I (Max 48M+AF)

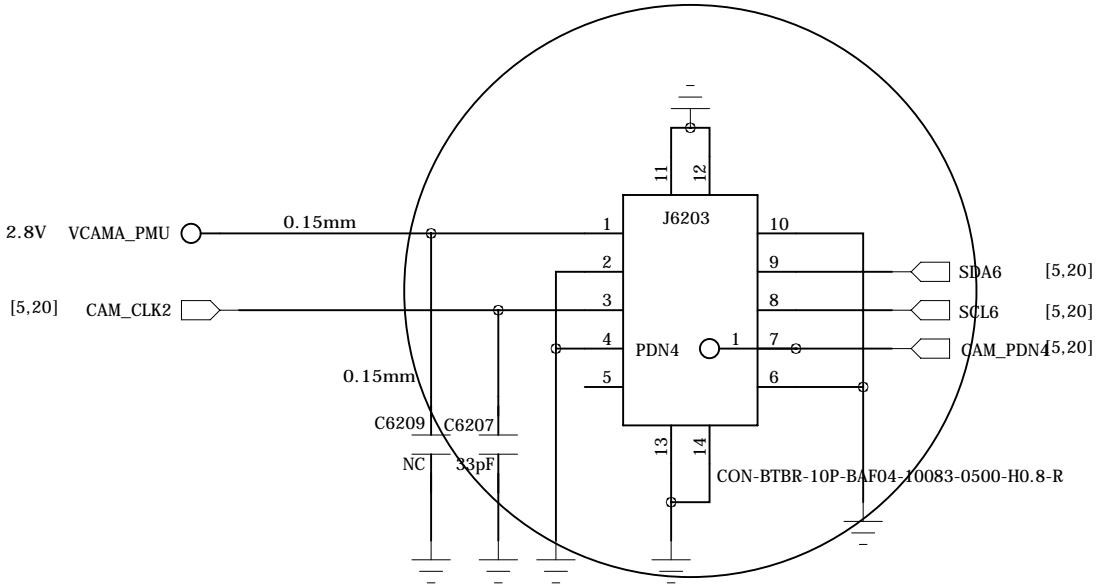


	SENSOR	I2C Address
8M	SENSOR(GC08A3-MCFD0) MOTOR(DW9714P)	Write:0x62 Read:0x63 Write:0x18 Read:0x19
13M	SENSOR(S5K3L6XX03-FGX0) MOTOR(DW9718T) EEPROM(P24C64E-C4H-MIR)	Write:0x20 Read:0x21 Write:0x18 Read:0x19 Write:0xA0 Read:0xA1
16M	SENSOR(S5K3L6XX03-FGX0) MOTOR(GT9772) EEPROM(BL24SA64-CS)	Write:0x20 Read:0x21 Write:0x18 Read:0x19 Write:0xA0 Read:0xA1
48M	SENSOR(OV16B10) MOTOR(DW9718T) EEPROM(P24C64F-A4H-MIR)	Write:0x20 Read:0x21 Write:0x18 Read:0x19 Write:0xA0 Read:0xA1

SENSOR	VCAMA	VCAMD	VCAMIO	AFVDD
GC8034-MCFD0	2.8V 35mA	1.25V 140mA	1.8V 10mA	2.8V 120mA
S5K3L6XX03-FGX0	2.8V 60mA	1.05V 200mA	1.8V 1mA	2.8V 123mA
OV16B10	2.8V 52mA	1.05V 200mA	1.8V 5mA	2.8V 100mA
OV48B2Q-GA5A-Z	2.8V 58.5mA	1.15V 461.5mA	1.8V 3.9mA	2.8V 100mA

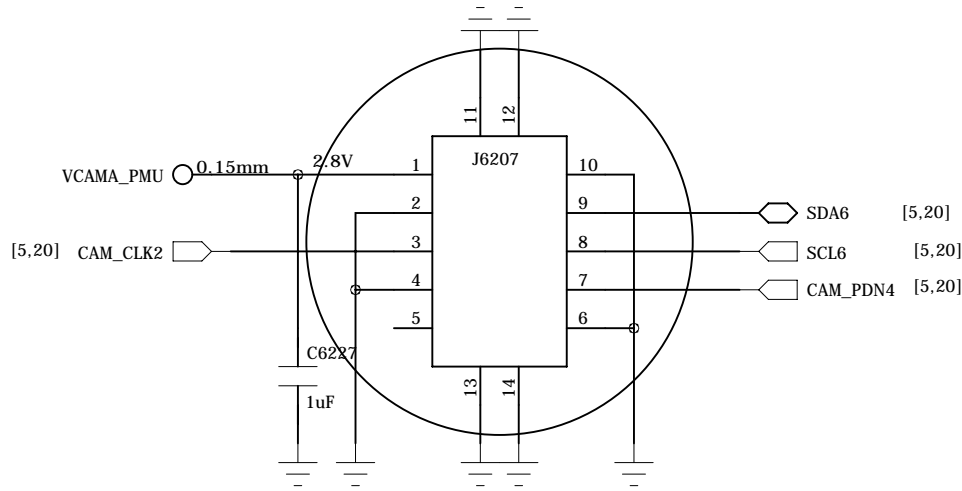
REAR CAMERA III(8W)

SENSOR	VCAMA	I2C Address
GC6153	2.8V 20mA	Write:0x80 Read:0x81



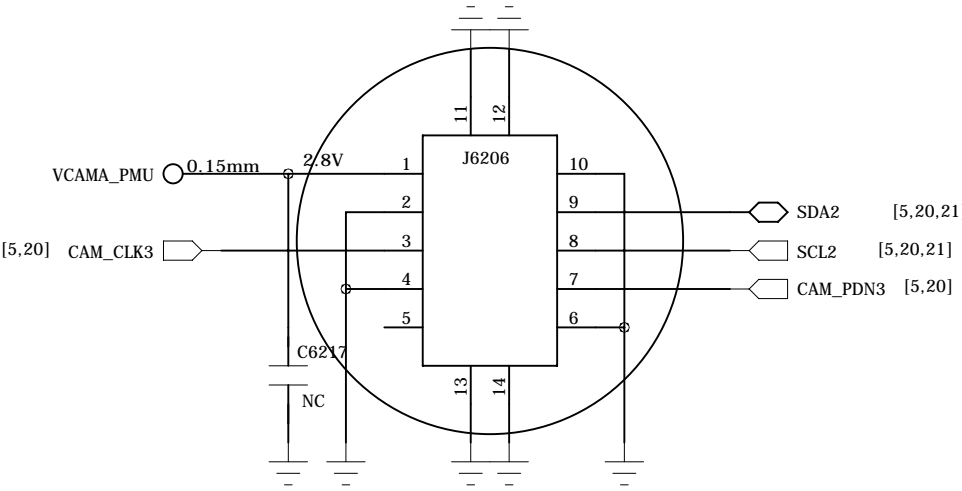
REAR CAMERA V(8W)

SENSOR	VCAMA	I2C Address
GC6153	2.8V 20mA	Write:0x80 Read:0x81

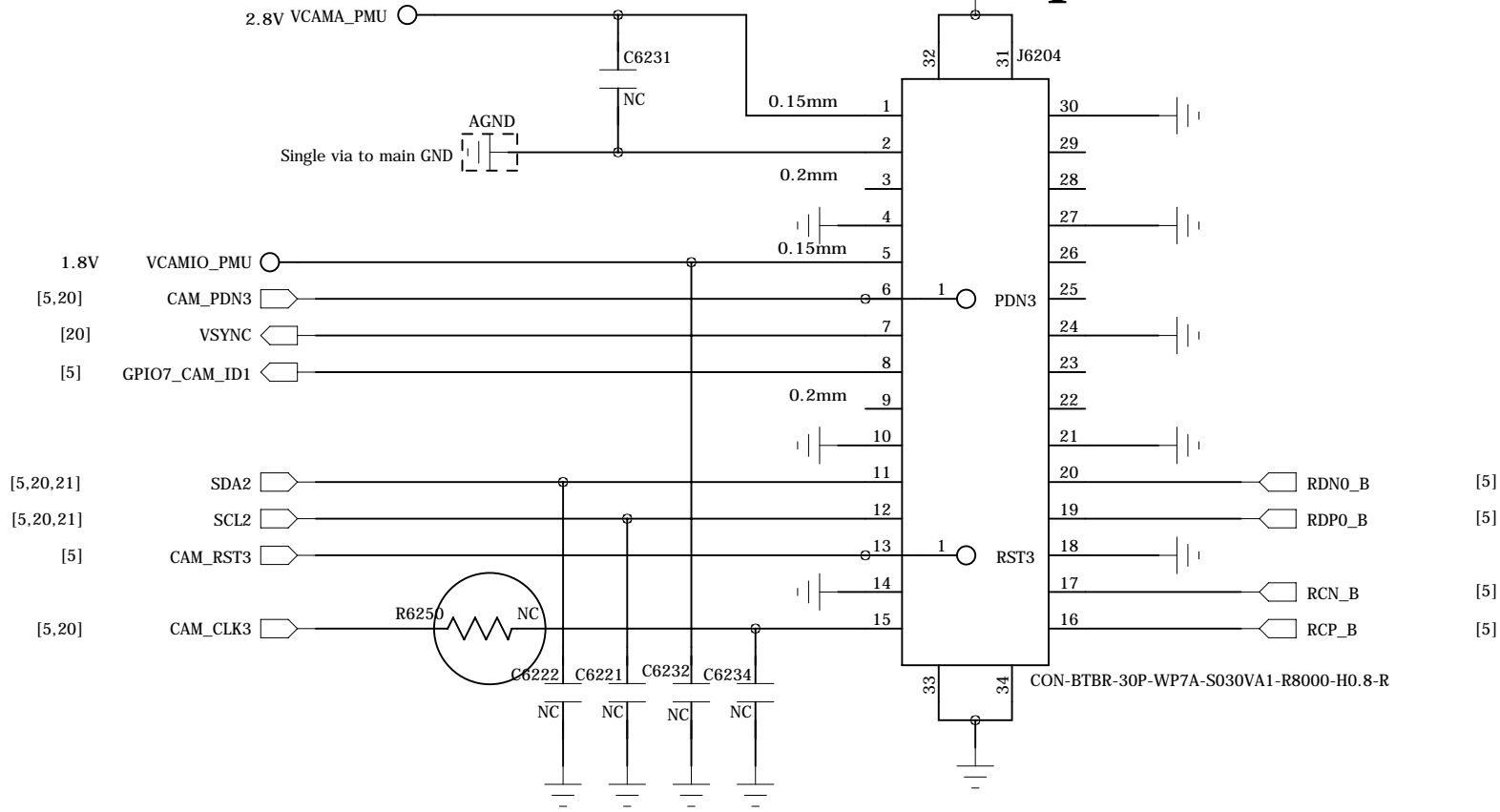


REAR CAMERA VI(8W)

SENSOR	VCAMA	I2C Address
GC6153	2.8V 20mA	Write:0x80 Read:0x81



REAR CAMERA II (2M Depth/Macro/Q)



SENSOR	VCAMA	VCAMD	VCAMIO	I2C Address
OV02B1B	2.8V 40mA	NC	1.8V 70mA	Write:0x7A Read:0x7B
GC02M1B-C24Y0	2.8V 40mA	NC	1.8V 70mA	Write:0x20 Read:0x21
OV02B10-A25A-001A	2.8V 35mA	NC	1.8V 45mA	Write:0x78 Read:0x79
GC02M1-C24YA	2.8V 40mA	NC	1.8V 70mA	Write:0x20 Read:0x21

COMPANY: TRANSSION HOLDINGS

MODEL: H6126

Modified Date: 2021/9/2

DRAWN DJF/TS DATED 20200928

TITLE: 62\_PERI\_REAR\_CAMERA

VERSION: V1.0

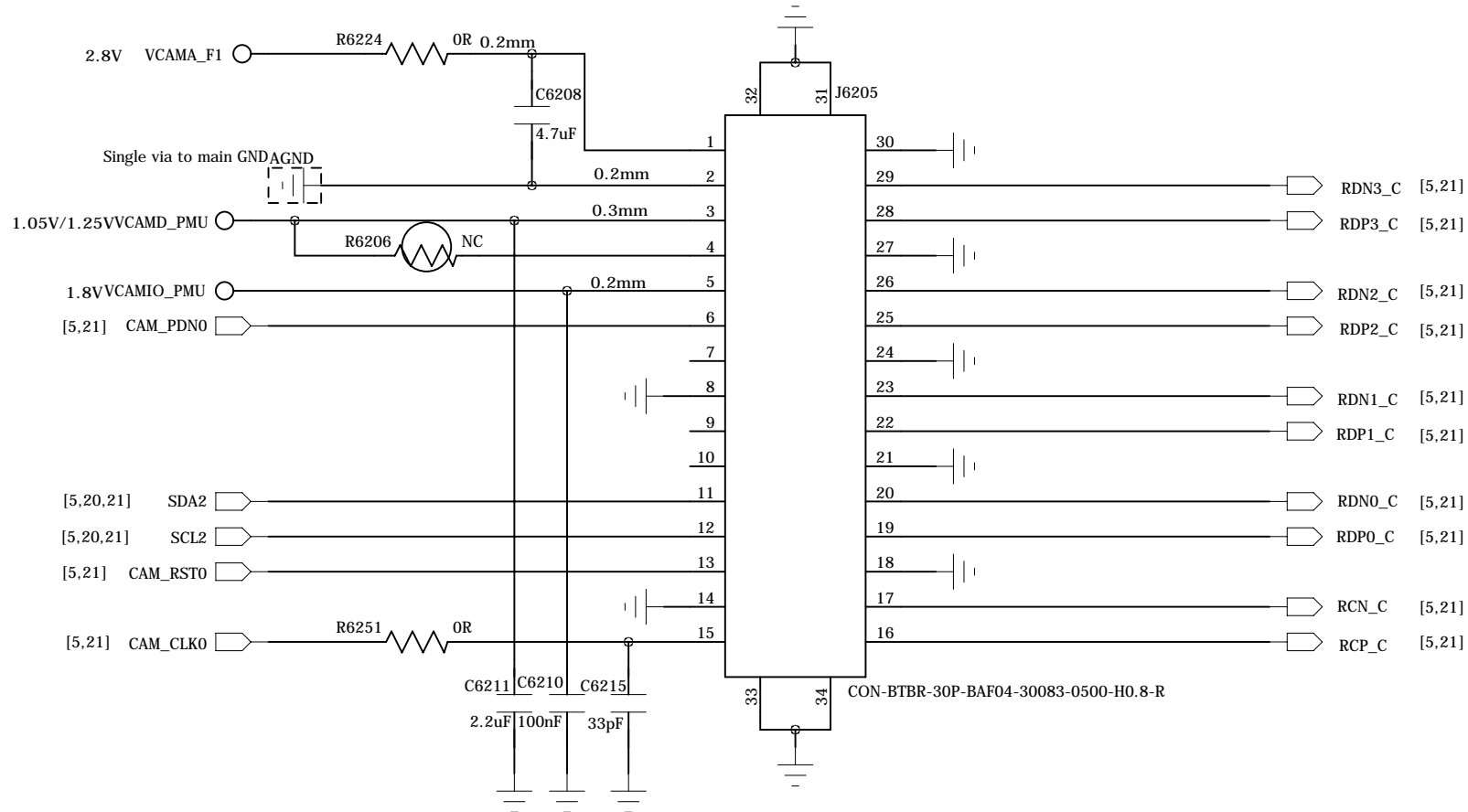
SHEET: 20 OF 24

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PERI\_FRONT\_CAMERA

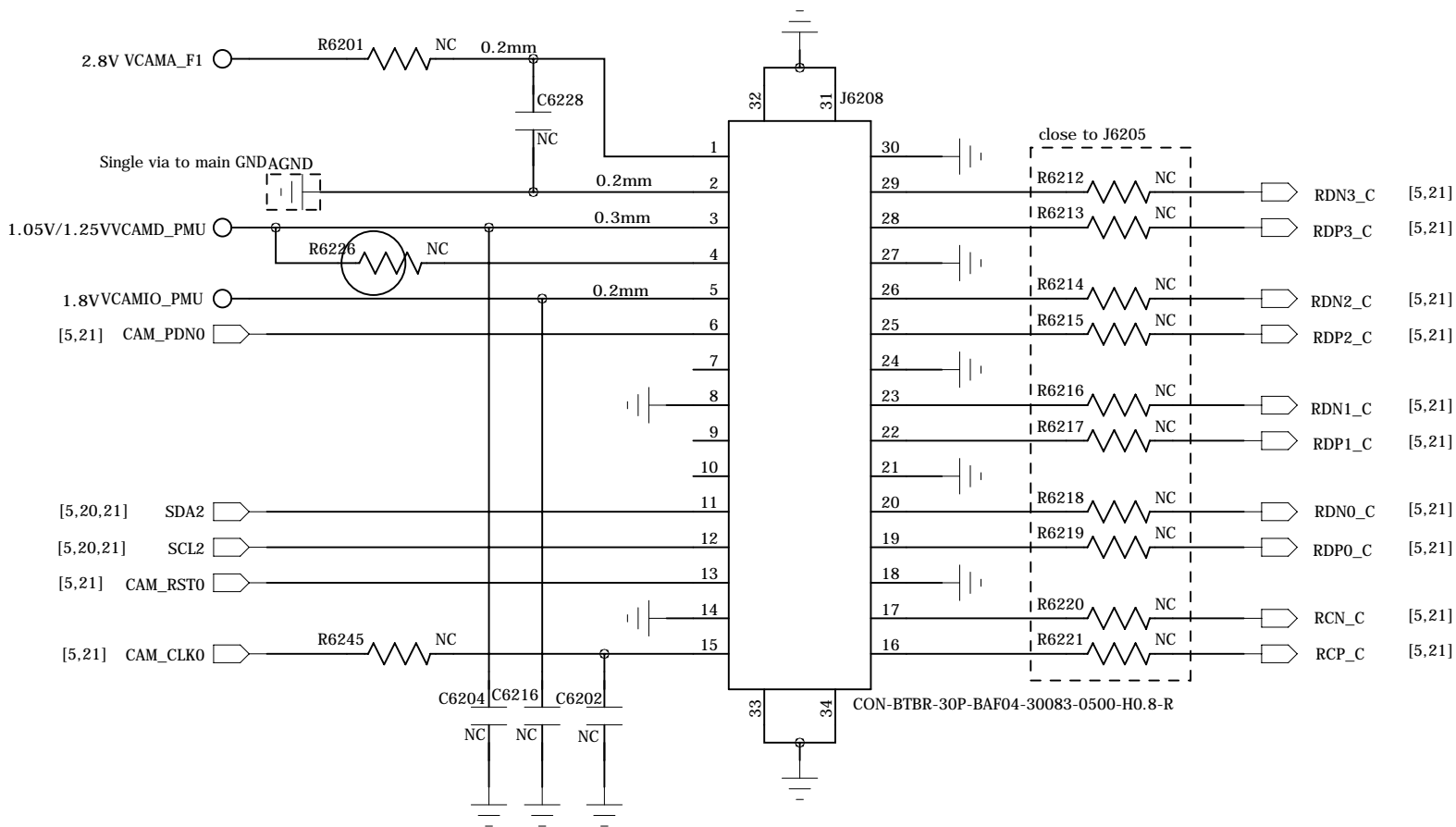
FRONT MAIN CAMERA (MAX 16M+ FF)  
For Drop



	SENSOR	I2C Address
5M	GC5035-MCHD0	Write:0x6E Read:0x6F
8M	GC8034-WC1X0	Write:0x6E Read:0x6F
16M	S5K3P9SX04-FGX9	Write:0x5A Read:0x5B
	P24C64E-C4H-MIR	Write:0xA2 Read:0xA3
	P24S64E-C4H-MIR	Write:0xA2 Read:0xA3

SENSOR	VCAMA	VCAMD	VCAMIO
GC5035-MCHD0	2.8V 35mA	1.2V 80mA	1.8V 3mA
GC8034-WC1X0	2.8V 35mA	1.25V 140mA	1.8V 10mA
S5K3P9SX04-FGX9	2.8V 57.5mA	1.05V 159.9mA	1.8V 0.5mA

For Blind



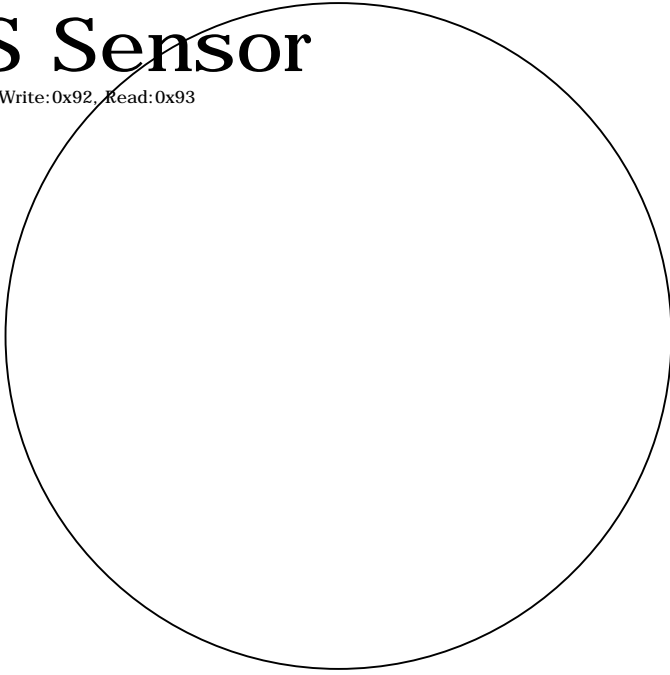
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CHECKED	<CHECKED>	DATED	< >	Confidentiality	CONFIDENTIAL		

PERI\_SENSORS

REVISION RECORD			
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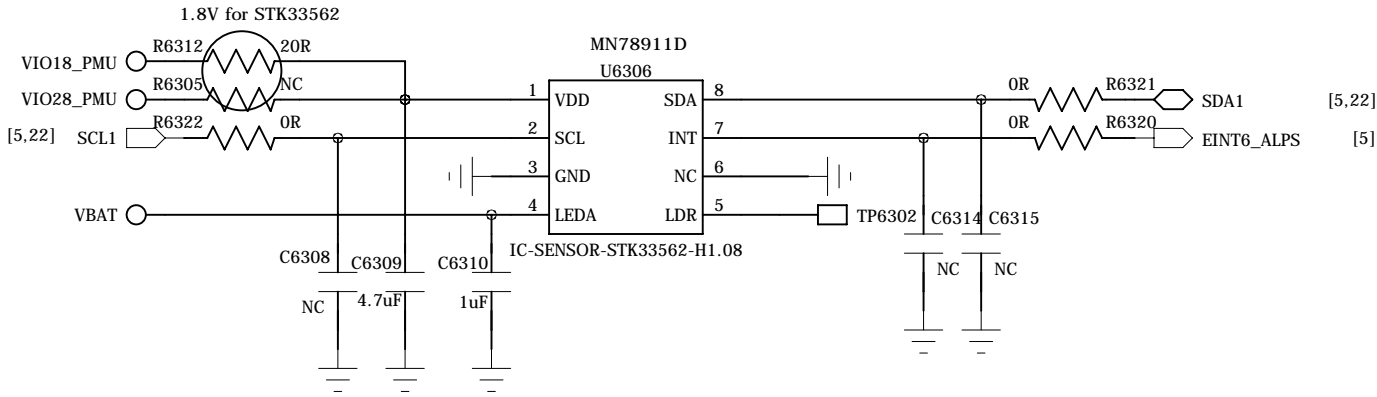
AL& PS Sensor

MN28233LKDN:12C address: Write:0x92, Read:0x93

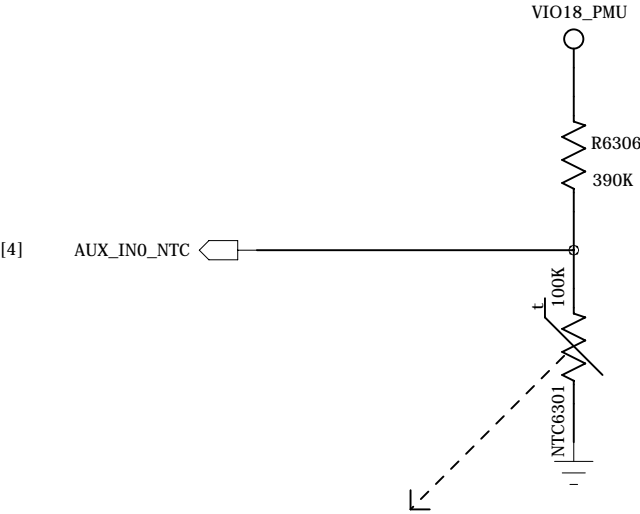


ALPS

STK3337X:12C address: Write:0x8E, Read:0x8F  
STK33562:12C address: Write:0x8C, Read:0x8D  
STK33562:12C address: Write:0x8C, Read:0x8D  
LTR-569ALS-WA:12C address: Write:0x46, Read:0x47  
MN78911D:12C address: Write:0x82, Read:0x83



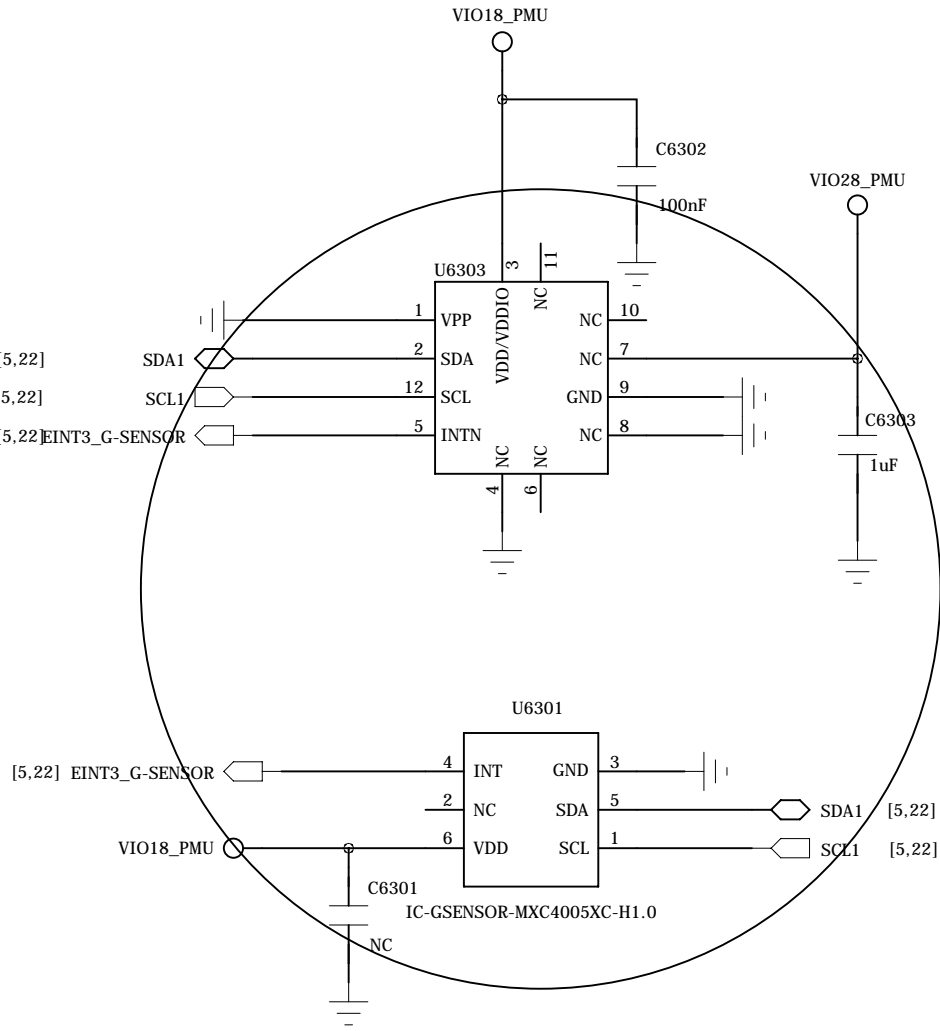
Thermistor to sense AP temperature



- 1. NTC6301must keep a distance about 6~8 mm away from AP and far from other heat sources 10 mm at least.
- 2. The distance is the shortest distance from package edge to edge.

G-Sensor

MXC6655XA:ADDRESS:0x2A(Write)/0x2B(Read)default  
STK8BA50-S/SC7A20:ADDRESS:0x30(Write)/0x31(Read)Reserve

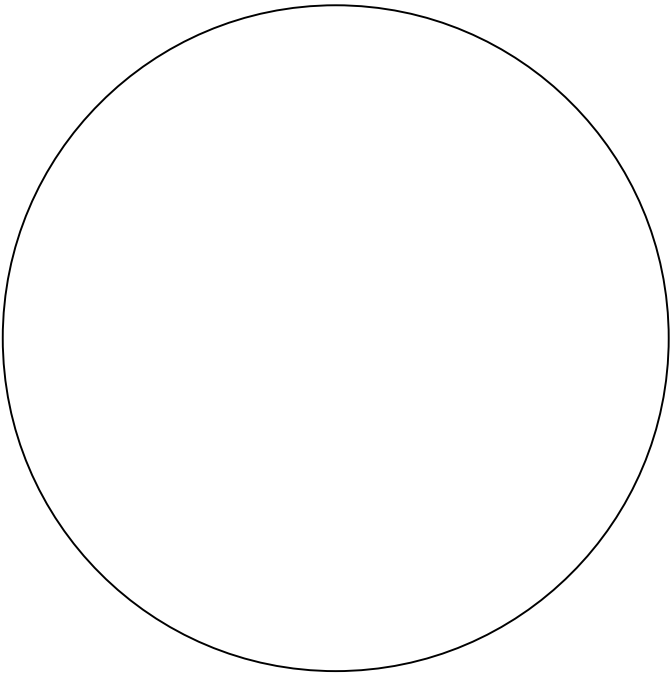


component	MXC6655XA	SC7A20	STK8BA50-S
C6302	NC	100nF	1uF
C6303	1uF	100nF	1uF

M-Sensor(COMPASS)

MMC5603NJL:12C ADDRESS:0x60(Write)/0x61(Read)Default

G-Sensor + Gyro Sensor

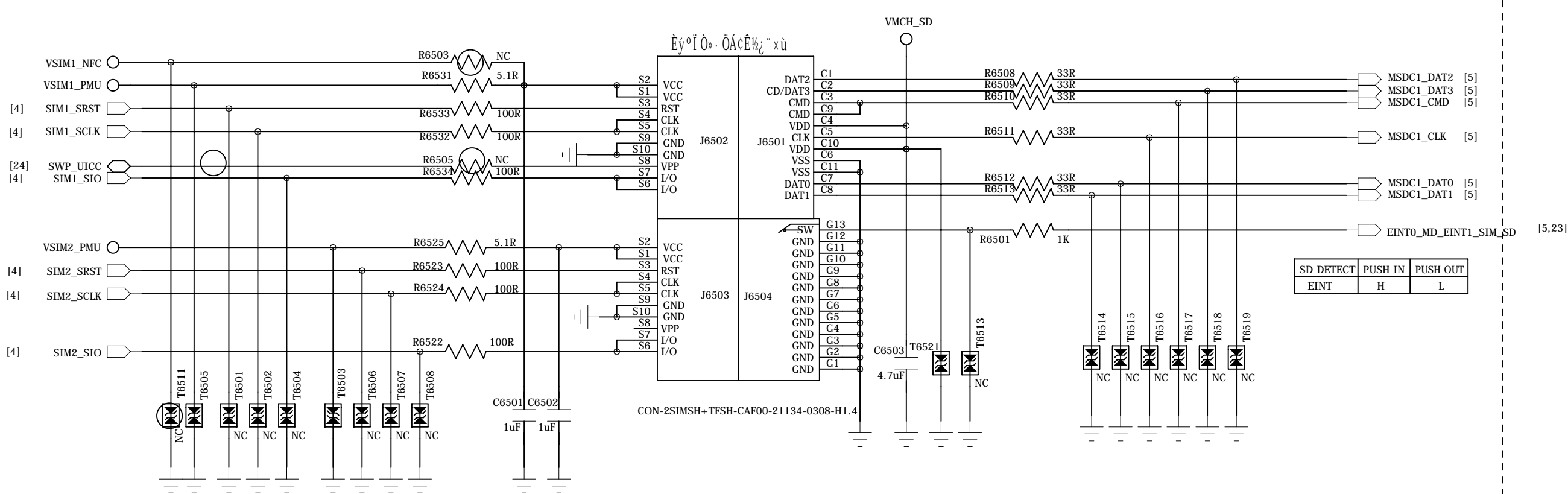


COMPANY: TRANSSION HOLDINGS				MODEL: H6126		Modified Date: 2021/9/2	
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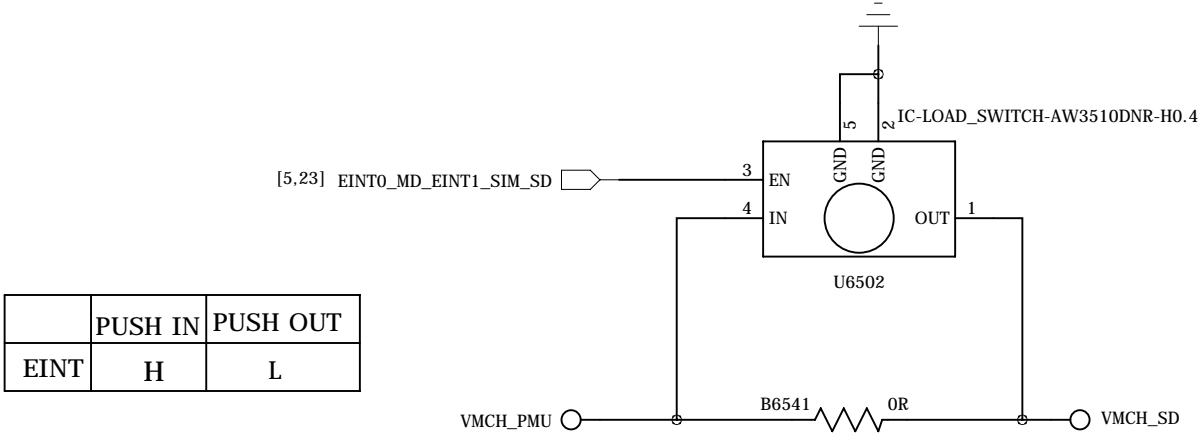
PERI\_SIM\_SD\_LED

REVISION RECORD			
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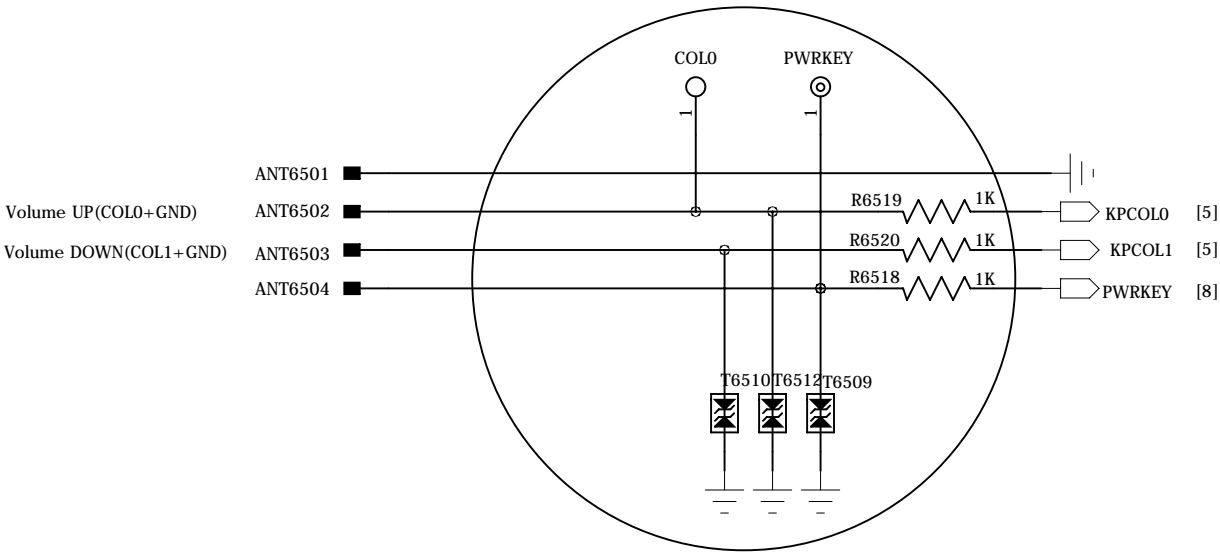
SIM/SD CARD



SD POWER CONTROL



SIDEKEY

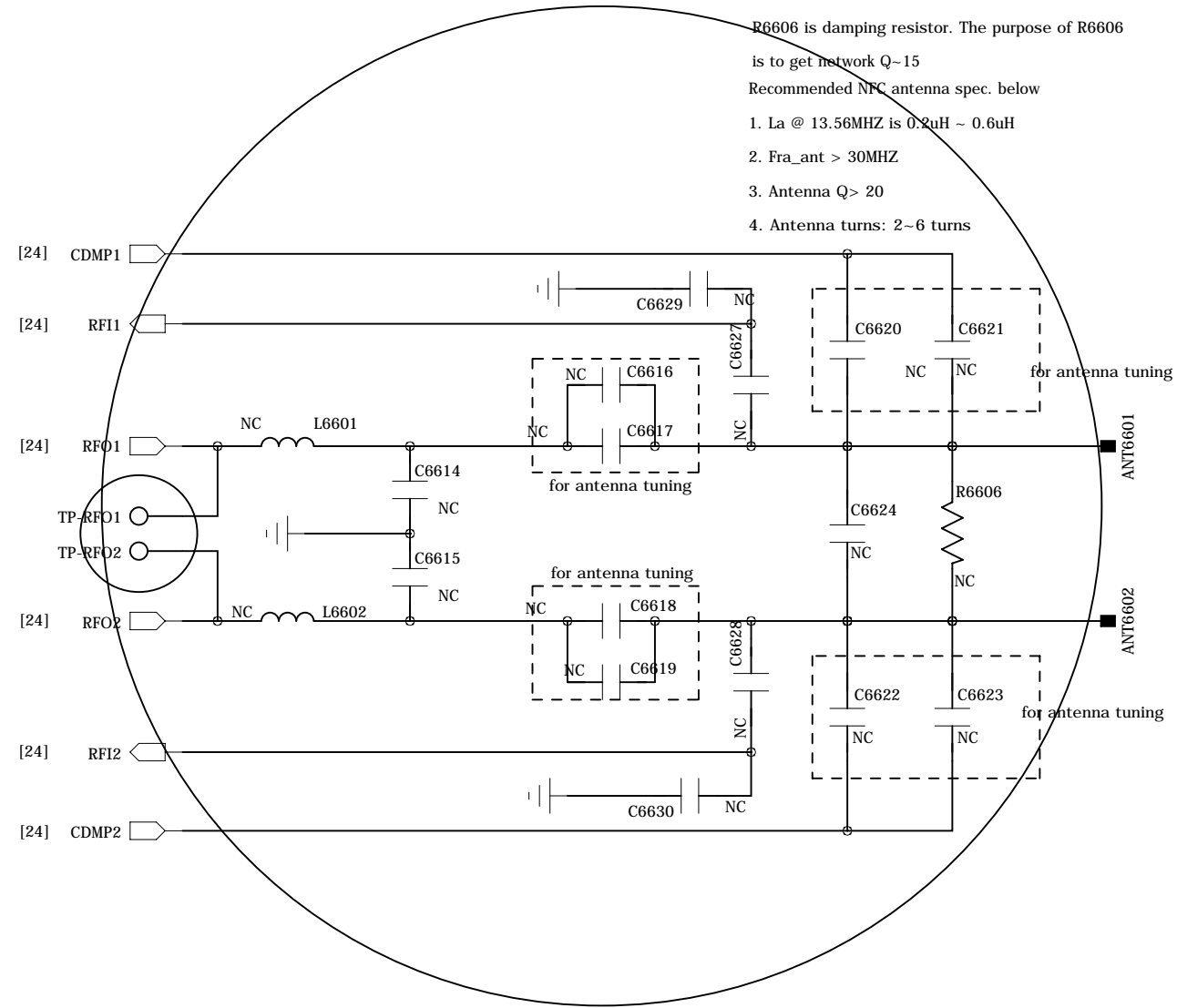
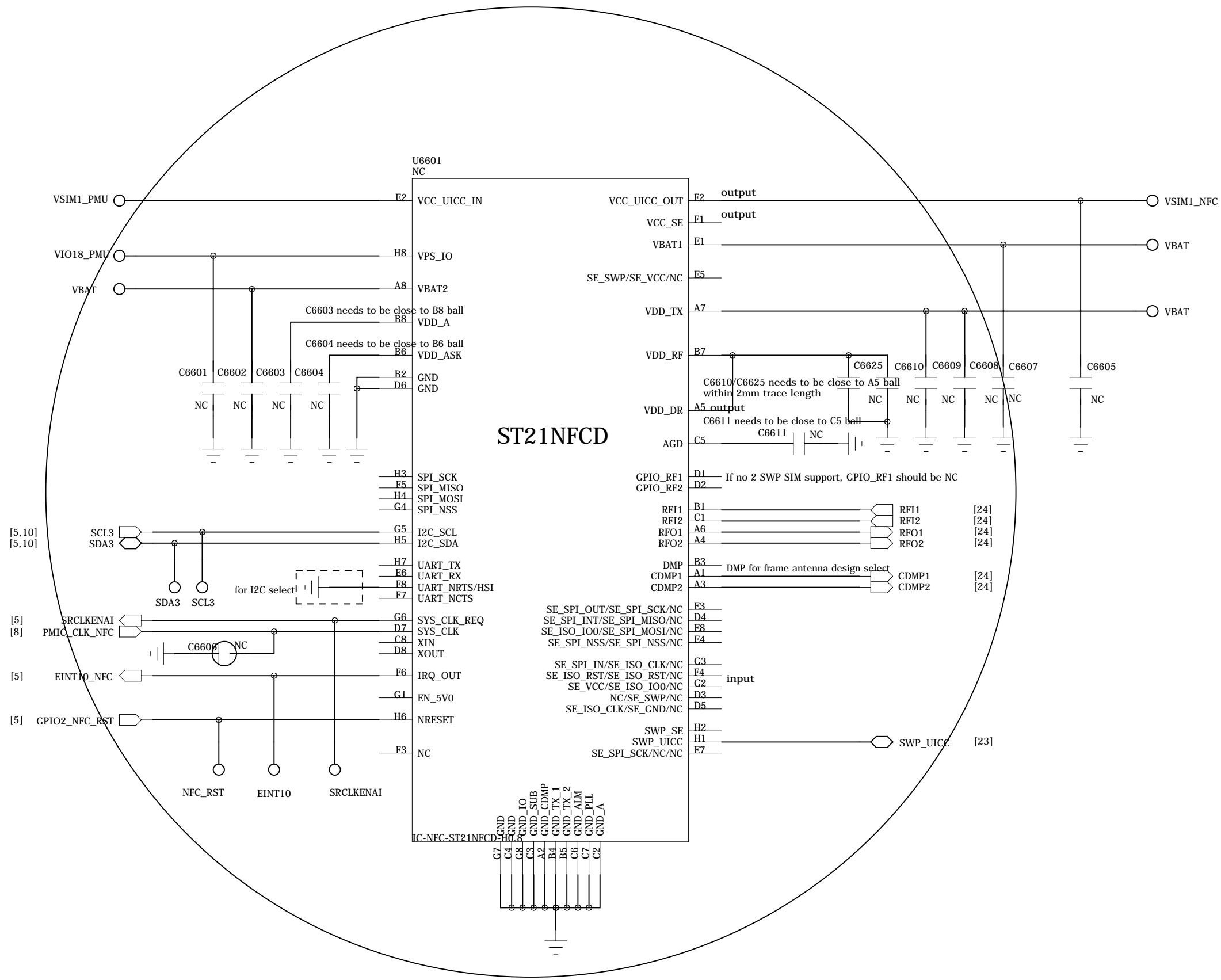


Indicator LED1

COMPANY: TRANSSION HOLDINGS				MODEL: H6126		Modified Date: 2021/9/2	
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PERI\_NFC

REVISION RECORD			
LTR	ECO NO:	APPROVED:	DATE:



COMPANY: TRANSSION HOLDINGS				MODEL: H6126		Modified Date: 2021/9/2	
DRAWN	DJF/TS	DATED	20200928	TITLE: 66_PERI_NFC		VERSION: V1.0	SHEET: 24 OF 24
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